- **Low Supply-Voltage Range, 1.8 V to 3.6 V**
- **Ultralow-Power Consumption:**
  - **Active Mode: 200 µA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.7 µA**
  - **Off Mode (RAM Retention): 0.1 µA**
- **Five Power-Saving Modes**
- **Wake-Up From Standby Mode in Less Than 6 µs**
- **Frequency-Locked Loop, FLL+**
- **16-Bit RISC Architecture, 125-ns Instruction Cycle Time**
- **Scan IF for Background Water, Heat, and Gas Volume Measurement**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **16-Bit Timer_A With Five Capture/Compare Registers**
- **Integrated LCD Driver for Up to 96 Segments**
- **On-Chip Comparator**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **Brownout Detector**
- **Supply Voltage Supervisor/Monitor With Programmable Level Detection**
- **Bootstrap Loader in Flash Devices**
- **Family Members Include:**
  - **MSP430FW423:**
    8KB + 256B Flash Memory,
    256B RAM
  - **MSP430FW425:**
    16KB + 256B Flash Memory,
    512B RAM
  - **MSP430FW427:**
    32KB + 256B Flash Memory,
    1KB RAM
- **Available in 64-Pin Quad Flat Pack (QFP)**
- **For Complete Module Descriptions, Refer to the *MSP430x4xx Family User's Guide*, Literature Number SLAU056**

description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6 µs.

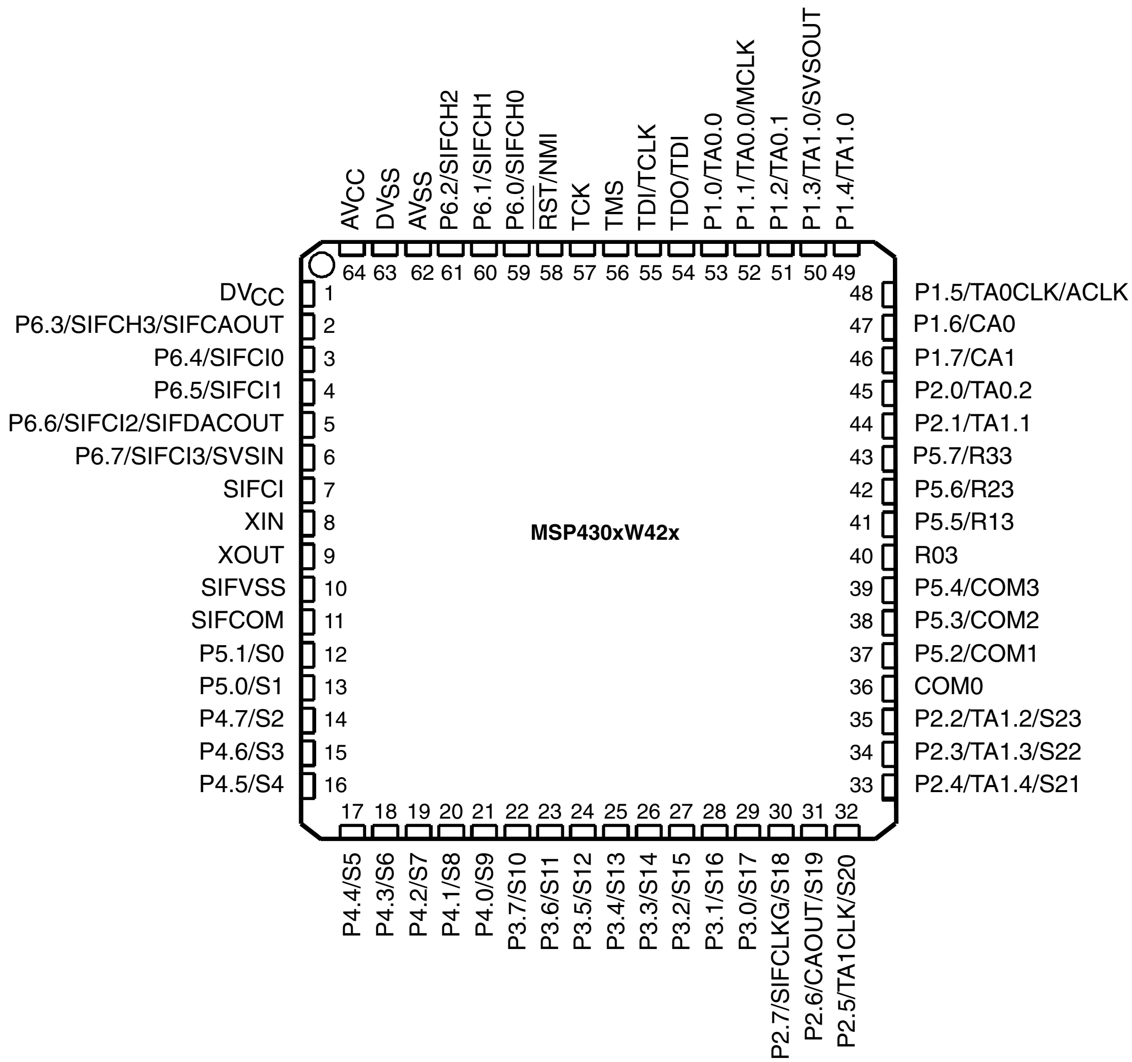
The MSP430xW42x series are microcontroller configurations with two built-in 16-bit timers, a comparator, 96 LCD segment drive capability, a scan interface, and 48 I/O pins.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and process the data and transmit them to a host system. The comparator and timers make the configurations ideal for gas, heat, and water meters, industrial meters, counter applications, handheld meters, etc.

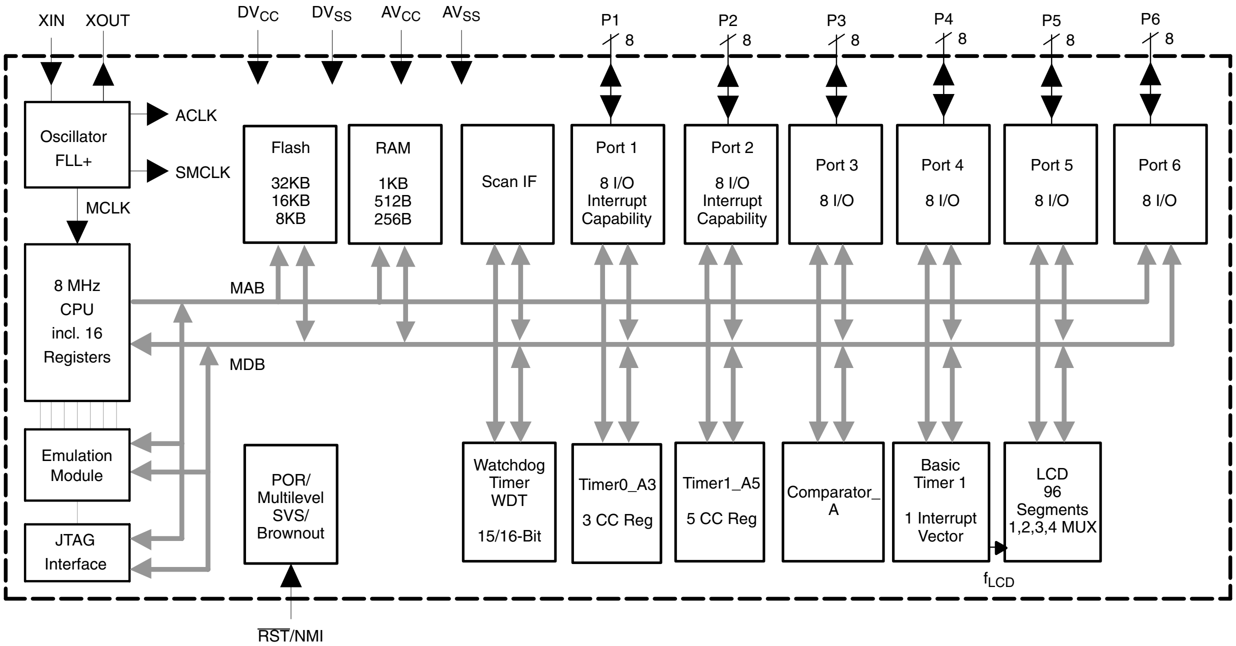
AVAILABLE OPTIONS

T_A	PACKAGED DEVICES PLASTIC 64-PIN QFP (PM)
−40°C to 85°C	MSP430FW423IPM MSP430FW425IPM MSP430FW427IPM

pin designation, MSP430xW42x



functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AV_{CC}	64		Analog supply voltage, positive terminal. Supplies SVS, brownout, oscillator, comparator_A, scan IF AFE, port 6, and LCD resistive divider circuitry; must not power up prior to DV_{CC}.
AV_{SS}	62		Analog supply voltage, negative terminal. Supplies SVS, brownout, oscillator, comparator_A, scan IF AFE. and port 6. Must be externally connected to DV_{SS}. Internally connected to DV_{SS}.
DV_{CC}	1		Digital supply voltage, positive terminal.
DV_{SS}	63		Digital supply voltage, negative terminal.
SIFVSS	10		Scan IF AFE reference supply voltage.
P1.0/TA0.0	53	I/O	General-purpose digital I/O/Timer0_A. Capture: CCI0A input, compare: Out0 output/BSL transmit
P1.1/TA0.0/MCLK	52	I/O	General-purpose digital I/O/Timer0_A. Capture: CCI0B input/MCLK output/BSL receive Note: TA0.0 is only an input on this pin.
P1.2/TA0.1	51	I/O	General-purpose digital I/O/Timer0_A, capture: CCI1A input, compare: Out1 output
P1.3/TA1.0/SVSOUT	50	I/O	General-purpose digital I/O/Timer1_A, capture: CCI0B input/SVS: output of SVS comparator Note: TA1.0 is only an input on this pin.
P1.4/TA1.0	49	I/O	General-purpose digital I/O/Timer1_A, capture: CCI0A input, compare: Out0 output
P1.5/TA0CLK/ACLK	48	I/O	General-purpose digital I/O/input of Timer0_A clock/output of ACLK
P1.6/CA0	47	I/O	General-purpose digital I/O/Comparator_A input
P1.7/CA1	46	I/O	General-purpose digital I/O/Comparator_A input
P2.0/TA0.2	45	I/O	General-purpose digital I/O/Timer0_A, capture: CCI2A input, compare: Out2 output
P2.1/TA1.1	44	I/O	General-purpose digital I/O/Timer0_A, capture: CCI1A input, compare: Out1 output
P2.2/TA1.2/S23	35	I/O	General-purpose digital I/O/Timer1_A, capture: CCI2A input, compare: Out2 output/LCD segment output 23 (see Note)
P2.3/TA1.3/S22	34	I/O	General-purpose digital I/O/Timer1_A, capture: CCI3A input, compare: Out3 output/LCD segment output 22 (see Note)
P2.4/TA1.4/S21	33	I/O	General-purpose digital I/O/Timer1_A, capture: CCI4A input, compare: Out4 output/LCD segment output 21 (see Note)
P2.5/TA1CLK/S20	32	I/O	General-purpose digital I/O/input of Timer1_A clock/LCD segment output 20 (see Note)
P2.6/CAOUT/S19	31	I/O	General-purpose digital I/O/Comparator_A output/LCD segment output 19 (see Note)
P2.7/SIFCLKG/S18	30	I/O	General-purpose digital I/O/Scan IF, signal SIFCLKG from internal clock generator/LCD segment output 18 (see Note)
P3.0/S17	29	I/O	General-purpose digital I/O/ LCD segment output 17 (see Note)
P3.1/S16	28	I/O	General-purpose digital I/O/ LCD segment output 16 (see Note)
P3.2/S15	27	I/O	General-purpose digital I/O/ LCD segment output 15 (see Note)
P3.3/S14	26	I/O	General-purpose digital I/O/ LCD segment output 14 (see Note)
P3.4/S13	25	I/O	General-purpose digital I/O/LCD segment output 13 (see Note)
P3.5/S12	24	I/O	General-purpose digital I/O/LCD segment output 12 (see Note)
P3.6/S11	23	I/O	General-purpose digital I/O/LCD segment output 11 (see Note)
P3.7/S10	22	I/O	General-purpose digital I/O/LCD segment output 10 (see Note)

NOTE: LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.

Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
P4.0/S9	21	I/O	General-purpose digital I/O/LCD segment output 9 (see Note)
P4.1/S8	20	I/O	General-purpose digital I/O/LCD segment output 8 (see Note)
P4.2/S7	19	I/O	General-purpose digital I/O/LCD segment output 7 (see Note)
P4.3/S6	18	I/O	General-purpose digital I/O/LCD segment output 6 (see Note)
P4.4/S5	17	I/O	General-purpose digital I/O/LCD segment output 5 (see Note)
P4.5/S4	16	I/O	General-purpose digital I/O/LCD segment output 4 (see Note)
P4.6/S3	15	I/O	General-purpose digital I/O/LCD segment output 3 (see Note)
P4.7/S2	14	I/O	General-purpose digital I/O/LCD segment output 2 (see Note)
P5.0/S1	13	I/O	General-purpose digital I/O/LCD segment output 1 (see Note)
P5.1/S0	12	I/O	General-purpose digital I/O/LCD segment output 0 (see Note)
COM0	36	O	Common output. COM0−3 are used for LCD backplanes
P5.2/COM1	37	I/O	General-purpose digital I/O/common output. COM0−3 are used for LCD backplanes
P5.3/COM2	38	I/O	General-purpose digital I/O/common output. COM0−3 are used for LCD backplanes
P5.4/COM3	39	I/O	General-purpose digital I/O/common output. COM0−3 are used for LCD backplanes
R03	40	I	Input port of fourth positive (lowest) analog LCD level (V5)
P5.5/R13	41	I/O	General-purpose digital I/O/input port of third most positive analog LCD level (V4 or V3)
P5.6/R23	42	I/O	General-purpose digital I/O/input port of second most positive analog LCD level (V2)
P5.7/R33	43	I/O	General-purpose digital I/O/output port of most positive analog LCD level (V1)
P6.0/SIFCH0	59	I/O	General-purpose digital I/O/Scan IF, channel 0 sensor excitation output and signal input
P6.1/SIFCH1	60	I/O	General-purpose digital I/O/Scan IF, channel 1 sensor excitation output and signal input
P6.2/SIFCH2	61	I/O	General-purpose digital I/O/Scan IF, channel 2 sensor excitation output and signal input
P6.3/SIFCH3/ SIFCAOUT	2	I/O	General-purpose digital I/O/Scan IF, channel 3 sensor excitation output and signal input/Scan IF comparator output
P6.4/SIFCI0	3	I/O	General-purpose digital I/O/Scan IF, channel 0 signal input to comparator
P6.5/SIFCI1	4	I/O	General-purpose digital I/O/Scan IF, channel 1 signal input to comparator
P6.6/SIFCI2/ SIFDACOUT	5	I/O	General-purpose digital I/O/Scan IF, channel 2 signal input to comparator/10-bit DAC output
P6.7/ SIFCI3/SVSIN	6	I/O	General-purpose digital I/O/Scan IF, channel 3 signal input to comparator/SVS, analog input
SIFCI	7	I	Scan IF input to Comparator.
SIFCOM	11	O	Common termination for Scan IF sensors.
$\overline{RST}$/NMI	58	I	Reset input or nonmaskable interrupt input port.
TCK	57	I	Test clock. TCK is the clock input port for device programming and test.
TDI/TCLK	55	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	54	I/O	Test data output port. TDO/TDI data output or programming data input terminal.
TMS	56	I	Test mode select. TMS is used as an input port for device programming and test.
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output terminal of crystal oscillator XT1.

NOTE: LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.

short-form description

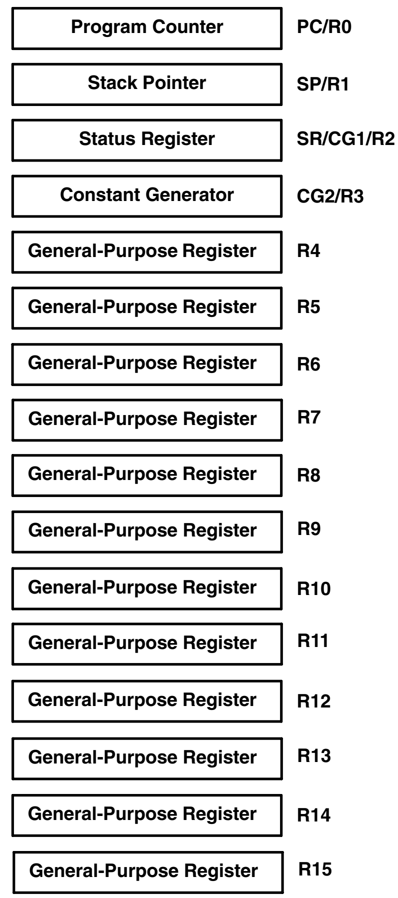
CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 –––> R5
Single operands, destination only	e.g. CALL R8	PC ––>(TOS), R8––> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	•	•	MOV Rs,Rd	MOV R10,R11	R10 ––> R11
Indexed	•	•	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)––> M(6+R6)
Symbolic (PC relative)	•	•	MOV EDE,TONI		M(EDE) ––> M(TONI)
Absolute	•	•	MOV &MEM,&TCDAT		M(MEM) ––> M(TCDAT)
Indirect	•		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) ––> M(Tab+R6)
Indirect autoincrement	•		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) ––> R11 R10 + 2––> R10
Immediate	•		MOV #X,TONI	MOV #45,TONI	#45 ––> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
    ACLK and SMCLK remain active, MCLK is available to modules
    FLL+ loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
    ACLK and SMCLK remain active, MCLK is available to modules
    FLL+ loop control is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
    MCLK, FLL+ loop control, and DCOCLK are disabled
    DCO's dc-generator remains enabled
    ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
    MCLK, FLL+ loop control, and DCOCLK are disabled
    DCO's dc-generator is disabled
    ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
    ACLK is disabled
    MCLK, FLL+ loop control, and DCOCLK are disabled
    DCO's dc-generator is disabled
    Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh – 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External Reset Watchdog Flash memory	WDTIFG KEYV (see Note 1)	Reset	0FFFEh	15, highest
NMI Oscillator Fault Flash memory access violation	NMIIFG OFIFG ACCVIFG (see Notes 1 & 3)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	14
Timer1_A5	TA1CCR0 CCIFG (see Note 2)	Maskable	0FFFAh	13
Timer1_A5	TA1CCR1 CCIFG to TA1CCR4 CCIFG, TA1CTL TAIFG (see Notes 1 & 2)	Maskable	0FFF8h	12
Comparator_A	CMPAIFG	Maskable	0FFF6h	11
Watchdog Timer	WDTIFG	Maskable	0FFF4h	10
Scan IF	SIFIFG0 to SIFIFG6 (See Note 1)	Maskable	0FFF2h	9
			0FFF0h	8
			0FFEEh	7
Timer0_A3	TA0CCR0 CCIFG (see Note 2)	Maskable	0FFECh	6
Timer0_A3	TA0CCR1 CCIFG, TA0CCR2 CCIFG, TA0CTL TAIFG (see Notes 1 & 2)	Maskable	0FFEAh	5
I/O port P1 (eight flags)	P1IFG.0 to P1IFG.7 (see Notes 1 & 2)	Maskable	0FFE8h	4
			0FFE6h	3
			0FFE4h	2
I/O port P2 (eight flags)	P2IFG.0 to P2IFG.7 (see Notes 1 & 2)	Maskable	0FFE2h	1
Basic Timer1	BTIFG	Maskable	0FFE0h	0, lowest

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module.
3. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt-enable cannot.

special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

Address	7	6	5	4	3	2	1	0
01h	BTIE							
	rw-0							

WDTIE: Watchdog-timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.

OFIE: Oscillator-fault-interrupt enable

NMIIE: Nonmaskable-interrupt enable

ACCVIE: Flash access violation interrupt enable

BTIE: Basic Timer1 interrupt enable

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG			OFIFG	WDTIFG
				rw-0			rw-1	rw-(0)

Address	7	6	5	4	3	2	1	0
03h	BTIFG							
	rw-0							

WDTIFG: Set on watchdog-timer overflow (in watchdog mode) or security key violation. Reset with V_{CC} power-up, or a reset condition at the $\overline{RST}$/NMI pin in reset mode.

OFIFG: Flag set on oscillator fault

NMIIFG: Set via $\overline{RST}$/NMI pin

BTIFG: Basic Timer1 interrupt flag

module enable registers 1 and 2

Address	7	6	5	4	3	2	1	0
04h/05h								

Legend:

rw:	Bit Can Be Read and Written
rw-0,1:	Bit Can Be Read and Written. It Is Reset or Set by PUC.
rw-(0,1):	Bit Can Be Read and Written. It Is Reset or Set by POR.
(shaded box)	SFR Bit Not Present in Device

memory organization

		MSP430FW423	MSP430FW425	MSP430FW427
Memory Interrupt vector Code memory	Size Flash Flash	8KB 0FFFFh – 0FFE0h 0FFFFh – 0E000h	16KB 0FFFFh – 0FFE0h 0FFFFh – 0C000h	32KB 0FFFFh – 0FFE0h 0FFFFh – 08000h
Information memory	Size	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h
Boot memory	Size	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h
RAM	Size	256 Byte 02FFh – 0200h	512 Byte 03FFh – 0200h	1KB 05FFh – 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h

bootstrap loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the Application report *Features of the MSP430 Bootstrap Loader*, Literature Number SLAA089.

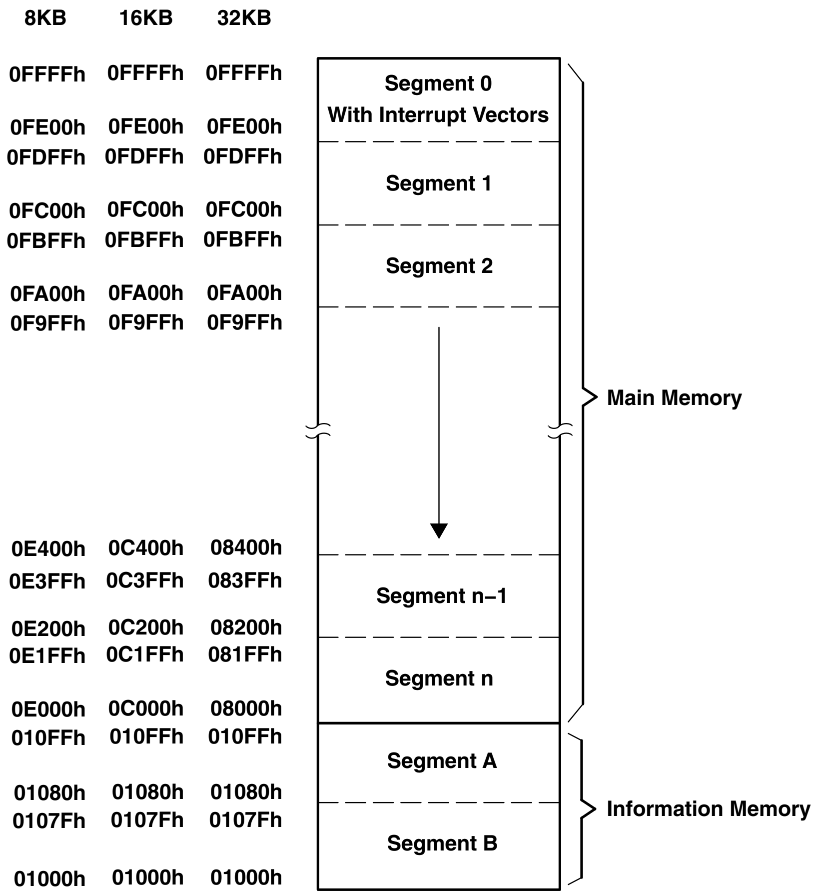
BSL Function	PM Package Pins
Data Transmit	53 - P1.0
Data Receive	52 - P1.1

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0–n.
  Segments A and B are also called *information memory.*
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.

flash memory (continued)



peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x4xx Family User's Guide*, literature number SLAU056.

oscillator and system clock

The clock system in the MSP430xW42x family of devices is supported by the FLL+ module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The FLL+ clock module is designed to meet the requirements of both low system cost and low-power consumption. The FLL+ features a digital frequency locked loop (FLL) hardware which in conjunction with a digital modulator stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 µs. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8.

brownout, supply voltage supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must insure the default FLL+ settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

digital I/O

There are six 8-bit I/O ports implemented—ports P1 through P6:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.

Basic Timer1

The Basic Timer1 has two independent 8-bit timers which can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. The Basic Timer1 can be used to generate periodic interrupts and clock for the LCD module.

LCD drive

The LCD driver generates the segment and common signals required to drive an LCD display. The LCD controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral.

watchdog timer

The primary function of the watchdog timer (WDT) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

comparator_A

The primary function of the comparator_A module is to support precision slope analog–to–digital conversions, battery–voltage supervision, and monitoring of external analog signals.

scan IF

The scan interface is used to measure linear or rotational motion and supports LC and resistive sensors such as GMR sensors. The scan IF incorporates a $V_{CC}/2$ generator, a comparator, and a 10-bit DAC and supports up to four sensors.

timer0_A3

Timer0_A3 is a 16-bit timer/counter with three capture/compare registers. Timer0_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer0_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer0_A3 Signal Connections

Input Pin Number	Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number
48 - P1.5	TA0CLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
48 - P1.5	$\overline{TA0CLK}$	INCLK			
53 - P1.0	TA0.0	CCI0A	CCR0	TA0.0	53 - P1.0
52 - P1.1	TA0.0	CCI0B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
51 - P1.2	TA0.1	CCI1A	CCR1	TA0.1	51 - P1.2
	CAOUT (internal)	CCI1B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
45 - P2.0	TA0.2	CCI2A	CCR2	TA0.2	45 - P2.0
	ACLK (internal)	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

timer1_A5

Timer1_A5 is a 16-bit timer/counter with five capture/compare registers. Timer1_A5 can support multiple capture/compares, PWM outputs, and interval timing. Timer1_A5 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer1_A5 Signal Connections

Input Pin Number	Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number
32 - P2.5	TA1CLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
32 - P2.5	$\overline{TA1CLK}$	INCLK			
49 - P1.4	TA1.0	CCI0A	CCR0	TA1.0	49 - P1.4
50 - P1.3	TA1.0	CCI0B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
44 - P2.1	TA1.1	CCI1A	CCR1	TA1.1	44 - P2.1
	CAOUT (internal)	CCI1B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
35 - P2.2	TA1.2	CCI2A	CCR2	TA1.2	35 - P2.2
	SIFO0sig (internal)	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
34 - P2.3	TA1.3	CCI3A	CCR3	TA1.3	34 - P2.3
	SIFO1sig (internal)	CCI3B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
33 - P2.4	TA1.4	CCI4A	CCR4	TA1.4	33 - P2.4
	SIFO2sig (internal)	CCI4B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog Timer control	WDTCTL	0120h
Timer1_A5	Timer1_A interrupt vector	TA1IV	011Eh
	Timer1_A control	TA1CTL	0180h
	Capture/compare control 0	TA1CCTL0	0182h
	Capture/compare control 1	TA1CCTL1	0184h
	Capture/compare control 2	TA1CCTL2	0186h
	Capture/compare control 3	TA1CCTL3	0188h
	Capture/compare control 4	TA1CCTL4	018Ah
	Reserved		018Ch
	Reserved		018Eh
	Timer1_A register	TA1R	0190h
	Capture/compare register 0	TA1CCR0	0192h
	Capture/compare register 1	TA1CCR1	0194h
	Capture/compare register 2	TA1CCR2	0196h
	Capture/compare register 3	TA1CCR3	0198h
	Capture/compare register 4	TA1CCR4	019Ah
	Reserved		019Ch
	Reserved		019Eh
Timer0_A3	Timer0_A interrupt vector	TA0IV	012Eh
	Timer0_A control	TA0CTL0	0160h
	Capture/compare control 0	TA0CCTL0	0162h
	Capture/compare control 1	TA0CCTL1	0164h
	Capture/compare control 2	TA0CCTL2	0166h
	Reserved		0168h
	Reserved		016Ah
	Reserved		016Ch
	Reserved		016Eh
	Timer0_A register	TA0R	0170h
	Capture/compare register 0	TA0CCR0	0172h
	Capture/compare register 1	TA0CCR1	0174h
	Capture/compare register 2	TA0CCR2	0176h
	Reserved		0178h
	Reserved		017Ah
	Reserved		017Ch
	Reserved		017Eh
Flash	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h

PERIPHERALS WITH WORD ACCESS (CONTINUED)			
Scan IF	SIF timing state machine 23	SIFTSM23	01FEh
	:	:	:
	SIF timing state machine 0	SIFTSM0	01D0h
	SIF DAC register 7	SIFDACR7	01CEh
	:	:	:
	SIF DAC register 0	SIFDACR0	01C0h
	SIF control register 5	SIFCTL5	01BEh
	SIF control register 4	SIFCTL4	01BCh
	SIF control register 3	SIFCTL3	01BAh
	SIF control register 2	SIFCTL2	01B8h
	SIF control register 1	SIFCTL1	01B6h
	SIF processing state machine vector	SIFPSMV	01B4h
	SIF counter CNT1/2	SIFCNT	01B2h
	Reserved	SIFDEBUG	01B0h
PERIPHERALS WITH BYTE ACCESS			
LCD	LCD memory 20	LCDM20	0A4h
	:	:	:
	LCD memory 16	LCDM16	0A0h
	LCD memory 15	LCDM15	09Fh
	:	:	:
	LCD memory 1	LCDM1	091h
	LCD control and mode	LCDCTL	090h
Comparator_A	Comparator_A port disable	CAPD	05Bh
	Comparator_A control 2	CACTL2	05Ah
	Comparator_A control 1	CACTL1	059h
Brownout, SVS	SVS control register	SVSCTL	056h
FLL+ Clock	FLL+ Control 1	FLL_CTL1	054h
	FLL+ Control 0	FLL_CTL0	053h
	System clock frequency control	SCFQCTL	052h
	System clock frequency integrator	SCFI1	051h
	System clock frequency integrator	SCFI0	050h
Basic Timer1	BT counter 2	BTCNT2	047h
	BT counter 1	BTCNT1	046h
	BT control	BTCTL	040h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

absolute maximum ratings†

Voltage applied at V_{CC} to V_{SS} . . . . –0.3 V to + 4.1 V
Voltage applied to any pin (see Note) . . . . –0.3 V to V_{CC} + 0.3 V
Diode current at any device terminal . . . . ±2 mA
Storage temperature (unprogrammed device) . . . . −55°C to 150°C
Storage temperature (programmed device) . . . . −40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNITS
Supply voltage during program execution (see Note 1), V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$)		MSP430xW42x	1.8		3.6	V
Supply voltage during program execution, SVS enabled, PORON = 1 (see Note 1 and Note 2), V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$)		MSP430xW42x	2.0		3.6	V
Supply voltage during programming flash memory (see Note 1), V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$)		MSP430FW42x	2.7		3.6	V
Supply voltage, V_{SS} ($AV_{SS} = DV_{SS} = V_{SS}$)			0		0	V
Operating free-air temperature range, T_A		MSP430xW42x	–40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 3)	LF selected, XTS_FLL=0	Watch crystal		32768		Hz
	XT1 selected, XTS_FLL=1	Ceramic resonator	450		8000	kHz
	XT1 selected, XTS_FLL=1	Crystal	1000		8000	kHz
Processor frequency (signal MCLK), $f_{(System)}$		V_{CC} = 1.8 V	DC		4.15	MHz
		V_{CC} = 3.6 V	DC		8	

NOTES: 1. It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V betweeen AV_{CC} and DV_{CC} can be tolerated during power up and operation.
2. The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing supply voltage. POR is going inactive when the supply voltage is raised above minimum supply voltage plus the hysteresis of the SVS circuitry.
3. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.

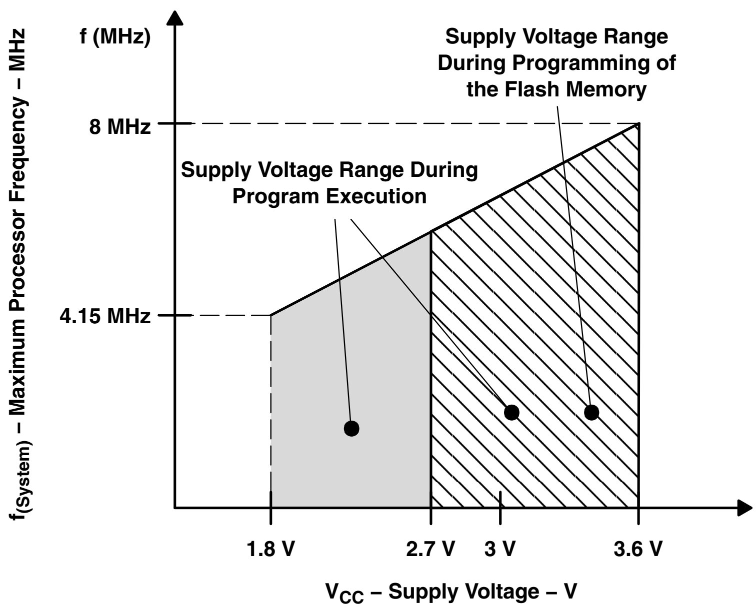


Figure 1. Maximum Frequency vs Supply Voltage

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AV_{CC} + DV_{CC} excluding external current, (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode, $f_{(MCLK)} = f_{(SMCLK)} = f_{(DCO)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz, XTS_FLL = 0 (FW42x: Program executes in flash)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		200	250	µA
			V_{CC} = 3 V		300	350	
$I_{(LPM0)}$	Low-power mode, (LPM0) $f_{(MCLK)} = f_{(SMCLK)} = f_{(DCO)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz, XTS_FLL = 0 FN_8=FN_4=FN_3=FN_2=0 (see Note 3)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		57	70	µA
			V_{CC} = 3 V		92	100	
$I_{(LPM2)}$	Low-power mode, (LPM2) (see Note 3)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		11	14	µA
			V_{CC} = 3 V		17	22	
$I_{(LPM3)}$	Low-power mode, (LPM3) (see Note 2 and Note 3)	T_A = –40°C	V_{CC} = 2.2 V		0.95	1.4	µA
		T_A = –10°C			0.8	1.3	
		T_A = 25°C			0.7	1.2	
		T_A = 60°C			0.95	1.4	
		T_A = 85°C			1.6	2.3	
		T_A = –40°C	V_{CC} = 3 V		1.1	1.7	
		T_A = –10°C			1.0	1.6	
		T_A = 25°C			0.9	1.5	
		T_A = 60°C			1.1	1.7	
		T_A = 85°C			2.0	2.6	
$I_{(LPM4)}$	Low-power mode, (LPM4) (see Note 3)	T_A = –40°C	V_{CC} = 2.2 V/3 V		0.1	0.5	µA
		T_A = 25°C			0.1	0.5	
		T_A = 85°C			0.8	2.5	

NOTES: 1. All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current. The current consumption is measured with active Basic Timer1 and LCD (ACLK selected).
The current consumption of the Comparator_A and the SVS module are specified in the respective sections.
2. The LPM3 currents are characterized with a KDS Daishinku DT−38 (6 pF) crystal.
3. Current for brownout included.

current consumption of active mode versus system frequency

$$I_{(AM)} = I_{(AM)\,[1\,MHz]} \times f_{(System)\,[MHz]}$$

current consumption of active mode versus supply voltage

$$I_{(AM)} = I_{(AM)\,[3\,V]} + 140\ \mu A/V \times (V_{CC} - 3\ V)$$

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs – Ports P1, P2, P3, P4, P5, and P6; $\overline{RST}$/NMI; JTAG: TCK, TMS, TDI/TCLK

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.5	V
		V_{CC} = 3 V	1.5		1.9	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	0.9		1.3	
V_{hys}	Input voltage hysteresis ($V_{IT+} – V_{IT-}$)	V_{CC} = 2.2 V	0.3		1.1	V
		V_{CC} = 3 V	0.45		1	

inputs Px.x, TAx.x

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger signal for the interrupt flag, (see Note 1)	2.2 V/3 V	1.5			cycle
			2.2 V	62			ns
			3 V	50			
$t_{(cap)}$	Timer_A, capture timing	TAx.x	2.2 V	62			ns
			3 V	50			
$f_{(TAext)}$	Timer_A clock frequency externally applied to pin	TAxCLK, INCLK $t_{(H)} = t_{(L)}$	2.2 V			8	MHz
			3 V			10	
$f_{(TAint)}$	Timer_A clock frequency	SMCLK or ACLK signal selected	2.2 V			8	MHz
			3 V			10	

NOTES: 1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ cycle and time parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$. Both the cycle and timing specifications must be met to ensure the flag is set. $t_{(int)}$ is measured in MCLK cycles.

leakage current – Ports P1, P2, P3, P4, P5, and P6 (see Note 1)

PARAMETER			TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{lkg(Px.x)}$	Leakage current	Port Px	Port x: $V_{(Px.x)}$ (see Note 2)	V_{CC} = 2.2 V/3 V			±50	nA

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as an input.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – Ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{CC}–0.25		V_{CC}	V
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{CC}–0.6		V_{CC}	
		$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{CC}–0.25		V_{CC}	
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 3 V,	See Note 2	V_{CC}–0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{SS}		V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{SS}		V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{SS}		V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 3 V,	See Note 2	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±24 mA to satisfy the maximum specified voltage drop.

output frequency

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{Px.y}$	(1 ≤ x ≤ 6, 0 ≤ y ≤ 7)	C_L = 20 pF, I_L = ± 1.5mA	V_{CC} = 2.2 V	DC		10	MHz
			V_{CC} = 3 V	DC		12	
f_{ACLK}, f_{MCLK}, f_{SMCLK}	P1.1/TA0.0/MCLK, P1.5/TA0CLK/ACLK	C_L = 20 pF	V_{CC} = 2.2 V			8	MHz
			V_{CC} = 3 V			12	
t_{Xdc}	Duty cycle of output frequency	P1.5/TA0CLK/ACLK, C_L = 20 pF V_{CC} = 2.2 V / 3 V	$f_{ACLK} = f_{LFXT1} = f_{XT1}$	40%		60%	
			$f_{ACLK} = f_{LFXT1} = f_{LF}$	30%		70%	
			$f_{ACLK} = f_{LFXT1/n}$		50%		
		P1.1/TA0.0/MCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{MCLK} = f_{LFXT1/n}$	50%– 15 ns	50%	50%+ 15 ns	
			$f_{MCLK} = f_{DCOCLK}$	50%– 15 ns	50%	50%+ 15 ns	

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs − Ports P1, P2, P3, P4, P5, and P6 (continued)

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

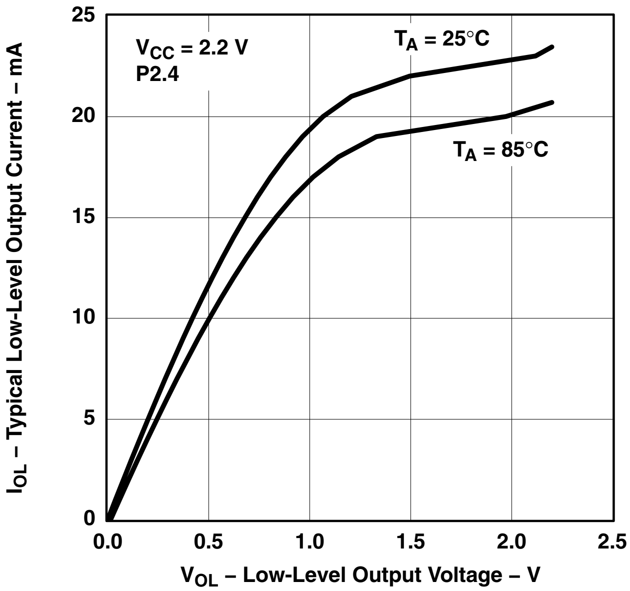


Figure 2

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

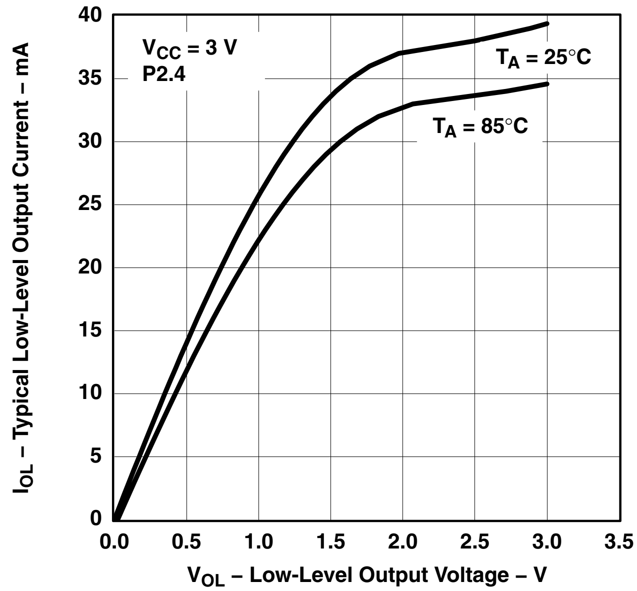


Figure 3

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

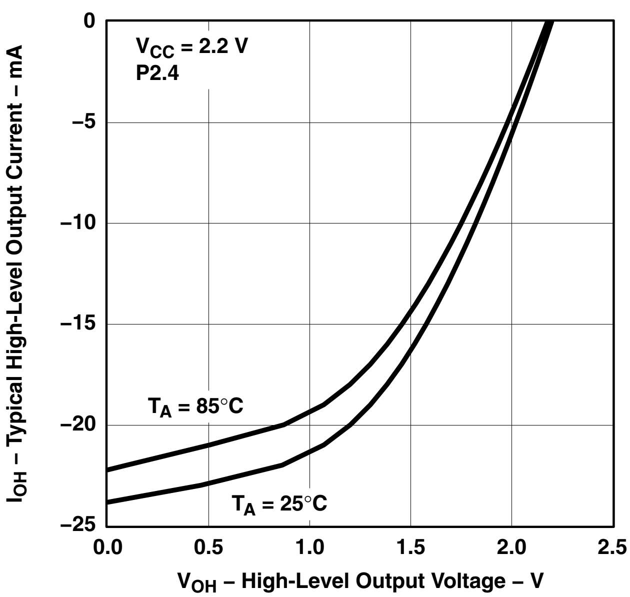


Figure 4

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

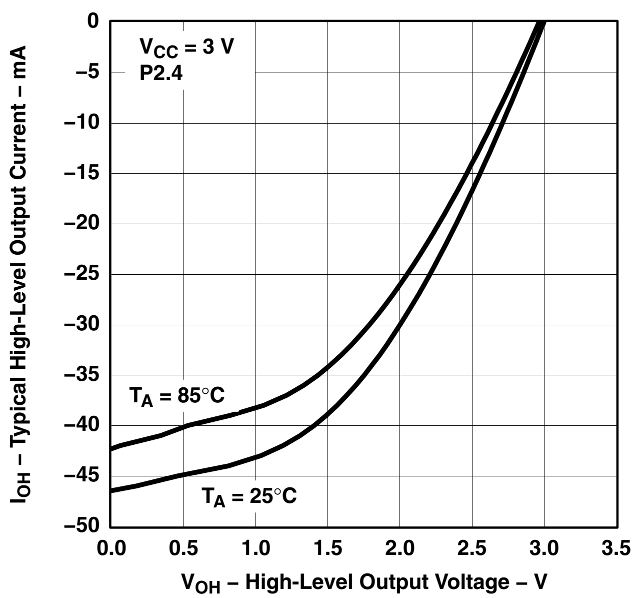


Figure 5

NOTE: One output loaded at a time

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

wake-up LPM3

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(LPM3)}$	Delay time	f = 1 MHz	V_{CC} = 2.2 V/3 V			6	µs
		f = 2 MHz				6	
		f = 3 MHz				6	

RAM (see Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VRAMh	CPU halted (see Note 1)	1.6			V

NOTES: 1. This parameter defines the minimum supply voltage when the data in the program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

LCD

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(33)}$	Analog voltage	Voltage at P5.7/R33	V_{CC} = 3 V	2.5		V_{CC} +0.2	V
$V_{(23)}$		Voltage at P5.6/R23			$(V_{33}–V_{03}) \times 2/3 + V_{03}$		
$V_{(13)}$		Voltage at P5.5/R13			$(V_{(33)}–V_{(03)}) \times 1/3 + V_{(03)}$		
$V_{(33)} – V_{(03)}$		Voltage at R33/R03		2.5		V_{CC} +0.2	
$I_{(R03)}$	Input leakage	R03 = V_{SS}	No load at all segment and common lines, V_{CC} = 3 V			±20	nA
$I_{(R13)}$		P5.5/R13 = $V_{CC}/3$				±20	
$I_{(R23)}$		P5.6/R23 = 2 × $V_{CC}/3$				±20	
$V_{(Sxx0)}$	Segment line voltage	$I_{(Sxx)}$ = −3 µA,	V_{CC} = 3 V	$V_{(03)}$		$V_{(03)}$ – 0.1	V
$V_{(Sxx1)}$				$V_{(13)}$		$V_{(13)}$ – 0.1	
$V_{(Sxx2)}$				$V_{(23)}$		$V_{(23)}$ – 0.1	
$V_{(Sxx3)}$				$V_{(33)}$		$V_{(33)}$ + 0.1	

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Comparator_A (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(CC)}$		CAON = 1, CARSEL = 0, CAREF = 0	V_{CC} = 2.2 V		25	40	µA
			V_{CC} = 3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at P1.6/CA0 and P1.7/CA1	V_{CC} = 2.2 V		30	50	µA
			V_{CC} = 3 V		45	71	
$V_{(Ref025)}$	$\frac{\text{Voltage @ 0.25 } V_{CC} \text{ node}}{V_{CC}}$	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P1.6/CA0 and P1.7/CA1	V_{CC} = 2.2 V / 3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage @ 0.5 } V_{CC} \text{ node}}{V_{CC}}$	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P1.6/CA0 and P1.7/CA1	V_{CC} = 2.2V / 3 V	0.47	0.48	0.50	
$V_{(RefVT)}$	(See Figure 6 and Figure 7)	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P1.6/CA0 and P1.7/CA1; T_A = 85°C	V_{CC} = 2.2 V	390	480	540	mV
			V_{CC} = 3.0 V	400	490	550	
$V_{(IC)}$	Common-mode input voltage range	CAON = 1	V_{CC} = 2. 2V/3 V	0		V_{CC}–1.0	V
$V_{(offset)}$	Offset voltage	See Note 2	VCC = 2.2 V/3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON = 1	V_{CC} = 2.2 V / 3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$		T_A = 25°C, Overdrive 10 mV, without filter: CAF = 0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C Overdrive 10 mV, with filter: CAF = 1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$		T_A = 25°C Overdrive 10 mV, without filter: CAF = 0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, with filter: CAF = 1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3.0 V	0.9	1.5	2.6	

NOTES: 1. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

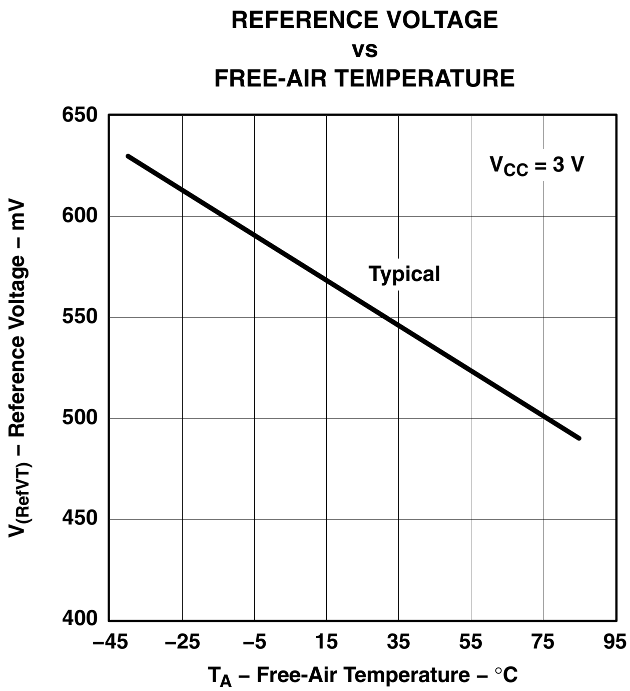


Figure 6

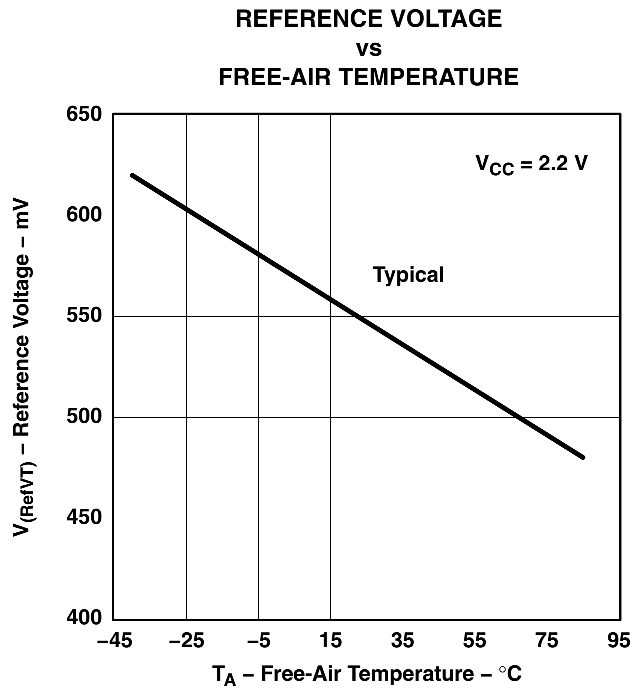


Figure 7

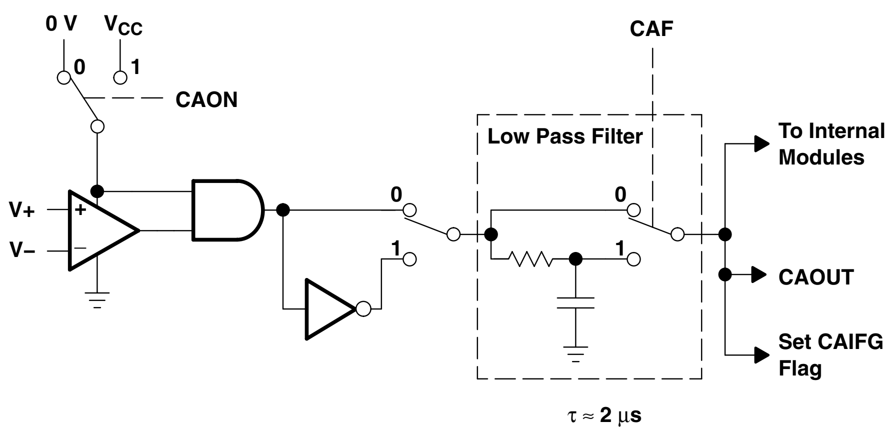


Figure 8. Block Diagram of Comparator_A Module

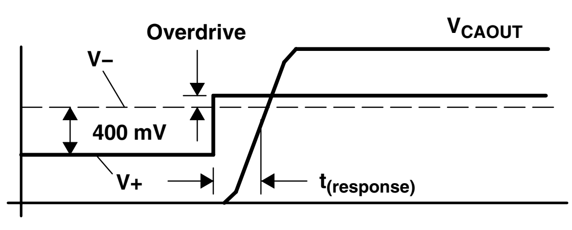


Figure 9. Overdrive Definition

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

POR brownout, reset (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(BOR)}$	Brownout				2000	µs
$V_{CC(start)}$	Brownout	$dV_{CC}/dt \le 3$ V/s (see Figure 10)		$0.7 \times V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$	Brownout	$dV_{CC}/dt \le 3$ V/s (see Figure 10, Figure 11, Figure 12)			1.71	V
$V_{hys(B\_IT-)}$	Brownout	$dV_{CC}/dt \le 3$ V/s (see Figure 10)	70	130	180	mV
$t_{(reset)}$	Brownout	Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally, V_{CC} = 2.2 V/3 V	2			µs

NOTES:
1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.
2. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default FLL+ settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide* (SLAU056) for more information on the brownout/SVS circuit.

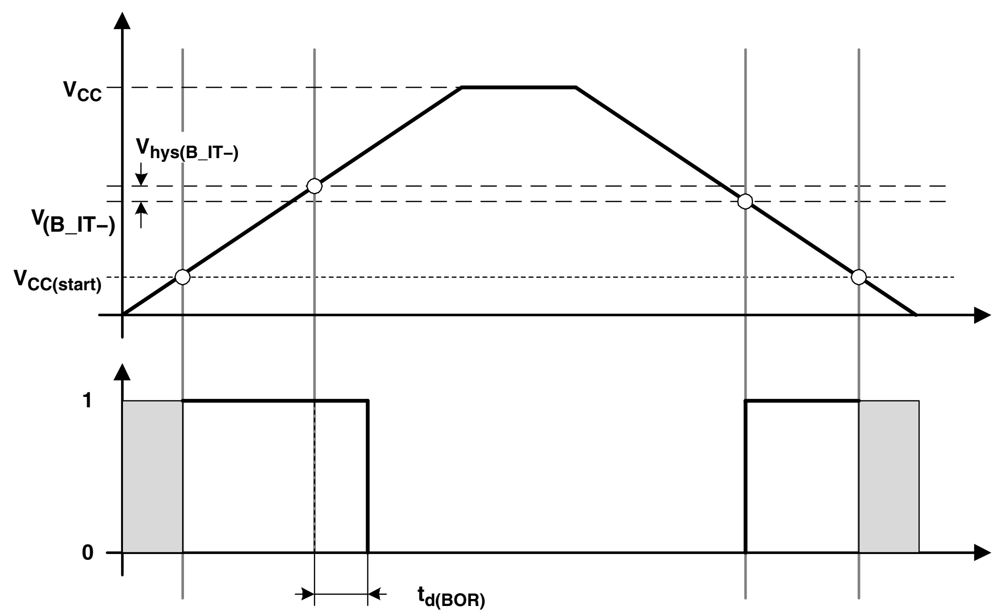


Figure 10. POR/Brownout Reset (BOR) vs Supply Voltage

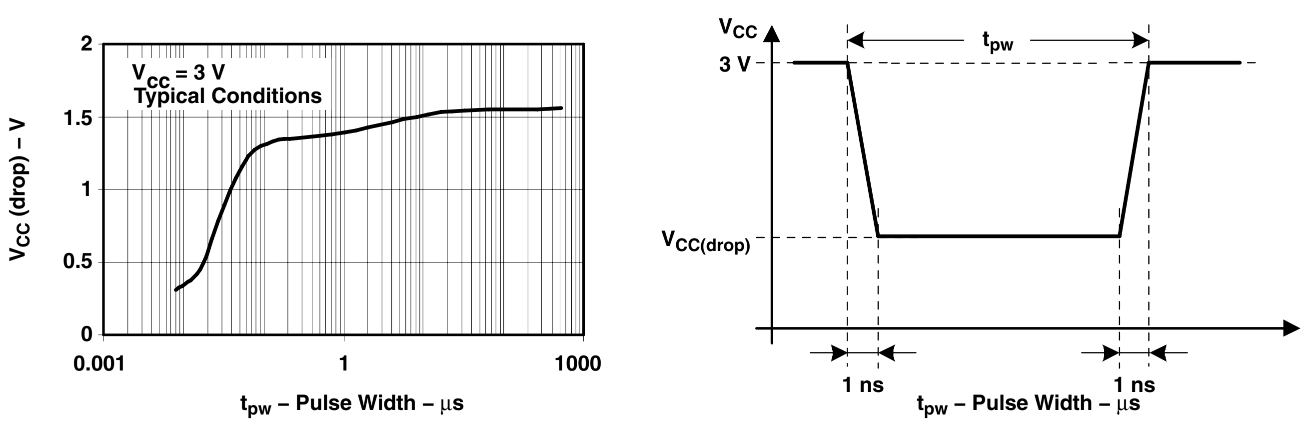


Figure 11. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

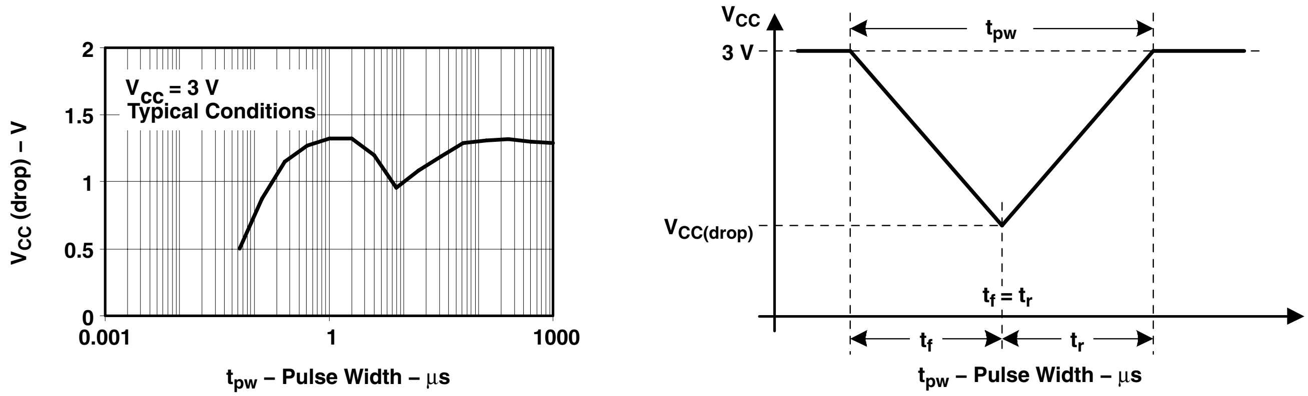


Figure 12. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

SVS (supply voltage supervisor/monitor) (See Notes 1 and 2)

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT
$t_{d(SVSR)}$	$dV_{CC}/dt > 30$ V/ms (see Figure 13)		5		150	µs
	$dV_{CC}/dt \leq 30$ V/ms				2000	µs
$t_{d(SVSon)}$	SVSon, switch from VLD=0 to VLD ≠ 0, V_{CC} = 3 V		20		150	µs
t_{settle}	VLD ≠ 0‡				12	µs
$V_{(SVSstart)}$	VLD ≠ 0, $V_{CC}/dt \leq 3$ V/s (see Figure 13)			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	$V_{CC}/dt \leq 3$ V/s (see Figure 13)	VLD = 1	70	120	155	mV
		VLD = 2 .. 14	$V_{(SVS\_IT-)}$ x 0.004		$V_{(SVS\_IT-)}$ x 0.008	
	$V_{CC}/dt \leq 3$ V/s (see Figure 13), external voltage applied on SVSIN	VLD = 15	4.4		10.4	mV
$V_{(SVS\_IT-)}$	$V_{CC}/dt \leq 3$ V/s (see Figure 13)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.25	
		VLD = 3	2.05	2.2	2.37	
		VLD = 4	2.14	2.3	2.48	
		VLD = 5	2.24	2.4	2.6	
		VLD = 6	2.33	2.5	2.71	
		VLD = 7	2.46	2.65	2.86	
		VLD = 8	2.58	2.8	3	
		VLD = 9	2.69	2.9	3.13	
		VLD = 10	2.83	3.05	3.29	
		VLD = 11	2.94	3.2	3.42	
		VLD = 12	3.11	3.35	3.61†	
		VLD = 13	3.24	3.5	3.76†	
		VLD = 14	3.43	3.7†	3.99†	
	$V_{CC}/dt \leq 3$ V/s (see Figure 13), external voltage applied on SVSIN	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (see Note 1)	VLD ≠ 0, V_{CC} = 2.2 V/3 V			10	15	µA

† The recommended operating voltage range is limited to 3.6 V.

‡ t_{settle} is the settling time that the comparator o/p needs to have a stable level after VLD is switched VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be > 50 mV.

NOTES: 1. The current consumption of the SVS module is not included in the I_{CC} current consumption data.
2. The SVS is not active at power up.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

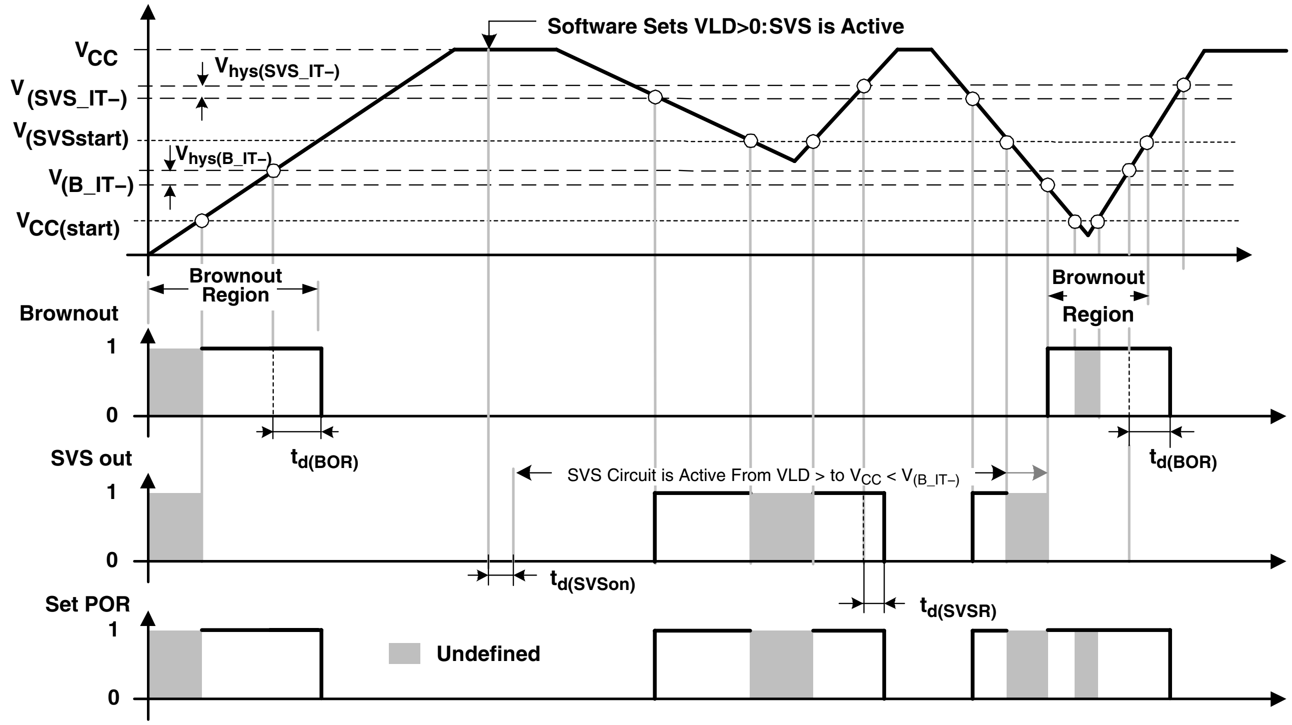


Figure 13. SVS Reset (SVSR) vs Supply Voltage

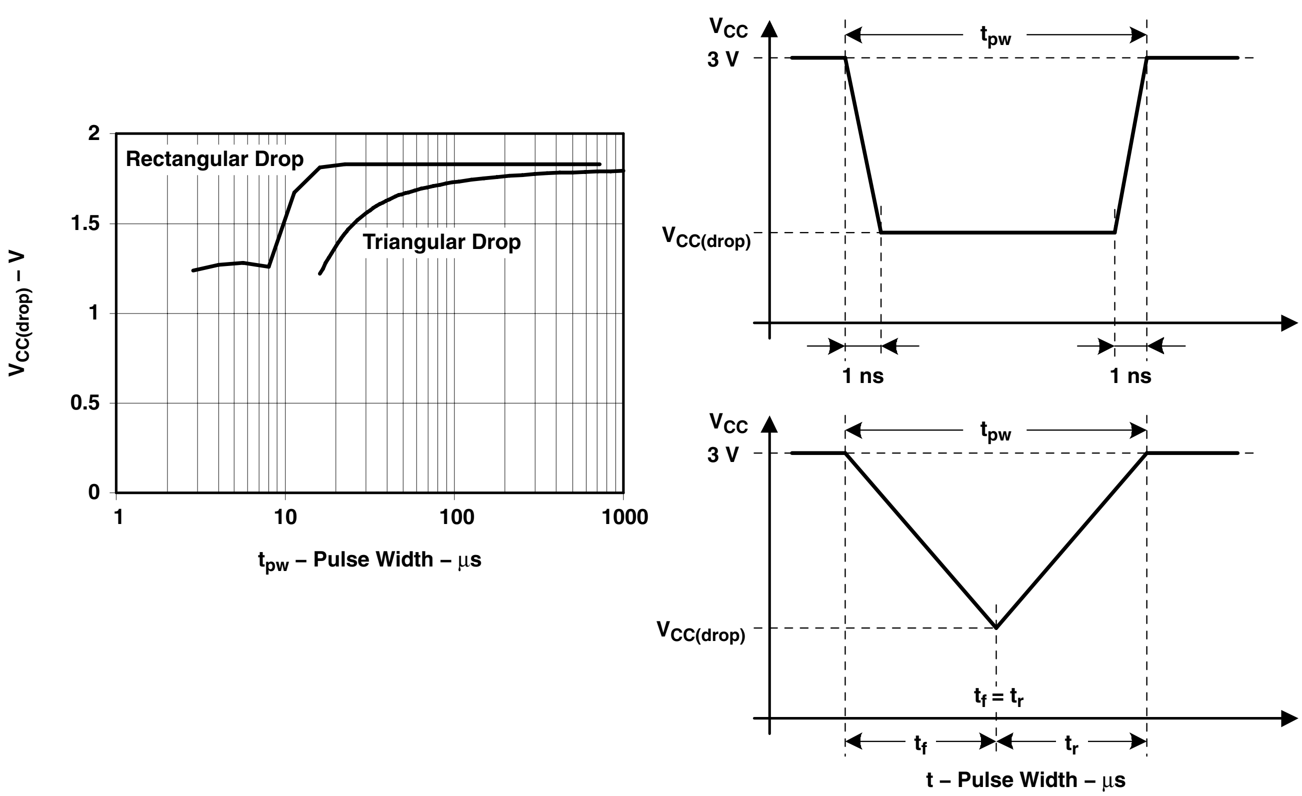


Figure 14. $V_{CC(drop)}$ With a Square Voltage Drop and a Triangle Voltage Drop to Generate an SVS Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

DCO

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{(DCOCLK)}$	$N_{(DCO)}$=01Eh, FN_8=FN_4=FN_3=FN_2=0, D = 2, DCOPLUS= 0, $f_{Crystal}$ = 32.738 kHz	2.2 V/3 V		1		MHz
$f_{(DCO=2)}$	FN_8=FN_4=FN_3=FN_2=0 , DCOPLUS = 1	2.2 V	0.3	0.65	1.25	MHz
		3 V	0.3	0.7	1.3	
$f_{(DCO=27)}$	FN_8=FN_4=FN_3=FN_2=0, DCOPLUS = 1	2.2 V	2.5	5.6	10.5	MHz
		3 V	2.7	6.1	11.3	
$f_{(DCO=2)}$	FN_8=FN_4=FN_3=0, FN_2=1; DCOPLUS = 1	2.2 V	0.7	1.3	2.3	MHz
		3 V	0.8	1.5	2.5	
$f_{(DCO=27)}$	FN_8=FN_4=FN_3=0, FN_2=1; DCOPLUS = 1	2.2 V	5.7	10.8	18	MHz
		3 V	6.5	12.1	20	
$f_{(DCO=2)}$	FN_8=FN_4=0, FN_3= 1, FN_2=x; DCOPLUS = 1	2.2 V	1.2	2	3	MHz
		3 V	1.3	2.2	3.5	
$f_{(DCO=27)}$	FN_8=FN_4=0, FN_3= 1, FN_2=x;, DCOPLUS = 1	2.2 V	9	15.5	25	MHz
		3 V	10.3	17.9	28.5	
$f_{(DCO=2)}$	FN_8=0, FN_4= 1, FN_3= FN_2=x; DCOPLUS = 1	2.2 V	1.8	2.8	4.2	MHz
		3 V	2.1	3.4	5.2	
$f_{(DCO=27)}$	FN_8=0, FN_4=1, FN_3= FN_2=x; DCOPLUS = 1	2.2 V	13.5	21.5	33	MHz
		3 V	16	26.6	41	
$f_{(DCO=2)}$	FN_8=1, FN_4=FN_3=FN_2=x; DCOPLUS = 1	2.2 V	2.8	4.2	6.2	MHz
		3 V	4.2	6.3	9.2	
$f_{(DCO=27)}$	FN_8=1,FN_4=FN_3=FN_2=x,DCOPLUS = 1	2.2 V	21	32	46	MHz
		3 V	30	46	70	
S_n	Step size between adjacent DCO taps: $S_n = f_{DCO(Tap\ n+1)} / f_{DCO(Tap\ n)}$ (see Figure 16 for taps 21 to 27)	1 < TAP ≤ 20	1.06		1.11	
		TAP = 27	1.07		1.17	
D_t	Temperature drift, $N_{(DCO)}$ = 01Eh, FN_8=FN_4=FN_3=FN_2=0 D = 2, DCOPLUS = 0	2.2 V	–0.2	–0.3	–0.4	%/°C
		3 V	–0.2	–0.3	–0.4	
D_V	Drift with V_{CC} variation, $N_{(DCO)}$ = 01Eh, FN_8=FN_4=FN_3=FN_2=0 D = 2, DCOPLUS = 0	2.2 V/3 V	0	5	15	%/V

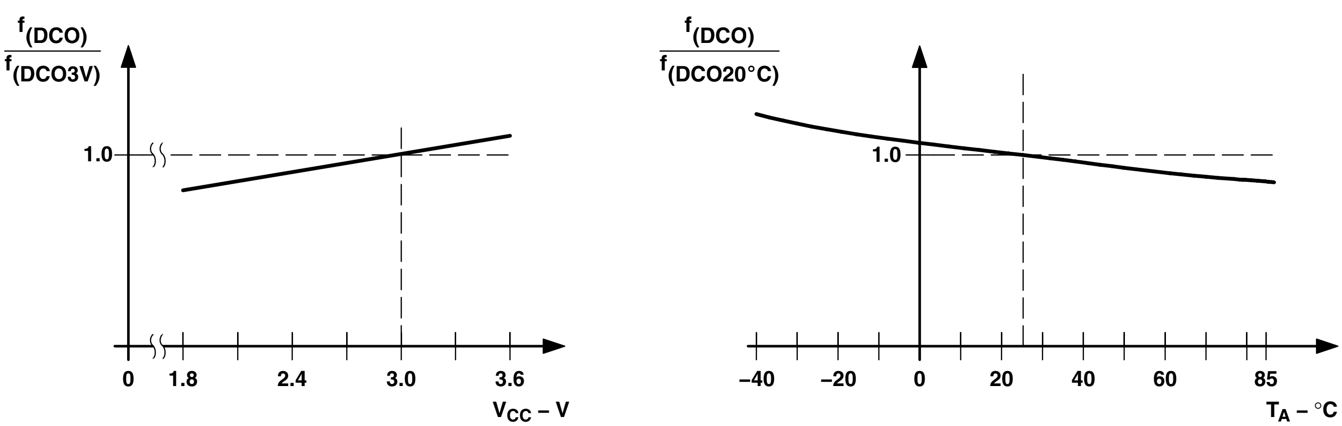


Figure 15. DCO Frequency vs Supply Voltage V_{CC} and vs Ambient Temperature

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

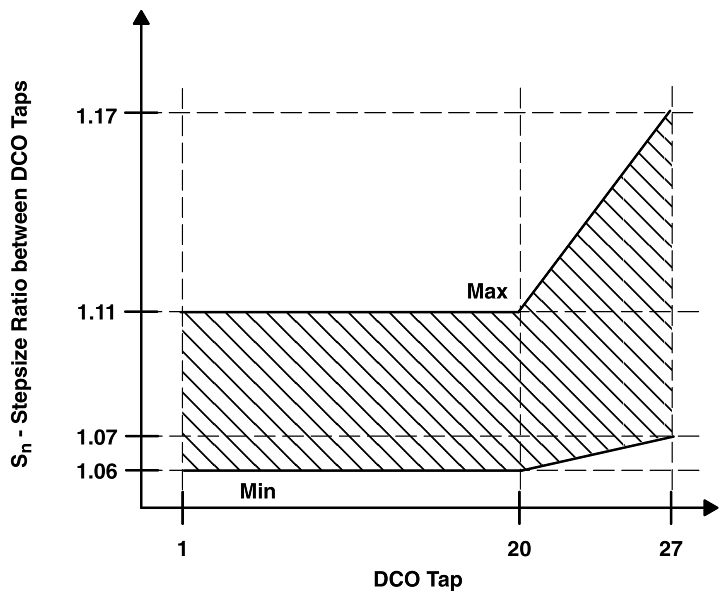


Figure 16. DCO Tap Step Size

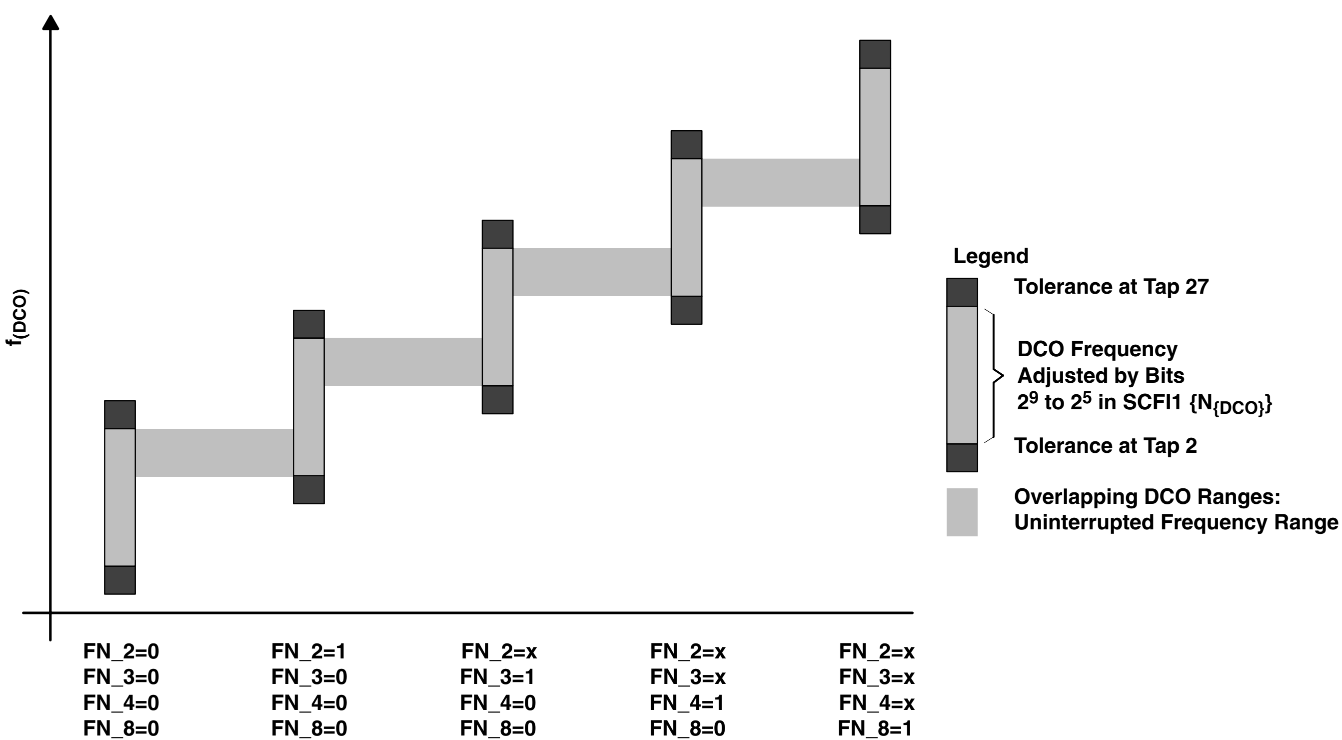


Figure 17. Five Overlapping DCO Ranges Controlled by FN_x Bits

crystal oscillator, LFXT1 oscillator (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{XIN}	Integrated load capacitance	OSCCAPx = 0h	2.2 V/3 V		0		pF
		OSCCAPx = 1h	2.2 V/3 V		10		
		OSCCAPx = 2h	2.2 V/3 V		14		
		OSCCAPx = 3h	2.2 V/3 V		18		
C_{XOUT}	Integrated load capacitance	OSCCAPx = 0h	2.2 V/3 V		0		pF
		OSCCAPx = 1h	2.2 V/3 V		10		
		OSCCAPx = 2h	2.2 V/3 V		14		
		OSCCAPx = 3h	2.2 V/3 V		18		
V_{IL}	Input levels at XIN	see Note 3	2.2 V/3 V	V_{SS}		$0.2{\times}V_{CC}$	V
V_{IH}				$0.8{\times}V_{CC}$		V_{CC}	

NOTES: 1. The parasitic capacitance from the package and board may be estimated to be 2pF. The effective load capacitor for the crystal is (C_{XIN} x C_{XOUT}) / (C_{XIN} + C_{XOUT}). It is independent of XTS_FLL.
2. To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines must be observe:
   - Keep as short a trace as possible between the 'xW42x and the crystal.
   - Design a good ground plane around oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to XIN an XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
3. Applies only when using an external logic-level clock source. XTS_FLL must be set. Not applicable when using a crystal or resonator.
4. External capacitance is recommended for precision real-time clock applications; OSCCAPx = 0h.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Scan IF, port drive, port timing

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{OL(SIFCHx)}$	Voltage drop due to excitation transistor's on–resistance. (see Figure 18)	$I_{(SIFCHx)}$ = 2.0 mA, SIFTEN = 1	3 V			0.3	V
$V_{OH(SIFCHx)}$ (see Note 1)	Voltage drop due to damping transistor's on–resistance. (see Figure 18)	$I_{(SIFCHx)}$ = –200 µA, SIFTEN = 1	3 V			0.1	V
$V_{OL(SIFCOM)}$		$I_{(SIFCOM)}$ = 3 mA, SIFSH = 1	2.2 V/3 V	0		0.1	V
$I_{SIFCHx(tri\text{-}state)}$		$V_{(SIFCHx)}$ = 0 V to AV_{CC}, port function disabled, SIFSH = 1	3 V	–50		50	nA
Δt_{dSIFCH} : $t_{wEx(tsm)}-t_{wSIFCH}$ (see Figure 18)	Change of pulse width of internal signal SIFEX(tsm) to pulse width at pin SIFCHx	$I_{(SIFCHx)}$ = 3 mA, $t_{Ex(SIFCHx)}$ = 500 ns ±20%	2.2 V/3 V	–20		20	ns

NOTE: 1. SIFCOM=1.5V , supplied externally. (See Figure 19).

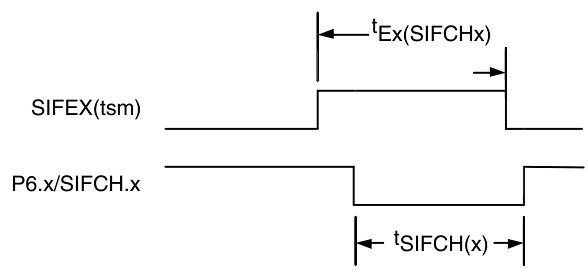


Figure 18. P6.x/SIFCHx timing, SIFCHx function selected

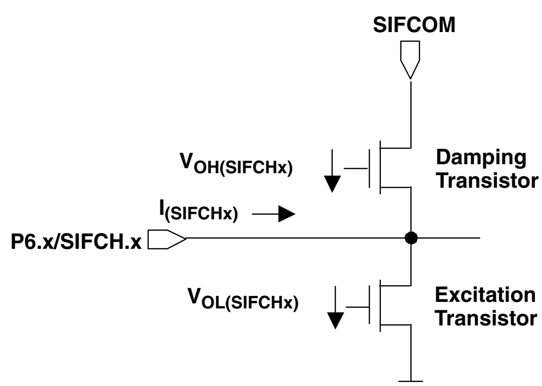


Figure 19. Voltage drop due to on-resistance

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Scan IF, sample capacitor/Ri timing

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$C_{SHC(SIFCHx)}$	Sample capacitance at SIFCHx pin	SIFEx(tsm) = 1, SIFSH = 1	2.2 V/3 V		5	7	pF
$Ri_{(SIFCHx)}$	Serial input resistance at the SIFCHx pin	SIFEx(tsm) = 1, SIFSH = 1	2.2 V/3 V		1.5	3	kΩ
t_{Hold} (See Note 1)	Maximum hold time	ΔV_{sample} < 3 mV		62			µs

NOTES: 1. The sampled voltage at the sample capacitance varies less than 3 mV (ΔV_{sample}) during the hold time $t_{Hold.}$ If the voltage is sampled after t_{Hold}, the sampled voltage may be any other value.
2. The minimum sampling time (7.6 x tau for 1/2 LSB accuracy) with maximum $C_{SHC(SIFCHx)}$ and $Ri_{(SIFCHx)}$ and $Ri_{(source)}$ is $t_{sample(min)}$ ~ 7.6 x $C_{SHC(SIFCHx)}$ x ($Ri_{(SIFCHx)}$ + $Ri_{(source)}$) with $Ri_{(source)}$ estimated at 3 kΩ, $t_{sample(min)}$ = 319 ns.

Scan IF, V_{CC}/2 generator

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} = DV_{CC} (connected together) AV_{SS} = DV_{SS} (connected together)		2.2		3.6	V
AI_{CC}	Scan IF V_{CC}/2 generator operating supply current into AV_{CC} terminal	C_L at SIFCOM pin = 470 nF ±20%, $f_{refresh(SIFCOM)}$ =32768 Hz	2.2 V		250	350	nA
			3 V		370	450	
$f_{refresh(SIFCOM)}$	V_{CC}/2 refresh frequency	Source clock = ACLK	2.2 V/3 V	30	32.768		kHz
$V_{(SIFCOM)}$	Output voltage at pin SIFCOM	C_L at SIFCOM pin = 470 nF ±20%, I_Load = 1µA		AV_{CC}/2 – .05	AV_{CC}/2	AV_{CC}/2 + .05	V
$I_{source(SIFCOM)}$	SIFCOM source current (see Note 2 and Figure 20)		2.2 V	–500			µA
			3 V	–900			
$I_{sink(SIFCOM)}$	SIFCOM sink current (see Note 2 and Figure 20)		2.2 V	150			nA
			3 V	180			
$t_{recovery(SIFCOM)}$	Time to recover from Voltage Drop on Load	I_{Load1} = I_{LOAD3} = 0 mA I_{Load2} = 3 mA, $t_{load(on)}$ = 500nS, C_L at SIFCOM pin = 470 nF ±20%	2.2 V/3 V			30	µs
$t_{on(SIFCOM)}$	Time to reach 98% after V_{CC}/2 is switched on	C_L at SIFCOM pin = 470 nF ±20% $f_{refresh(SIFCOM)}$ = 32768 Hz	2.2 V/3 V		1.7	6	ms
$t_{VccSettle(SIFCOM)}$ (See Note 1)	Settling time to ±V_{CC}/512 (2 LSB) after AV_{CC} voltage change	SIFEN =1, SIFVCC2 =1, SIFSH =0, AV_{CC} = AV_{CC} –100 mV $f_{refresh(SIFCOM)}$ = 32768 Hz	2.2 V/3 V		80		ms
		AV_{CC} = AV_{CC} + 100mV $f_{refresh(SIFCOM)}$ = 32768 Hz	2.2 V/3 V		3		

NOTES: 1. The settling time after an AV_{CC} voltage change is the time to for the voltage at pin SIFCOM to settle to $AV_{CC}/2 \pm$ 2LSB.
2. The sink and source currents are a function of the voltage at the pin SIFCOM. The maximum currents are reached if SIFCOM is shorted to GND or V_{CC}. Due to the topology of the output section (refer to Figure 20) the V_{CC}/2 generator can source relatively large currents but can sink only small currents.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

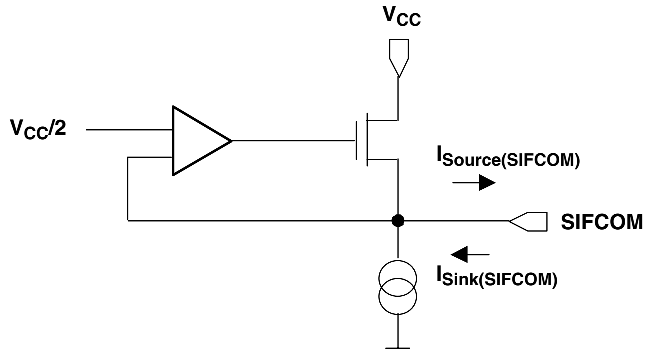


Figure 20. P6.x/SIFCHx timing, SIFCHx function selected

Scan IF, 10-bit DAC (See Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$ (connected together) $AV_{SS} = DV_{SS}$ (connected together)		2.2		3.6	V
AI_{CC}	Scan IF 10-bit DAC operating supply current into AV_{CC} terminal	C_L at SIFCOM pin = 470 nF ±20%, $f_{refresh(SIFCOM)}$ = 32768 Hz	2.2 V		23	45	µA
			3 V		33	60	
Resolution					10		bit
INL	R_L = 1000 MΩ, C_L = 20 pF		2.2 V/3 V		±2	±5	LSB
DNL	R_L = 1000 MΩ, C_L = 20 pF		2.2 V/3 V			±1	LSB
E_{ZS}	Zero Scale Error		2.2 V/3 V			±10	mV
E_G	Gain Error		2.2 V/3 V			0.6	%
R_O	Output resistance				25	50	kΩ
$t_{on(SIFDAC)}$	On time after AV_{CC} of SIFDAC is switched on	$V_{+SIFCA} - V_{SIFDAC}$ = ±6 mV	2.2 V/3 V			2.0	µs
$t_{Settle(SIFDAC)}$	Settling time	SIFDAC code = 1C0h → 240h $V_{SIFDAC(240h)} - V_{+SIFCA}$ = +6 mV	2.2 V/3 V			2.0	µs
		SIFDAC code = 240h → 1C0h, $V_{SIFDAC(1C0h)} - V_{+SIFCA}$ = −6 mV	2.2 V/3 V			2.0	µs

NOTES: 1. The SIFDAC operates from AV_{CC} and $SIFV_{SS}$. All parameters are based on these references.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Scan IF, Comparator

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$ (connected together) $AV_{SS} = DV_{SS}$ (connected together)		2.2		3.6	V
AI_{CC}	Scan IF comparator operating supply current into AV_{CC} terminal		2.2 V		25	35	µA
			3 V		35	50	
V_{IC}	Common Mode Input Voltage Range	(see Note 1)	2.2 V/3 V	0.9		AV_{CC} – 0.5	V
V_{Offset}	Input Offset Voltage		2.2 V/3 V			±30	mV
dV_{Offset}/dT	Temperature coefficient of V_{Offset}		2.2 V/3 V		10		µV/°C
dV_{Offset}/dV_{CC}	V_{Offset} supply voltage (V_{CC}) sensitivity		2.2 V/3 V		0.3		mV/V
V_{hys}	Input Voltage Hysteresis	$V_{+terminal} = V_{-terminal} = 0.5 \times V_{CC}$	2.2V	0		5.0	mV
			3.0V	0		6.0	
$t_{on(SIFCA)}$	On time after SIFCA is switched on	$V_{+SIFCA} - V_{SIFDAC} = +6$ mV $V_{+SIFCA} = 0.5 \times AV_{CC}$	2.2 V/3 V			2.0	us
$t_{Settle(SIFCA)}$	Settle time	$V_{+SIFCA} - V_{SIFDAC} =$ -12 mV → 6 mV $V_{+SIFCA} = 0.5 \times AV_{CC}$	2.2 V/3 V			2.0	us

NOTES: 1. The comparator output is reliable when at least one of the input signals is within the common mode input voltage range.

Scan IF, SIFCLK Oscillator

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$ (connected together) $AV_{SS} = DV_{SS}$ (connected together)		2.2		3.6	V
AI_{CC}	Scan IF oscillator operating supply current into AV_{CC} terminal		2.2 V			75	µA
			3 V			90	
$f_{SIFCLKG} = 0$	Scan IF oscillator at minimum setting	T_A=25°C, SIFCLKFQ=0000	SIFNOM = 0	1.8		3.2	MHz
			SIFNOM = 1	0.45		0.8	
$f_{SIFCLKG} = 8$	Scan IF oscillator at nominal setting	T_A=25°C, SIFCLKFQ=0000	SIFNOM = 0		4		
			SIFNOM = 1		1		
$f_{SIFCLKG} = 15$	Scan IF oscillator at maximum setting	T_A=25°C, SIFCLKFQ=0000	SIFNOM = 0	4.48		6.8	
			SIFNOM = 1	1.12		1.7	
$t_{on(SIFCLKG)}$	Settling time to full operation after V_{CC} is switched on		2.2 V/3 V	150		500	ns
$S_{(SIFCLK)}$	Frequency Change per ±1 $SIFCLKFQ_{(SIFCTL5)}$ step	$S_{(SIFCLK)} = f_{(SIFCLKFQ + 1)} / f_{(SIFCLKFQ)}$	2.2 V/3 V	1.01	1.05	1.18	Hz/Hz
D_t	Temperature Coefficient	$SIFCLKFQ_{(SIFCTL5)} = 8$	2.2 V/3 V			0.35	%/°C
D_V	Frequency vs. supply voltage V_{CC} variation	$SIFCLKFQ_{(SIFCTL5)} = 8$	2.2 V/3 V			2	%/V

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Flash Memory

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and Erase supply voltage			2.7		3.6	V
f_{FTG}	Flash Timing Generator frequency			257		476	kHz
I_{PGM}	Supply current from DV_{CC} during program		2.7 V/ 3.6 V		3	5	mA
I_{ERASE}	Supply current from DV_{CC} during erase		2.7 V/ 3.6 V		3	7	mA
t_{CPT}	Cumulative program time	see Note 1	2.7 V/ 3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time	see Note 2	2.7 V/ 3.6 V	200			ms
	Program/Erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	see Note 3			35		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				30		
$t_{Block, 1-63}$	Block program time for each additional byte or word				21		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				5297		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1 ms (= 5297x1/f_{FTG},max = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
3. These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

JTAG Interface

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
f_{TCK}	TCK input frequency	see Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pull-up resistance on TMS, TCK, TDI/TCLK	see Note 2	2.2 V/ 3 V	25	60	90	kΩ

NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.
2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

JTAG Fuse (see Note 1)

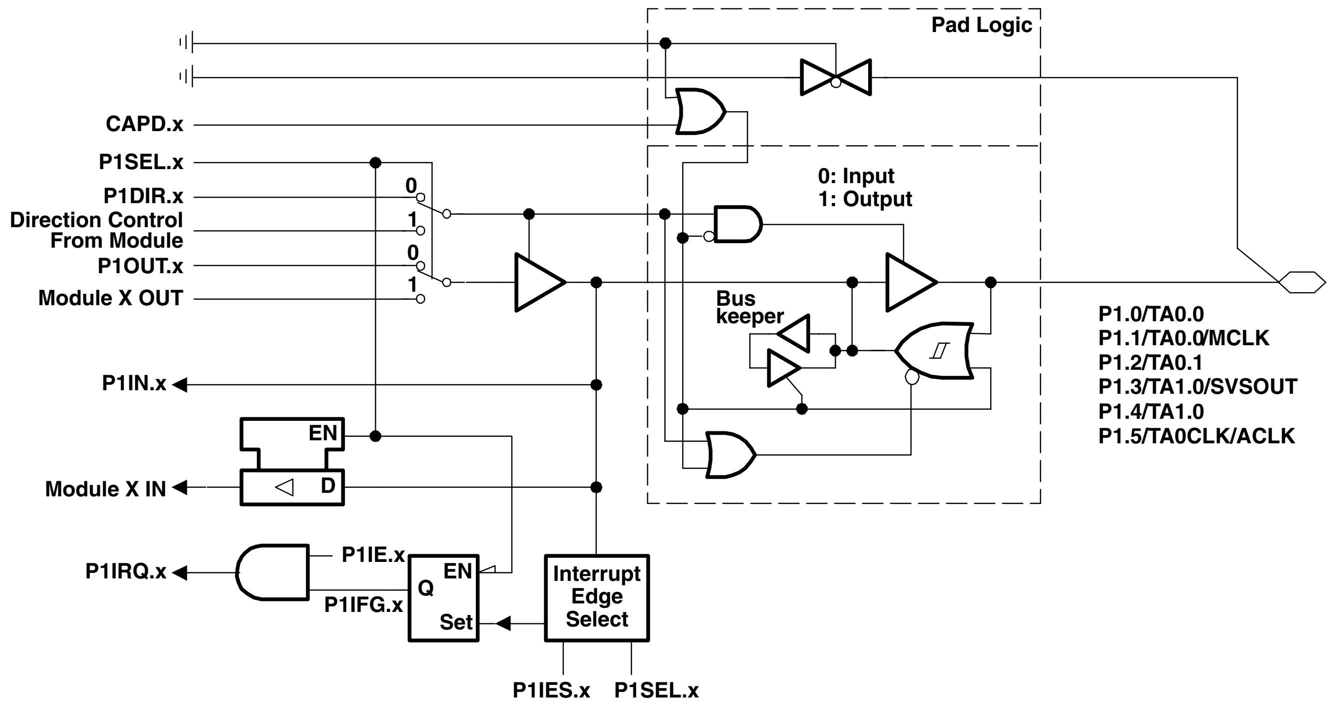
PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C		2.5			V
V_{FB}	Voltage level on TDI/TCLK for fuse-blow			6		7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow					100	mA
t_{FB}	Time to blow fuse					1	ms

NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

APPLICATION INFORMATION

input/output schematic

Port P1, P1.0 to P1.5, input/output with Schmitt-trigger



NOTE: 0 ≤ x ≤ 5.
Port Function is Active if CAPD.x = 0

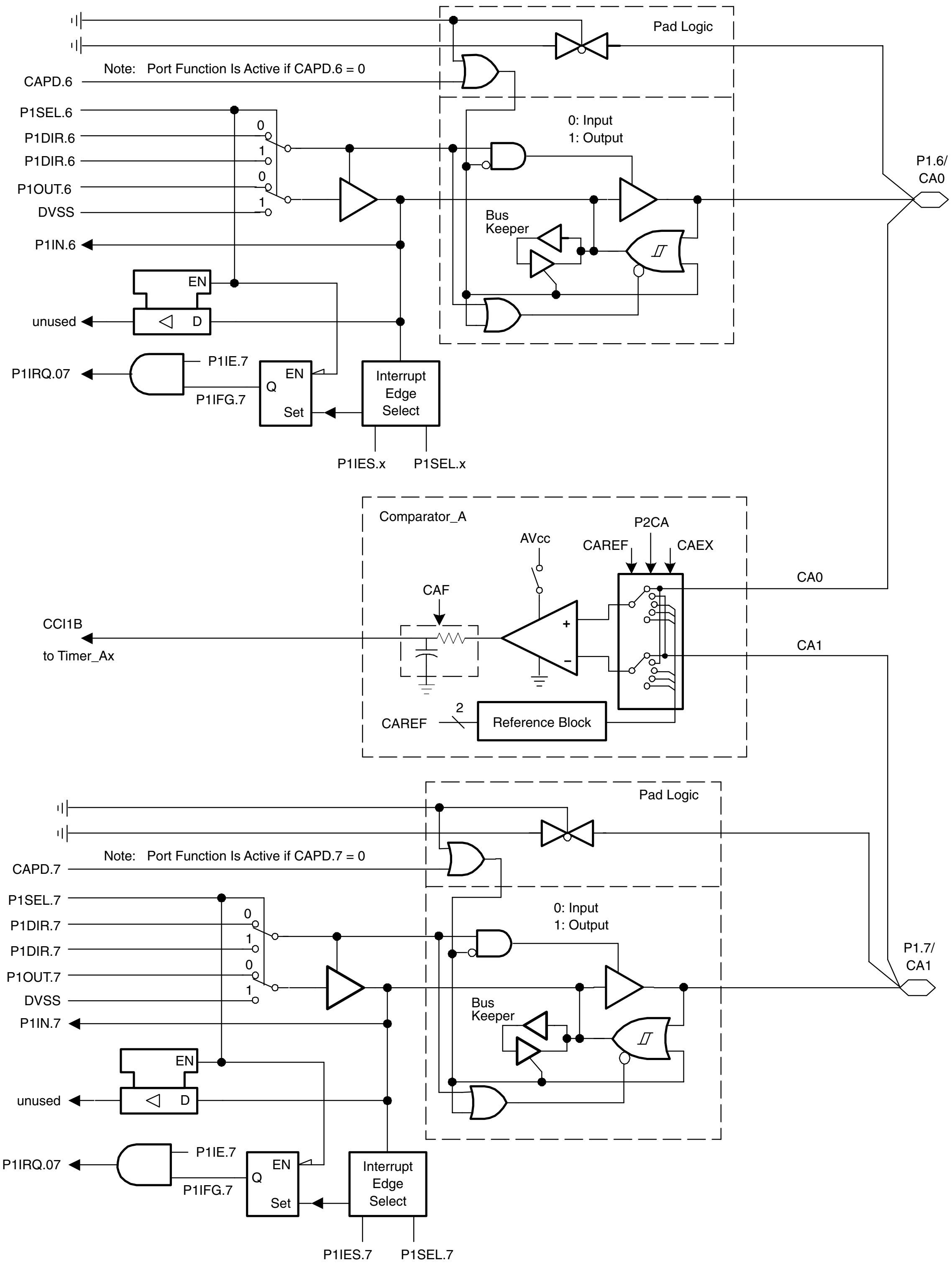
PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P1SEL.0	P1DIR.0	P1DIR.0	P1OUT.0	Out0 Sig.†	P1IN.0	CCI0A†	P1IE.0	P1IFG.0	P1IES.0
P1SEL.1	P1DIR.1	P1DIR.1	P1OUT.1	MCLK	P1IN.1	CCI0B†	P1IE.1	P1IFG.1	P1IES.1
P1SEL.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 Sig.†	P1IN.2	CCI1A†	P1IE.2	P1IFG.2	P1IES.2
P1SEL.3	P1DIR.3	P1DIR.3	P1OUT.3	SVSOUT	P1IN.3	CCI0B‡	P1IE.3	P1IFG.3	P1IES.3
P1SEL.4	P1DIR.4	P1DIR.4	P1OUT.4	Out0 Sig.‡	P1IN.4	CCI0A‡	P1IE.4	P1IFG.4	P1IES.4
P1SEL.5	P1DIR.5	P1DIR.5	P1OUT.5	ACLK	P1IN.5	T0ACLK†	P1IE.5	P1IFG.5	P1IES.5

† Timer0_A
‡ Timer1_A

APPLICATION INFORMATION

input/output schematic (continued)

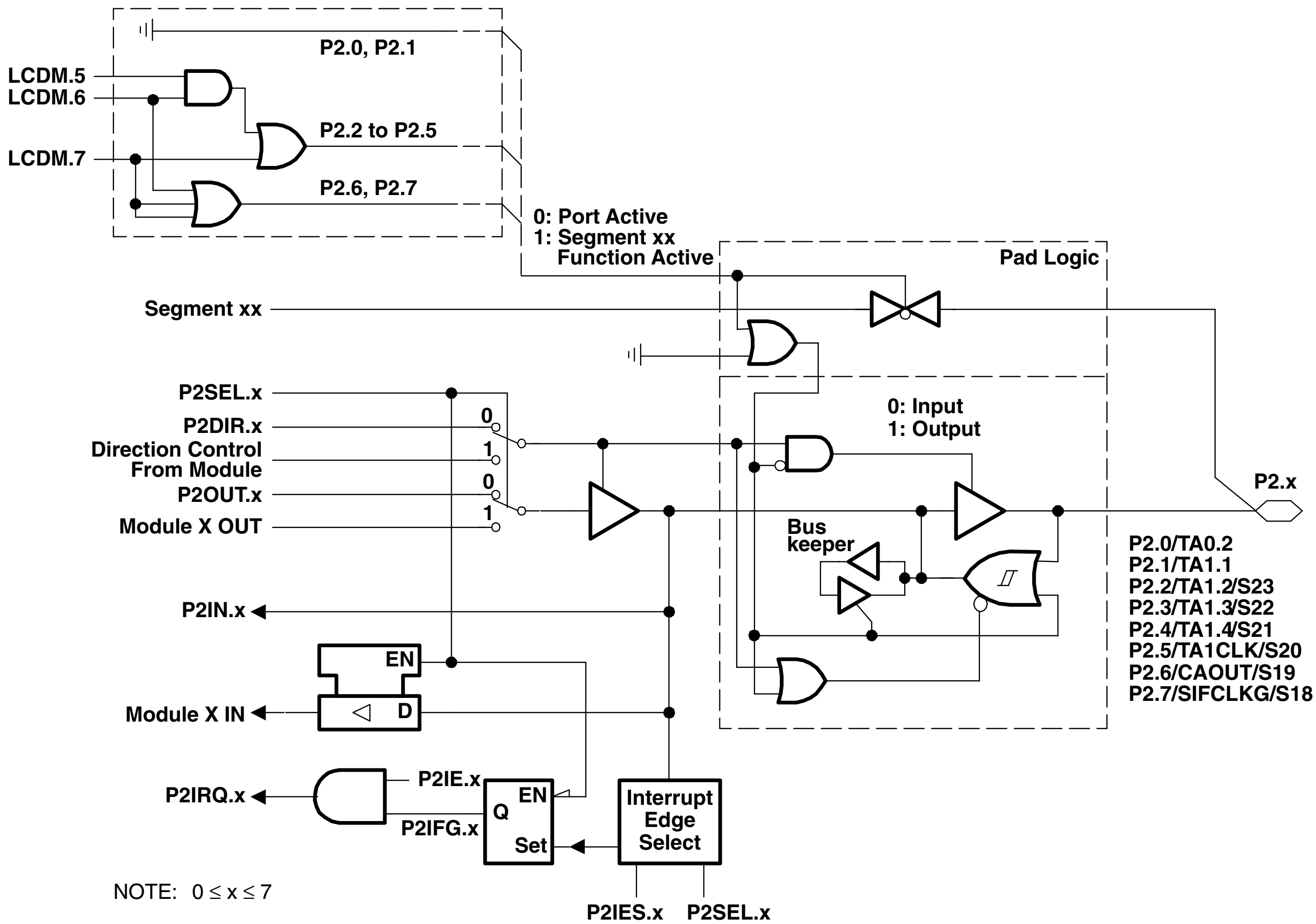
Port P1, P1.6, P1.7 input/output with Schmitt-trigger



APPLICATION INFORMATION

input/output schematic (continued)

port P2, P2.0 to P2.7, input/output with Schmitt-trigger



NOTE: $0 \leq x \leq 7$

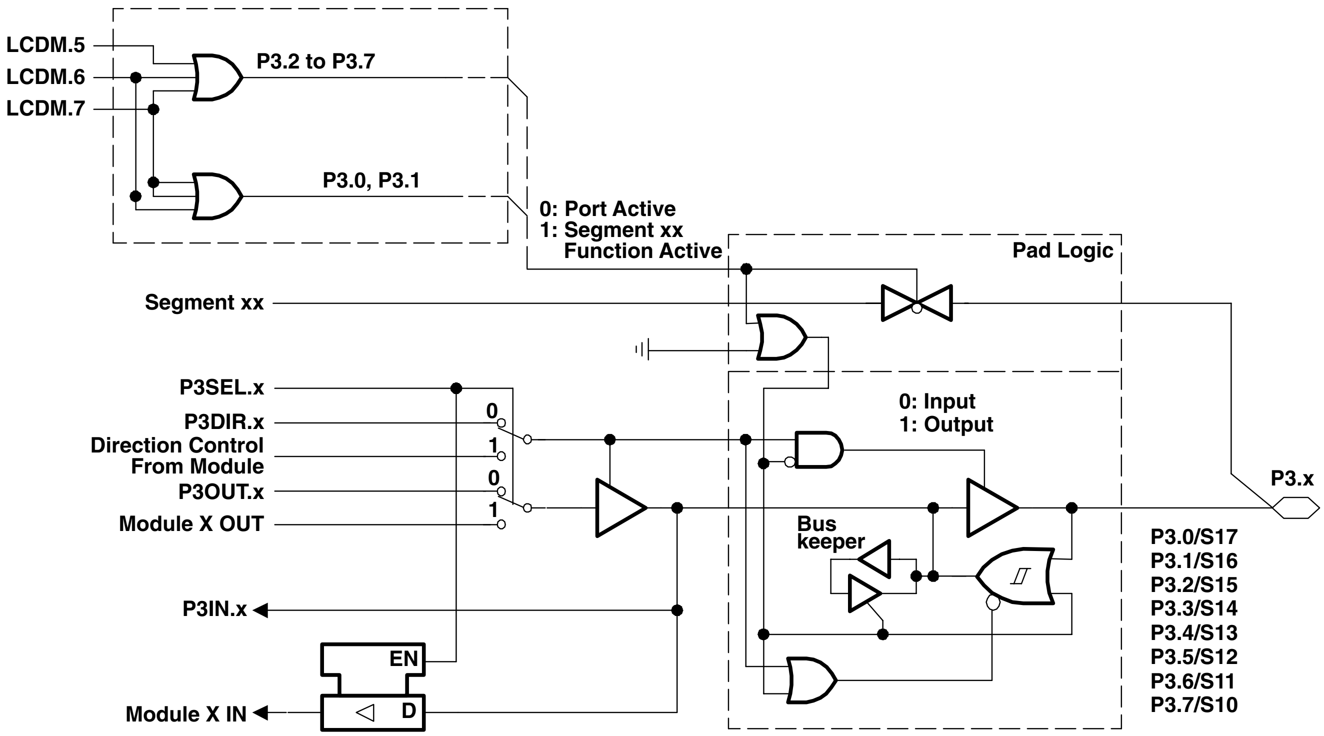
PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2SEL.0	P2DIR.0	P2DIR.0	P2OUT.0	Out2 Sig.†	P2IN.0	CCI2A†	P2IE.0	P2IFG.0	P2IES.0
P2SEL.1	P2DIR.1	P2DIR.1	P2OUT.1	Out1 Sig.‡	P2IN.1	CCI1A‡	P2IE.1	P2IFG.1	P2IES.1
P2SEL.2	P2DIR.2	P2DIR.2	P2OUT.2	Out2 Sig.‡	P2IN.2	CCI2A‡	P2IE.2	P2IFG.2	P2IES.2
P2SEL.3	P2DIR.3	P2DIR.3	P2OUT.3	Out3 Sig.‡	P2IN.3	CCI3A‡	P2IE.3	P2IFG.3	P2IES.3
P2SEL.4	P2DIR.4	P2DIR.4	P2OUT.4	Out4 Sig.‡	P2IN.4	CCI4A‡	P2IE.4	P2IFG.4	P2IES.4
P2SEL.5	P2DIR.5	P2DIR.5	P2OUT.5	DVSS	P2IN.5	TA1CLK1‡	P2IE.5	P2IFG.5	P2IES.5
P2SEL.6	P2DIR.6	P2DIR.6	P2OUT.6	CAOUT	P2IN.6	Unused	P2IE.6	P2IFG.6	P2IES.6
P2SEL.7	P2DIR.7	P2DIR.7	P2OUT.7	SIFCLKG§	P2IN.7	Unused	P2IE.7	P2IFG.7	P2IES.7

†Timer0_A
‡Timer1_A
§Scan IF

APPLICATION INFORMATION

input/output schematic (continued)

port P3, P3.0 to P3.7, input/output with Schmitt-trigger



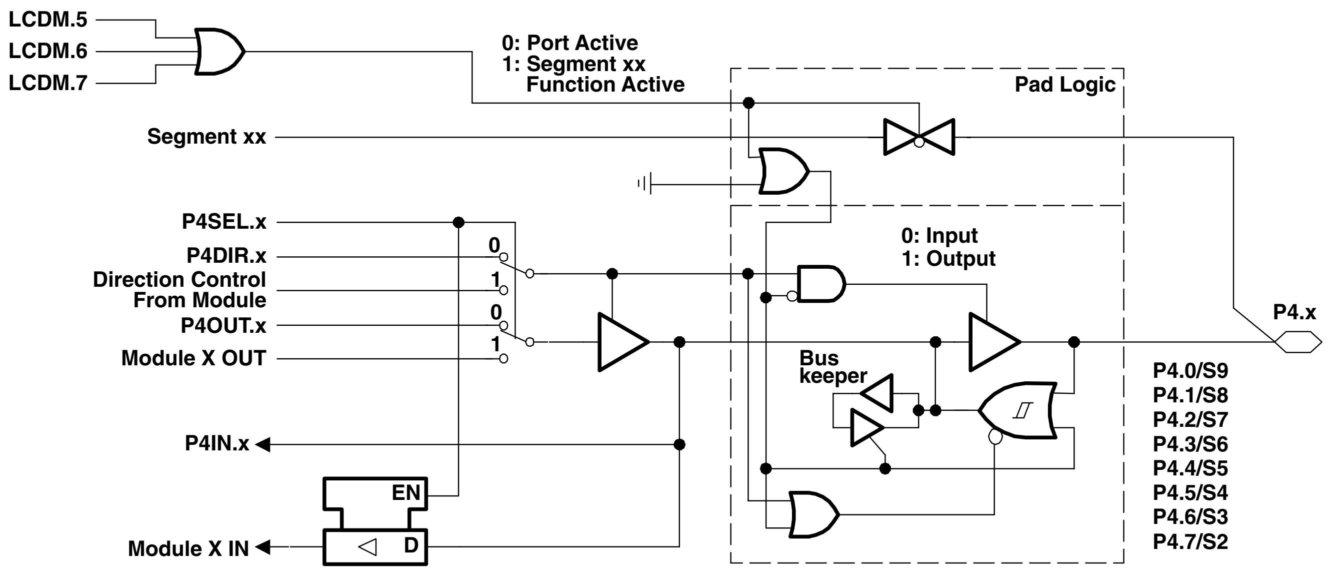
NOTE: $0 \leq x \leq 7$

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P3SEL.0	P3DIR.0	P3DIR.0	P3OUT.0	DVSS	P3IN.0	Unused
P3SEL.1	P3DIR.1	P3DIR.1	P3OUT.1	DVSS	P3IN.1	Unused
P3SEL.2	P3DIR.2	P3DIR.2	P3OUT.2	DVSS	P3IN.2	Unused
P3SEL.3	P3DIR.3	P3DIR.3	P3OUT.3	DVSS	P3IN.3	Unused
P3SEL.4	P3DIR.4	P3DIR.4	P3OUT.4	DVSS	P3IN.4	Unused
P3SEL.5	P3DIR.5	P3DIR.5	P3OUT.5	DVSS	P3IN.5	Unused
P3SEL.6	P3DIR.6	P3DIR.6	P3OUT.6	DVSS	P3IN.6	Unused
P3SEL.7	P3DIR.7	P3DIR.7	P3OUT.7	DVSS	P3IN.7	Unused

APPLICATION INFORMATION

input/output schematic (continued)

port P4, P4.0 to P4.7, input/output with Schmitt-trigger



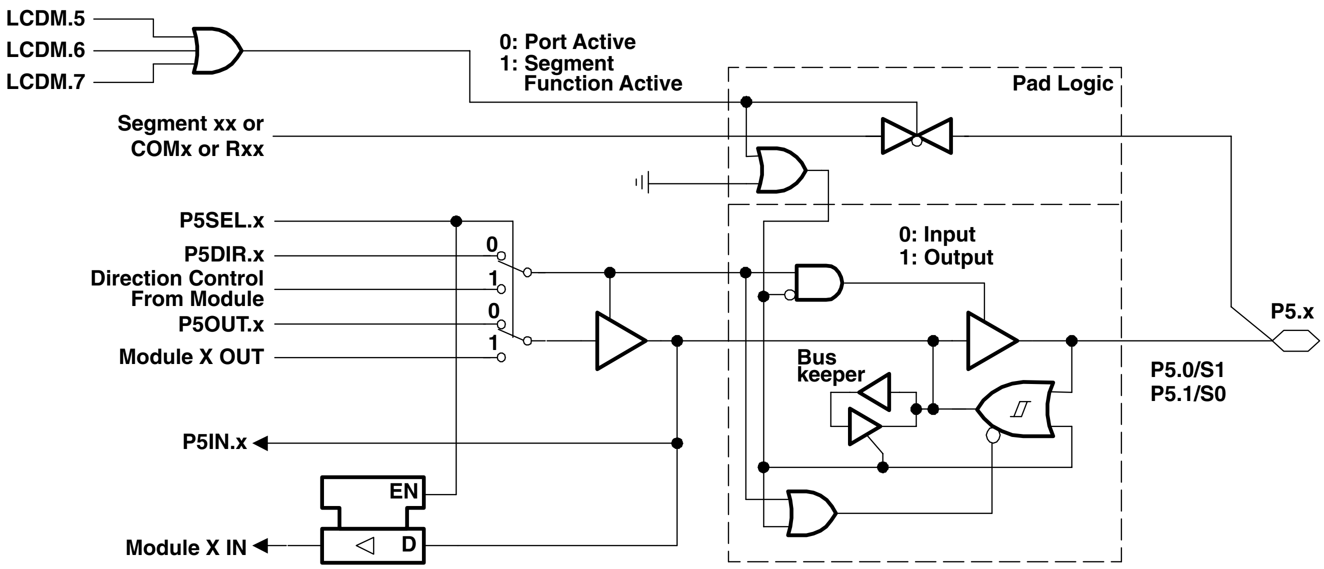
NOTE: 0 ≤ x ≤ 7

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P4SEL.0	P4DIR.0	P4DIR.0	P4OUT.0	DVSS	P4IN.0	Unused
P4SEL.1	P4DIR.1	P4DIR.1	P4OUT.1	DVSS	P4IN.1	Unused
P4SEL.2	P4DIR.2	P4DIR.2	P4OUT.2	DVSS	P4IN.2	Unused
P4SEL.3	P4DIR.3	P4DIR.3	P4OUT.3	DVSS	P4IN.3	Unused
P4SEL.4	P4DIR.4	P4DIR.4	P4OUT.4	DVSS	P4IN.4	Unused
P4SEL.5	P4DIR.5	P4DIR.5	P4OUT.5	DVSS	P4IN.5	Unused
P4SEL.6	P4DIR.6	P4DIR.6	P4OUT.6	DVSS	P4IN.6	Unused
P4SEL.7	P4DIR.7	P4DIR.7	P4OUT.7	DVSS	P4IN.7	Unused

APPLICATION INFORMATION

input/output schematic (continued)

port P5, P5.0, P5.1, input/output with Schmitt-trigger



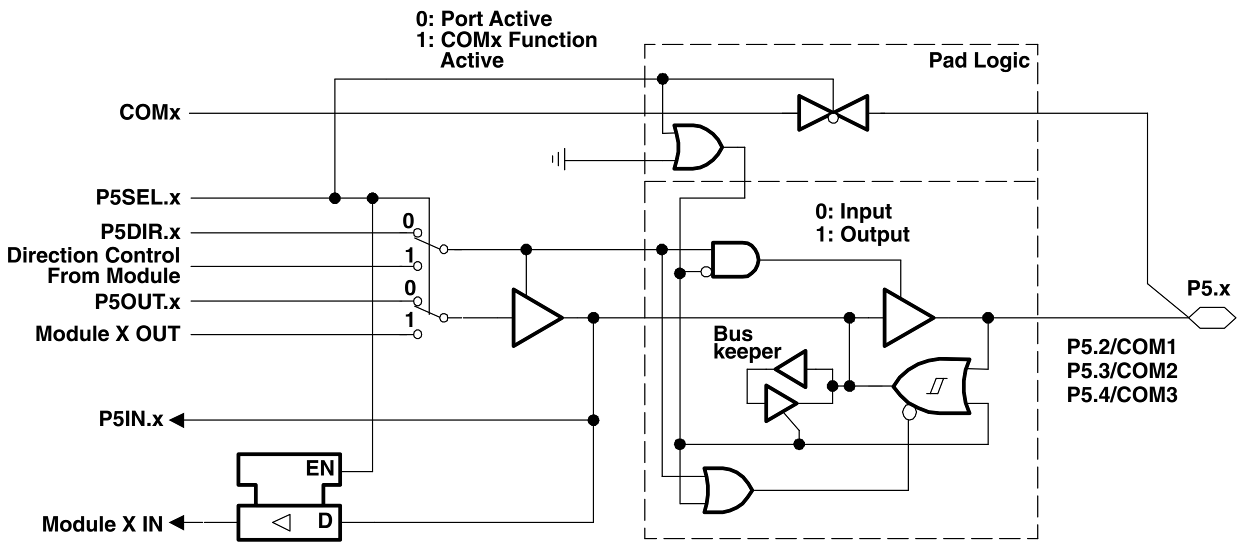
NOTE: x = 0, 1

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	Segment
P5SEL.0	P5DIR.0	P5DIR.0	P5OUT.0	DVSS	P5IN.0	Unused	S1
P5SEL.1	P5DIR.1	P5DIR.1	P5OUT.1	DVSS	P5IN.1	Unused	S0

APPLICATION INFORMATION

input/output schematic (continued)

port P5, P5.2 to P5.4, input/output with Schmitt-trigger



NOTE: $2 \leq x \leq 4$

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	COMx
P5SEL.2	P5DIR.2	P5DIR.2	P5OUT.2	DVSS	P5IN.2	Unused	COM1
P5SEL.3	P5DIR.3	P5DIR.3	P5OUT.3	DVSS	P5IN.3	Unused	COM2
P5SEL.4	P5DIR.4	P5DIR.4	P5OUT.4	DVSS	P5IN.4	Unused	COM3

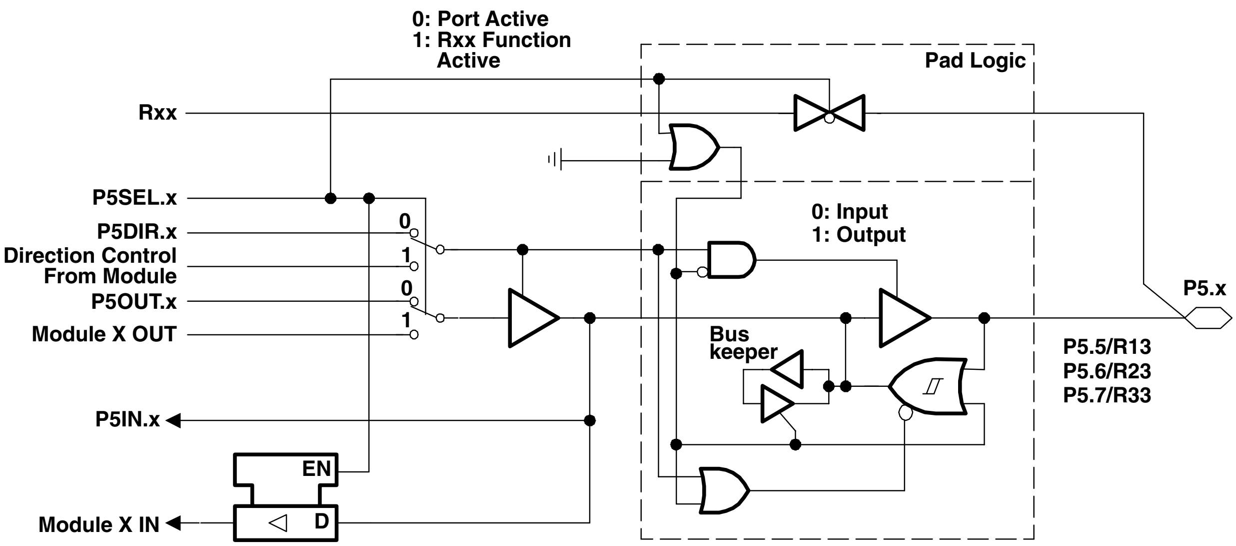
NOTE:

The direction control bits P5SEL.2, P5SEL.3, and P5SEL.4 are used to distinguish between port and common functions. Note that a 4MUX LCD requires all common signals COM3 to COM0, a 3MUX LCD requires COM2 to COM0, 2MUX LCD requires COM1 to COM0, and a static LCD requires only COM0.

APPLICATION INFORMATION

input/output schematic (continued)

port P5, P5.5 to P5.7, input/output with Schmitt-trigger



NOTE: 5 ≤ x ≤ 7

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	Rxx
P5SEL.5	P5DIR.5	P5DIR.5	P5OUT.5	DVSS	P5IN.5	Unused	R13
P5SEL.6	P5DIR.6	P5DIR.6	P5OUT.6	DVSS	P5IN.6	Unused	R23
P5SEL.7	P5DIR.7	P5DIR.7	P5OUT.7	DVSS	P5IN.7	Unused	R33

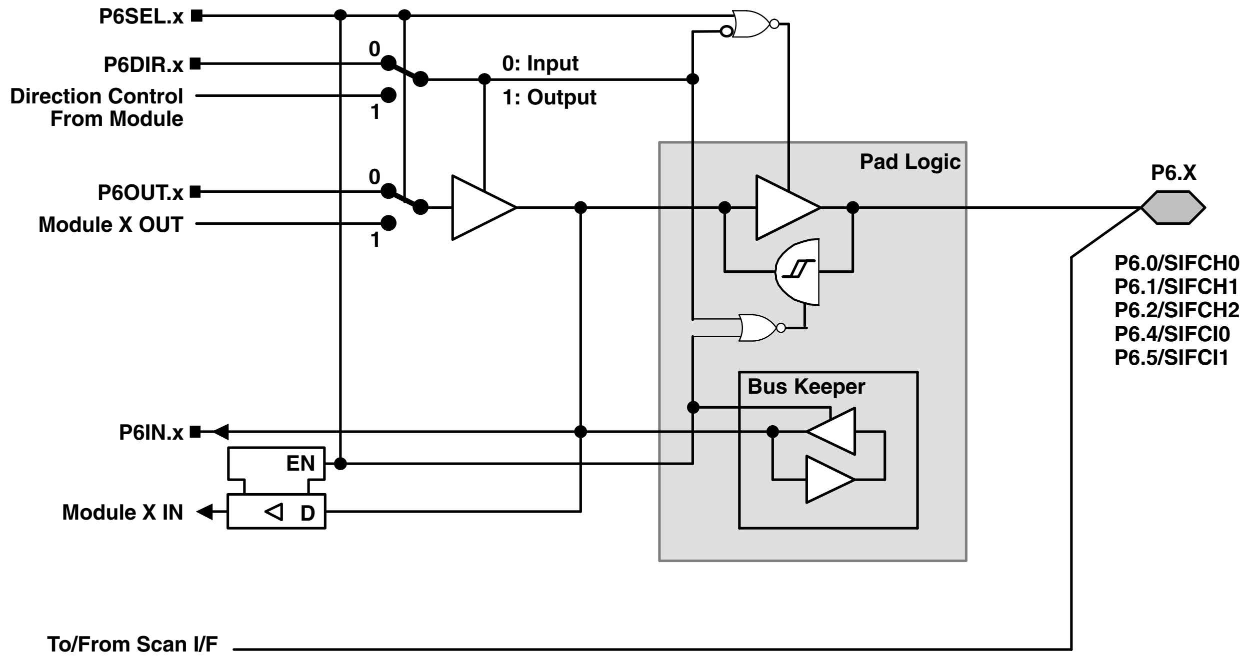
NOTE:

The direction control bits P5SEL.5, P5SEL.6, and P5SEL.7 are used to distinguish between port and LCD analog level functions. Note that 4MUX and 3MUX LCDs require all Rxx signals R33 to R03, a 2MUX LCD requires R33, R13, and R03, and a static LCD requires only R33 and R03.

APPLICATION INFORMATION

input/output schematic (continued)

port P6, P6.0, P6.1, P6.2, P6.4, P6.5, input/output with Schmitt-trigger



P6SEL.x must be set if the corresponding pins are used by the Scan IF.

x: Bit Identifier = 0, 1, 2, 4, or 5

NOTE: Analog signals applied to digital gates can cause current flow from the positive to the negative terminal. The throughput current flows if the analog signal is in the range of transitions 0→1 or 1→0. The value of the throughput current depends on the driving capability of the gate. For MSP430, it is approximately 100 µA.
Use P6SEL.x=1 to prevent throughput current. P6SEL.x should be set, if an analog signal is applied to the pin.

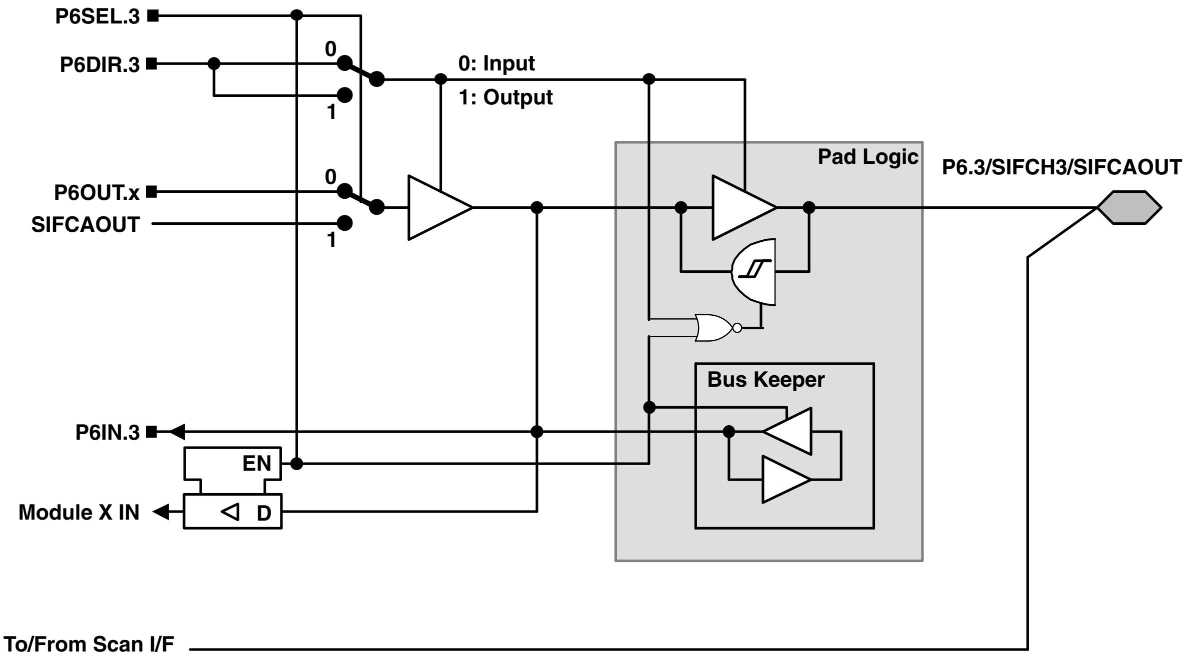
PnSEL.x	PnDIR.x	Dir. Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P6Sel.0	P6DIR.0	P6DIR.0	P6OUT.0	DV_{SS}	P6IN.0	unused
P6Sel.1	P6DIR.1	P6DIR.1	P6OUT.1	DV_{SS}	P6IN.1	unused
P6Sel.2	P6DIR.2	P6DIR.2	P6OUT.2	DV_{SS}	P6IN.2	unused
P6Sel.4	P6DIR.4	P6DIR.4	P6OUT.4	DV_{SS}	P6IN.4	unused
P6Sel.5	P6DIR.5	P6DIR.5	P6OUT.5	DV_{SS}	P6IN.5	unused

NOTE: The signal at pins P6.x/SIFCHx and P6.x/SIFCIx are shared by Port P6 and the San IF module. P6SEL.x must be set if the corresponding pins are used by the Scan IF.

APPLICATION INFORMATION

input/output schematic (continued)

port P6, P6.3 input/output with Schmitt-trigger



P6SEL.x must be set if the corresponding pins are used by the Scan IF.

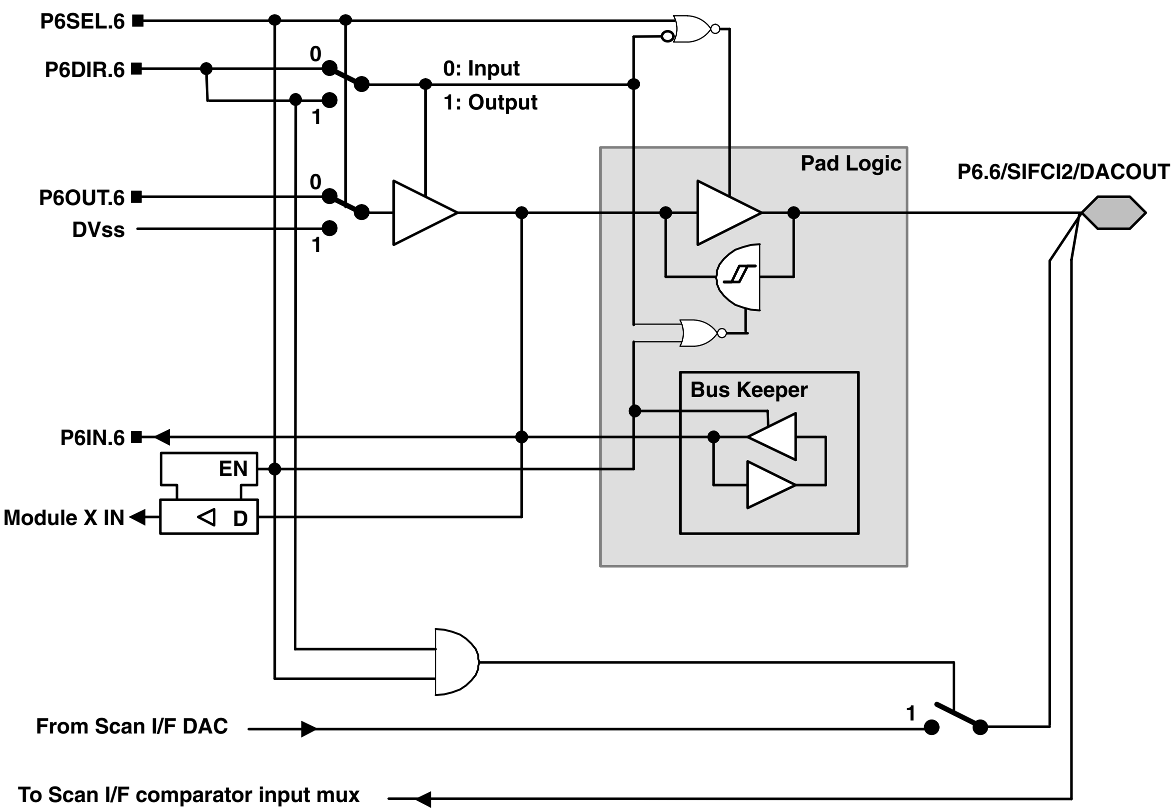
NOTE: Analog signals applied to digital gates can cause current flow from the positive to the negative terminal. The throughput current flows if the analog signal is in the range of transitions 0→1 or 1→0. The value of the throughput current depends on the driving capability of the gate. For MSP430, it is approximately 100 µA.
Use P6SEL.x=1 to prevent throughput current. P6SEL.x should be set, if an analog signal is applied to the pin.

P6SEL.3	P6DIR.3	Port Function
0	0	P6.3 Input
0	1	P6.3 Output
1	0	SIFCH3 (Scan IF channel 3 excitation output and comparator input)
1	1	SIFCAOUT (Comparator output)

APPLICATION INFORMATION

input/output schematic (continued)

port P6, P6.6 input/output with Schmitt-trigger



P6SEL.x must be set if the corresponding pins are used by the Scan IF.

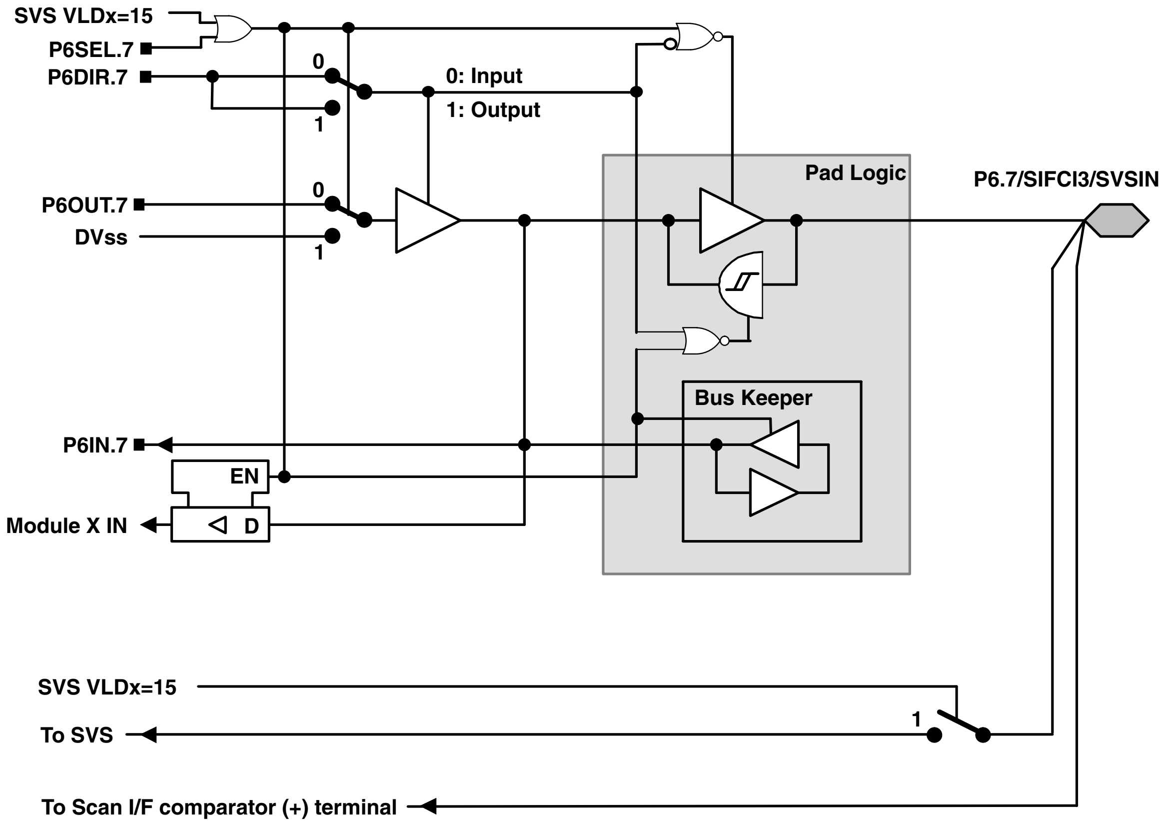
NOTE: Analog signals applied to digital gates can cause current flow from the positive to the negative terminal. The throughput current flows if the analog signal is in the range of transitions 0→1 or 1→0. The value of the throughput current depends on the driving capability of the gate. For MSP430, it is approximately 100 µA.
Use P6SEL.x=1 to prevent throughput current. P6SEL.x should be set, if an analog signal is applied to the pin.

P6SEL.6	P6DIR.6	Port Function
0	0	P6.6 Input
0	1	P6.6 Output
1	0	SIFCI2 (Scan IF channel 2 comparator input)
1	1	SIFDAOUT (Scan IF DAC output)

APPLICATION INFORMATION

input/output schematic (continued)

port P6, P6.7 input/output with Schmitt-trigger



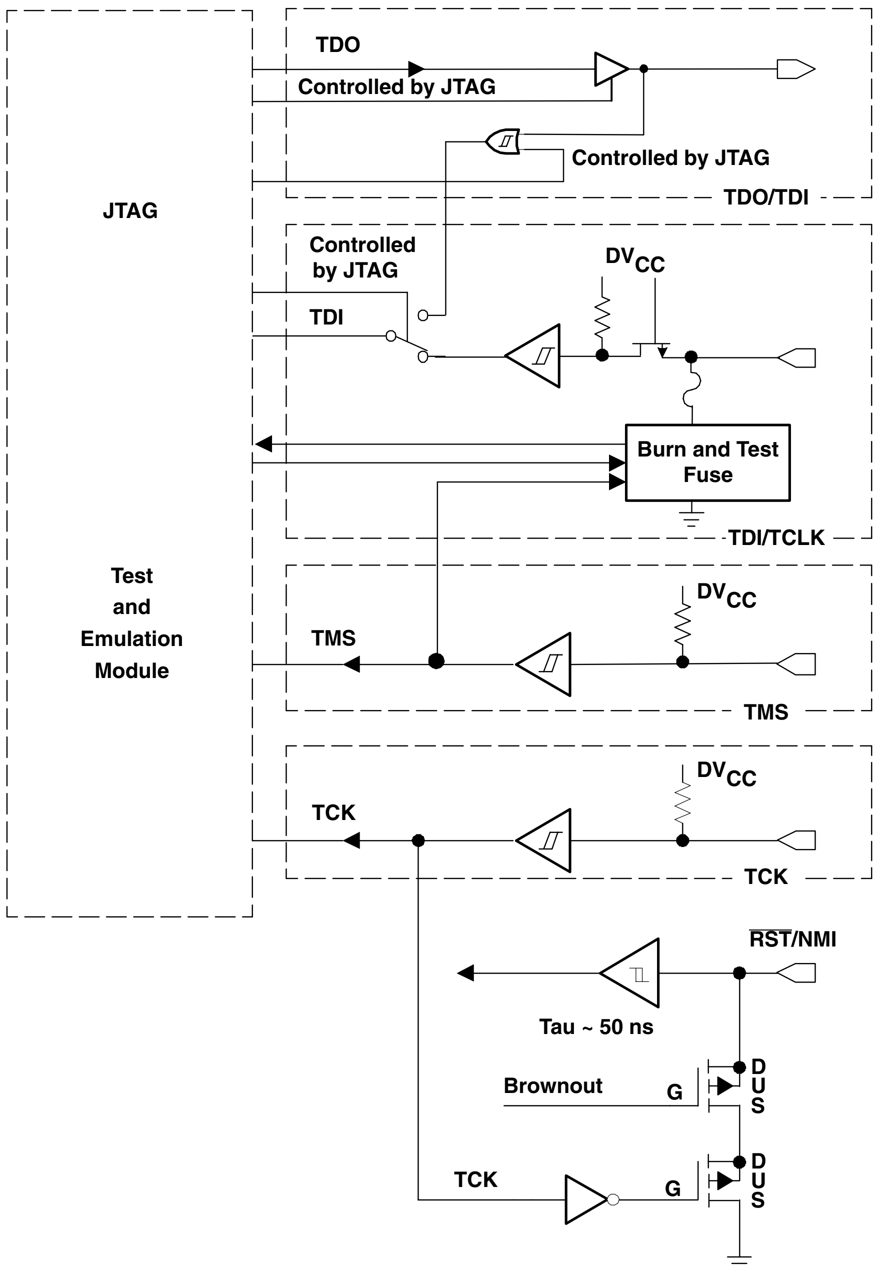
P6SEL.x must be set if the corresponding pins are used by the Scan IF.

NOTE: Analog signals applied to digital gates can cause current flow from the positive to the negative terminal. The throughput current flows if the analog signal is in the range of transitions 0→1 or 1→0. The value of the throughput current depends on the driving capability of the gate. For MSP430, it is approximately 100 µA.
Use P6SEL.x=1 to prevent throughput current. P6SEL.x should be set, if an analog signal is applied to the pin.

SVS VLDx = 15	P6SEL.7	P6DIR.7	Port Function
0	0	0	P6.7 Input
0	0	1	P6.7 Output
0	1	X	SIFCI3 (Scan IF channel 3 comparator input)
1	X	X	SVSIN

APPLICATION INFORMATION

JTAG pins TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt-trigger or output



APPLICATION INFORMATION

JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF}, of 1.8 mA at 3 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 21). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

The JTAG pins are terminated internally, and therefore do not require external termination.

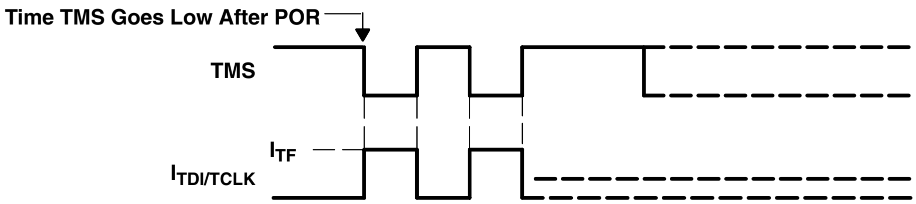


Figure 21. Fuse Check Mode Current, MSP430FW42x

Data Sheet Revision History

Literature Number	Summary
SLAS383B	Updated functional block diagram (page 3) Clarified test conditions in recommended operating conditions table (page 18) Clarified test conditions in electrical characteristics table (page 19) Added $I_{lkg(Px.x)}$ for all ports in leakage current table (page 20) Clarified test conditions in DCO table (page 29) Changed t_{CPT} maximum value from 4 ms to 10 ms in Flash memory table (page 36)

NOTE: Page and figure numbers refer to the respective document revision.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
MSP430FW423IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430FW423IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430FW425IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430FW425IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430FW427IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430FW427IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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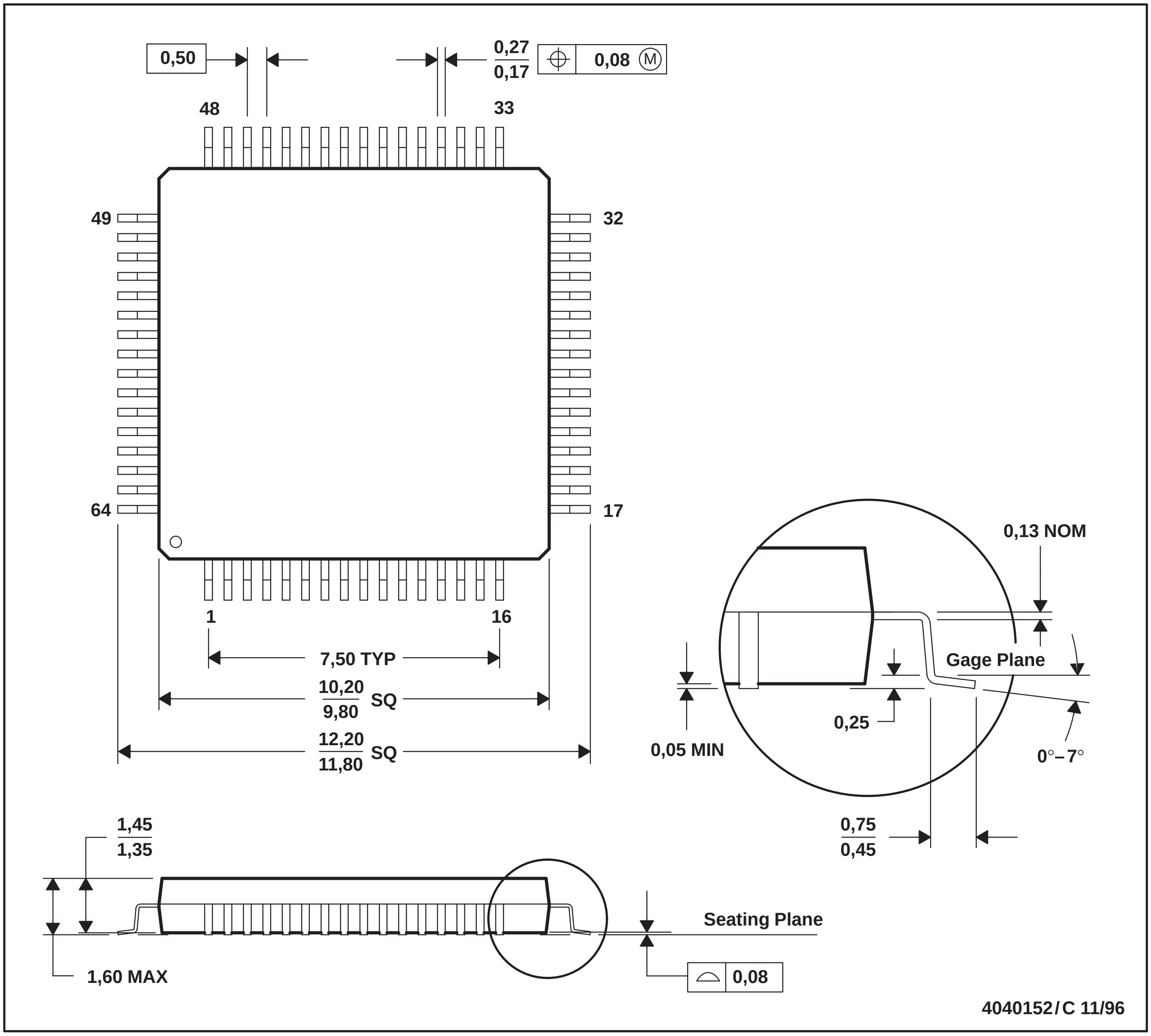
PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

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