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LV5980MD

Bi-CMOS IC

Low power consumption and highefficiency Step-down Switching Regulator

Overview

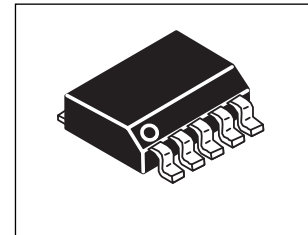
LV5980MD is 1ch DCDC converter with built-in power Pch MOSFET.

The recommended operating range is 4.5V to 23V.

The maximum current is 3A. The operating current is about 63 μ A, and low power consumption is achieved.

Features and Functions

- 1ch SBD rectification DCDC converter IC with built-in power Pch MOSFET
- Typical value of light load mode current is 63 μ A
- 4.5V to 23V Operating input voltage range
- 100m Ω High-side switch
- Output voltage adjustable to 1.235V
- The oscillatory frequency is 370kHz
- ON/OFF Function
- built-in OCP circuit with P-by-P method
- When P-by-P is generated continuously, it shifts to the HICCUP operation
- External capacitor Soft-start
- Under voltage lock-out, thermal shutdown

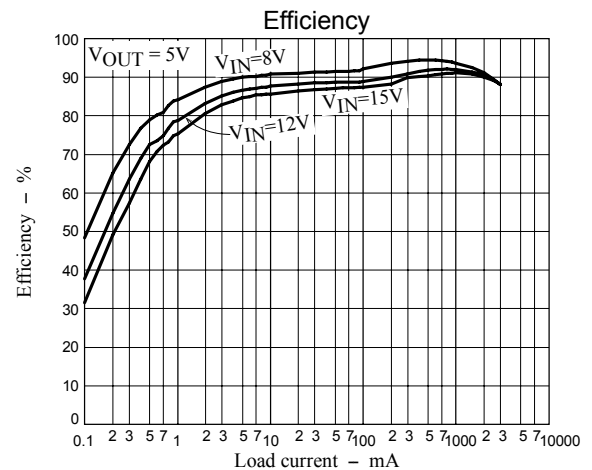
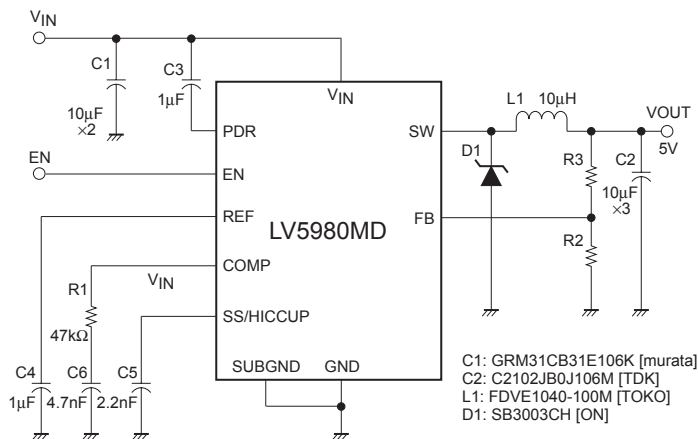


SOIC10

Applications

- Set top boxes
- Point of load DC/DC converters
- White Goods
- DVD/Blu-ray™ drivers and HDD
- Office Equipment
- LCD monitors and TVs
- POS System

Application Circuit Example



ORDERING INFORMATION

See detailed ordering and shipping information on page 20 of this data sheet.

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Specifications

Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------------|------------------------|-----------------|------|
| Input voltage | V _{IN} max | | 25 | V |
| Allowable pin voltage | V _{IN-SW} | | 30 | V |
| | EN | | V _{IN} | |
| | V _{IN-PDR} | | 6 | V |
| | REF | | 6 | V |
| | SS/HICcup | | REF | V |
| | FB | | REF | V |
| | COMP | | REF | V |
| Allowable power dissipation | Pd max | Specified substrate *1 | 1.3 | W |
| Operating temperature | T _{OPR} | | -40 to +85 | °C |
| Storage temperature | T _{STG} | | -55 to +150 | °C |

*1 Specified substrate: 50.0 mm × 50.0 mm × 1.6 mm, fiberglass epoxy printed circuit board, 4 layers

Caution 1) Absolute maximum ratings represent the values which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---------------------|-----------------|------------|-----------|------|
| Input voltage range | V _{IN} | | 4.5 to 23 | V |

Electrical Characteristics at Ta=25°C, V_{IN}=15V

| Characteristic | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-------------------------------------|----------------------|---|-------------------------|-------------------------|-------------------------|-------|
| [Reference Voltage] | | | | | | |
| Internal Reference Voltage | V _{REF} | | 1.210 | 1.235 | 1.260 | V |
| Pch Drive Voltage | V _{PDR} | I _{OUT} =0 ~ -5mA | V _{IN} -5.5 | V _{IN} -5.0 | V _{IN} -4.5 | V |
| [Saw Wave Oscillator] | | | | | | |
| Oscillatory Frequency | F _{OSC} | | 310 | 370 | 430 | kHz |
| [ON/OFF Circuit] | | | | | | |
| IC startup voltage (EN PIN) | V _{CNT_ON} | | 2.0 | | V _{IN} | V |
| Disable voltage (EN PIN) | V _{CNT_OFF} | | | | 0.3 | V |
| [Soft Start Circuit] | | | | | | |
| Soft Start • Source Current | I _{SS_SC} | | 1.2 | 1.8 | 2.4 | uA |
| Soft Start • Sink Current | I _{SS_SK} | V _{IN} = 3V, EN > 2V V _{SS} = 0.4V | | 300 | | uA |
| [UVLO Circuit] | | | | | | |
| UVLO Release Voltage | V _{UVLON} | FB = COMP | 3.3 | 3.7 | 4.1 | V |
| UVLO Lock Voltage | V _{UVLOF} | FB = COMP | 3.02 | 3.42 | 3.82 | V |
| [Error Amplifier] | | | | | | |
| Input Bias Current | I _{EA_IN} | | -100 | -10 | | nA |
| Error amplifier gain | G _{EA} | | 100 | 220 | 380 | uA/V |
| Output Sink Current | I _{EA_OSK} | FB = 1.75V | -30 | -17 | -8 | uA |
| Output Source Current | I _{ES_OSC} | FB = 0.75V | 8 | 17 | 30 | uA |
| [Over Current Limit Circuit] | | | | | | |
| Current Limit Peak | I _{CL} | *2 Test circuit | 3.5 | 4.7 | 6.2 | A |
| HICcup Timer Start-up Cycle | N _{CYC} | | | 15 | | cycle |
| HICcup Comparator Threshold Voltage | V _{HIC} | | | 0.15 | | V |
| HICcup Timer Discharge Current | I _{HIC} | | | 0.25 | | uA |

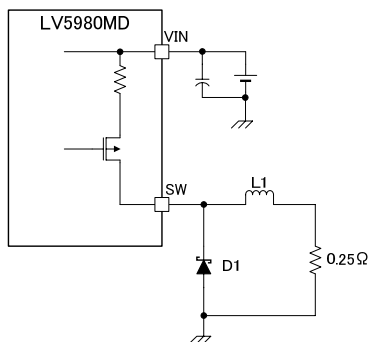
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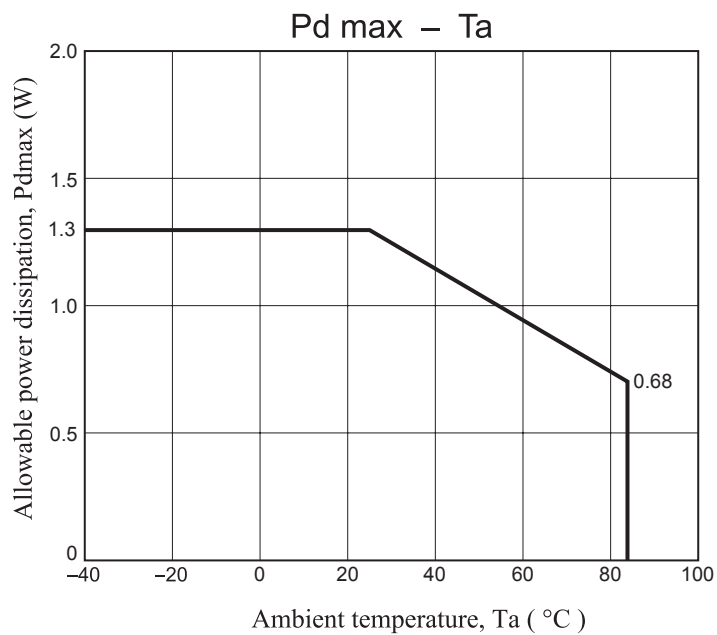
| Characteristic | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-------------------------------------|-------------|---------------------|------|------|------|-------------|
| [PWM Comparator] | | | | | | |
| Maximum On-Duty | D_{MAX} | | 94 | | | % |
| [Output] | | | | | | |
| Output On Resistance | R_{ON} | $I_o = 0.5A$ | | 100 | | m Ω |
| [The entire device] | | | | | | |
| Standby current | I_{CCS} | $EN < 0.3V$ | | | 1 | μA |
| Light Load Mode Consumption Current | I_{SLEEP} | No switching | | 63 | 83 | μA |
| Thermal Shutdown | TSD | *3 Design guarantee | | 170 | | $^{\circ}C$ |

*2 Test circuit



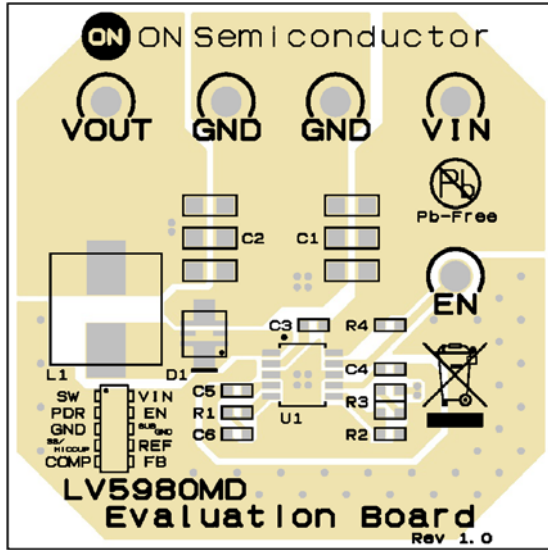
*3 Design guarantee: Signifies target value in design. These parameters are not tested in an independent IC.

Pdmax - Ta

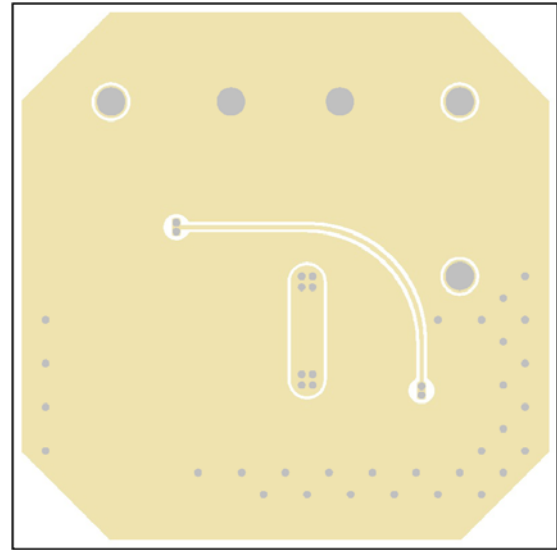


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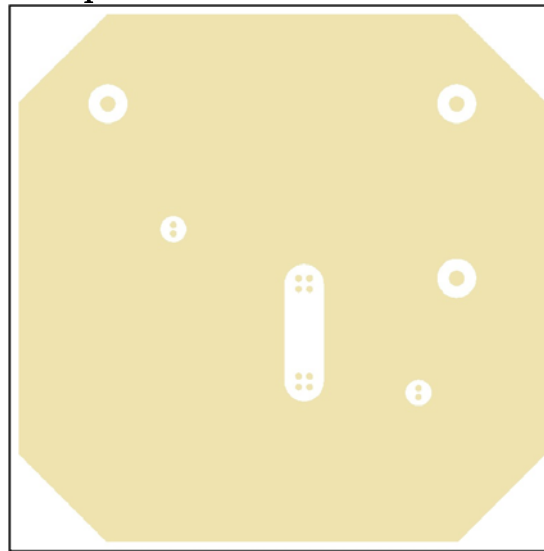
Specified substrate



Top



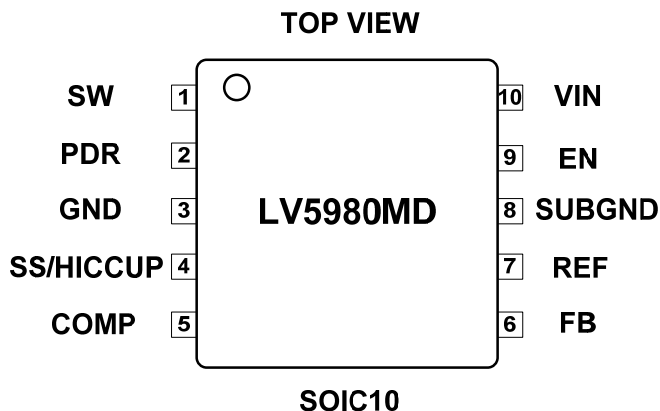
Bottom



2nd/3rd layers

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Pin Connections

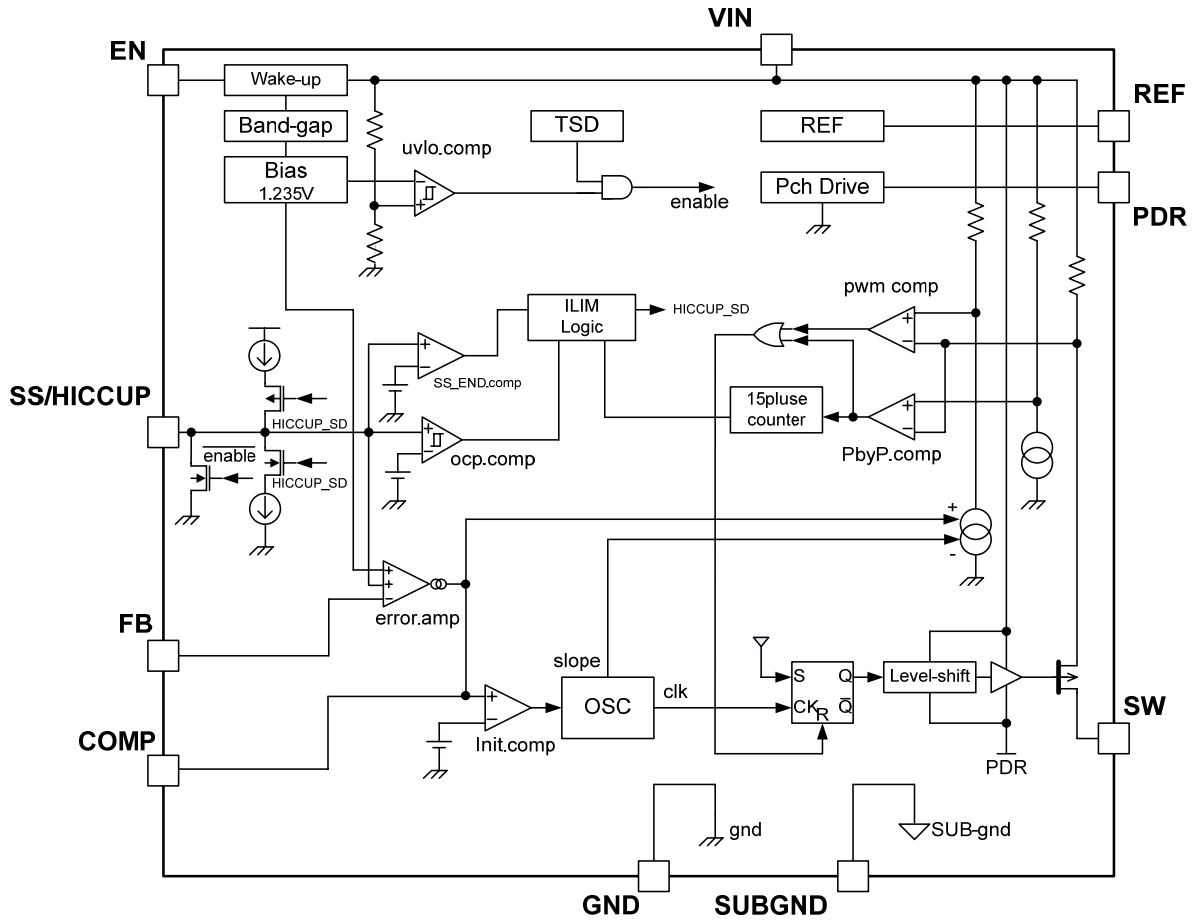


Pin Function Description

| Pin | Pin Name | Description |
|-----|-----------|---|
| 1 | SW | High-side Pch MOSFET drain Pin. |
| 2 | PDR | Pch MOSFET gate drive Voltage. The bypass capacitor is necessarily connected between this pin and Vin. |
| 3 | GND | Ground Pin. Ground pin voltage is reference voltage |
| 4 | SS/HICCUP | Capacitor connection pin for soft start and setting re-startup cycle in HICCUP mode. About 1.8uA current charges the soft start capacitor. |
| 5 | COMP | Error Amplifier Output Pin. The phase compensation network is connected between GND pin and COMP pin. Thanks to current-mode control, comp pin voltage would tell you the output current amplitude. Comp pin is connected internally to an Inlt.comparator which compares with 0.9V reference. If comp pin voltage is larger than 0.9V, IC operates in "continuous mode". If comp pin voltage is smaller than 0.9V, IC operates in "discontinuous mode (low consumption mode)". |
| 6 | FB | Error amplifier reverse input pin. ICs make its voltage keep 1.235V. Output voltage is divided by external resistances and it across FB. |
| 7 | REF | Reference voltage. |
| 8 | SUBGND | Short-circuited and use 3pin and 8pin as GND |
| 9 | EN | ON/OFF Pin. |
| 10 | VIN | Supply voltage pin. It is observed by the UVLO function. When its voltage becomes 3.7V or more, ICs startup in soft start. |

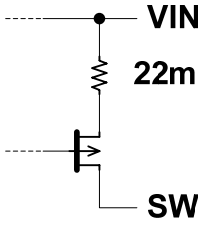
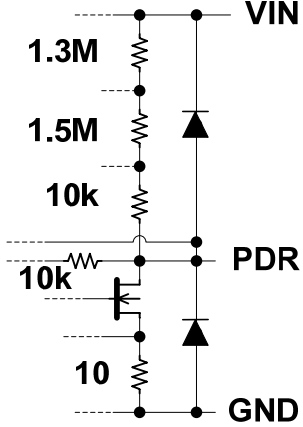
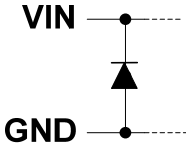
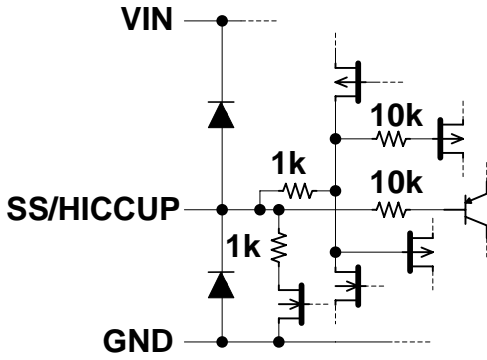
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Block Diagram



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Pin Equivalent Circuit

| Pin No. | Pin Name | Equivalent Circuit |
|---------|-----------|--|
| 1 | SW |  |
| 2 | PDR |  |
| 3 | GND |  |
| 4 | SS/HICCUP |  |

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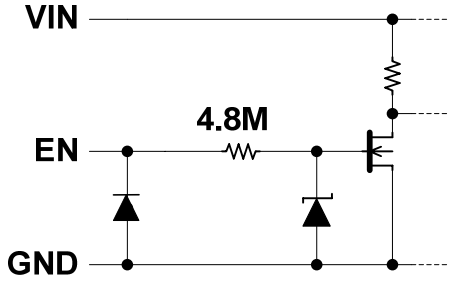
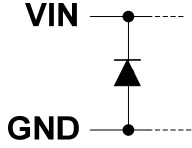
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| Pin No. | Pin Name | Equivalent Circuit |
|---------|----------|--------------------|
| 5 | COMP | |
| 6 | FB | |
| 7 | REF | |
| 8 | SUBGND | |

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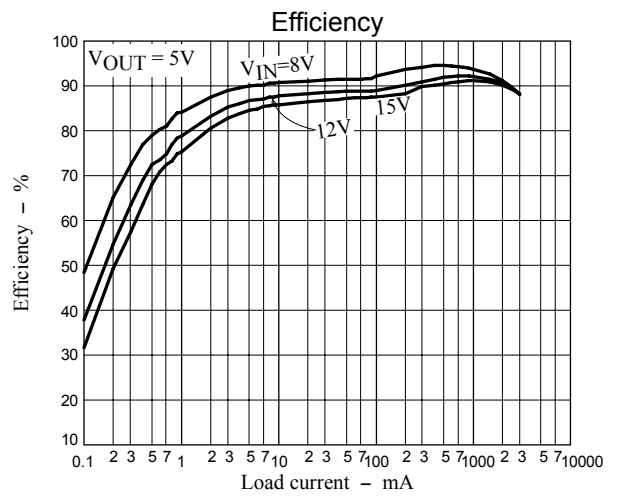
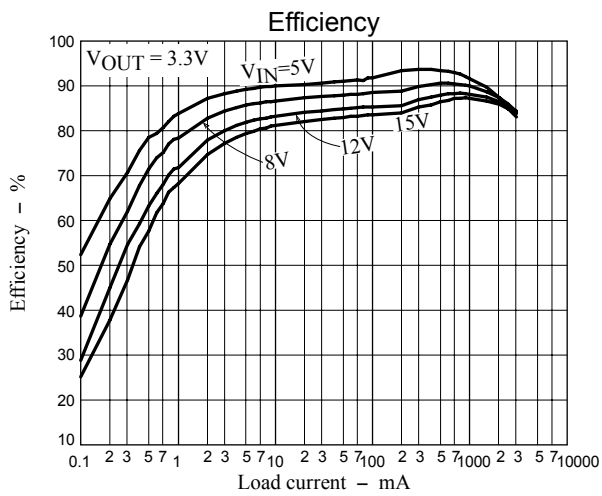
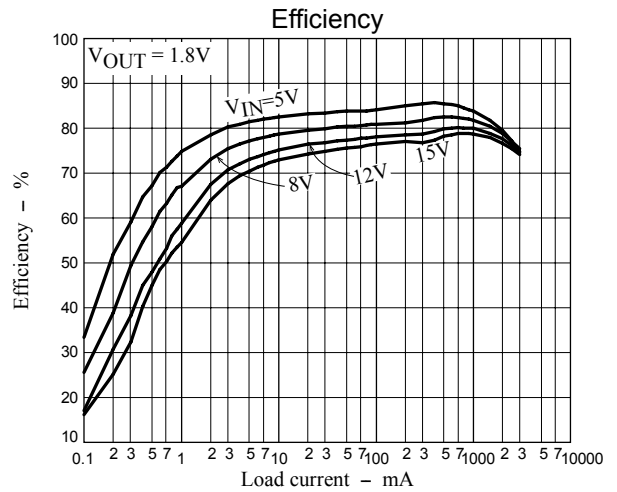
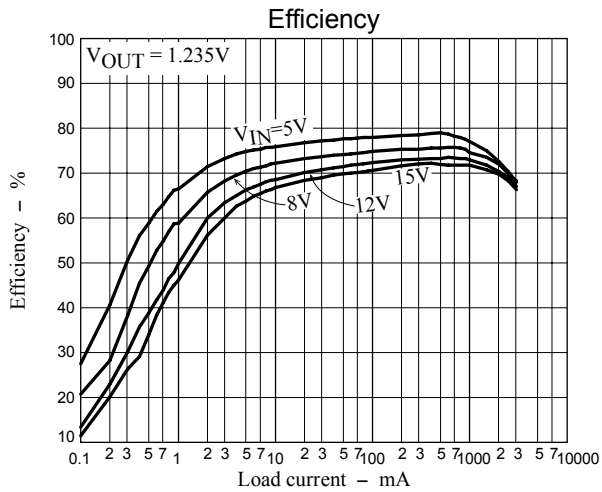
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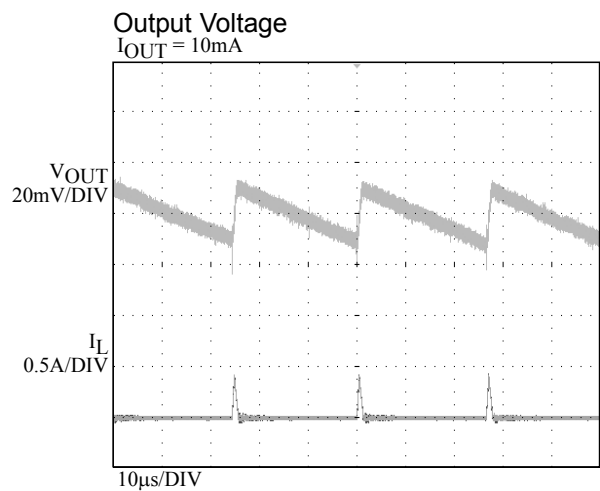
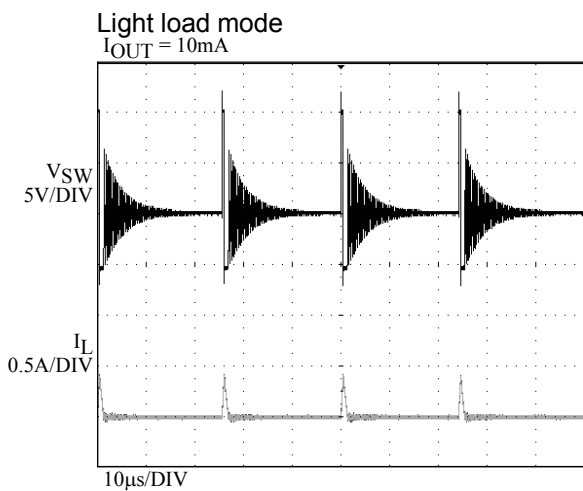
| Pin No. | Pin Name | Equivalent Circuit |
|---------|----------|--|
| 9 | EN |  |
| 10 | VIN |  |

LV5980MD

Typical Performance Characteristics Application Curves at $T_a = 25^\circ\text{C}$

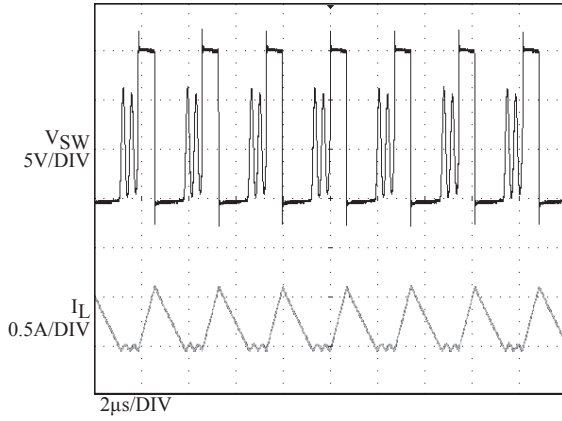


Operation Waveforms (Circuit from Typical Application, $T_a = 25^\circ\text{C}$, $V_{IN} = 15\text{V}$, $V_{OUT} = 5\text{V}$)



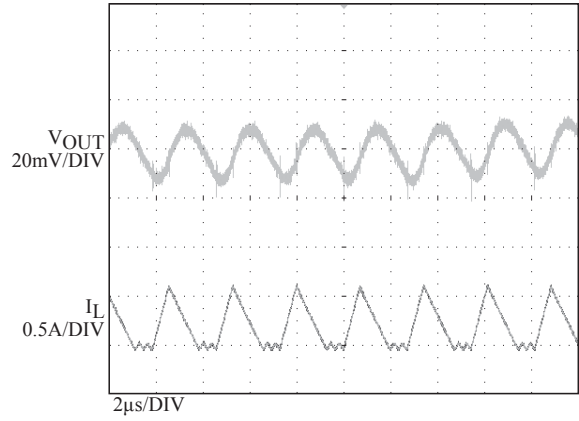
Discontinuous current mode

$I_{OUT} = 200\text{mA}$



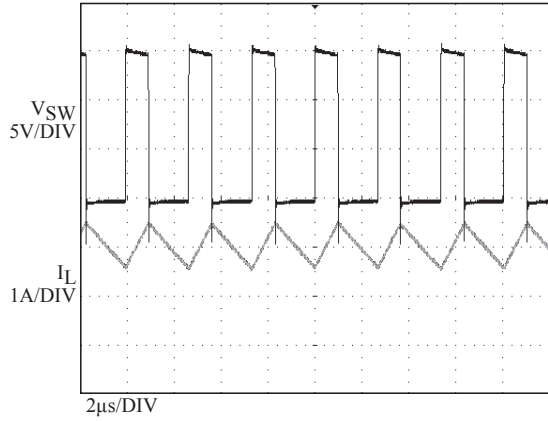
Output Voltage

$I_{OUT} = 200\text{mA}$



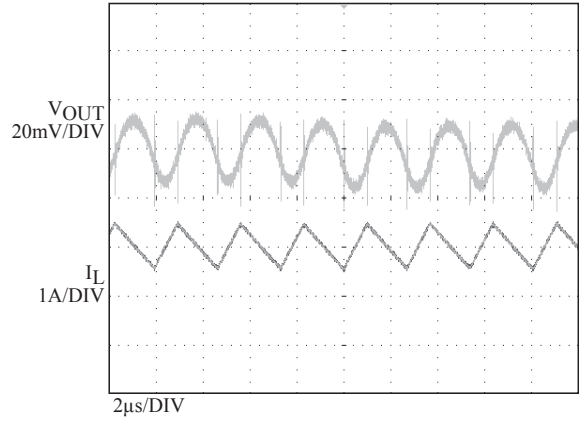
Continuous current mode

$I_{OUT} = 2\text{A}$



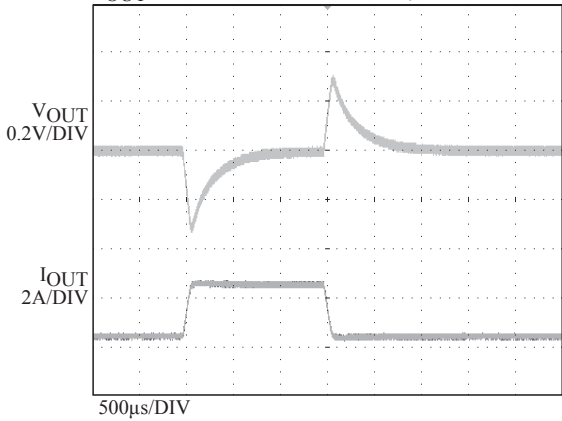
Output Voltage

$I_{OUT} = 2\text{A}$



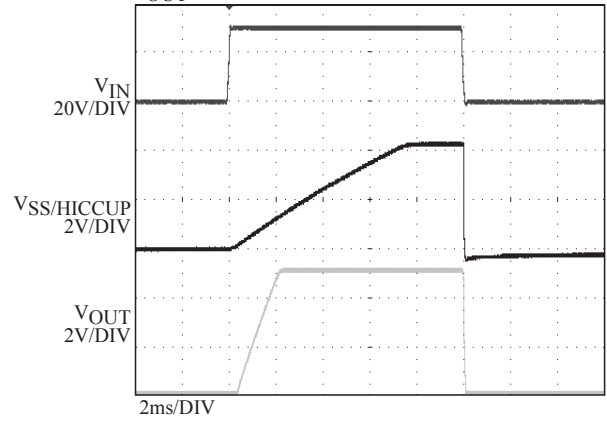
Load Transient response

$I_{OUT} = 0.5 \leftrightarrow 2.5\text{A}$, Slew Rate = $100\mu\text{S}$



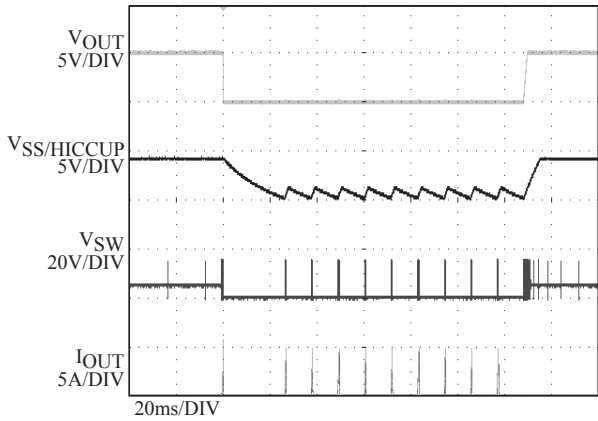
Soft start and shutdown

$I_{OUT} = 2\text{A}$



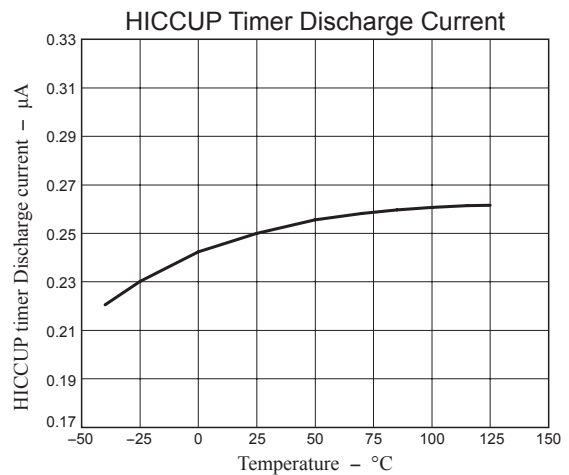
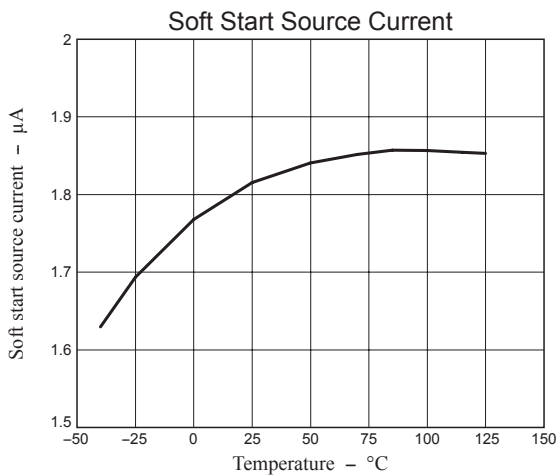
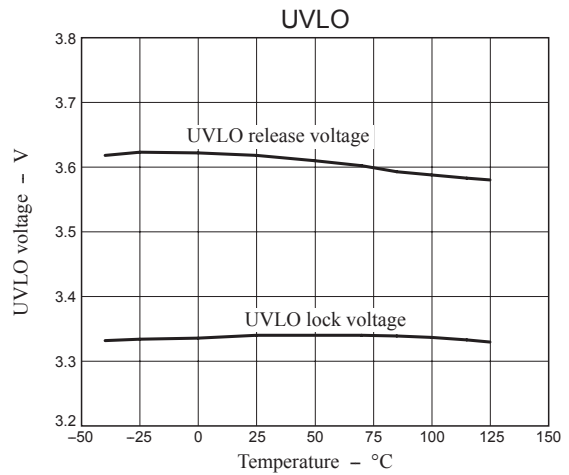
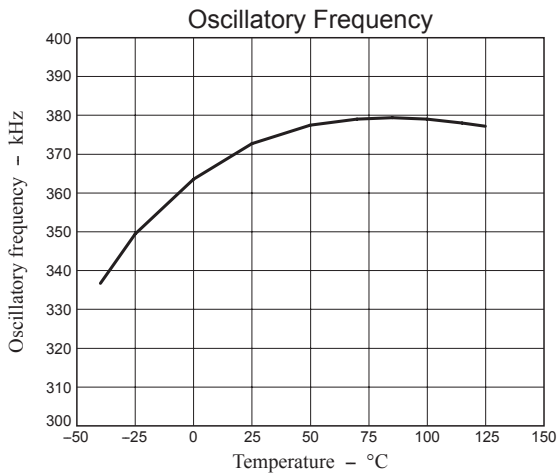
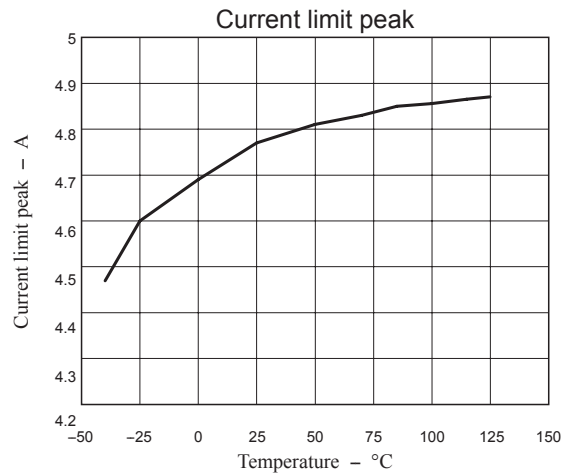
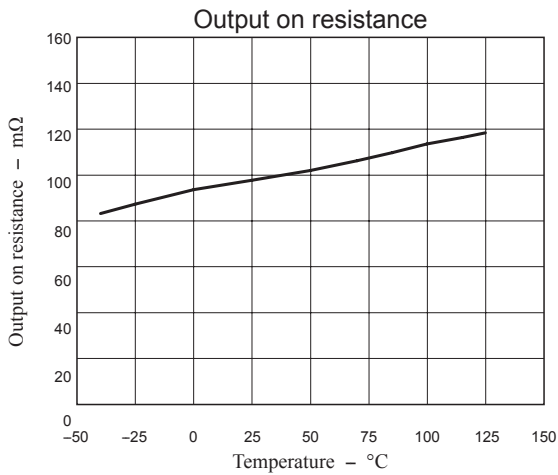
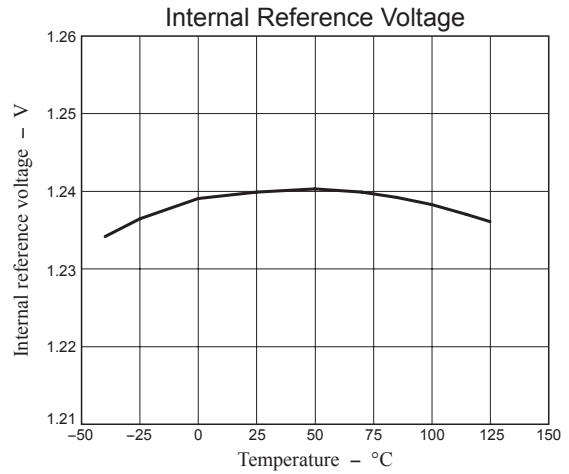
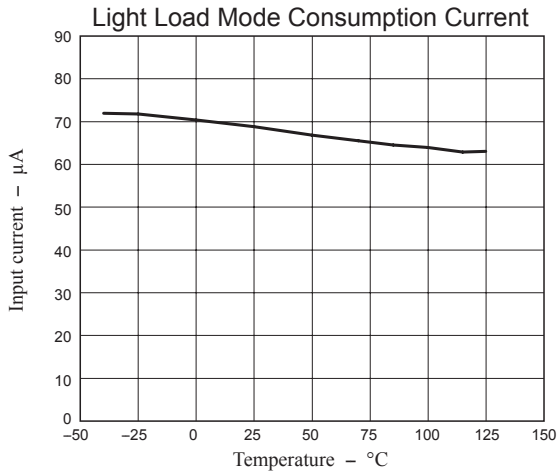
Over current protection

OUT - GND short

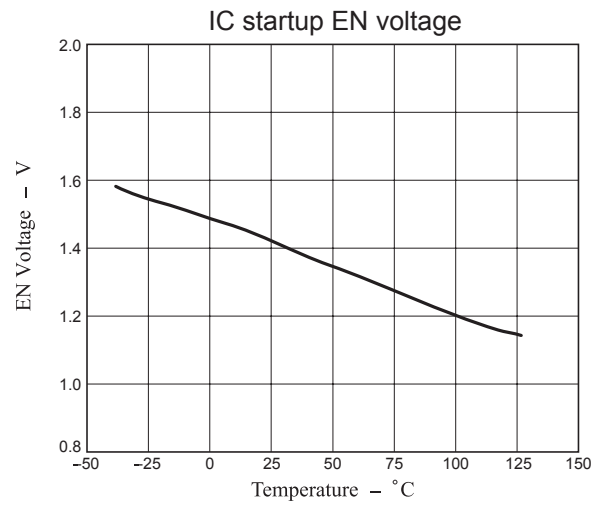
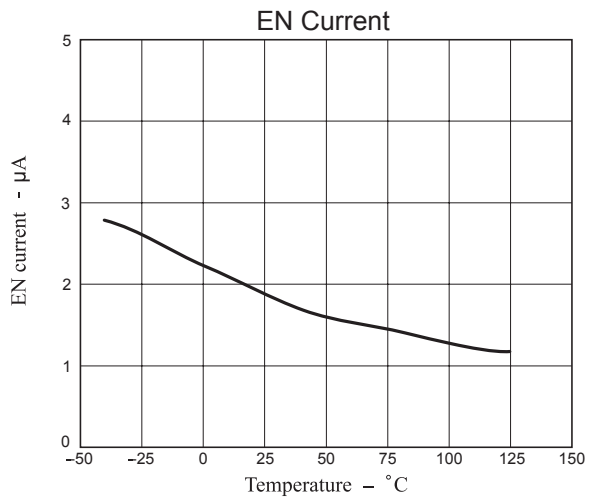


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Characterization Curves at $T_a = 25^\circ\text{C}$, $V_{IN} = 15\text{V}$



LV5980MD



Detailed Description

Power-save Feature

The LV5980MC has Power-saving feature to enhance efficiency when the load is light. By shutting down unnecessary circuits, operating current of the IC is minimized and high efficiency is realized.

Output Voltage Setting

Output voltage (V_{OUT}) is configurable by the resistance R_3 between V_{OUT} and FB and the R_2 between FB and GND. V_{OUT} is given by the following equation (1).

$$V_{OUT} = \left(1 + \frac{R_3}{R_2}\right) \times V_{REF} = \left(1 + \frac{R_3}{R_2}\right) \times 1.235 \text{ [V]} \quad (1)$$

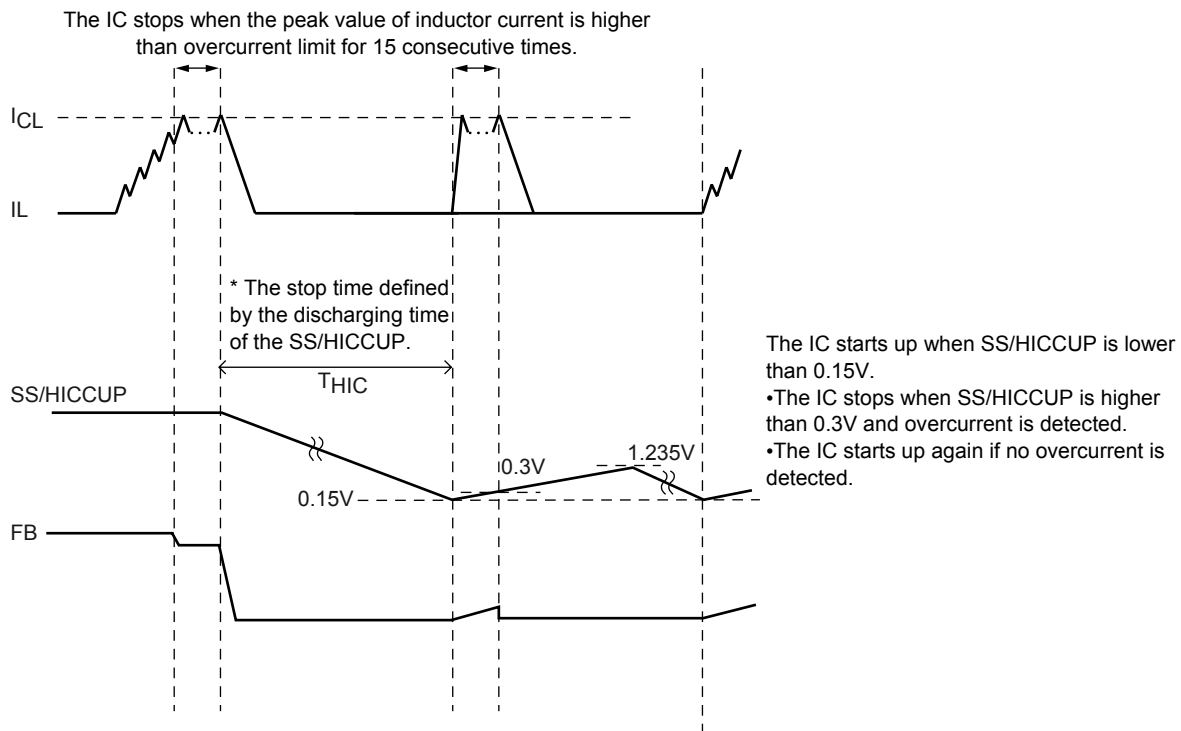
Soft Start

Soft start time (T_{SS}) is configurable by the capacitor (C_5) between SS/HICCUP and GND. The setting value of T_{SS} is given by the equation (2).

$$T_{SS} = C_5 \times \frac{V_{REF}}{I_{SS}} = C_5 \times \frac{1.235}{1.8 \times 10^{-6}} \text{ [ms]} \quad (2)$$

Hiccup Over-Current Protection

Over-current limit (I_{CL}) is set to 4.7A in the IC. When the peak value of inductor current is higher than 4.7A for 15 consecutive times, the protection deems it as over current and stops the IC. Stop period (T_{HIC}) is defined by the discharging time of the SS/HICCUP. When SS/HICCUP is lower than 0.15V, the IC starts up. When SS/HICCUP is higher than 0.3V and then over current is detected, the IC stops again. And when SS/HICCUP is higher than 1.235V, the discharge starts again. When the protection does not detect over-current status, the IC starts up again.



Design Procedure

Inductor Selection

When conditions for input voltage, output voltage and ripple current are defined, the following equations (3) give inductance value.

$$\left. \begin{aligned} L &= \frac{V_{IN} - V_{OUT}}{\Delta I_R} \times T_{ON} \\ T_{ON} &= \frac{1}{\{(V_{IN} - V_{OUT}) \div (V_{OUT} + V_F) + 1\} \times F_{OSC}} \\ F_{OSC} &: \text{Oscillatory Frequency} \\ V_F &: \text{Forward voltage of Schottky Barrier diode} \\ V_{IN} &: \text{Input voltage} \\ V_{OUT} &: \text{Output voltage} \end{aligned} \right\} \quad (3)$$

- Inductor current: Peak value (I_{RP})

Current peak value (I_{RP}) of the inductor is given by the equation (4).

$$I_{RP} = I_{OUT} + \frac{V_{IN} - V_{OUT}}{2L} \times T_{ON} \quad (4)$$

Make sure that rating current value of the inductor is higher than a peak value of ripple current.

- Inductor current: ripple current (ΔI_R)

Ripple current (ΔI_R) is given by the equation (5).

$$\Delta I_R = \frac{V_{IN} - V_{OUT}}{L} \times T_{ON} \quad (5)$$

When load current (I_{OUT}) is less than 1/2 of the ripple current, inductor current flows discontinuously.

Output Capacitor Selection

Make sure to use a capacitor with low impedance for switching power supply because of large ripple current flows through output capacitor.

This IC is a switching regulator which adopts current mode control method. Therefore, you can use capacitor such as ceramic capacitor and OS capacitor in which equivalent series resistance (ESR) is exceedingly small.

Effective value is given by the equation (6) because the ripple current (AC) that flows through output capacitor is saw tooth wave.

$$I_{C_OUT} = \frac{1}{2\sqrt{3}} \times \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times F_{OSC} \times V_{IN}} \quad [\text{Arms}] \quad (6)$$

Input Capacitor Selection

Ripple current flows through input capacitor which is higher than that of the output capacitors.

Therefore, caution is also required for allowable ripple current value.

The effective value of the ripple current flows through input capacitor is given by the equation (7).

$$I_{C_IN} = \sqrt{D(1-D)} \times I_{OUT} \quad [\text{Arms}] \quad (7)$$

$$D = \frac{T_{ON}}{T} = \frac{V_{OUT}}{V_{IN}}$$

In (7), D signifies the ratio between ON/OFF period. When the value is 0.5, the ripple current is at a maximum. Make sure that the input capacitor does not exceed the allowable ripple current value given by (7). With (7), if $V_{IN}=15V$, $V_{OUT}=5V$, $I_{OUT}=1.0A$ and $F_{OSC}=370 \text{ kHz}$, then I_{C_IN} value is about 0.471Arms.

In the board wiring from input capacitor, \bar{V}_{IN} to GND, make sure that wiring is wide enough to keep impedance low because of the current fluctuation. Make sure to connect input capacitor near output capacitor to lower voltage bound due to regeneration current. When change of load current is excessive (I_{OUT} : high \Rightarrow low), the power of output electric capacitor is regenerated to input capacitor. If input capacitor is small, input voltage increases. Therefore, you need to implement a large input capacitor. Regeneration power changes according to the change of output voltage, inductance of a coil and load current.

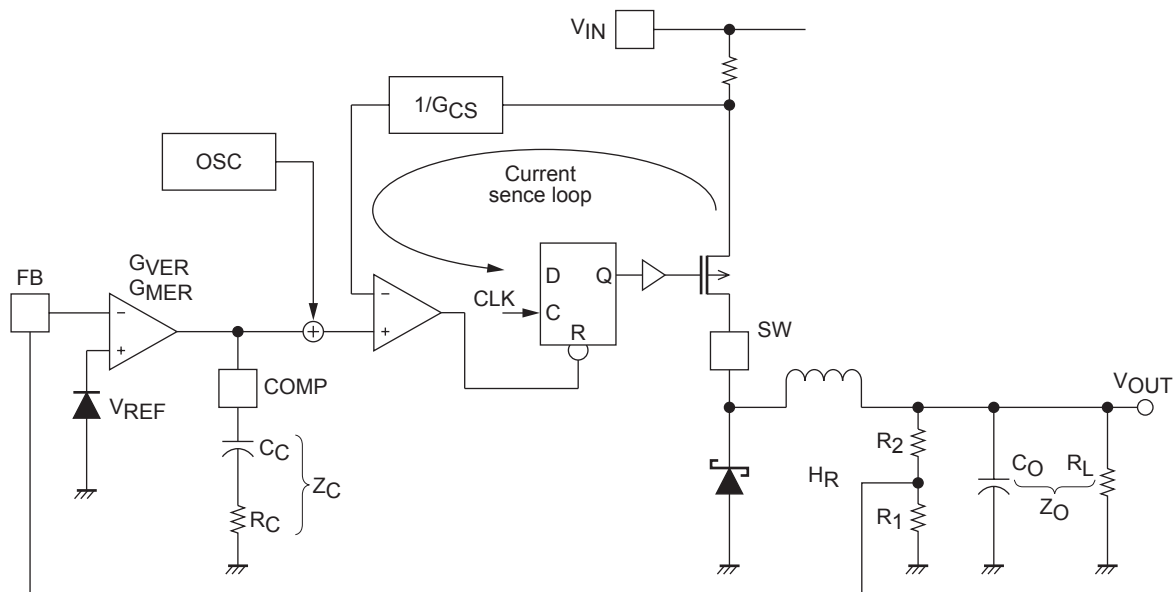
Selection of external phase compensation component

This IC adopts current mode control which allows use of ceramic capacitor with low ESR and solid polymer capacitor such as OS capacitor for output capacitor with simple phase compensation. Therefore, you can design long-life and high quality step-down power supply circuit easily.

Frequency Characteristics

The frequency characteristic of this IC is constituted with the following transfer functions.

- | | |
|--|-------------|
| (1) Output resistance breeder | : H_R |
| (2) Voltage gain of error amplifier | : G_{VEA} |
| Current gain | : G_{MEA} |
| (3) Impedance of phase compensation external element | : Z_C |
| (4) Current sense loop gain | : G_{CS} |
| (5) Output smoothing impedance | : Z_O |



Closed loop gain is obtained with the following formula (8).

$$G = H_R \cdot G_{MER} \cdot Z_C \cdot G_{CS} \cdot Z_O$$

$$= \frac{V_{REF}}{V_{OUT}} \cdot G_{MER} \cdot \left(R_C + \frac{1}{sC_C} \right) \cdot G_{CS} \cdot \frac{R_L}{1 + sC_O \cdot R_L} \quad (8)$$

Frequency characteristics of the closed loop gain is given by pole fp1 consists of output capacitor C_O and output load resistance R_L , zero point fz consists of external capacitor C_C of the phase compensation and resistance R_C , and pole fp2 consists of output impedance Z_{ER} of error amplifier and external capacitor of phase compensation C_C as shown in formula (8). fp1, fz, fp2 are obtained with the following equations (9) to (11).

$$fp1 = \frac{1}{2\pi \cdot C_O \cdot R_L} \quad (9)$$

$$fz = \frac{1}{2\pi \cdot C_C \cdot R_C} \quad (10)$$

$$fp2 = \frac{1}{2\pi \cdot Z_{ER} \cdot C_C} \quad (11)$$

Calculation of external phase compensation constant

Generally, to stabilize switching regulator, the frequency where closed loop gain is 1 (zero-cross frequency f_{ZC}) should be 1/10 of the switching frequency (or 1/5). Since the switching frequency of this IC is 370kHz, the zero-cross frequency should be 37kHz. Based on the above condition, we obtain the following formula (12).

$$\frac{V_{REF}}{V_{OUT}} \cdot G_{MER} \cdot \left(R_C + \frac{1}{SC_C} \right) \cdot G_{CS} \cdot \frac{R_L}{1 + SC_O \cdot R_L} = 1 \quad (12)$$

As for zero-cross frequency, since the impedance element of phase compensation is $RC \gg 1/SC_C$, the following equation (13) is obtained.

$$\frac{V_{REF}}{V_{OUT}} \cdot G_{MER} \cdot R_C \cdot G_{CS} \cdot \frac{R_L}{1 + 2\pi \cdot f_{ZC} \cdot C_O \cdot R_L} = 1 \quad (13)$$

Phase compensation external resistance can be obtained with the following formula (14), the variation of the formula (13). Since $2\pi \cdot f_{ZC} \cdot C_O \cdot R_L \gg 1$ in the equation (14), we know that the external resistance is independent of load resistance.

$$R_C = \frac{V_{OUT}}{V_{REF}} \cdot \frac{1}{G_{MER}} \cdot \frac{1}{G_{CS}} \cdot \frac{1 + 2\pi \cdot f_{ZC} \cdot C_O \cdot R_L}{R_L} \quad (14)$$

When output is 5V and load resistance is 5Ω (1A load), the resistances of phase compensation are as follows.
 $G_{CS} = 2.7A/V$, $G_{MER} = 220\mu A/V$, $f_{ZC} = 37kHz$

$$R_C = \frac{5}{1.235} \times \frac{1}{220 \times 10^{-6}} \times \frac{1}{2.7} \times \frac{1 + 2 \times 3.14 \times (37 \times 10^3) \times (30 \times 10^{-6}) \times 5}{5} = 48.898... \times 10^3$$

$$= 48.90 \text{ [k}\Omega\text{]}$$

If frequency of zero point f_z and pole f_{p1} are in the same position, they cancel out each other. Therefore, only the pole frequency remains for frequency characteristics of the closed loop gain.
 In other words, gain decreases at -20dB/dec and phase only rotates by 90° and this allows characteristics where oscillation never occurs.

$$f_{p1} = f_z$$

$$\frac{1}{2\pi \cdot C_O \cdot R_L} \cdot \frac{1}{2\pi \cdot C_O \cdot R_C}$$

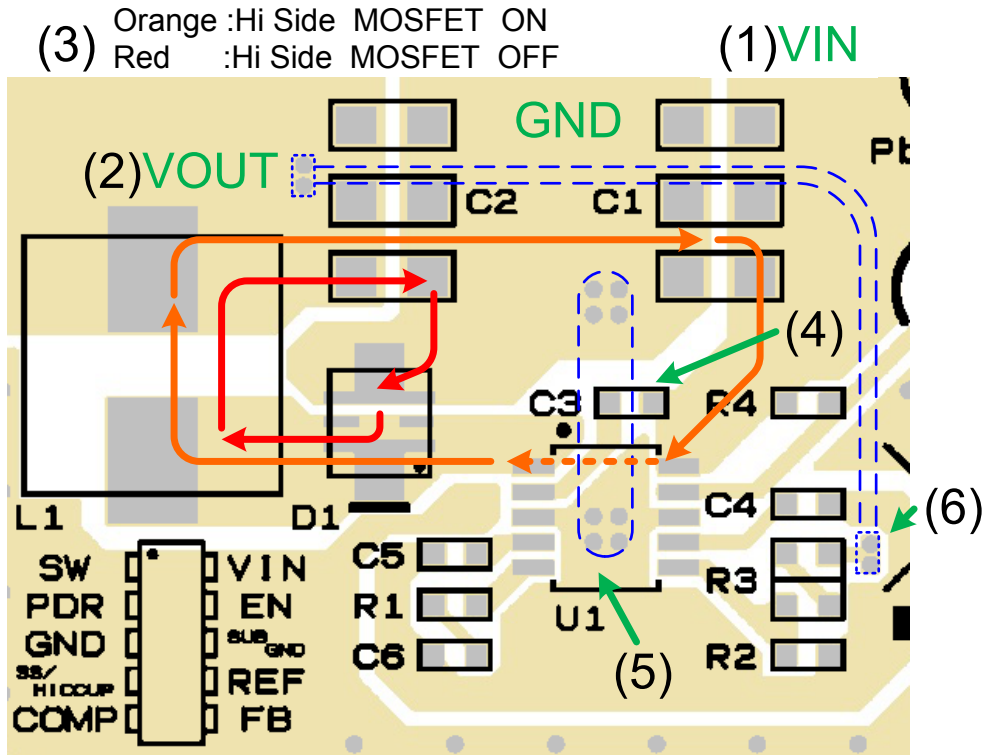
$$C_C = \frac{R_L \cdot C_O}{R_C} \cdot \frac{5 \times (30 \times 10^{-6})}{48.9 \times 10^3} = 3.067... \times 10^{-9}$$

$$= 3.07 \text{ [nF]}$$

The above shows external compensation constant obtained through ideal equations. In reality, we need to define phase constant through testing to verify constant IC operation at all temperature range, load range and input voltage range. In the evaluation board for delivery, phase compensation constants are defined based on the above constants. The zero-cross frequency required in the actual system board, in other word, transient response is adjusted by external compensation resistance. Also, if the influence of noise is significant, use of external phase compensation capacitor with higher value is recommended.

Caution in pattern design

Pattern design of the board affects the characteristics of DC-DC converter. This IC switches high current at a high speed. Therefore, if inductance element in a pattern wiring is high, it could be the cause of noise. Make sure that the pattern of the main circuit is wide and short.



- (1) Pattern design of the input capacitor
Connect a capacitor near the IC for noise reduction between V_{IN} and the GND. The change of current is at the largest in the pattern between an input capacitor and V_{IN} as well as between GND and an input capacitor among all the main circuits. Hence make sure that the pattern is as fat and short as possible.
- (2) Pattern design of an inductor and the output capacitor
High electric current flows into the choke coil and the output capacitor. Therefore this pattern should also be as fat and short as possible.
- (3) Pattern design with current channel into consideration
Make sure that when High side MOSFET is ON (red arrow) and OFF (orange arrow), the two current channels runs through the same channel and an area is minimized.
- (4) Pattern design of the capacitor between V_{IN} -PDR
Make sure that the pattern of the capacitor between V_{IN} and PDR is as short as possible.
- (5) Pattern design of the small signal GND
The GND of the small signal should be separated from the power GND.
- (6) Pattern design of the FB-OUT line
Wire the line shown in red between FB and OUT to the output capacitor as near as possible. When the influence of noise is significant, use of feedback resistors R2 and R3 with lower value is recommended.

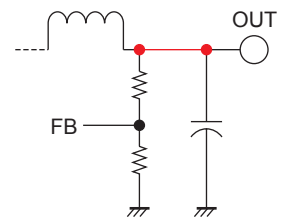
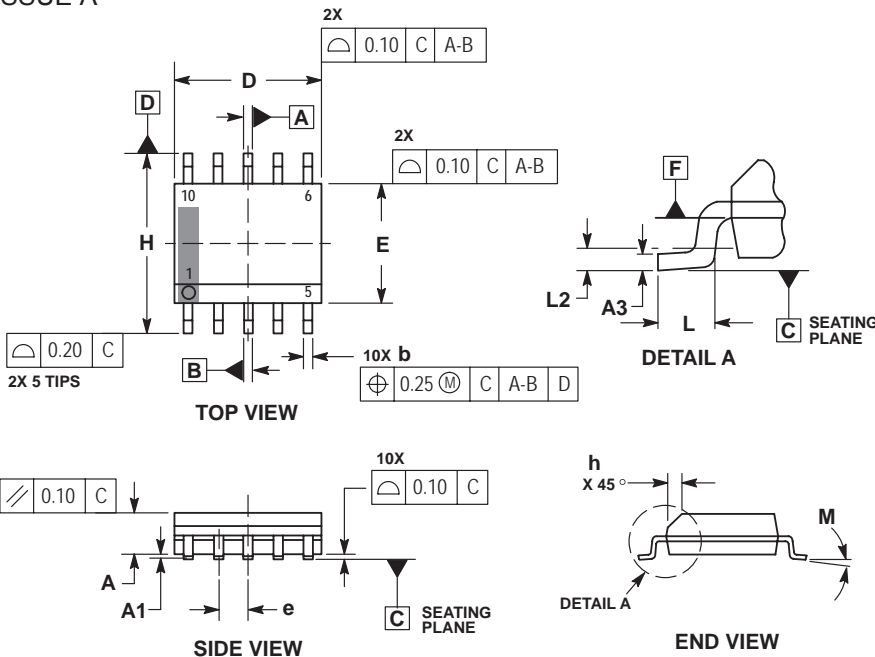


Fig: FB-OUT Line

PACKAGE DIMENSIONS

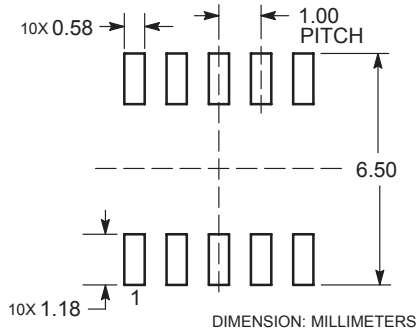
SOIC-10NB
CASE 751BQ-01
ISSUE A



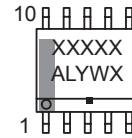
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF 'b' AT MAXIMUM MATERIAL CONDITION.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
 5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
 6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| MILLIMETERS | | |
|-------------|----------|------|
| DIM | MIN | MAX |
| A | 1.25 | 1.75 |
| A1 | 0.10 | 0.25 |
| A3 | 0.17 | 0.25 |
| b | 0.31 | 0.51 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.00 BSC | |
| H | 5.80 | 6.20 |
| h | 0.37 REF | |
| L | 0.40 | 1.27 |
| L2 | 0.25 BSC | |
| M | 0° | 8° |

RECOMMENDED
SOLDERING FOOTPRINT*



GENERIC
MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|-------------|------------------------------------|--------------------------|
| LV5980MD-AH | SOIC10 (Pb-Free / Halogen Free) | 2500 / Tape & Reel |

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