

Features

- Thin small outline package-I (TSOP-I) configurable as 2 M × 16 or as 4 M × 8 static RAM (SRAM)
- High-speed up to 55 ns
- Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra low standby power
 - Typical standby current: 3 μA
 - Maximum standby current: 25 μA
- Ultra low active power
 - Typical active current: 4.5 mA at f = 1 MHz
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} Features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 48-ball TSOP-I package

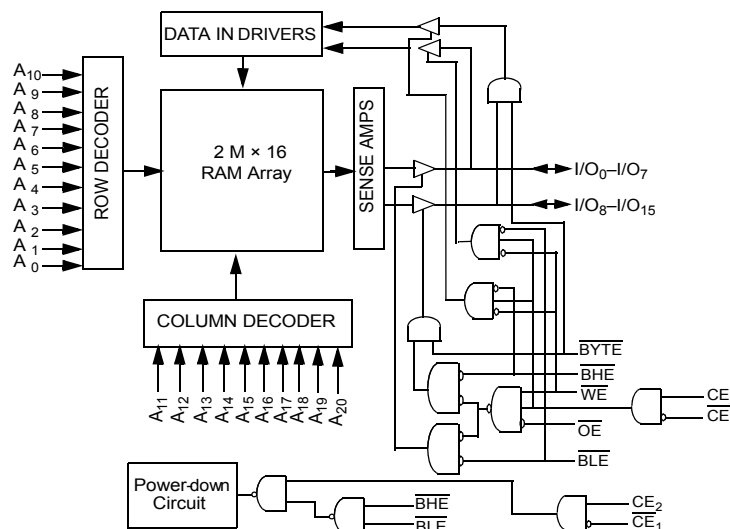
Functional Description

The CY62177ESL is a high performance CMOS static RAM organized as 2 M words by 16 bits and 4 M words by 8 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99 percent when addresses are not toggling. The device can also be put into standby mode when deselected (\overline{CE}_1 HIGH or CE_2 LOW or both \overline{BHE} and \overline{BLE} are HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when: deselected (\overline{CE}_1 HIGH or CE_2 LOW), outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a write operation (\overline{CE}_1 LOW, CE_2 HIGH and \overline{WE} LOW).

To write to the device, take Chip Enables (\overline{CE}_1 LOW and CE_2 HIGH) and Write Enable (\overline{WE}) input LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{20}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written to the location specified on the address pins (A_0 through A_{20}). To read from the device, take Chip Enables (\overline{CE}_1 LOW and CE_2 HIGH) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O_8 to I/O_{15} . See the [Truth Table](#) on page 11 for a complete description of read and write modes.

For a complete list of related documentation, [click here](#).

Logic Block Diagram

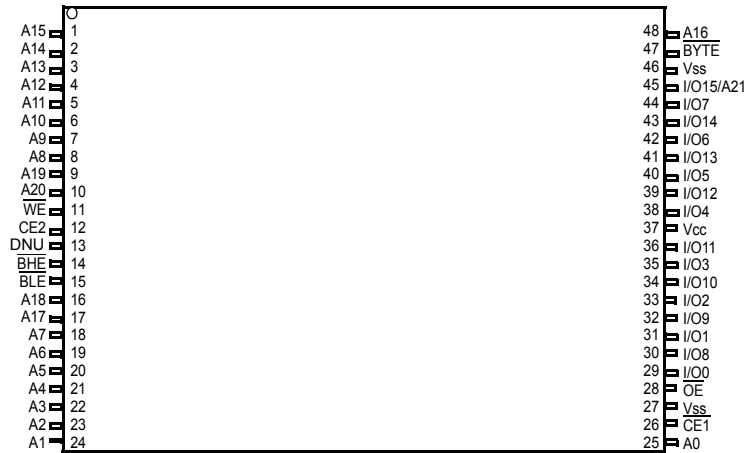


Contents

Pin Configuration	3	Ordering Information	12
Product Portfolio	3	Ordering Code Definitions	12
Maximum Ratings	4	Package Diagrams	13
Operating Range	4	Acronyms	14
Electrical Characteristics	4	Document Conventions	14
Capacitance	5	Units of Measure	14
Thermal Resistance	5	Document History Page	15
AC Test Loads and Waveforms	5	Sales, Solutions, and Legal Information	16
Data Retention Characteristics	6	Worldwide Sales and Design Support	16
Data Retention Waveform	6	Products	16
Switching Characteristics	7	PSoC [®] Solutions	16
Switching Waveforms	8	Cypress Developer Community	16
Truth Table	11	Technical Support	16

Pin Configuration

Figure 1. 48-pin TSOP I pinout (Front View) [1, 2]



Product Portfolio

Product	V _{CC} Range (V) ^[3]	Speed (ns)	Power Dissipation					
			Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
			f = 1 MHz		f = f _{Max}			
			Typ ^[4]	Max	Typ ^[4]	Max	Typ ^[4]	Max
CY62177ESL	2.2 V to 3.6 V and 4.5 V to 5.5 V	55	4.5	5.5	35	45	3	25

Notes

1. NC pins are not connected on the die.
2. The BYTE pin in the 48-pin TSOP-I package has to be tied to V_{CC} to use the device as a 2 M × 16 SRAM. The 48-pin TSOP-I package can also be used as a 4 M × 8 SRAM by tying the BYTE signal to V_{SS}. In the 4 M × 8 configuration, Pin 45 is A21, while BHE, BLE, and I/O₈ to I/O₁₄ pins are not used.
3. Datasheet Specifications are not guaranteed in the range of 3.6 V to 4.5 V.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V, and V_{CC} = 5 V, T_A = 25 °C

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to + 150 °C

Ambient temperature with power applied -55 °C to + 125 °C

Supply voltage to ground potential -0.3 V to $V_{CC(max)}$ + 0.3 V

DC voltage applied to outputs in high Z state ^[5, 6] -0.3 V to $V_{CC(max)}$ + 0.3 V

DC input voltage ^[5, 6] -0.3 V to $V_{CC(max)}$ + 0.3 V

Output current into outputs (LOW) 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) ≥ 2001 V

Latch-up current ≥ 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} ^[7]
CY62177ESL	Industrial	-40 °C to +85 °C	2.2 V to 3.6 V and 4.5 V to 5.5 V

Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions	55 ns			Unit
			Min	Typ ^[8]	Max	
V_{OH}	Output HIGH voltage	$2.2\text{ V} \leq V_{CC} \leq 2.7\text{ V}$ $I_{OH} = -0.1\text{ mA}$	2.0	–	–	V
		$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ $I_{OH} = -1.0\text{ mA}$	2.4	–	–	V
		$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ $I_{OH} = -1.0\text{ mA}$	2.4	–	–	V
V_{OL}	Output LOW voltage	$2.2\text{ V} \leq V_{CC} \leq 2.7\text{ V}$ $I_{OL} = 0.1\text{ mA}$	–	–	0.4	V
		$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ $I_{OL} = 2.1\text{ mA}$	–	–	0.4	V
		$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ $I_{OL} = 2.1\text{ mA}$	–	–	0.4	V
V_{IH}	Input HIGH voltage	$2.2\text{ V} \leq V_{CC} \leq 2.7\text{ V}$	1.8	–	$V_{CC} + 0.3\text{ V}$	V
		$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$	2.2	–	$V_{CC} + 0.3\text{ V}$	V
		$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	2.2	–	$V_{CC} + 0.3\text{ V}$	V
V_{IL}	Input LOW voltage	$2.2\text{ V} \leq V_{CC} \leq 2.7\text{ V}$	-0.3	–	0.6	V
		$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$	-0.3	–	0.7 ^[9]	V
		$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	-0.3	–	0.7 ^[9]	V
I_{IX}	Input leakage current	$\text{GND} \leq V_I \leq V_{CC}$	-1	–	+1	μA
I_{OZ}	Output leakage current	$\text{GND} \leq V_O \leq V_{CC}$, Output disabled	-1	–	+1	μA
I_{CC}	V_{CC} operating supply current	$f = f_{Max} = 1/t_{RC}$ $V_{CC} = V_{CC(max)}$	–	35	45	mA
		$f = 1\text{ MHz}$ $I_{OUT} = 0\text{ mA}$ CMOS levels	–	4.5	5.5	mA
I_{SB2} ^[10]	Automatic power-down current — CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $\overline{CE}_2 \leq 0.2\text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$, $f = 0$, $V_{CC} = 3.6\text{ V}$	–	3	25	μA

Notes

- $V_{IL(min)}$ = -2.0 V for pulse durations less than 20 ns.
- $V_{IH(max)}$ = $V_{CC} + 0.75\text{ V}$ for pulse durations less than 20 ns.
- Full Device AC operation assumes a 100 μs ramp time from 0 to V_{CC} (min) and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 3\text{ V}$, and $V_{CC} = 5\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$
- Under DC conditions the device meets a V_{IL} of 0.8 V. However, in dynamic conditions Input LOW voltage applied to the device must not be higher than 0.7 V.
- Chip enables (\overline{CE}_1 and \overline{CE}_2), byte enables (\overline{BHE} and \overline{BLE}) and BYTE must be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

Parameter ^[11]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)}	15	pF
C _{OUT}	Output capacitance		15	pF

Thermal Resistance

Parameter ^[11]	Description	Test Conditions	TSOP I	Unit
Θ _{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	55.91	°C/W
Θ _{JC}	Thermal resistance (junction to case)		9.39	°C/W

AC Test Loads and Waveforms

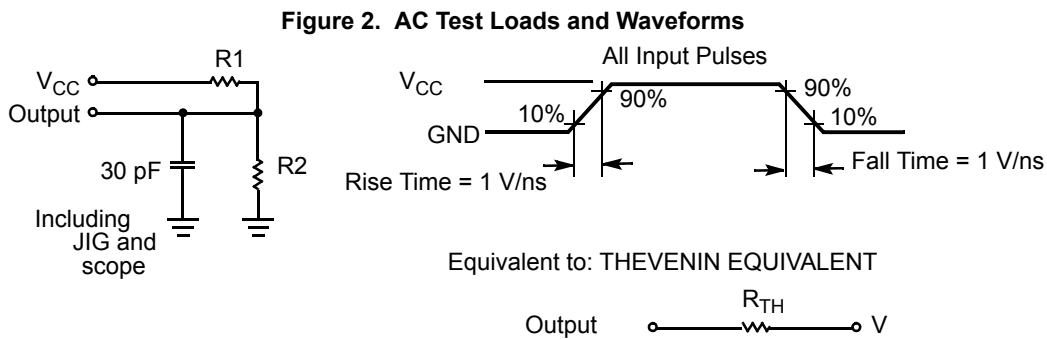


Table 1. AC Test Loads

Parameter	2.5 V	3.0 V	5.0 V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R _{TH}	8000	645	639	Ω
V _{TH}	1.20	1.75	1.77	V

Note

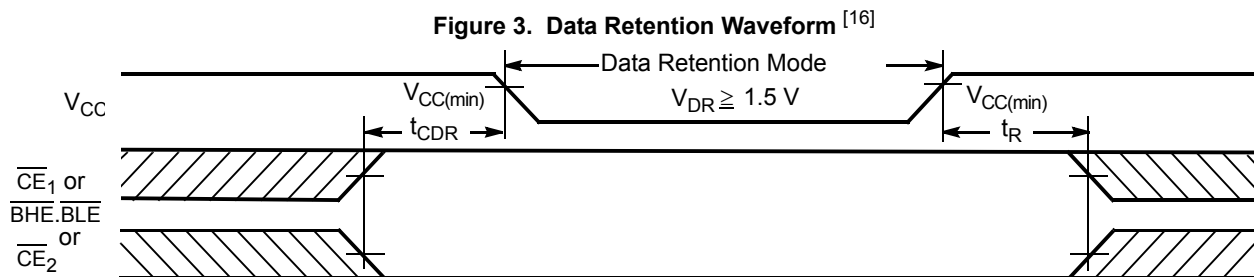
11. Tested initially and after any design or process changes that may effect these parameters.

Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions	Min	Typ ^[12]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
I_{CCDR} ^[13]	Data retention current	$V_{CC} = 1.5\text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	17	μA
t_{CDR} ^[14]	Chip deselect to data retention time	–	0	–	–	ns
t_R ^[15]	Operation recovery time	–	55	–	–	ns

Data Retention Waveform



Notes

12. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at $V_{CC} = 3\text{ V}$, and $V_{CC} = 5\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$.
13. Chip enables (CE1 and CE2), byte enables (BHE and BLE) and BYTE must be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
14. Tested initially and after any design or process changes that may affect these parameters.
15. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min)} \geq 100\text{ }\mu\text{s}$.
16. BHE.BLE is the AND of both BHE and BLE. Chip is deselected by either disabling the chip enable signals or by disabling both BHE and BLE.

Switching Characteristics

Over the operating range

Parameter [17, 18]	Description	55 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	55	–	ns
t_{AA}	Address to data valid	–	55	ns
t_{OHA}	Data hold from address change	6	–	ns
t_{ACE}	\overline{CE}_1 LOW and CE_2 HIGH to data valid	–	55	ns
t_{DOE}	\overline{OE} LOW to data valid	–	25	ns
t_{LZOE}	\overline{OE} LOW to low Z ^[19]	5	–	ns
t_{HZOE}	\overline{OE} HIGH to high Z ^[19, 20]	–	18	ns
t_{LZCE}	\overline{CE}_1 LOW and CE_2 HIGH to low Z ^[19]	10	–	ns
t_{HZCE}	\overline{CE}_1 HIGH and CE_2 LOW to high Z ^[19, 20]	–	18	ns
t_{PU}	\overline{CE}_1 LOW and CE_2 HIGH to power-up	0	–	ns
t_{PD}	\overline{CE}_1 HIGH and CE_2 LOW to power-down	–	55	ns
t_{DBE}	BLE/BHE LOW to data valid	–	55	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to low Z ^[19]	10	–	ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to high Z ^[19, 20]	–	18	ns
Write Cycle^[21]				
t_{WC}	Write cycle time	55	–	ns
t_{SCE}	\overline{CE}_1 LOW and CE_2 HIGH to write end	40	–	ns
t_{AW}	Address setup to write end	40	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	\overline{WE} pulse width	40	–	ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	40	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	\overline{WE} LOW to high Z ^[19, 20]	–	20	ns
t_{LZWE}	\overline{WE} HIGH to low Z ^[19]	10	–	ns

Notes

17. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Note is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
18. Test conditions for all parameters other than tristate parameters assume signal transition time of 1 V/ns, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in Figure 2 on page 5.
19. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
20. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
21. The internal Write time of the memory is defined by the overlap of \overline{WE} , $CE_1 = V_{IL}$, BHE and/or $BLE = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [22, 23]

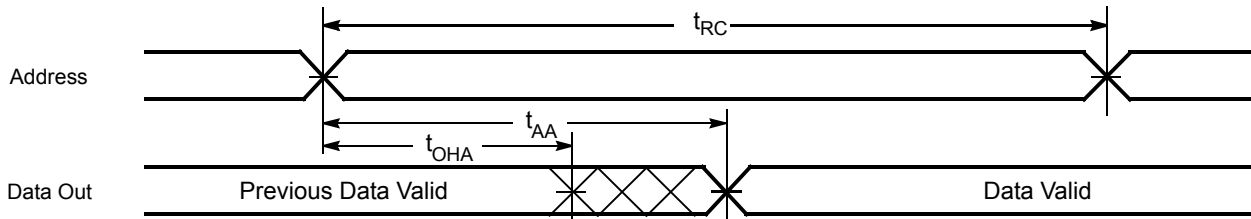
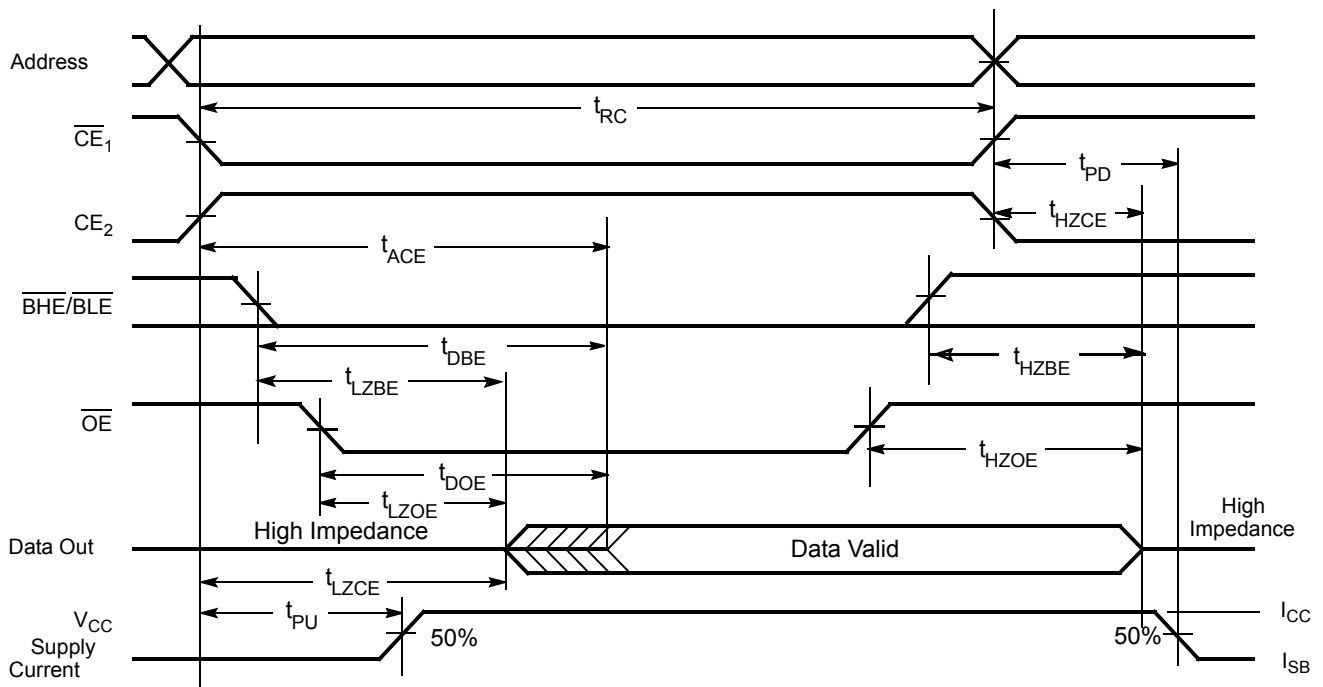


Figure 5. Read Cycle No. 2 (\overline{OE} Controlled) [23, 24]



Notes

22. The device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$.

23. \overline{WE} is HIGH for read cycle.

24. Address valid prior to or coincident with \overline{CE}_1 , \overline{BHE} , \overline{BLE} transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 (\overline{WE} Controlled) [25, 26, 27]

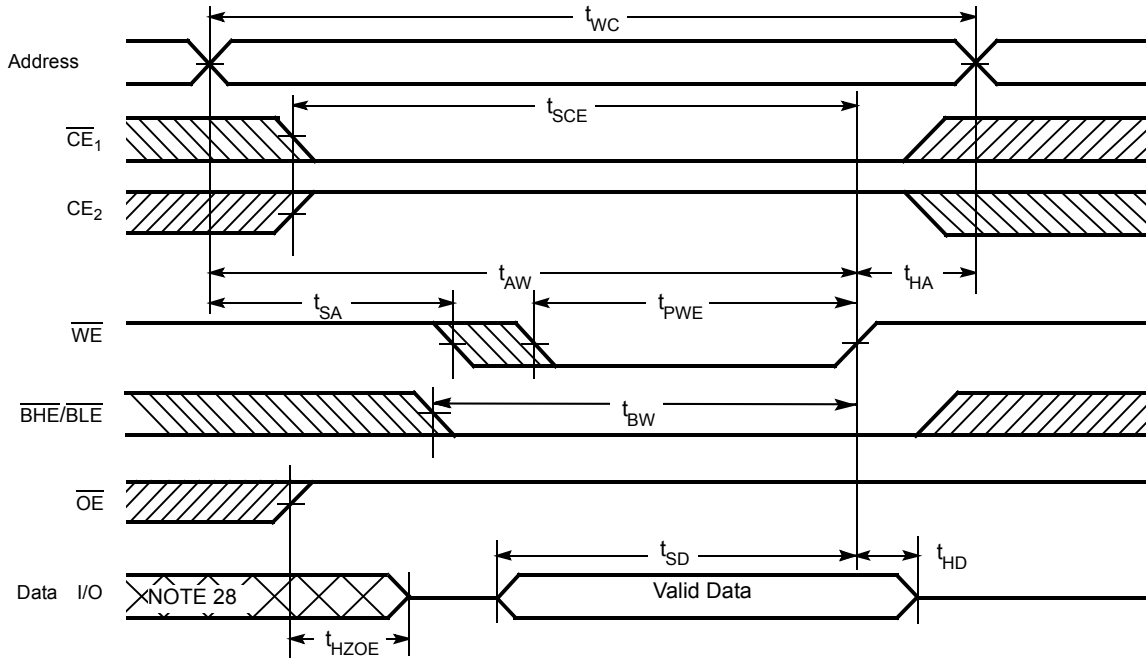
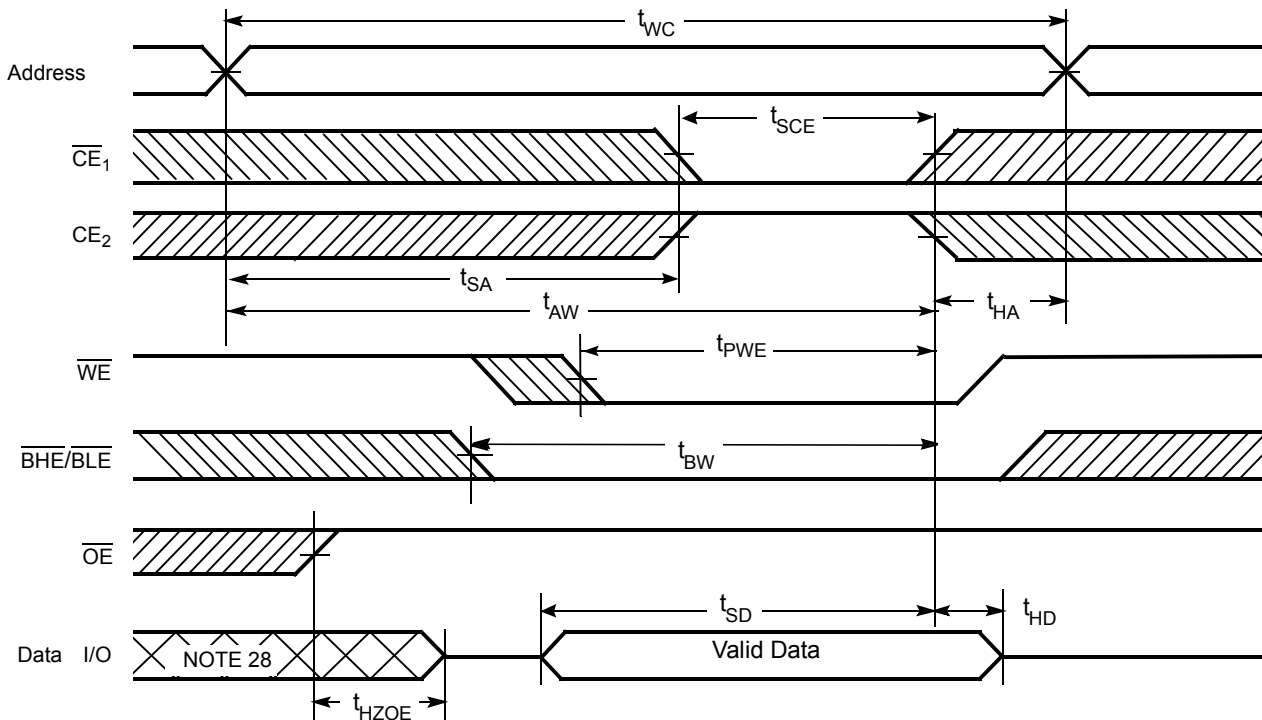


Figure 7. Write Cycle No. 2 (\overline{CE}_1 or CE_2 Controlled) [25, 26, 27]



Notes

- 25. The internal Write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 26. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 27. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 28. During this period the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[29]

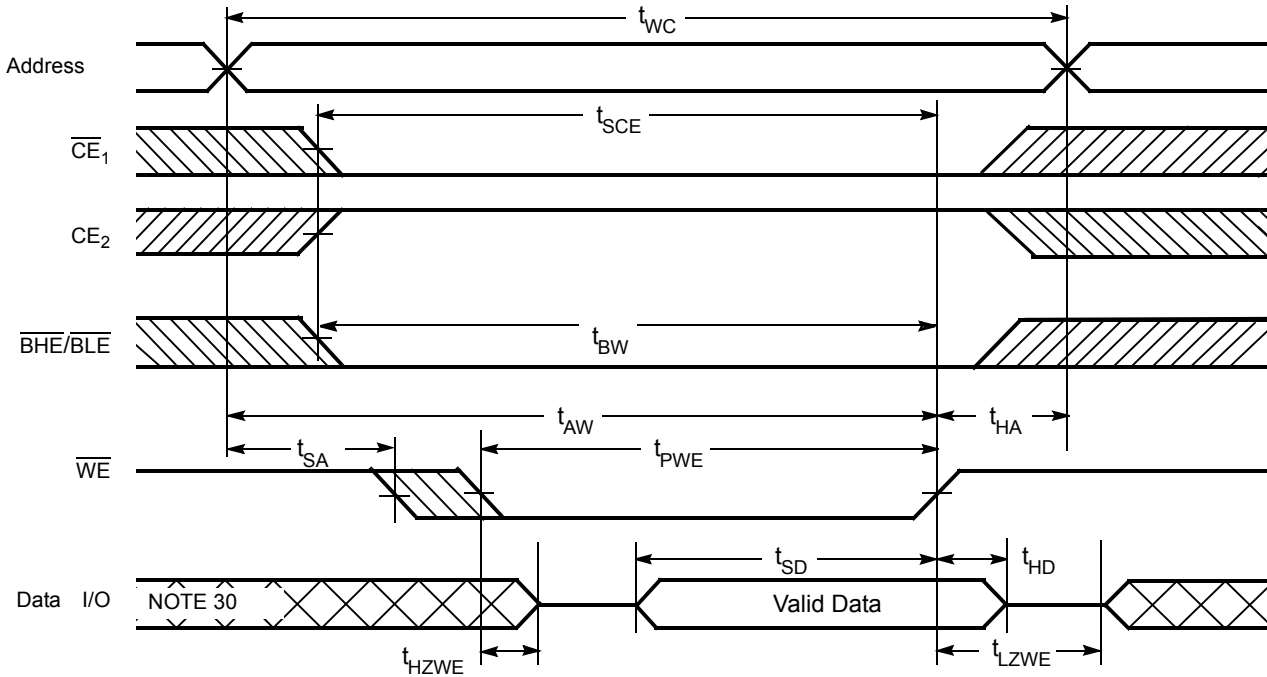
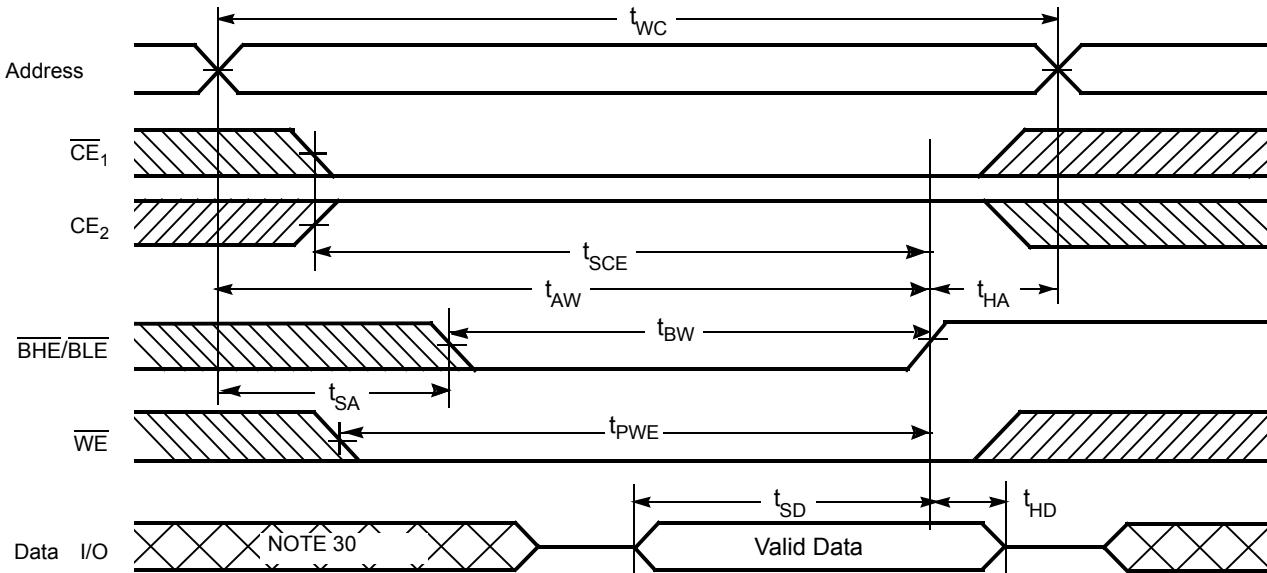


Figure 9. Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ Controlled, \overline{OE} LOW)^[29]



Notes

- 29. If \overline{CE}_1 goes HIGH and \overline{CE}_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 30. During this period the I/Os are in output state and input signals should not be applied.

Truth Table

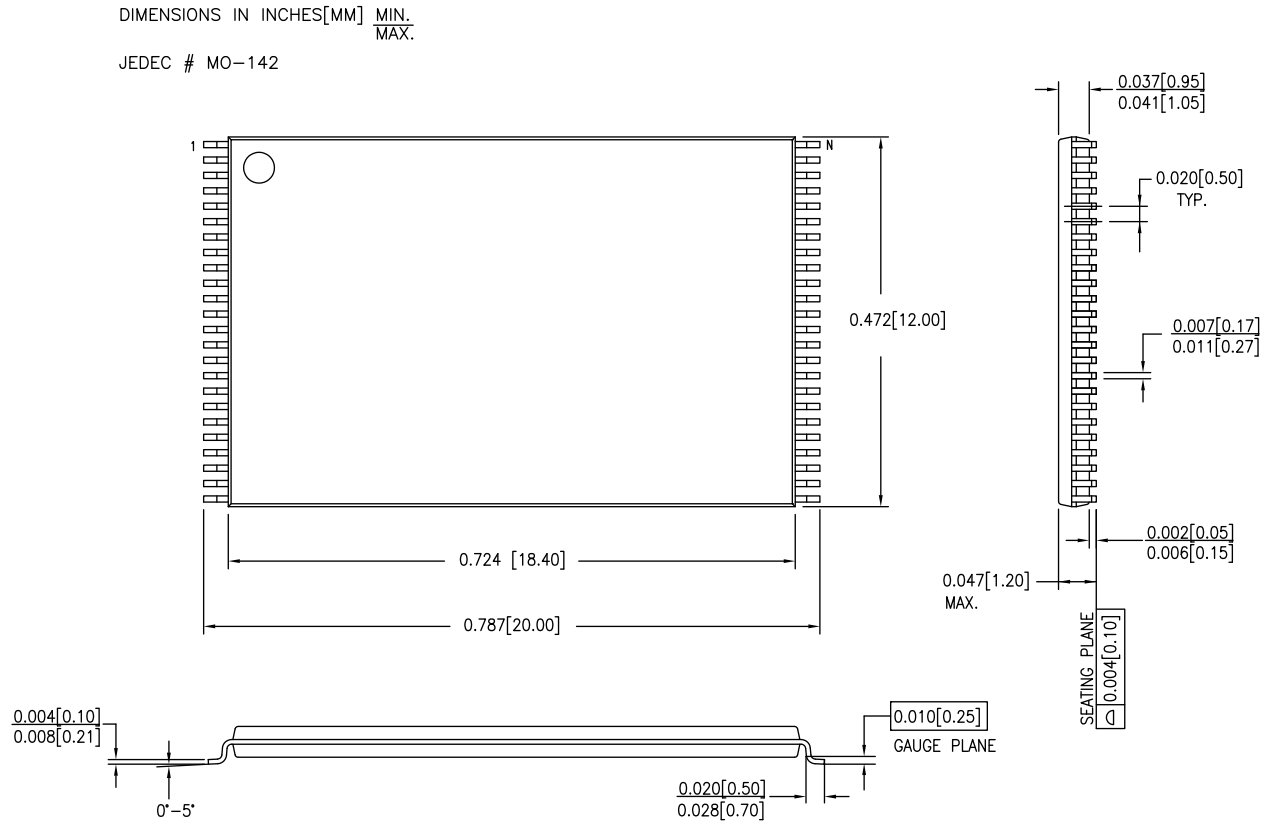
CE ₁	CE ₂	WE	OE	BHE	BLE	Inputs Outputs	Mode	Power
H	X ^[31]	X	X	X ^[31]	X ^[31]	High Z	Deselect/Power-down	Standby (I _{SB})
X ^[31]	L	X	X	X ^[31]	X ^[31]	High Z	Deselect/Power-down	Standby (I _{SB})
X ^[31]	X ^[31]	X	X	H	H	High Z	Deselect/Power-down	Standby (I _{SB})
L	H	H	L	L	L	Data out (I/O ₀ –I/O ₁₅)	Read	Active (I _{CC})
L	H	H	L	H	L	High Z (I/O ₈ –I/O ₁₅); Data out (I/O ₀ –I/O ₇)	Read	Active (I _{CC})
L	H	H	L	L	H	Data out (I/O ₈ –I/O ₁₅); High Z (I/O ₀ –I/O ₇)	Read	Active (I _{CC})
L	H	L	X	L	L	Data in (I/O ₀ –I/O ₁₅)	Write	Active (I _{CC})
L	H	L	X	H	L	High Z (I/O ₈ –I/O ₁₅); Data in (I/O ₀ –I/O ₇)	Write	Active (I _{CC})
L	H	L	X	L	H	Data in (I/O ₈ –I/O ₁₅); High Z (I/O ₀ –I/O ₇)	Write	Active (I _{CC})
L	H	H	H	L	H	High Z	Output disabled	Active (I _{CC})
L	H	H	H	H	L	High Z	Output disabled	Active (I _{CC})
L	H	H	H	L	L	High Z	Output disabled	Active (I _{CC})

Note

31. The 'X' (Don't care) state for the chip enables and byte enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Package Diagrams

Figure 10. 48-pin TSOP I (12 × 18.4 × 1 mm) Z48A Package Outline, 51-85183



51-85183 *D

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62177ESL MoBL®, 32-Mbit (2 M × 16/4 M × 8) Static RAM Document Number: 001-64709				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3077028	RAME	11/02/10	New data sheet.
*A	3103863	RAME	12/07/2010	Updated Ordering Information : No change in part numbers. The specified part in the ordering information table is moved to production.
*B	3433813	TAVA	11/16/2011	Updated Functional Description : Removed Note "For best practice recommendations, refer to the Cypress application note System Design Guidelines ." and its reference. Updated Pin Configuration : Updated Figure 1 (Changed pin 13 from NC to DNU).
*C	4101093	VINI	08/21/2013	Updated Switching Characteristics : Added Note 17 and referred the same note in "Parameter" column. Updated to new template.
*D	4573215	VINI	11/18/2014	Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end. Completing Sunset Review.
*E	5016184	NILE	11/17/2015	Updated Thermal Resistance : Replaced "two-layer" with "four-layer" in "Test Conditions" column. Changed value of θ_{JA} parameter corresponding to TSOP I package from 44.66 °C/W to 55.91 °C/W. Changed value of θ_{JC} parameter corresponding to TSOP I package from 12.12 °C/W to 9.39 °C/W. Updated Package Diagrams : spec 51-85183 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC[®] Solutions

psoc.cypress.com/solutions
PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

Technical Support

cypress.com/go/support

© Cypress Semiconductor Corporation, 2010-2015. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and/or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.