AKD4632-A
AK4632 Evaluation board Rev.0

GENERAL DESCRIPTION

AKD4632-A is an evaluation board for the AK4632, 16bit mono CODEC with MIC/SPK/VIDEO amplifier. The AKD4632-A can evaluate A/D converter and D/A converter separately in addition to loopback mode (A/D → D/A). AKD4632-A also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4632-A --- Evaluation board for AK4632
(Cable for connecting with printer port of IBM-AT, compatible PC and control software are packed with this. This control software does not support Windows NT.)

FUNCTION

- **DIT/DIR with optical input/output**
- **BNC connector for an external clock input**
- **10pin Header for serial control mode**

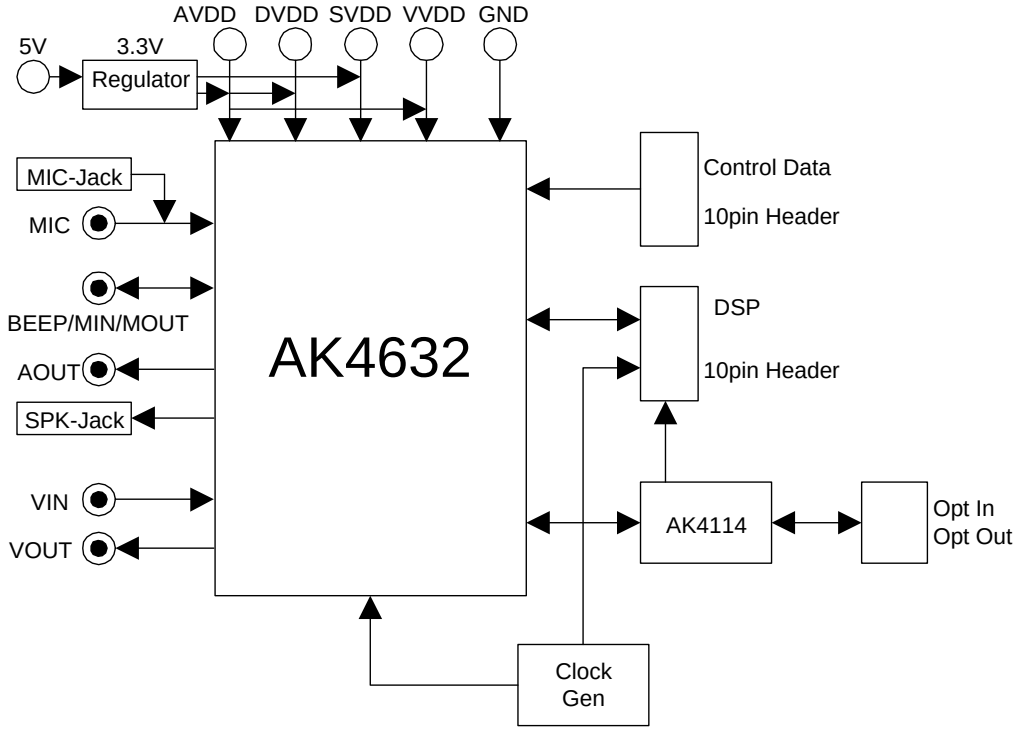


Figure 1. AKD4632-A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

Evaluation Board Manual

■ Operation sequence

1) Set up the power supply lines.

1-1) When AVDD, DVDD, SVDD, VVDD and VCC are supplied from the regulator. (AVDD, DVDD, SVDD, VVDD and VCC jack should be open.). See "**Other jumper pins set up** (page 10)". <default>

[REG]	(red)	= 5V	
[AVDD]	(orange)	= open	: 3.3V is supplied to AVDD of AK4632 from regulator.
[DVDD]	(orange)	= open	: 3.3V is supplied to DVDD of AK4632 from regulator.
[SVDD]	(blue)	= open	: 3.3V is supplied to SVDD of AK4632 from regulator.
[VVDD]	(blue)	= open	: 3.3V is supplied to VVDD of AK4632 from regulator.
[VCC]	(orenge)	= open	: 3.3V is supplied to logic block from regulator.
[AVSS]	(black)	= 0V	: for analog ground
[AGND]	(black)	= 0V	: for analog ground
[DGND]	(black)	= 0V	: for logic ground

1-2) When AVDD, DVDD, SVDD, VVDD and VCC are not supplied from the regulator. (AVDD, DVDD, SVDD, VVDD and VCC jack should be junction.) See "**Other jumper pins set up** (page 10)".

[REG]	(red)	= "REG" jack should be open.
[AVDD]	(orange)	= 2.6 ~ 3.6V : for AVDD of AK4632 (typ. 3.3V)
[DVDD]	(orange)	= 2.6 ~ 3.6V : for DVDD of AK4632 (typ. 3.3V)
[SVDD]	(blue)	= 2.6 ~ 5.25V: for SVDD of AK4632 (typ. 3.3V, 5.0V)
[VVDD]	(blue)	= 2.6 ~ 5.25V: for VVDD of AK4632 (typ. 3.3V, 5.0V)
[VCC]	(orenge)	= 2.6 ~ 3.6V : for logic (typ. 3.3V)
[AVSS]	(black)	= 0V : for analog ground
[AGND]	(black)	= 0V : for analog ground
[DGND]	(black)	= 0V : for logic ground

Each supply line should be distributed from the power supply unit.
AVDD and DVDD must be same voltage level.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.
The AK4632 and AK4114 should be reset once bringing SW1, 2 "L" upon power-up.

■ Evaluation mode

In case of AK4632 evaluation using AK4114, it is necessary to correspond to audio interface format for AK4632 and AK4114. About AK4632's audio interface format, refer to datasheet of AK4632. About AK4114's audio interface format, refer to Table 2 in this manual.

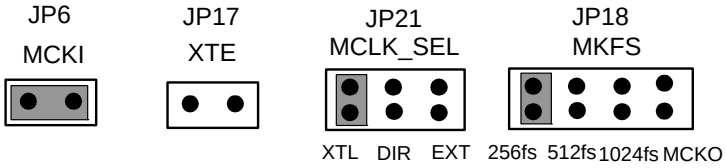
Applicable Evaluation Mode

(1) Evaluation of loop-back mode (A/D → D/A) : PLL, Master Mode (Default)
(2) Evaluation of loop-back mode (A/D → D/A) : PLL, Slave Mode (PLL Reference CLOCK: MCKI pin)
(3) Evaluation of loop-back mode (A/D → D/A) : PLL, Slave Mode (PLL Reference CLOCK: BICK or FCK pin)
(4) Evaluation of using DIR of AK4114 (opt-connector) : EXT, Slave Mode
(5) Evaluation of using DIT of AK4114 (opt-connector) : EXT, Slave Mode

(1) Evaluation of loop-back mode (A/D → D/A) : PLL, Master Mode (Default)

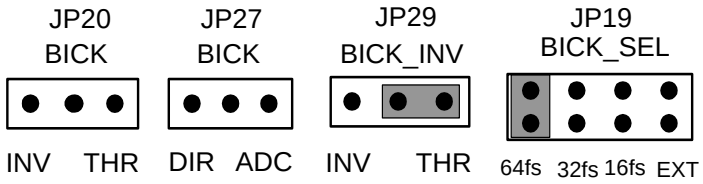
a) Set up jumper pins of MCKI clock

"MCKPD bit" in the AK4632 should be set to "0".
X'tal of 11.2896MHz, 12MHz, 12.288MHz, 13MHz, 24MHz or 27MHz can be set in X1. X'tal of 12.288MHz (Default) is set on the AKD4632-A. Set "No.8 of SW3" to "H".
When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13MHz, 24MHz or 27MHz) through a RCA connector (J8: EXT/BICK) is supplied, select EXT on JP21 (MCLK_SEL) and short JP17 (XTE). JP23 (EXT1) and R26 should be properly selected in order to much the output impedance of the clock generator.

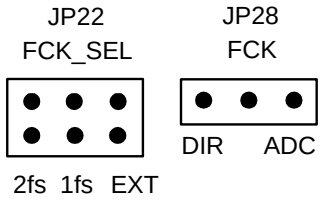


b) Set up jumper pins of BICK clock

Output frequency (16fs/32fs/64fs) of BICK should be set by "BCKO1-0 bit" in the AK4632.
There is no necessity for set up JP19.

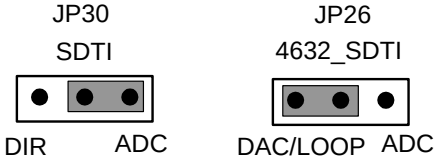


c) Set up jumper pins of FCK clock



d) Set up jumper pins of DATA

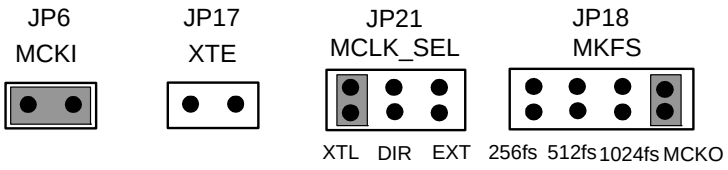
When the AK4632 is evaluated by loop-back mode (A/D → D/A), the jumper pins should be set to the following.



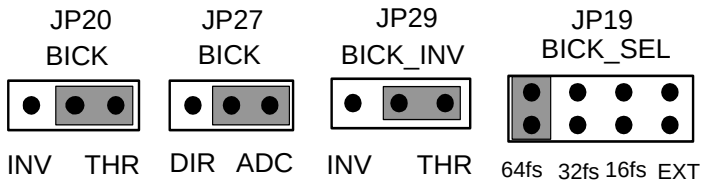
(2) Evaluation of loop-back mode (A/D → D/A) : PLL, Slave Mode (PLL Reference CLOCK: MCKI pin)

a) Set up jumper pins of MCKI clock

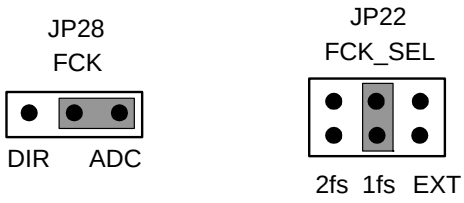
"MCKPD bit" in the AK4632 should be set to "0".
X'tal of 12.288MHz (Default) is set on the AKD4632-A. In this case, the AK4632 corresponds to PLL reference clock of 12.288MHz. In this evaluation mode, the output clock from MCKO-pin of the AK4632 is supplied to a divider (U3: 74VHC4040), BICK and FCK clocks are generated by the divider. Then "MCKO bit" in the AK4632 is set to "1". When an external clock through a RCA connector (J8: EXT/BICK) is supplied, select EXT on JP21 (MCLK_SEL) and short JP17 (XTE). JP23 (EXT1) and R26 should be properly selected in order to much the output impedance of the clock generator.



b) Set up jumper pins of BICK clock

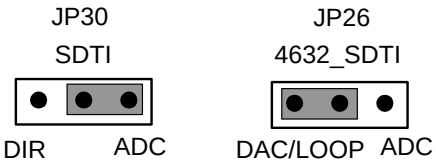


c) Set up jumper pins of FCK clock



d) Set up jumper pins of DATA

When the AK4632 is evaluated by loop-back mode (A/D → D/A), the jumper pins should be set to the following.



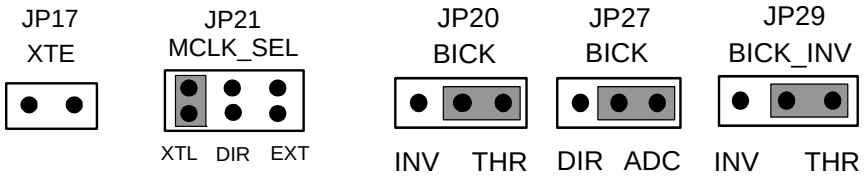
(3) Evaluation of loop-back mode (A/D → D/A) : PLL, Slave Mode (PLL Reference CLOCK: BICK or FCK pin)

a) Set up jumper pins of MCKI clock

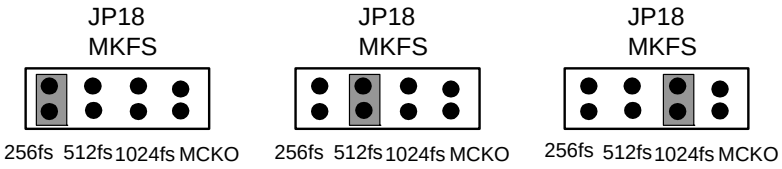
"MCKPD bit" in the AK4632 should be set to "1". JP6 (MCKI) should be open.

b) Set up jumper pins of BICK clock

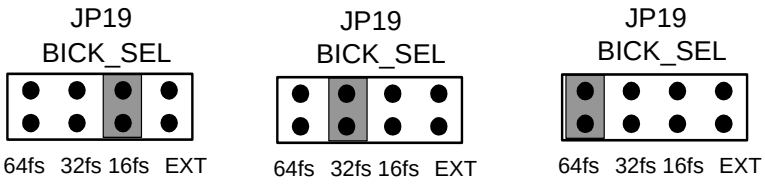
When an external clock through a RCA connector J8 (EXT/BICK) is supplied, select EXT on JP19 (MCLK_SEL) and short JP17 (XTE). JP23 (EXT1) and R26 should be properly selected in order to much the output impedance of the clock generator.



In this evaluation mode, the selected clock from JP21 (MCLK_SEL) is supplied to a divider (U3: 74VHC4040), BICK and FCK clocks are generated by the divider. Input frequency of master clock is set up in turn "256fs", "512fs", "1024fs" from left.

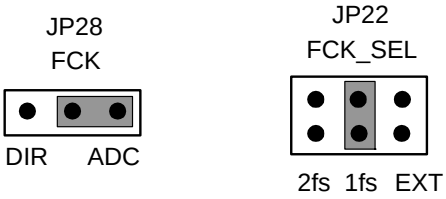


And input frequency of BICK is set up in turn "16fs", "32fs", "64fs" from left.



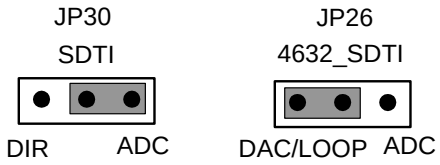
c) Set up jumper pins of FCK clock

When an external clock through a RCA connector J9 (FCK) is supplied, select EXT on JP22 (FCK_SEL). JP24 (EXT2) and R27 should be properly selected in order to much the output impedance of the clock generator.



d) Set up jumper pins of DATA

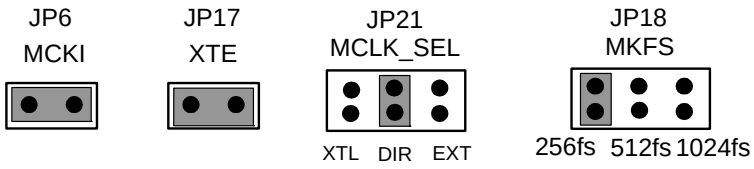
When the AK4632 is evaluated by loop-back mode (A/D → D/A), the jumper pins should be set to the following.



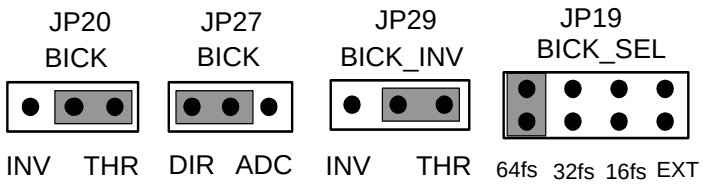
(4) Evaluation of using DIR of AK4114 (opt-connector) : EXT, Slave Mode

a) Set up jumper pins of MCKI clock

"MCKPD bit" in the AK4632 should be set to "0".

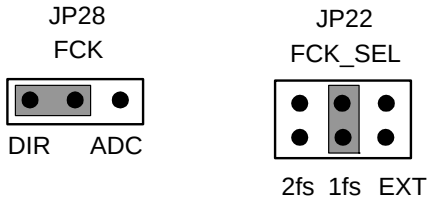


b) Set up jumper pins of BICK clock



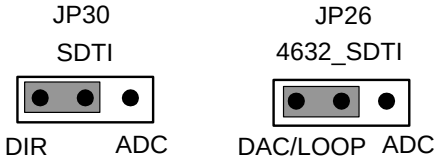
c) Set up jumper pins of FCK clock

JP24 (EXT2) and R27 should be properly selected in order to much the output impedance of the clock generator.



d) Set up jumper pins of DATA

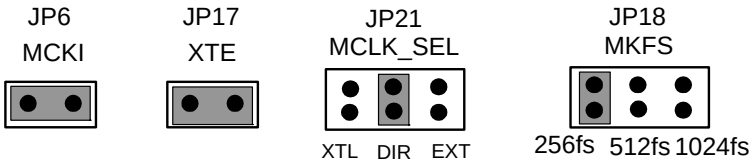
When D/A converter of the AK4632 is evaluated by using DIR of AK4114, the jumper pins should be set to the following.



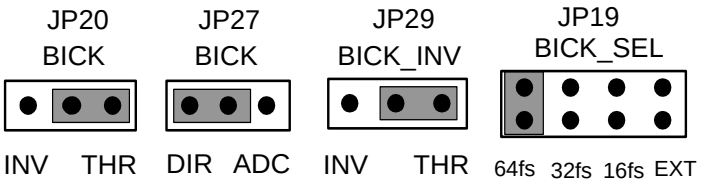
(5) Evaluation of using DIT of AK4114 (opt-connector) : EXT, Slave Mode

a) Set up jumper pins of MCKI clock

"MCKPD bit" in the AK4632 should be set to "0".

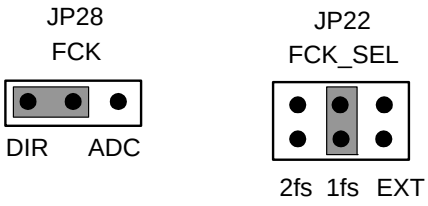


b) Set up jumper pins of BICK clock



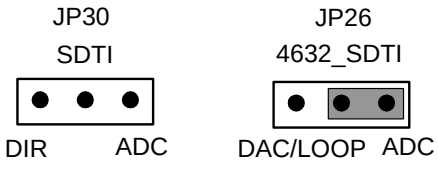
c) Set up jumper pins of FCK clock

JP24 (EXT2) and R27 should be properly selected in order to much the output impedance of the clock generator.



d) Set up jumper pins of DATA

When A/D converter of the AK4632 is evaluated by using DIR of AK4114, the jumper pins should be set to the following.



■ DIP Switch set up

[SW3] (MODE) : Mode Setting of AK4632 and AK4114
ON is "H", OFF is "L".

No.	Name	ON ("H")	OFF ("L")
1	DIF0	AK4114 Audio Format Setting See Table 2	
2	DIF1		
3	CM2		
4	CM0	Clock Operation Mode select See Table 3	
5	CM1		
6	OCKS0	Master Clock Frequency Select See Table 4	
7	OCKS1		
8	M/S	Master mode	Slave mode

Note. When the AK4632 is evaluated Master mode, "No.8 of SW3" is set to "H".
Table 1. Mode Setting for AK4632 and AK4114

Register setting for AK4632 Audio Interface Format		Setting for AK4114 Audio Interface Format					
DIF1 bit	DIF0 bit	DIF0	DIF1	DIF2	DAUX	SDTO	
0	1	L	L	L	24bit, Left justified	16bit, Right justified	
1	0	L	L	H	24bit, Left justified	24bit, Left justified	Default
1	1	H	L	H	24bit, I^2S	24bit, I^2S	

Note. When the AK4632 is evaluated by using DIR/DIT of AK4114, "No.8 of SW3" is set to "L".
Table 2. Setting for AK4114 Audio Interface Format

Mode	CM1	CM0	UNLOCK	PLL	X'tal	Clock source	SDTO	
0	0	0	-	ON	ON(Note)	PLL	RX	
1	0	1	-	OFF	ON	X'tal	DAUX	
2	1	0	0	ON	ON	PLL	RX	Default
			1	ON	ON	X'tal	DAUX	
3	1	1	-	ON	ON	X'tal	DAUX	

ON: Oscillation (Power-up), OFF: STOP (Power-down)
Note : When the X'tal is not used as clock comparison for fs detection (i.e. XTL1,0= "1,1"), the X'tal is off.

Table 3. Clock Operation Mode select

No.	OCKS1	MCKO1	MCKO2	X'tal	
0	0	256fs	256fs	256fs	Default
2	1	512fs	256fs	512fs	

Table 4. Master Clock Frequency Select (Stereo mode)

■ Other jumper pins set up

1. JP1 (GND) : Analog ground and Digital ground
   - OPEN : Separated.
   - SHORT : Common. (The connector “DGND” can be open.) <Default>

2. JP2 (AIN) : Connection between MICOUT pin and AIN pin of the AK4632.
   - OPEN : No connection.
   - SHORT : Connection. <Default>

3. JP3 (AVDD_SEL) : AVDD of the AK4632
   - REG : AVDD is supplied from the regulator (“AVDD” jack should be open). < Default >
   - AVDD : AVDD is supplied from “AVDD ” jack.

4. JP8 (VVDD_SEL) : VVDD of the AK4632
   - AVDD : AVDD is supplied from “AVDD”. < Default >
   - VVDD : VVDD is supplied from “VVDD ” jack.

5. JP9 (DVDD_SEL) : DVDD of the AK4632
   - AVDD : DVDD is supplied from “AVDD”. < Default >
   - DVDD : DVDD is supplied from “DVDD ” jack.

6. JP10 (LVC_SEL) : Logic block of LVC is selected supply line.
   - DVDD : Logic block of LVC is supplied from “DVDD”. < Default >
   - VCC : Logic block of LVC is supplied from “VCC ” jack.

7. JP11 (VCC_SEL) : Logic block is selected supply line.
   - LVC : Logic is supplied from supply line of LVC. < Default >
   - VCC : Logic block of LVC is supplied from “VCC ” jack.

8. JP4 (SVDD_SEL) : SVDD of the AK4632
   - REG : SVDD is supplied from the regulator (“SVDD” jack should be open). < Default >
   - SVDD : SVDD is supplied from “SVDD ” jack.

9. JP8 (MCKO_SEL) : Master Clock Frequency is selected clock from MCKO1 or MCKO2 of the AK4114.
   - MCKO1 : The check from MCKO1 of AK4114 is provided to MCKI of the AK4632. < Default >
   - MCKO2 : The check from MCKO2 of AK4114 is provided to MCKI of the AK4632.

■ The function of the toggle SW

[SW1] (DIR) : Power control of AK4114. Keep “H” during normal operation.
Keep “L” when AK4114 is not used.

[SW2] (PDN) : Power control of AK4632. Keep “H” during normal operation.

■ Indication for LED

[LED1] (ERF): Monitor INT0 pin of the AK4114. LED turns on when some error has occurred to AK4114.

■ Serial Control

The AK4632 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT2 (CTRL) with PC by 10 wire flat cable packed with the AKD4632-A

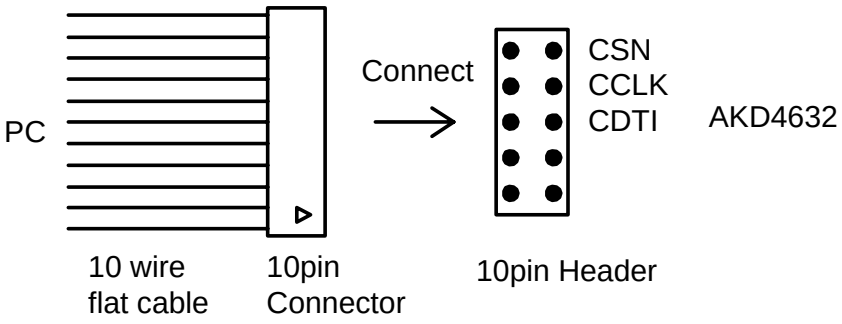


Figure 2. Connect of 10 wire flat cable

■ Analog Input / Output Circuits

(1) Input Circuits

a) MIC Input Circuit

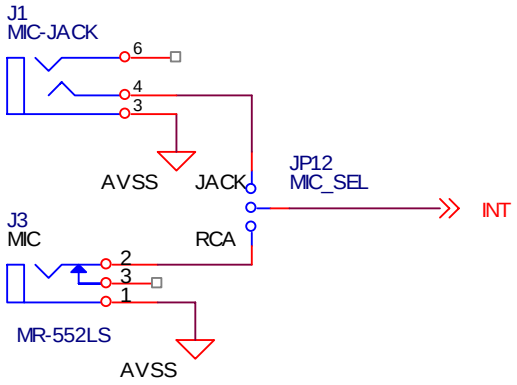
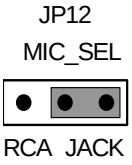
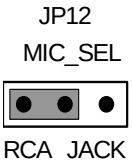


Figure 3. MIC Input Circuit

(a-1) Analog signal is input to INT pin via J1 connector.



(a-2) Analog signal is input to INT pin via J3 connector.



b) VIN Input Circuit

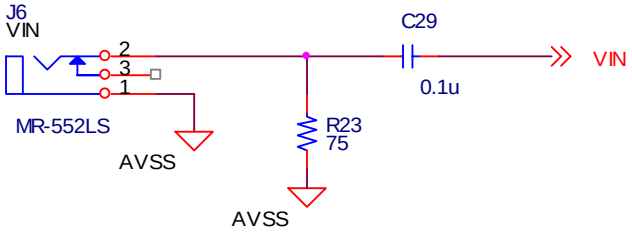


Figure 4. VIN Input Circuit

(2) Output Circuits

a) AOUT Output Circuit

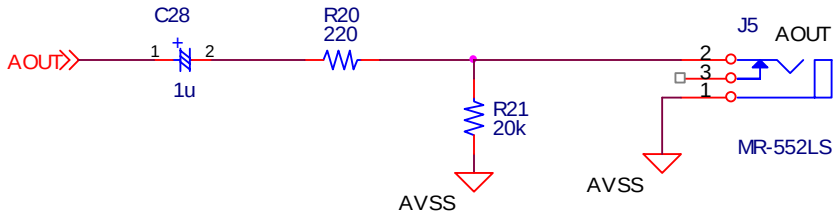


Figure 5. AOUT Output Circuit

b) VOUT Output Circuit

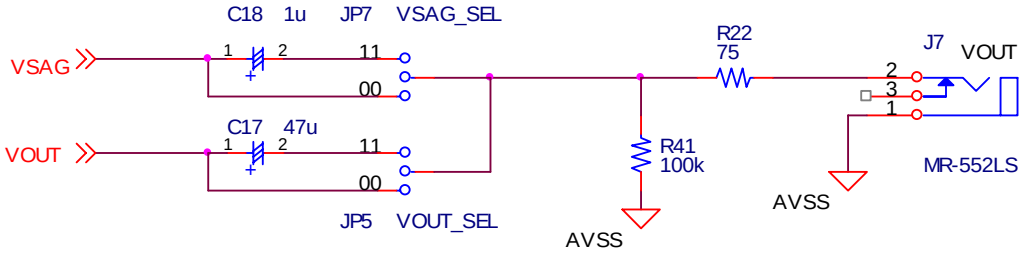
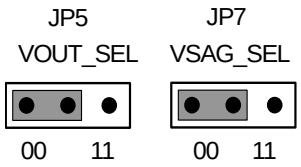
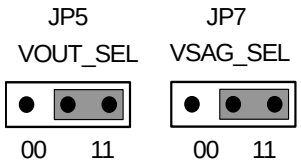


Figure 6. VOUT Output Circuit

(b-1) “DC Output” is output from J7 connector.



(b-2) “SAG Trimming Circuit ” is output from J7 connector.



C) SPK Output Circuit

Note. When mini-jack is inserted or pulled out J2 (SPK-JACK) connector, JP13 (SPP_SEL) and JP14 (SPN_SEL) should be open, or "PMSPK bit" in the AK4632 should be set to "0".

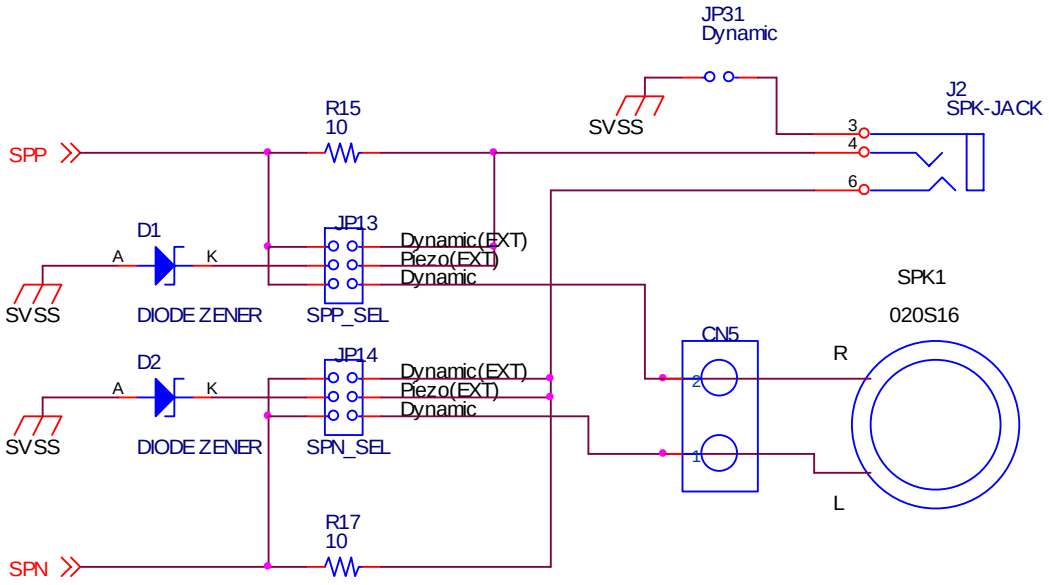
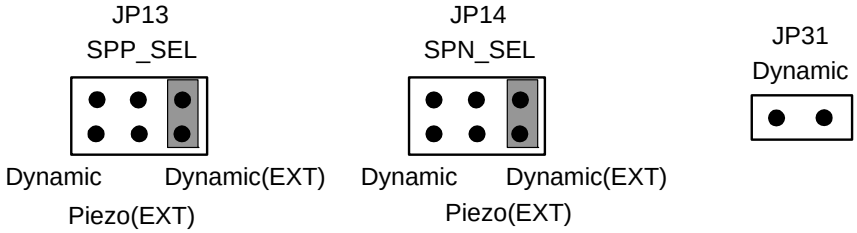
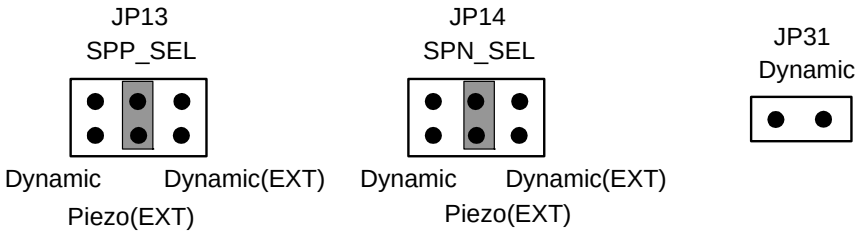


Figure 7. SPK Output Circuit

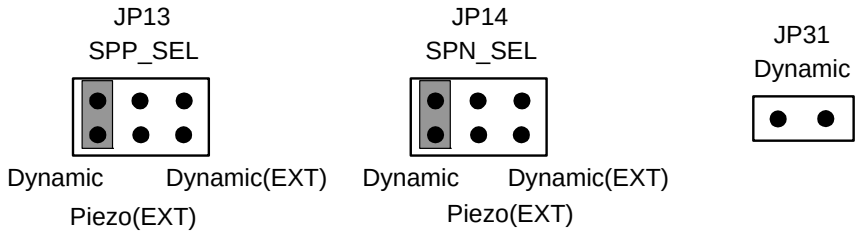
(C-1) "Dynamic Speaker" of external is evaluated by using J2 (SPK-JACK) connector.



(C-2) "Piezo (Ceramic) Speaker" of external is evaluated by using J2 (SPK-JACK) connector.



(C-3) Analog signal of SPP/SPN pins are output “Dynamic Speaker” on the evaluation (SPK1).



(3) BEEP/MIN/MOUT Input and Output Circuit

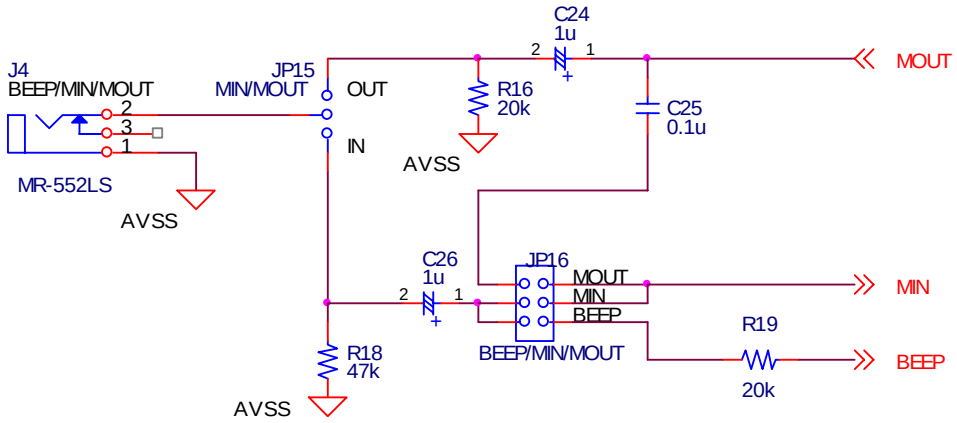
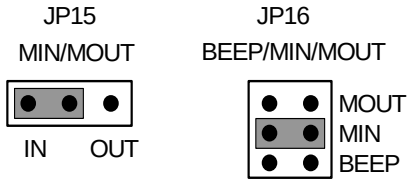
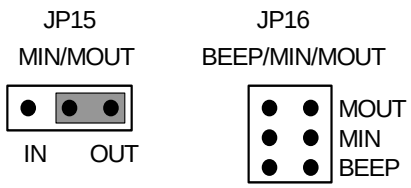


Figure 8. BEEP/MIN/MOUT Input and Output Circuit

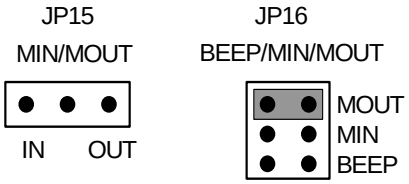
(3-1) Analog signal is input to MIN pin from J4 connector.



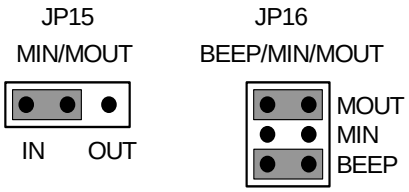
(3-2) Analog signal of MOUT pin is output from J4 connector.



(3-3) Analog signal of MOUT pin is input to MIN pin.



(3-4) Analog signal is input to BEEP pin from J4 connector.



∗ AKM assumes no responsibility for the trouble when using the above circuit examples.

Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4632-A according to previous term.

2. Connect IBM-AT compatible PC with AKD4632-A by 10-line type flat cable (packed with AKD4632-A). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer “Installation Manual of Control Software Driver by AKM device control software”. In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled “AKD4632-A Evaluation Kit” into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of “akd4632.exe” to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click “Port Reset” button.
3. Click “Write default” button

■ Explanation of each buttons

1. [Port Reset] : Set up the USB interface board (AKDUSBIF-A) when using the board.
2. [Write default] : Initialize the register of the AK4632.
3. [All Write] : Write all registers that is currently displayed.
4. [Function1] : Dialog to write data by keyboard operation.
5. [Function2] : Dialog to write data by keyboard operation.
6. [Function3] : The sequence of register setting can be set and executed.
7. [Function4] : The sequence that is created on [Function3] can be assigned to buttons and executed.
8. [Function5]: The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
9. [SAVE] : Save the current register setting.
10. [OPEN] : Write the saved values to all register.
11. [Write] : Dialog to write data by mouse operation.

■ Indication of data

Input data is indicated on the register map. Red letter indicates “H” or “1” and blue one indicates “L” or “0”. Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

If you want to write the input data to the AK4632, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog] : Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

If you want to write the input data to the AK4632, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog] : Dialog to evaluate DATT

There are dialogs corresponding to register of 09h and 0Ah.

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to the AK4632 by this interval.
Step Box: Data changes by this step.
Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to the AK4632, click [OK] button. If not, click [Cancel] button.

4. [SAVE] and [OPEN]

4-1. [SAVE]

All of current register setting values displayed on the main window are saved to the file. The extension of file name is “akr”.

<Operation flow>
(1) Click [SAVE] Button.
(2) Set the file name and click [SAVE] Button. The extension of file name is “akr”.

4-2. [OPEN]

The register setting values saved by [SAVE] are written to the AK4632. The file type is the same as [SAVE].

<Operation flow>
(1) Click [OPEN] Button.
(2) Select the file (*.akr) and Click [OPEN] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

(2) Set the control sequence.
Set the address, Data and Interval time. Set “-1” to the address of the step where the sequence should be paused.

(3) Click [START] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [SAVE] and [OPEN] button on the Function3 window. The extension of file name is “aks”.

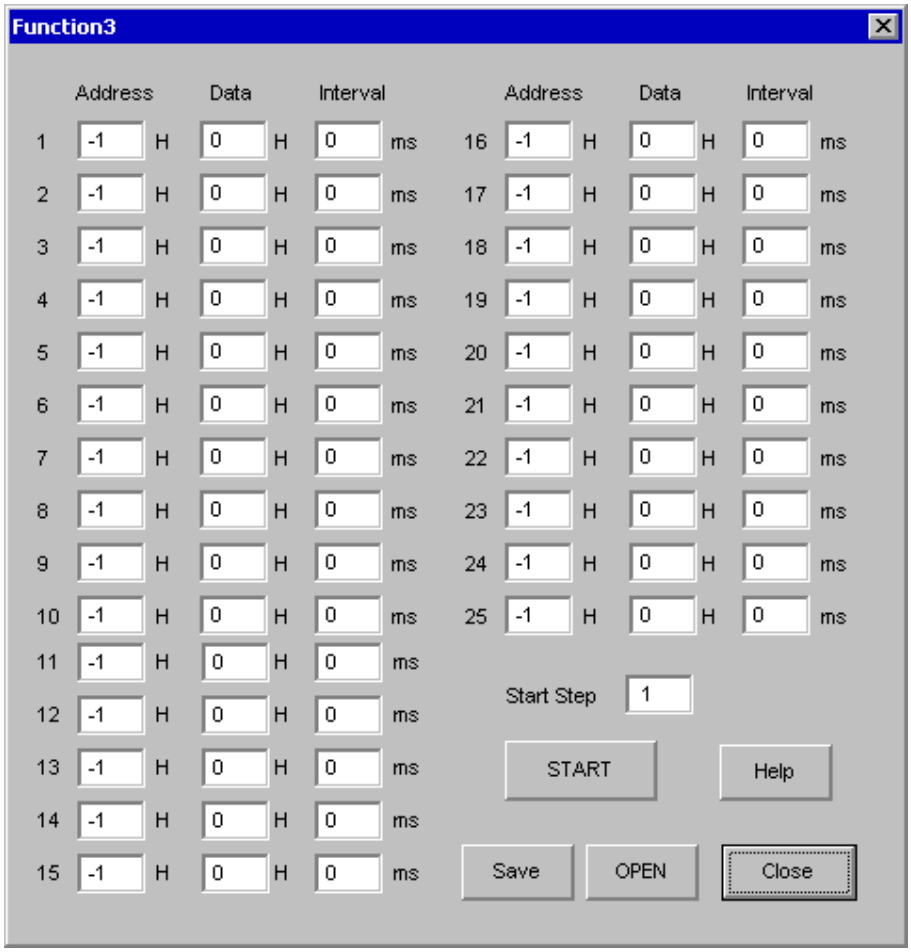


Figure 1. Window of [F3]

6. [Function4 Dialog]

The sequence file (*.aks) saved by [Function3] can be listed up to 10 files, assigned to buttons and then executed. When [F4] button is clicked, the window as shown in Figure 2 opens.

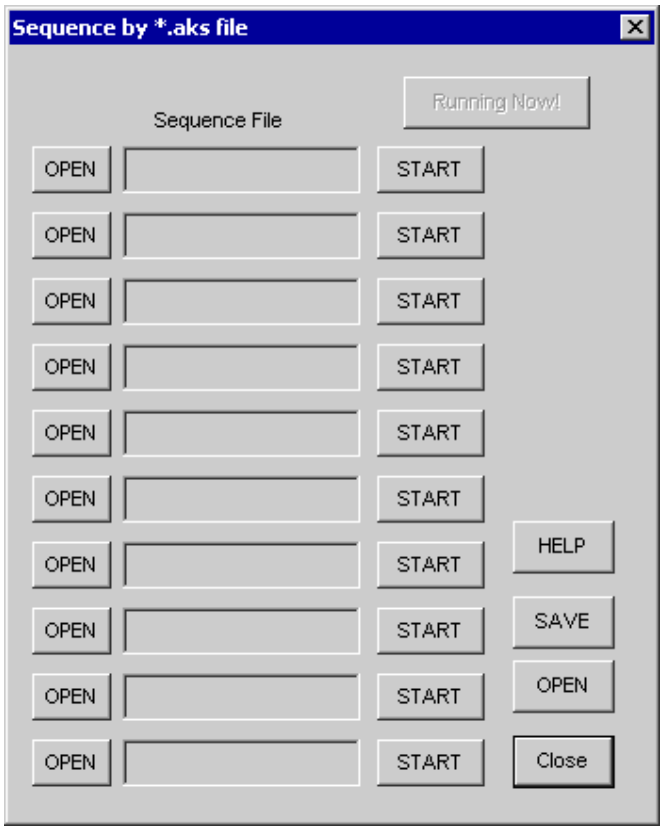


Figure 2. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks) saved by [Function3].

The sequence file name is displayed as shown in Figure 3. (In case that the selected sequence file name is "DAC_Stereo_ON.aks")

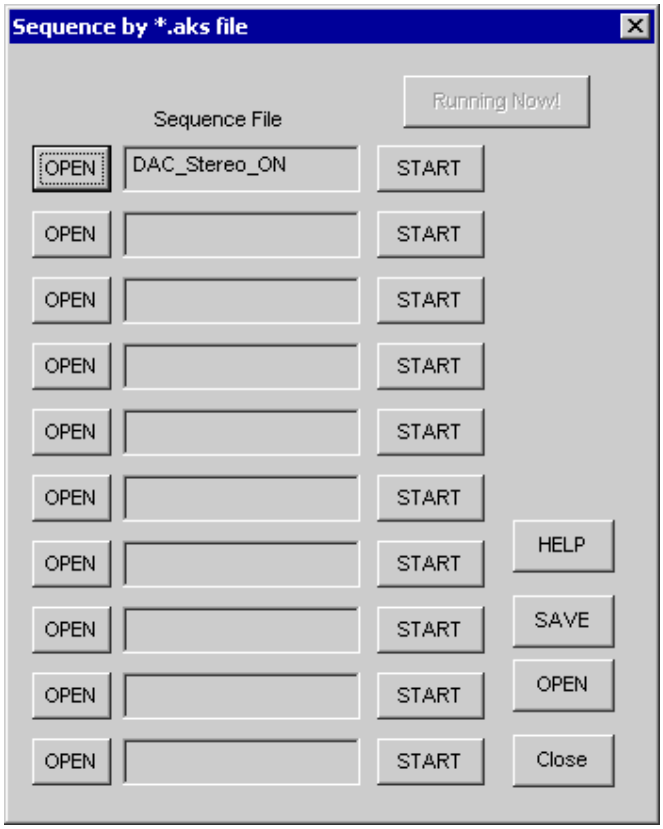


Figure 3. [F4] window(2)

(2) Click [START] button, then the sequence is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of sequence file displayed on [Function4] window can be saved to the file. The file name is "*.ak4".

[OPEN] : The name assign of sequence file(*.ak4) saved by [SAVE] is loaded.

6-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(3) When the sequence is changed in [Function3], the sequence file (*.aks) should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting file(*.akr) saved by [SAVE] function on main window can be listed up to 10 files, assigned to buttons and then executed. When [F5] button is clicked, the window as shown in Figure 4 opens.

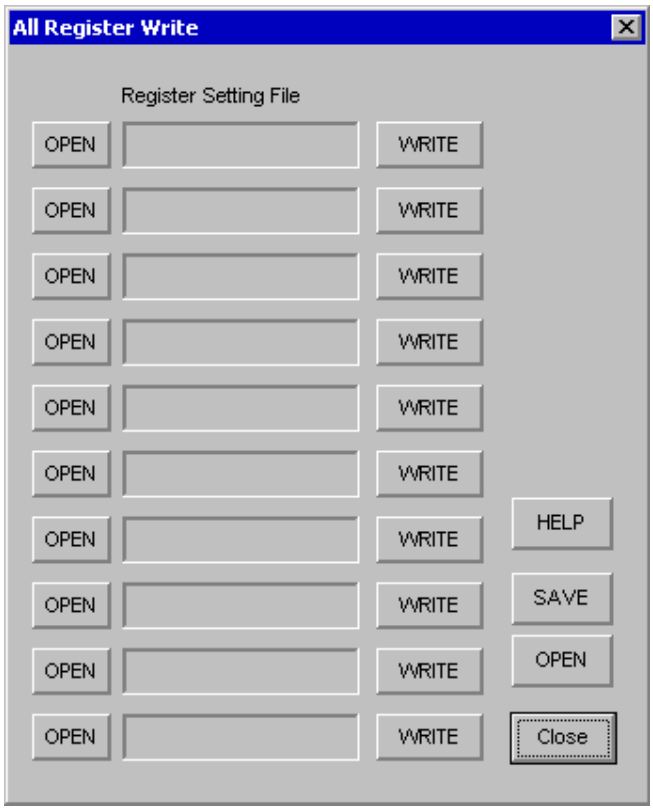


Figure 4. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

The register setting file name is displayed as shown in Figure 5. (In case that the selected file name is "DAC_Output.akr")

(2) Click [WRITE] button, then the register setting is executed.

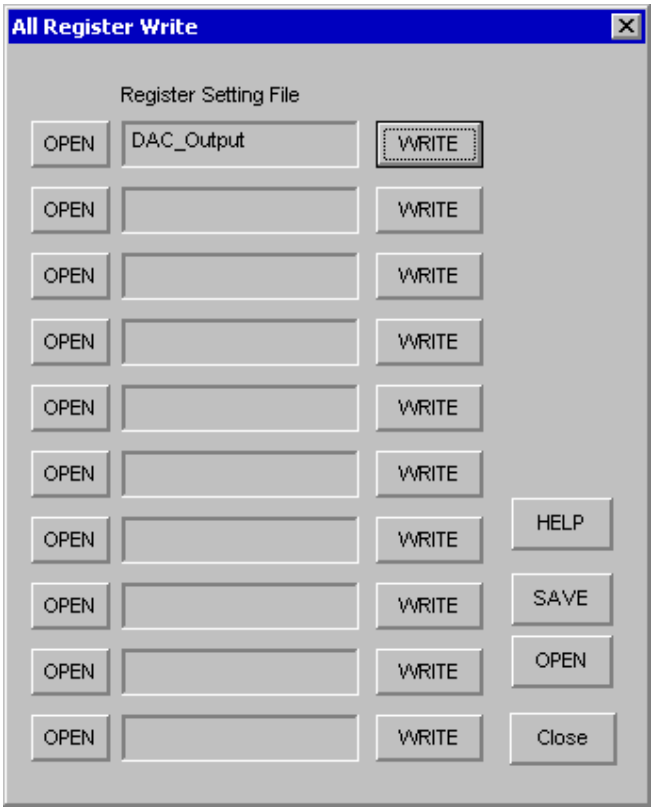


Figure 5. [F5] windows(2)

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of register setting file displayed on [Function5] window can be saved to the file. The file name is "*.ak5".
[OPEN] : The name assign of register setting file(*.ak5) saved by [SAVE] is loaded.

7-3. Note

(1) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(2) When the register setting is changed by [SAVE] Button on the main window, the register setting file (*.akr) should be loaded again in order to reflect the change.

MEASUREMENT RESULTS EXAMPLE

1.AK4632 Mode: EXT mode (Slave)

[Measurement condition]

- Measurement unit: ROHDE & SCHWARZ, UPD05
- MCKI: 256fs, 512fs
- BICK: 64fs
- Bit: 16bit
- Sampling Frequency: 8kHz & 16kHz
- Measurement Frequency: 20 ~ 3.4kHz (fs=8kHz), 20 ~ 8kHz (fs=16kHz)
- Power Supply: AVDD=DVDD=VVDD=3.3V,SVDD=3.3V/5.0V
- Temperature: Room
- Input Frequency: 1kHz

[Measurement Results]

1.ADC characteristics (MIC Gain = +20dB, IPGA=0dB, ALC1 = OFF, MIC → IPGA → ADC)

	Result			
MCKI clock	512fs		256fs	
Sampling Frequency	8kHz	16kHz	8kHz	16kHz
S/(N+D) (-1dBFS)	84.3dB	84.1dB	84.4dB	84.0dB
D-Range (-60dBFS)	88.1dB	86.4dB	85.2dB	86.3dB
S/N	88.1dB	86.3dB	88.2dB	86.3dB

2. DAC characteristics (AOUT) (DAC → AOUT, DVOL = 0dB)

	Result			
MCKI clock	512fs		256fs	
Sampling Frequency	8kHz	16kHz	8kHz	16kHz
S/(N+D) (0dBFS)	91.5dB	89.6dB	90.8dB	89.5dB
D-Range (-60dBFS)	94.8dB	92.0dB	94.5dB	92.1dB
S/N	95.5dB	93.5dB	95.0dB	93.5dB

3. Speaker-Amp characteristics (DAC → MOUT → MIN → SPP/SPN, ALC2=OFF)

			Result
S/(N+D)	SVDD=3.3V	SPKG1-0 = “00” (-0.5dBFS)	69.6dB
	RL=8Ω	SPKG1-0 = “01” (-0.5dBFS)	73.5dB
	SVDD=5.0V	SPKG1-0 = “10” (-0.5dBFS)	73.2dB
	RL=10Ω, CL=3uF	SPKG1-0 = “11” (-0.5dBFS)	73.8dB
S/N	SVDD=3.3V	SPKG1-0 = “00”	90.4dB
	RL=8Ω	SPKG1-0 = “01”	91.7dB
	SVDD=5.0V	SPKG1-0 = “10”	90.6dB
	RL=10Ω, CL=3uF	SPKG1-0 = “11”	91.0dB

4. Loop-back (MIC → ADC → DAC → AOUT)

	Result			
MCKI clock	512fs		256fs	
Sampling Frequency	8kHz	16kHz	8kHz	16kHz
S/(N+D) (-1dBFS)	84.2dB	83.2dB	84.2dB	83.4dB
D-Range (-60dBFS)	88.4dB	85.9dB	87.0dB	85.9dB
S/N	88.4dB	86.0dB	87.0dB	86.0dB

2.AK4632 Mode: PLL SLAVE mode

[Measurement condition]

- Measurement unit: ROHDE & SCHWARZ, UPD05
- Bit: 16bit
- Sampling Frequency: 8kHz & 16kHz
- Measurement Frequency: 20 ~ 3.4kHz (fs=8kHz), 20 ~ 8kHz (fs=16kHz)
- Power Supply: AVDD=DVDD=SVDD=VVDD=3.3V
- Temperature: Room
- Input Frequency: 1kHz

[Measurement Results]

2-1. PLL Reference clock : BICK or FCK pin

Loop-back (MIC → ADC → DAC → AOUT)

	Result			
PLL Reference clock	1fs (FCK pin)		16fs (BICK pin)	
Sampling Frequency	8kHz	16kHz	8kHz	16kHz
S/(N+D) (-1dBFS)	75.3dB	78.6dB	84.7dB	83.8dB
D-Range (-60dBFS)	86.5dB	86.0dB	87.7dB	85.9dB
S/N	86.5dB	85.9dB	87.6dB	85.8dB

2-2. PLL Reference clock : MCKI pin

Loop-back (MIC → ADC → DAC → AOUT)

	Result	
PLL Reference clock	12.288MHz	
Sampling Frequency	8kHz	16kHz
S/(N+D) (-1dBFS)	84.7dB	83.8dB
D-Range (-60dBFS)	87.4dB	85.8dB
S/N	88.0dB	85.8dB

3.AK4632 Mode: PLL MASTER mode

[Measurement condition]

- Measurement unit: ROHDE & SCHWARZ, UPD05
- MCKI: 12.288MHz
- BICK: 16fs
- Bit: 16bit
- Sampling Frequency: 8kHz & 16kHz
- Measurement Frequency: 20 ~ 3.4kHz (fs=8kHz), 20 ~ 8kHz (fs=16kHz)
- Power Supply: AVDD=DVDD=SVDD=VVDD=3.3V
- Temperature: Room
- Input Frequency: 1kHz

[Measurement Results]

Loop-back (MIC → ADC → DAC → AOUT)

	Result	
	8kHz	16kHz
S/(N+D) (-1dBFS)	84.2dB	83.3dB
D-Range (-60dBFS)	86.9dB	85.0dB
S/N	87.0dB	85.0dB

4.PLOT DATA (EXT Slave mode)

4-1.ADC (MIC → ADC) PLOT DATA

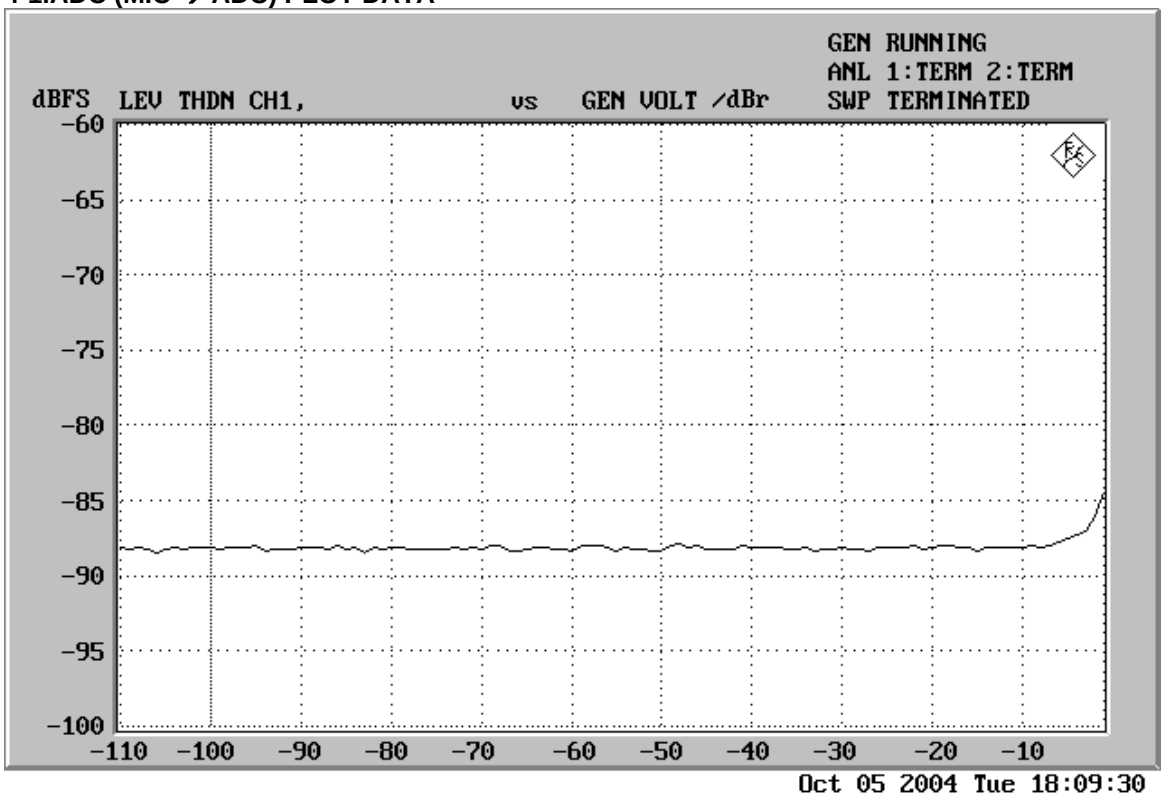


Figure 1. THD+N vs. Input Level

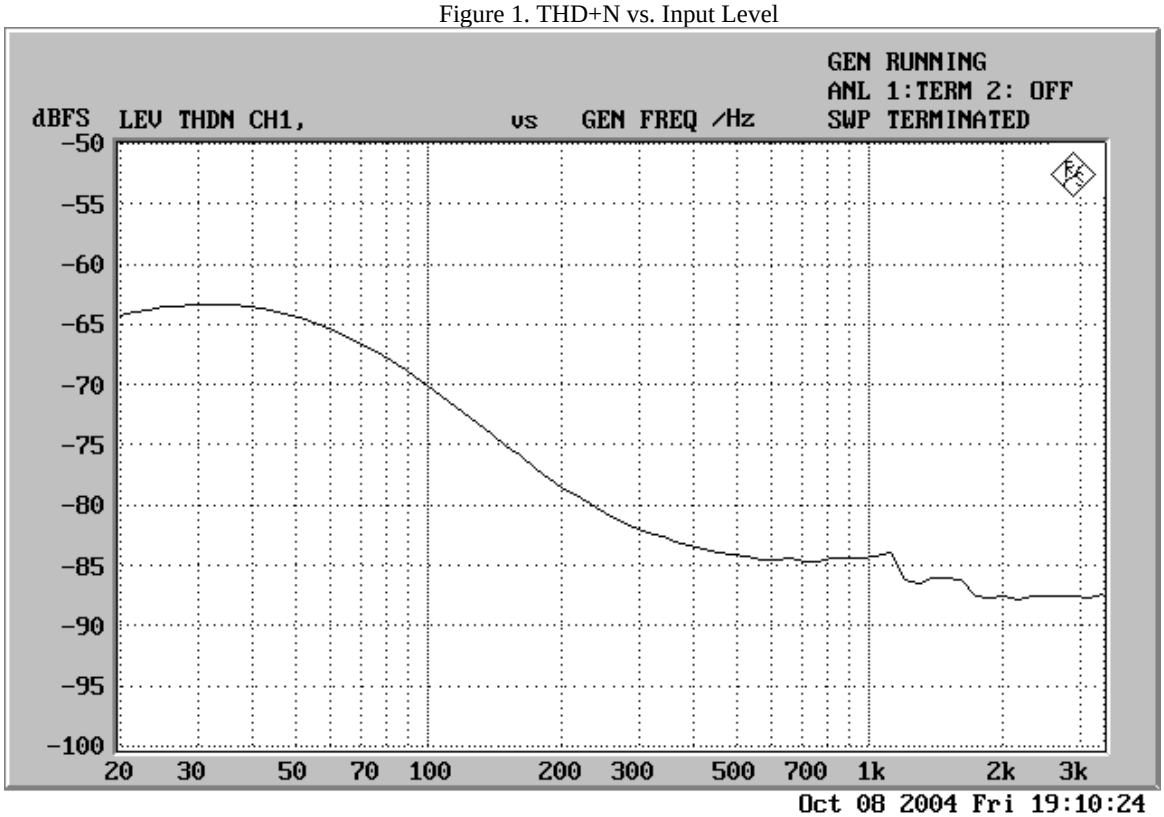


Figure 2. THD+N vs. Input Frequency (Input Level = -1dBFS), C7: Ceramic Condenser

In this case, a ceramic condenser is used as C7 between MICOUT pin as AIN pin on the AKD4632-A.As the performance of Ceramic condenser is not so good about low frequency signal. Refer to Figure 3 about the performance of AK4632.

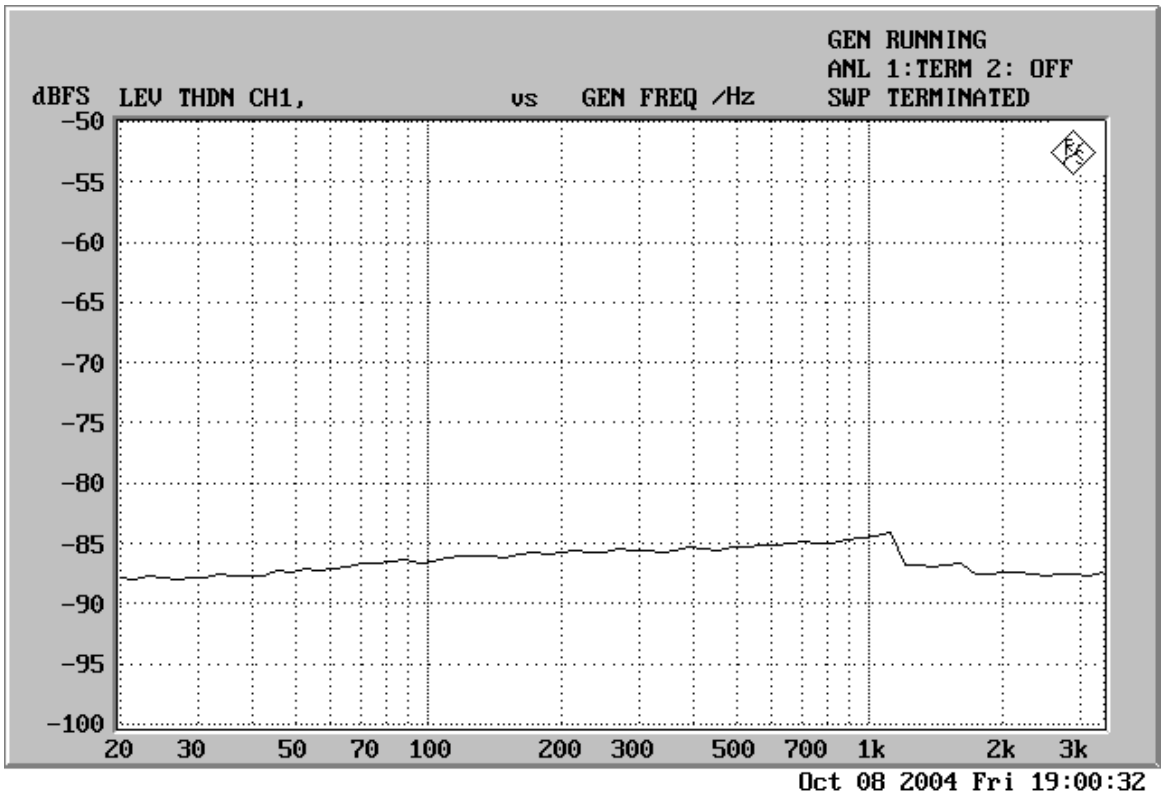


Figure 3. THD+N vs. Input Frequency (Input Level = -1dBFS), C7: Film Condenser

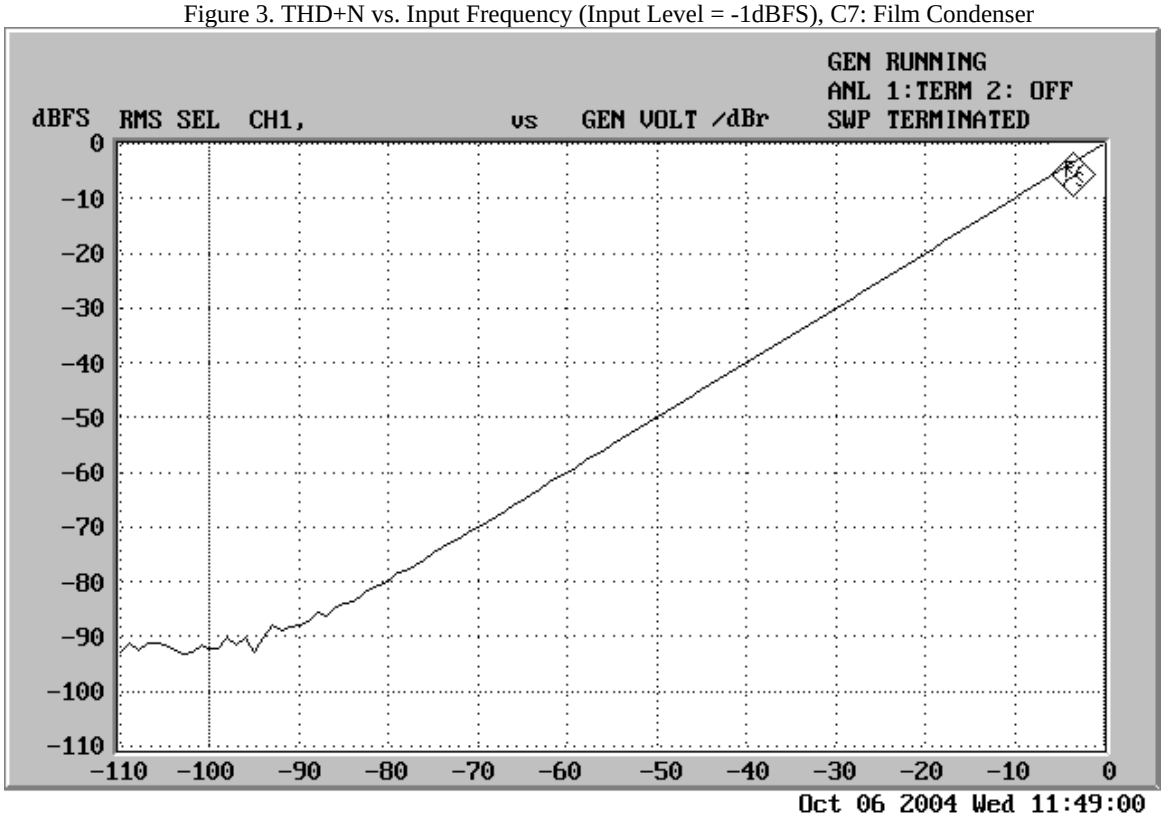


Figure 4. Linearity

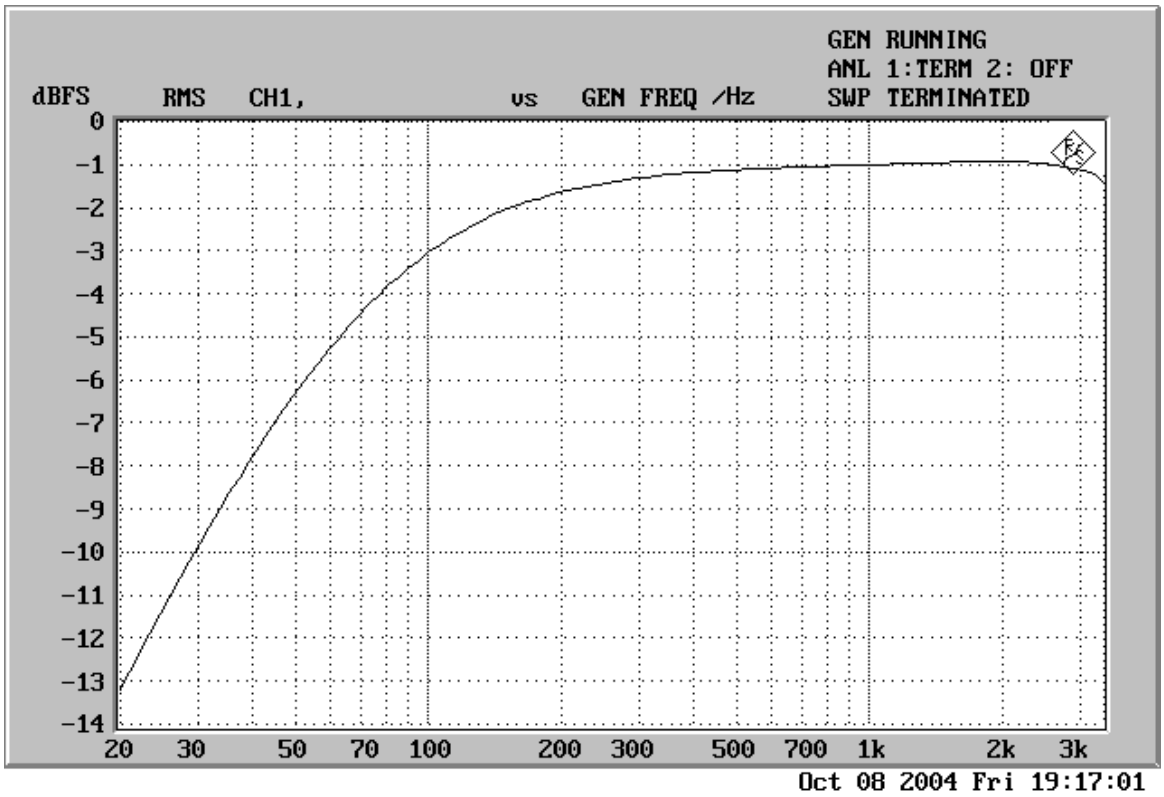


Figure 5. Frequency Response (by the board of AKD4632-A)

High pass filter is composed by the input impedance of AIN pin and C7 between MICOUT pin and AIN pin. Refer to Figure 6 about frequency response of AK4632's ADC.

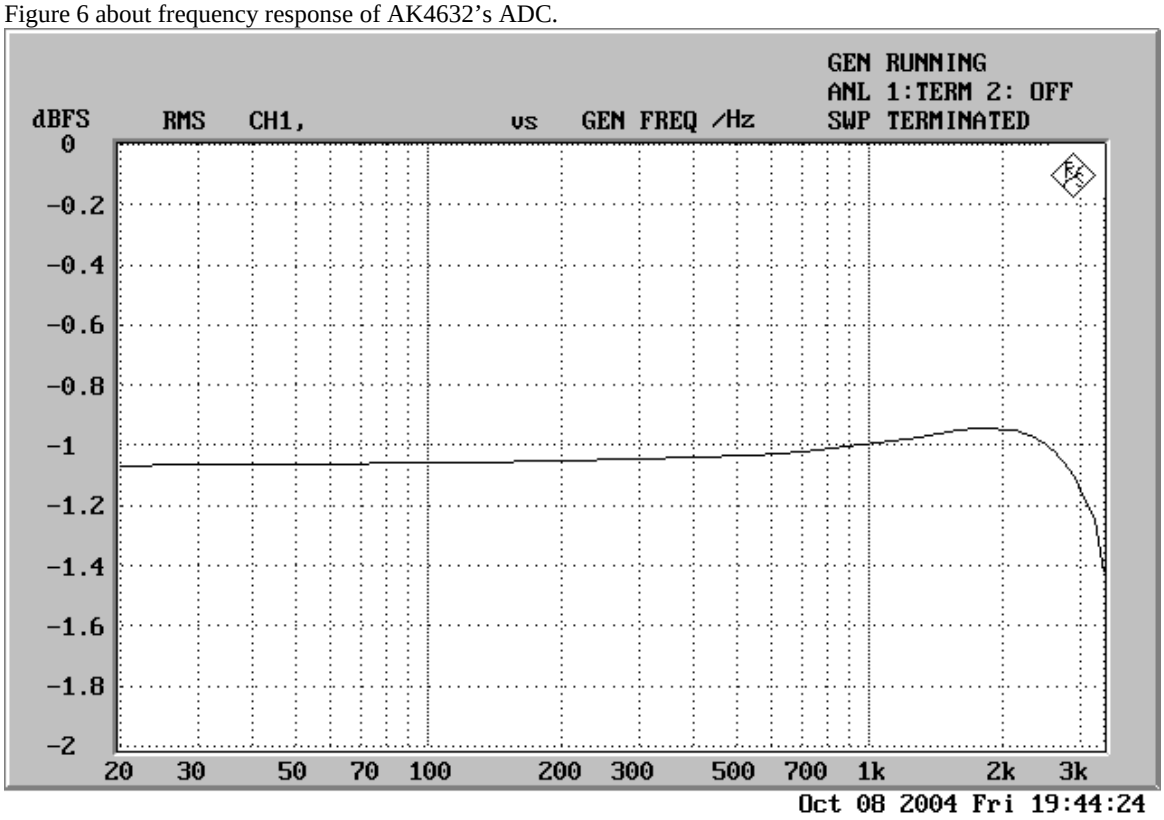


Figure 6. Frequency Response (AIN → ADC)

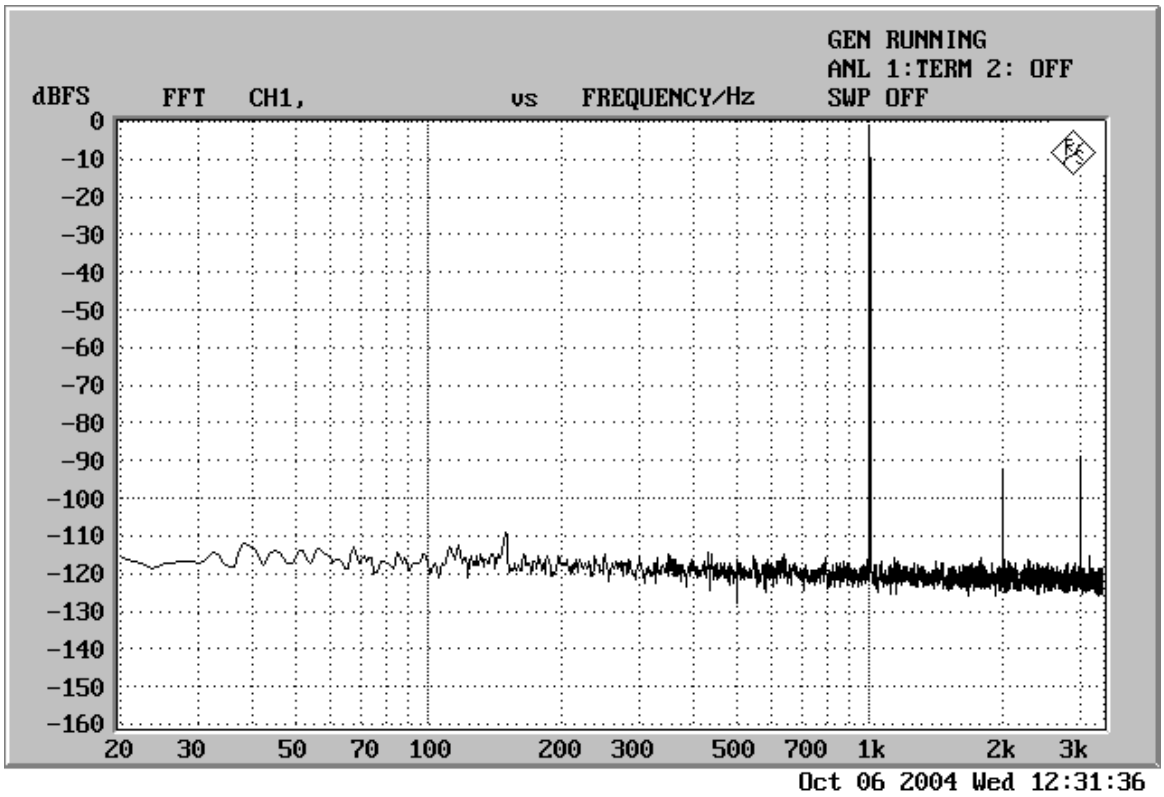


Figure 7. FFT Plot (Input level=-1.0dBFS)

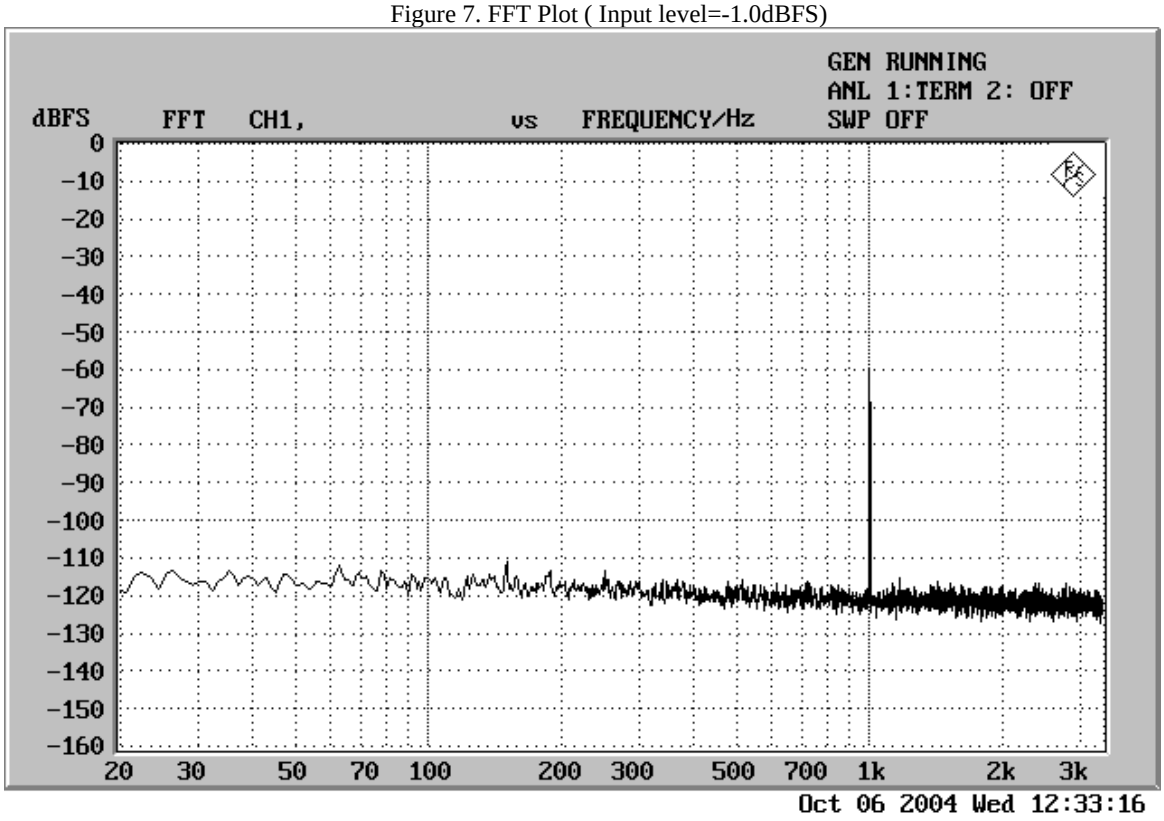


Figure 8. FFT Plot (Input level=-60.0dBFS)

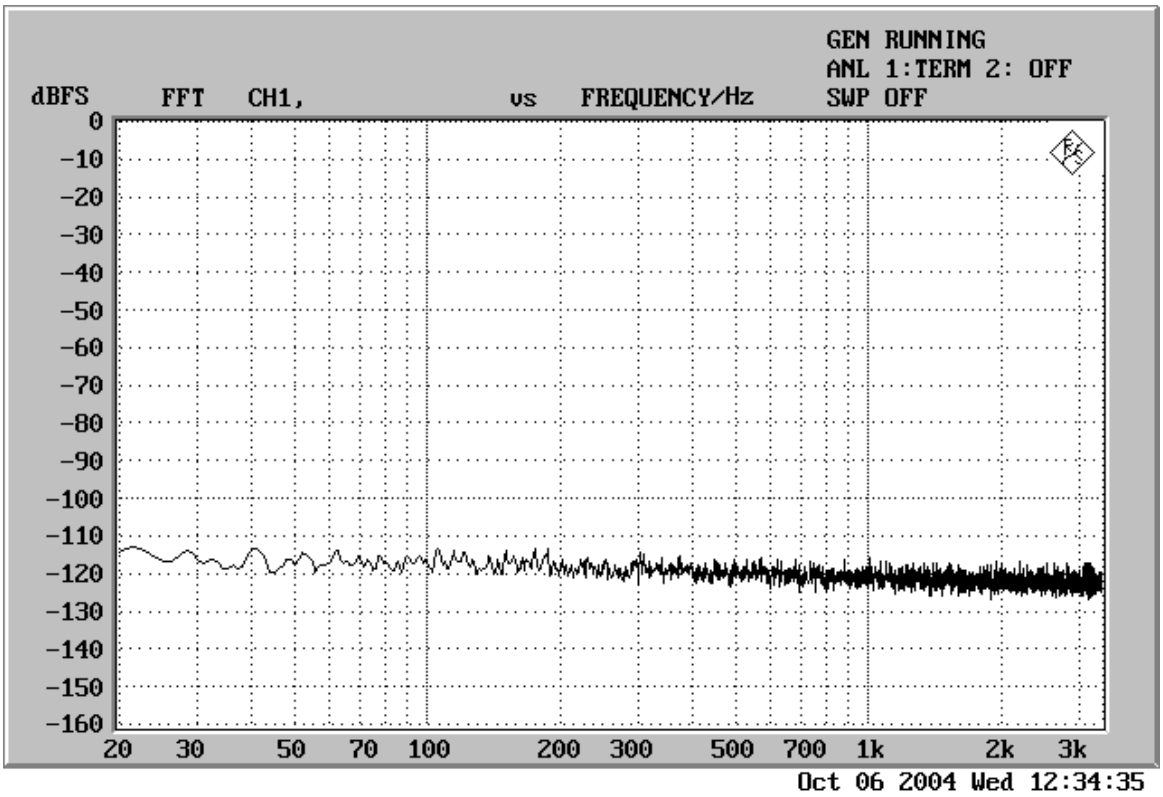


Figure 9. FFT Plot (“0” data input)

4-2. DAC (DAC → AOUT) PLOT DATA

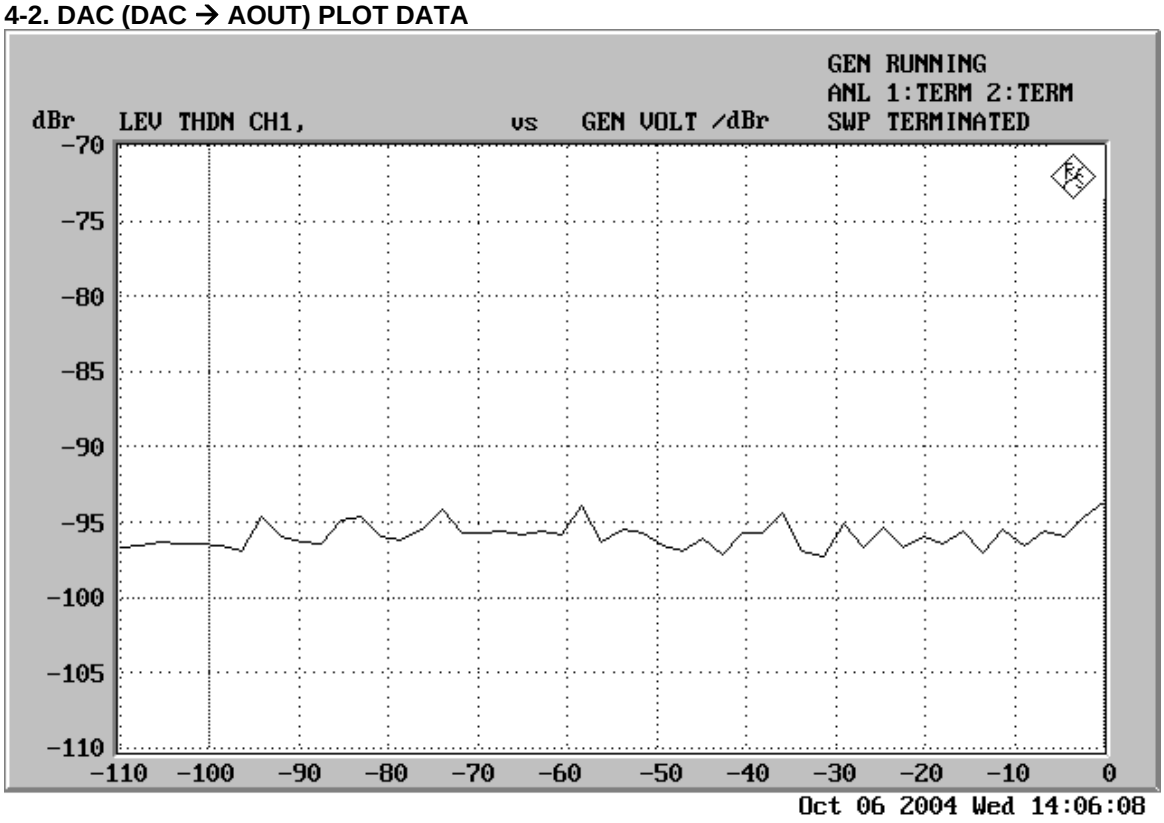


Figure 10. THD+N vs. Input Level

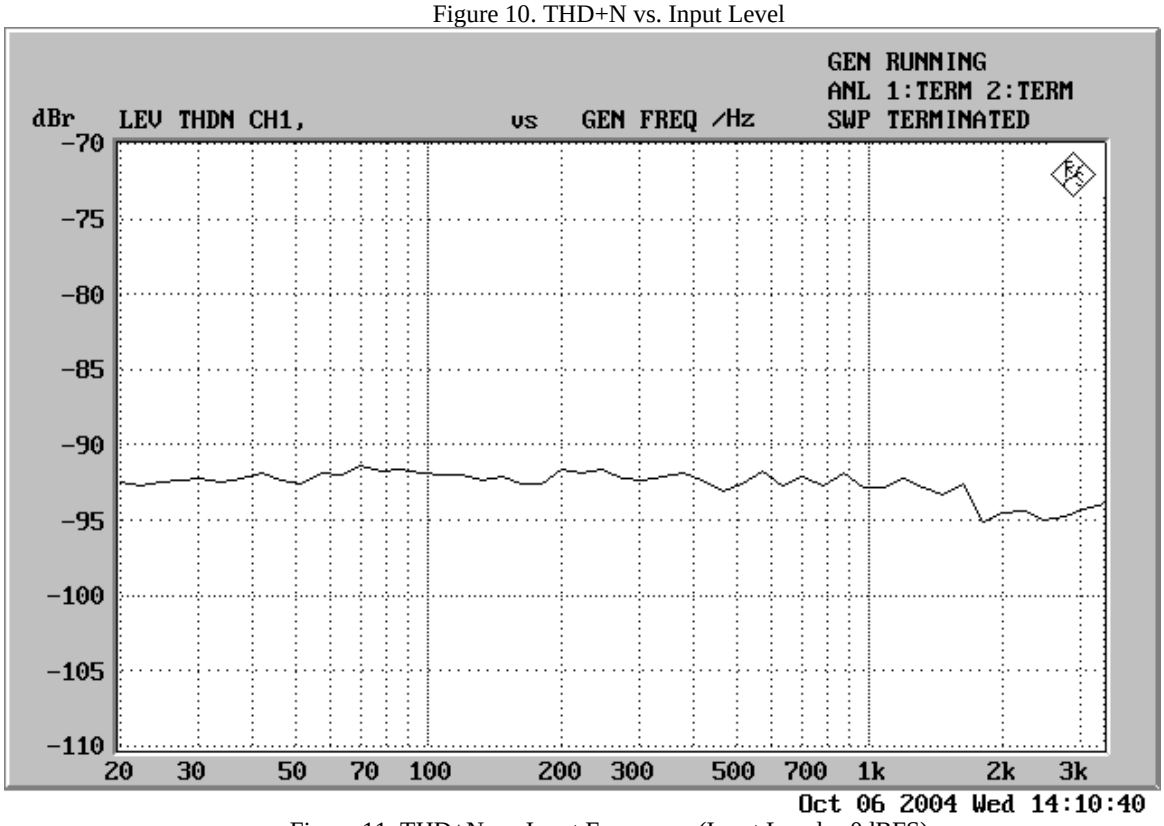


Figure 11. THD+N vs. Input Frequency (Input Level = 0dBFS)

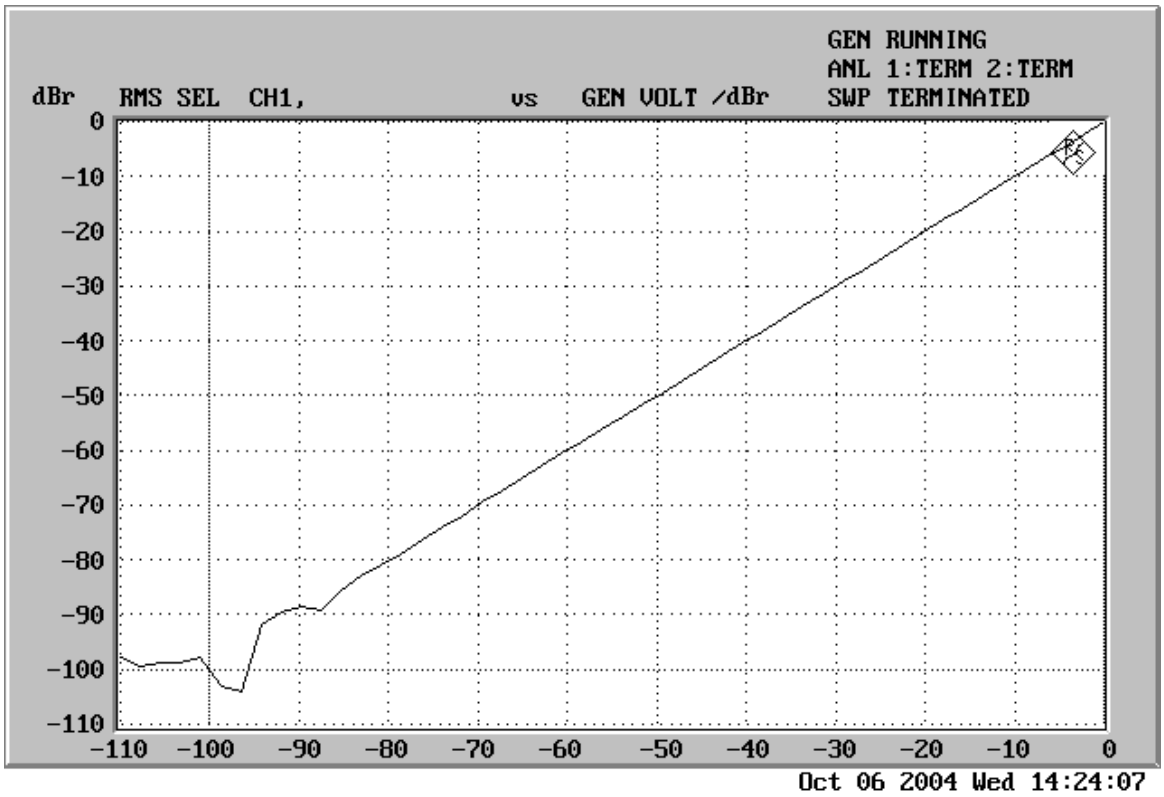


Figure 12. Linearity

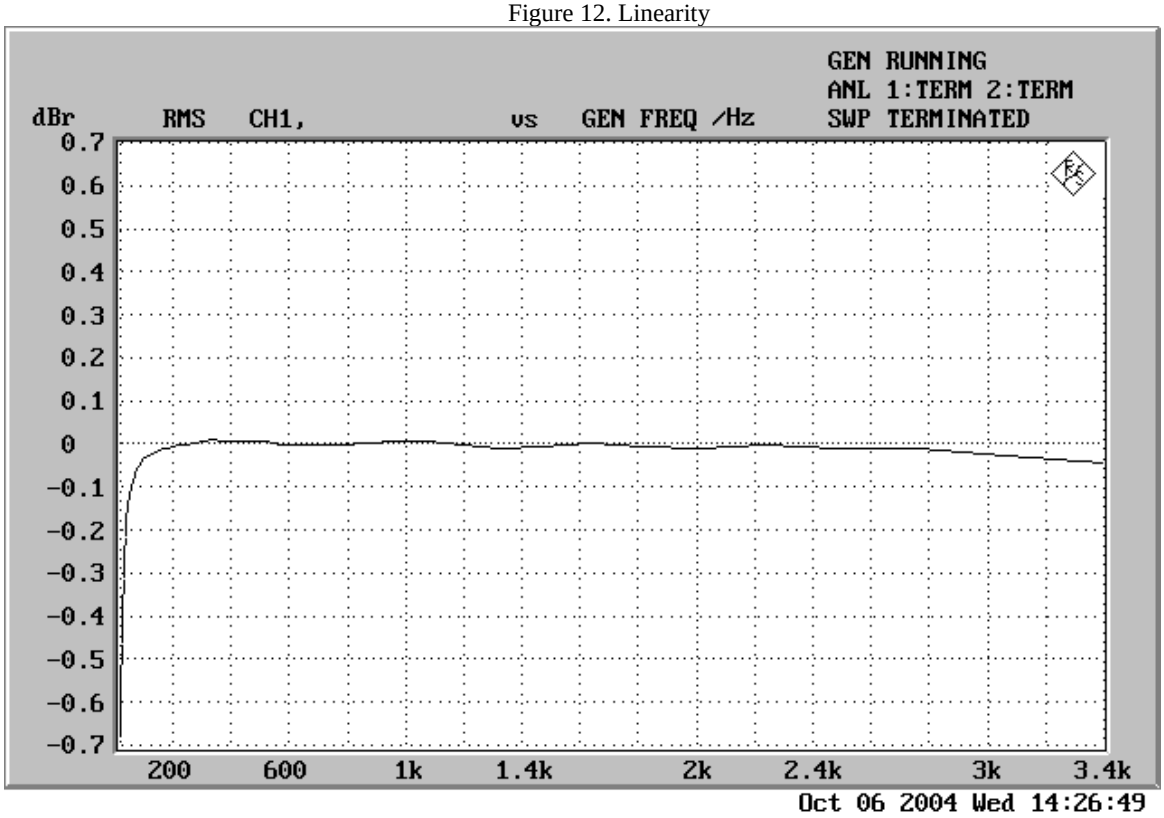


Figure 13. Frequency Response

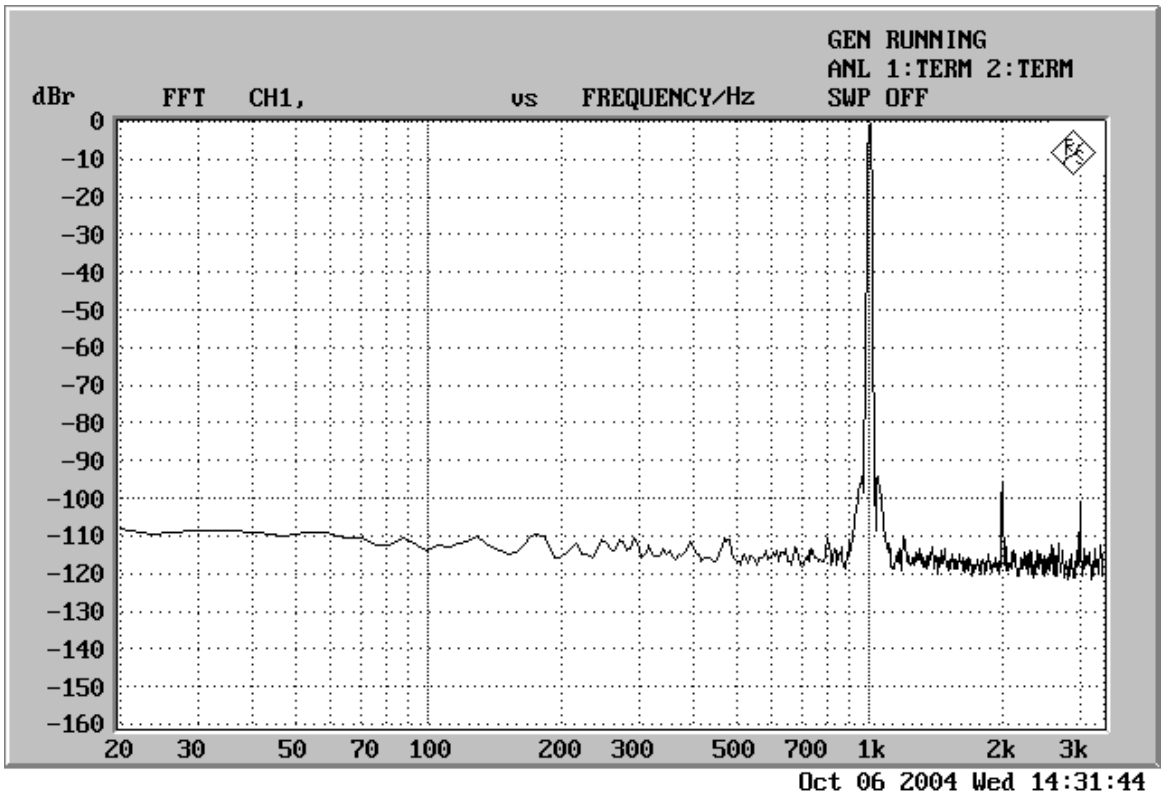


Figure 14. FFT Plot (Input level=0dBFS)

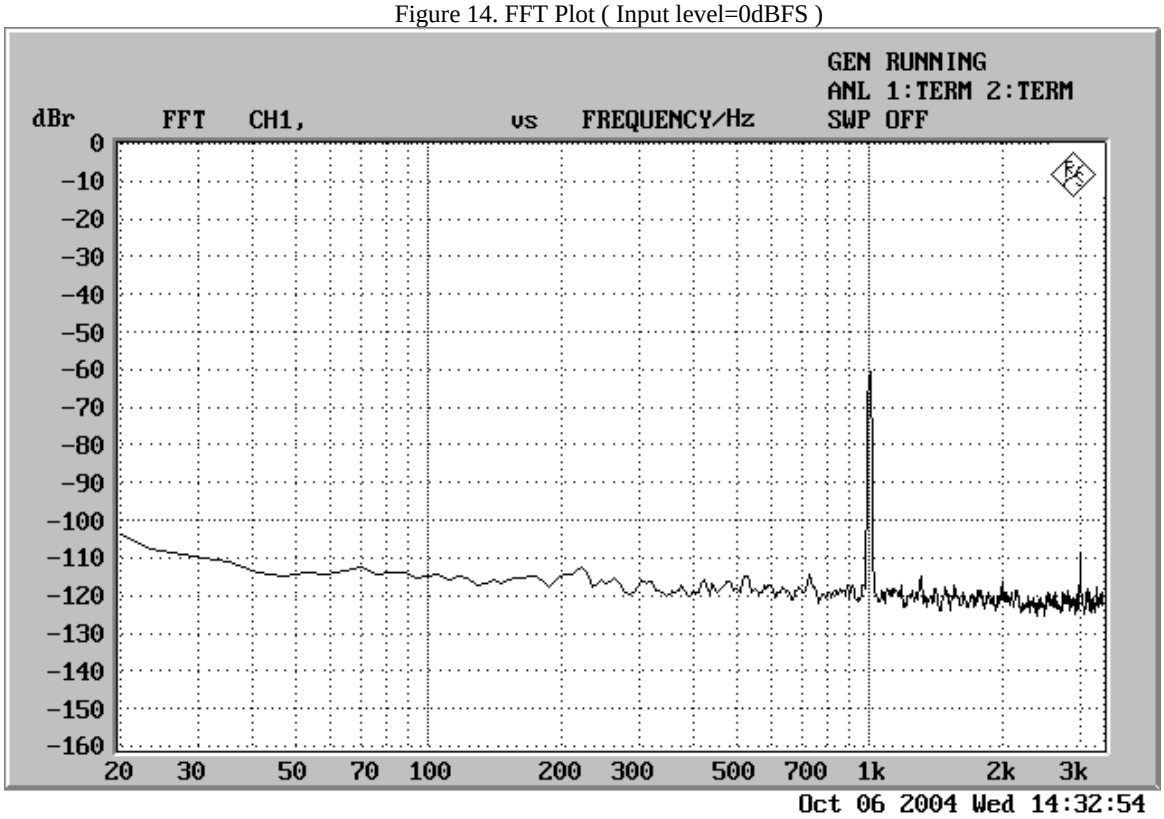


Figure 15. FFT Plot (Input level=-60.0dBFS)

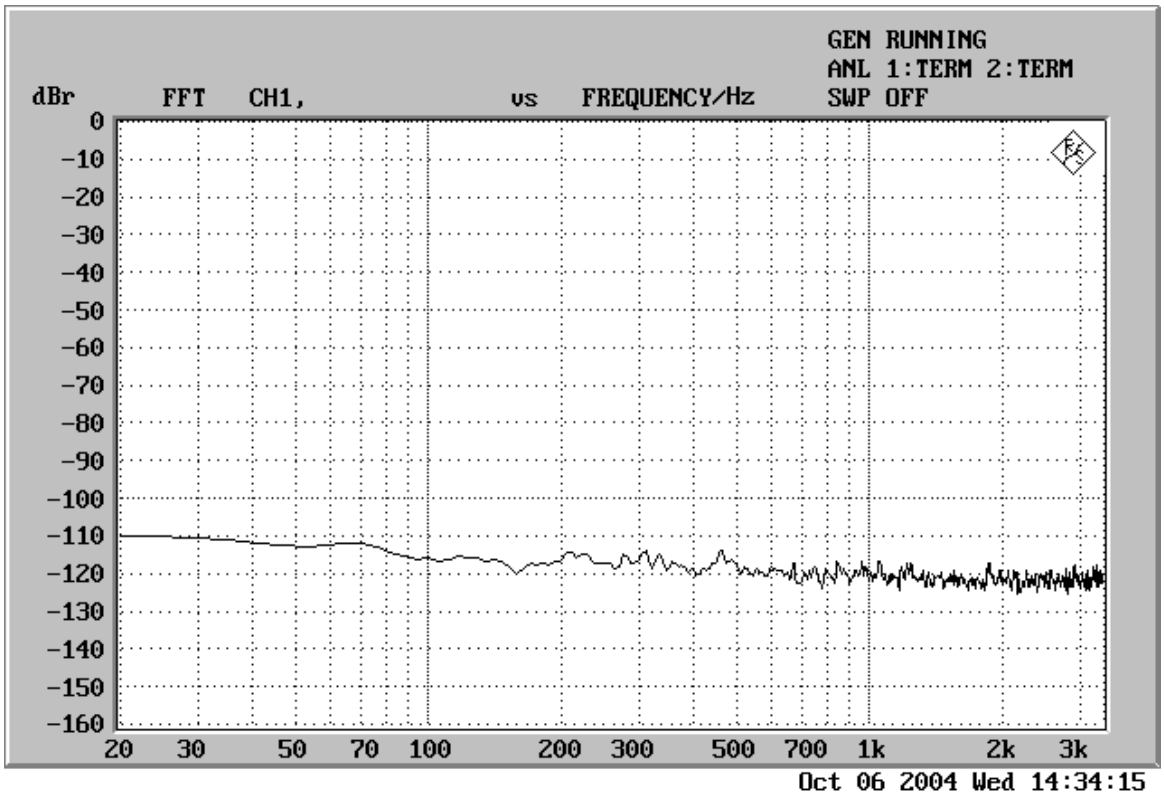


Figure 16. FFT Plot (“0” data input)

4-3. VIDEO PLOT DATA

[Measurement condition]

- Measurement unit: Tektronix VM700T Video Measurement set
- Power Supply: AVDD=DVDD=SVDD=3.3V,VVDD=3.3V
- Temperature: Room
- Input Frequency: 1kHz

4-3-1. S/N

- Measurement Frequency: 100kH ~ 6MHz

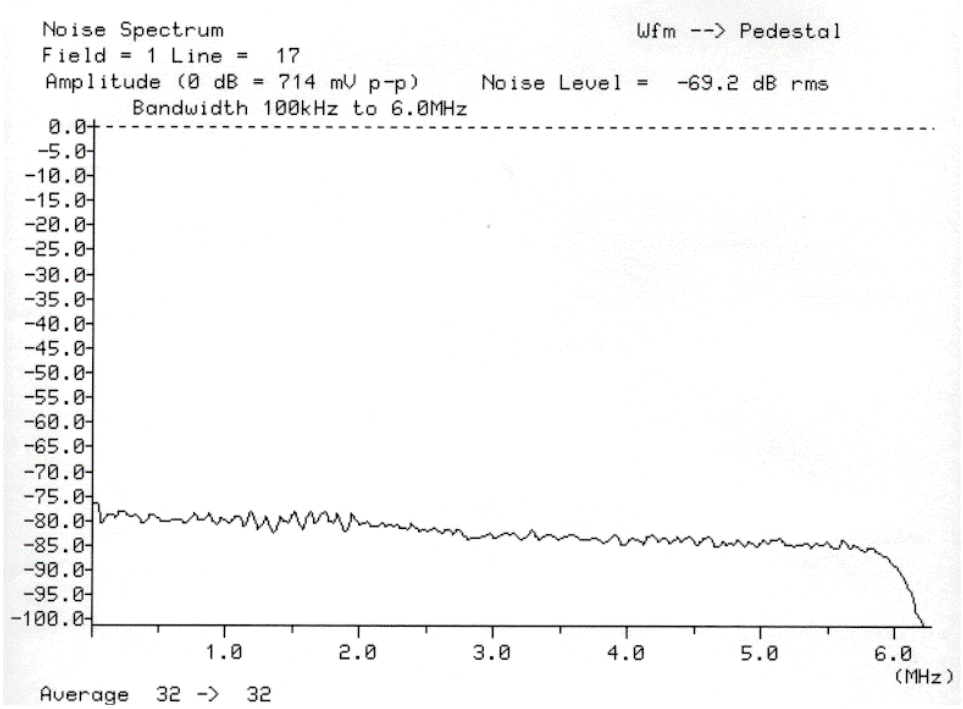


Figure 1. Noise Spectrum

4-3-2. SAG

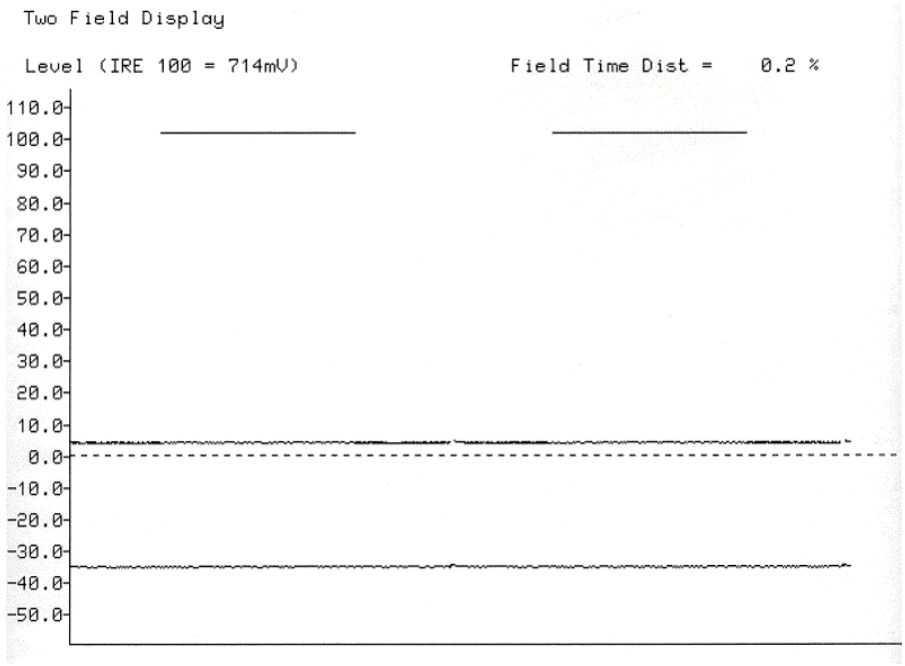


Figure 2. Field Time Distortion (DC Output, SAGC bits = “00”)

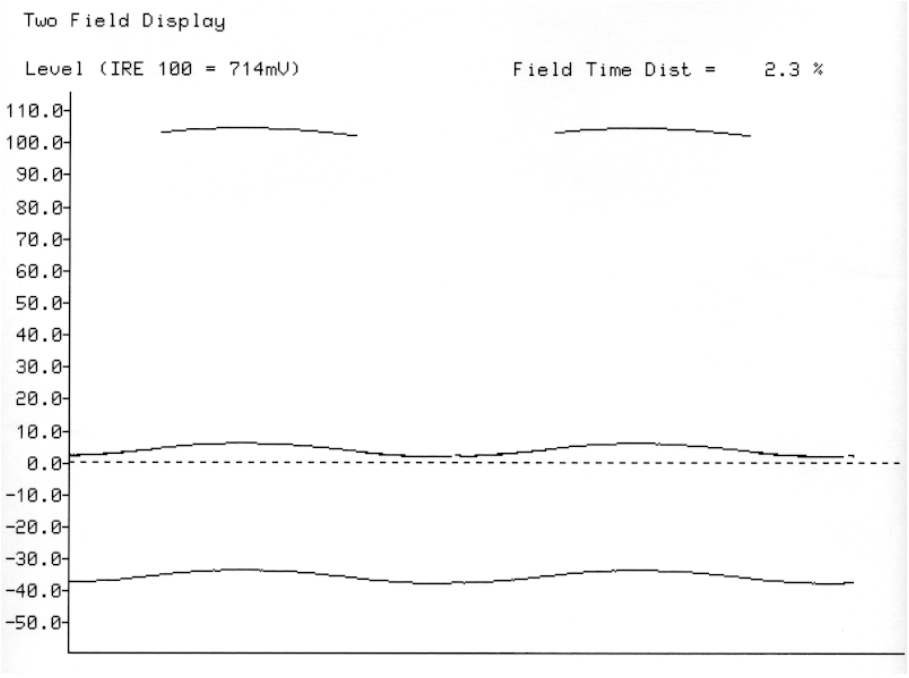


Figure 3. Field Time Distortion (SAG Trimming 47µF+ 1.0uF, SAGC bits = “10”)

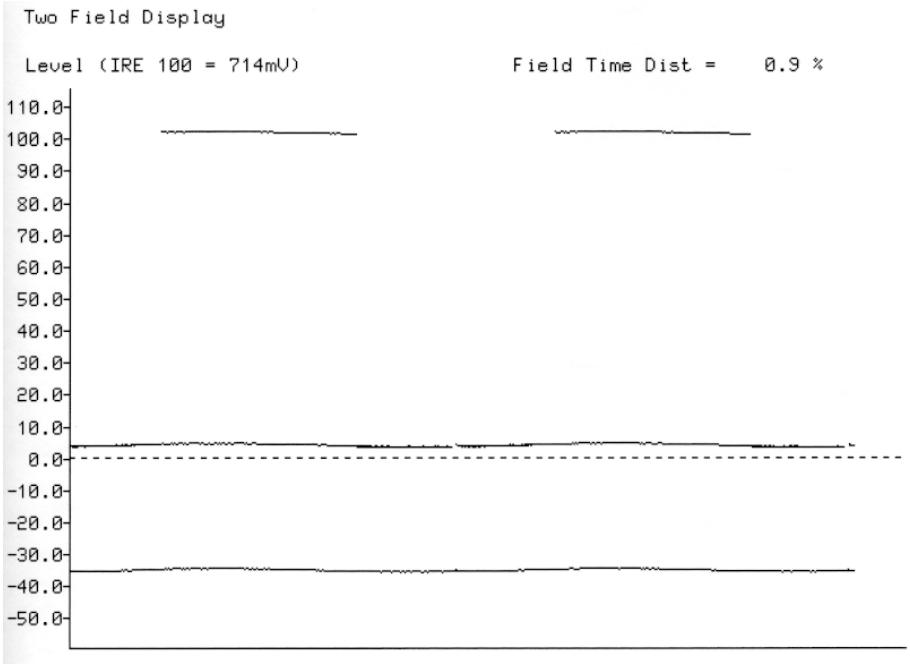


Figure 4. Field Time Distortion (SAG Trimming 100µF+ 2.2uF, SAGC bits = "11")

4-3-3. Vector

- Input signal: 75% color

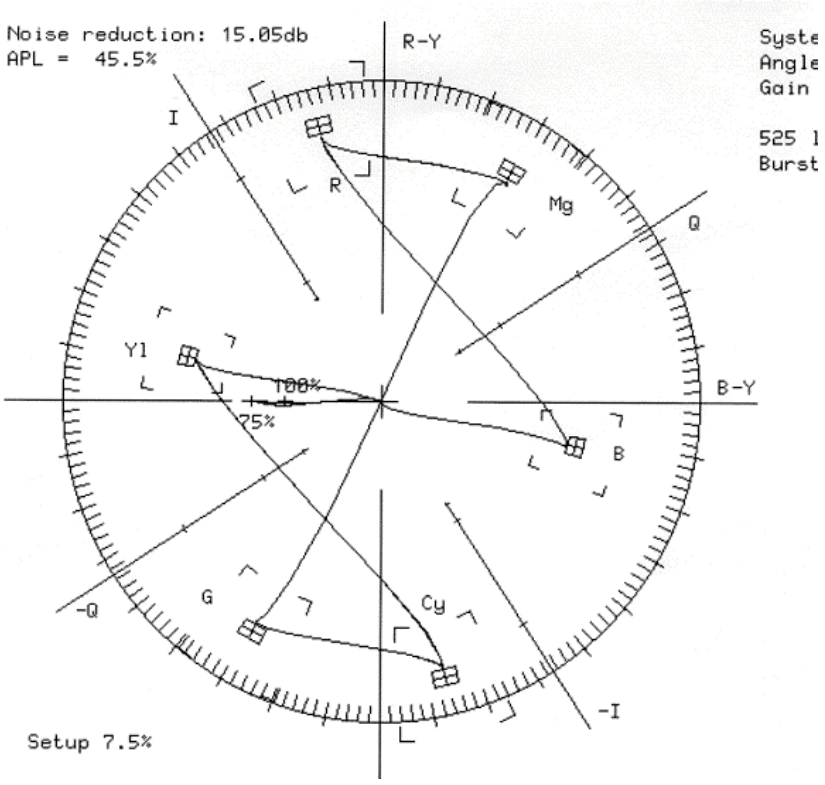


Figure 5. 75% Color Vector (SAG Trimming 47µF+ 1.0uF, SAGC bits = "10")

Revision History

Date	Manual Revision	Board Revision	Reason	Contents
04/11/24	KM075601	0	First Edition	
05/04/05	KM075602	0	Change	"Control Software Manual" chapter is changed by version up of control software.

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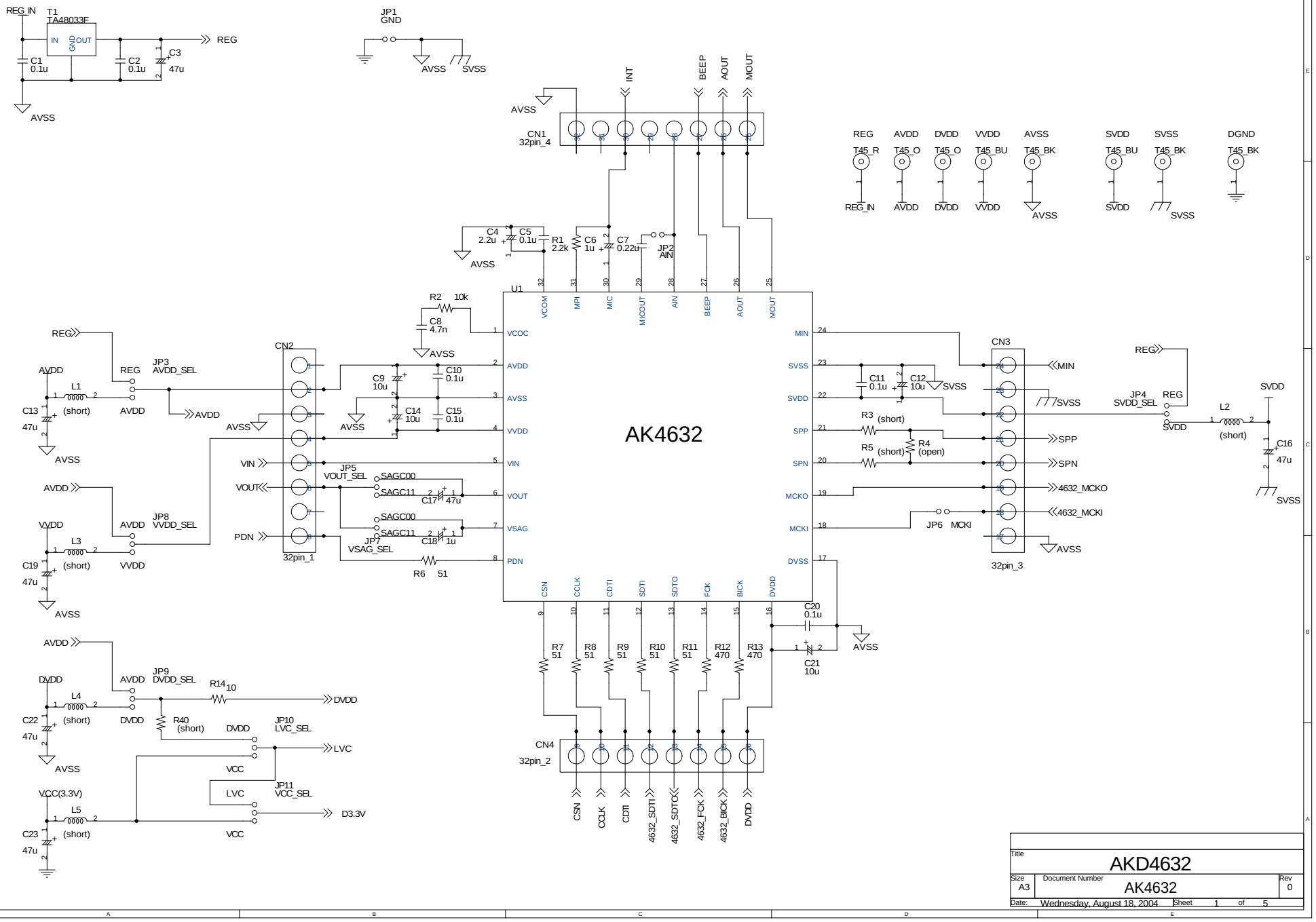

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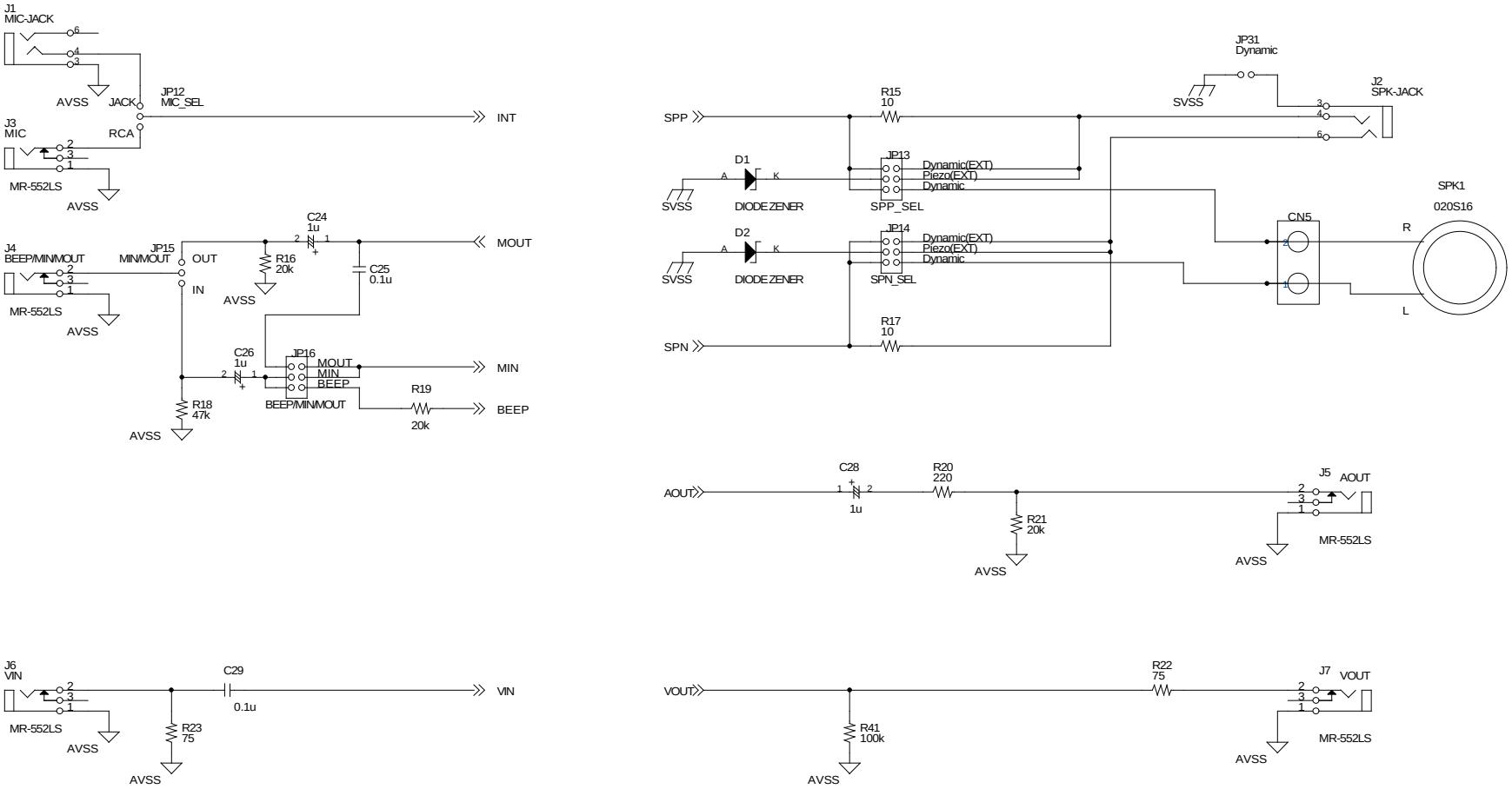
Date: Wednesday, August 18, 2004	Sheet 1 of 5	



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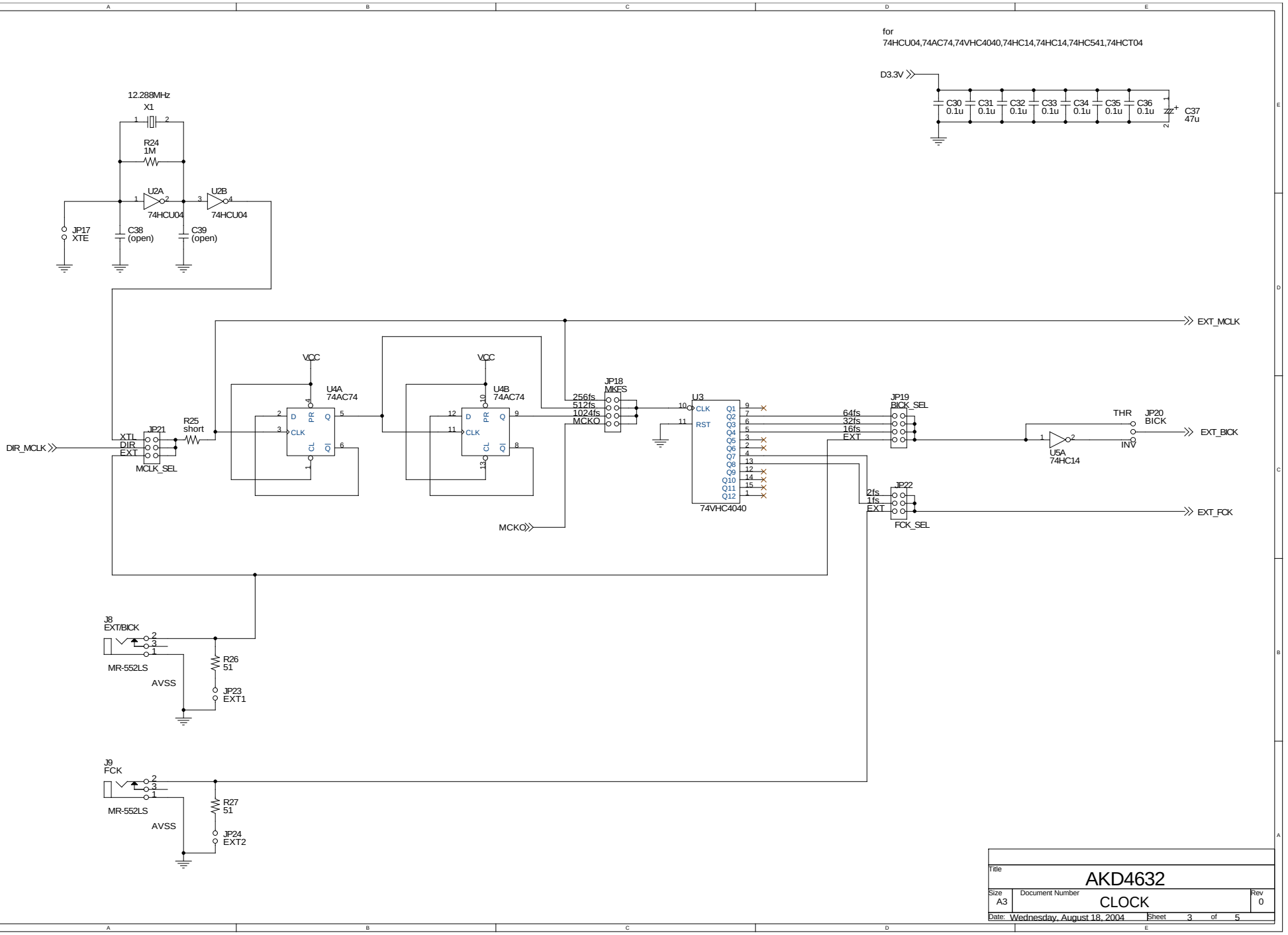

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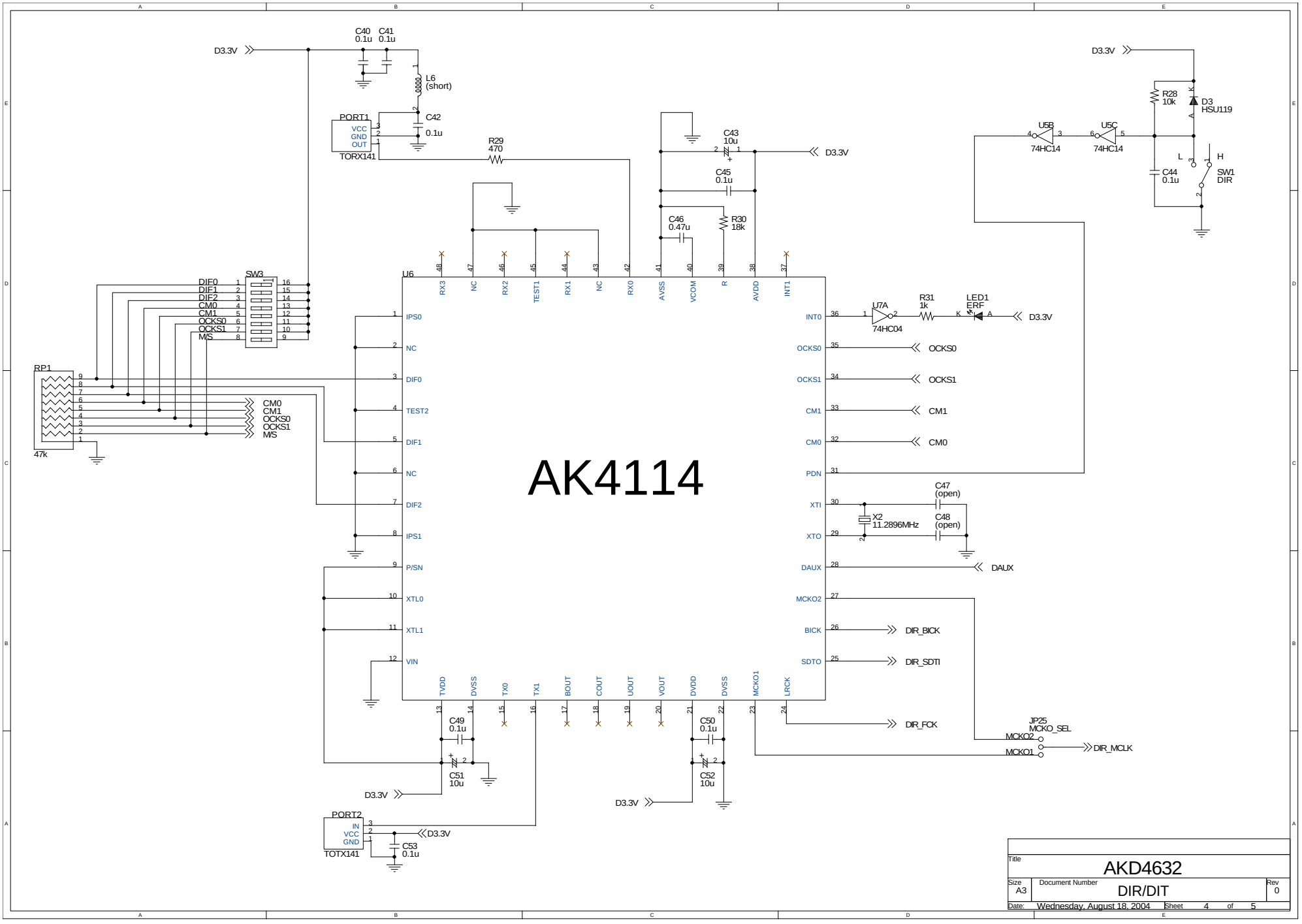
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RP1
PORT1
PORT2
TORX141
TOTX141
U5B
U5C
U7A
74HC14
74HC04
D3
HSU119
SW1
DIR
JP25
MCKO_SEL
X2
11.2896MHz
LED1
ERF
R28
10k
R29
470
R30
18k
R31
1k
C40
C41
C42
C43
C44
C45
C46
C47
C48
C49
C50
C51
C52
C53
L6
(short)
D3.3V
OCKS0
OCKS1
CM0
CM1
DAUX
DIR_BICK
DIR_SDTI
DIR_FCK
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Wednesday, August 18, 2004
Sheet
4
of
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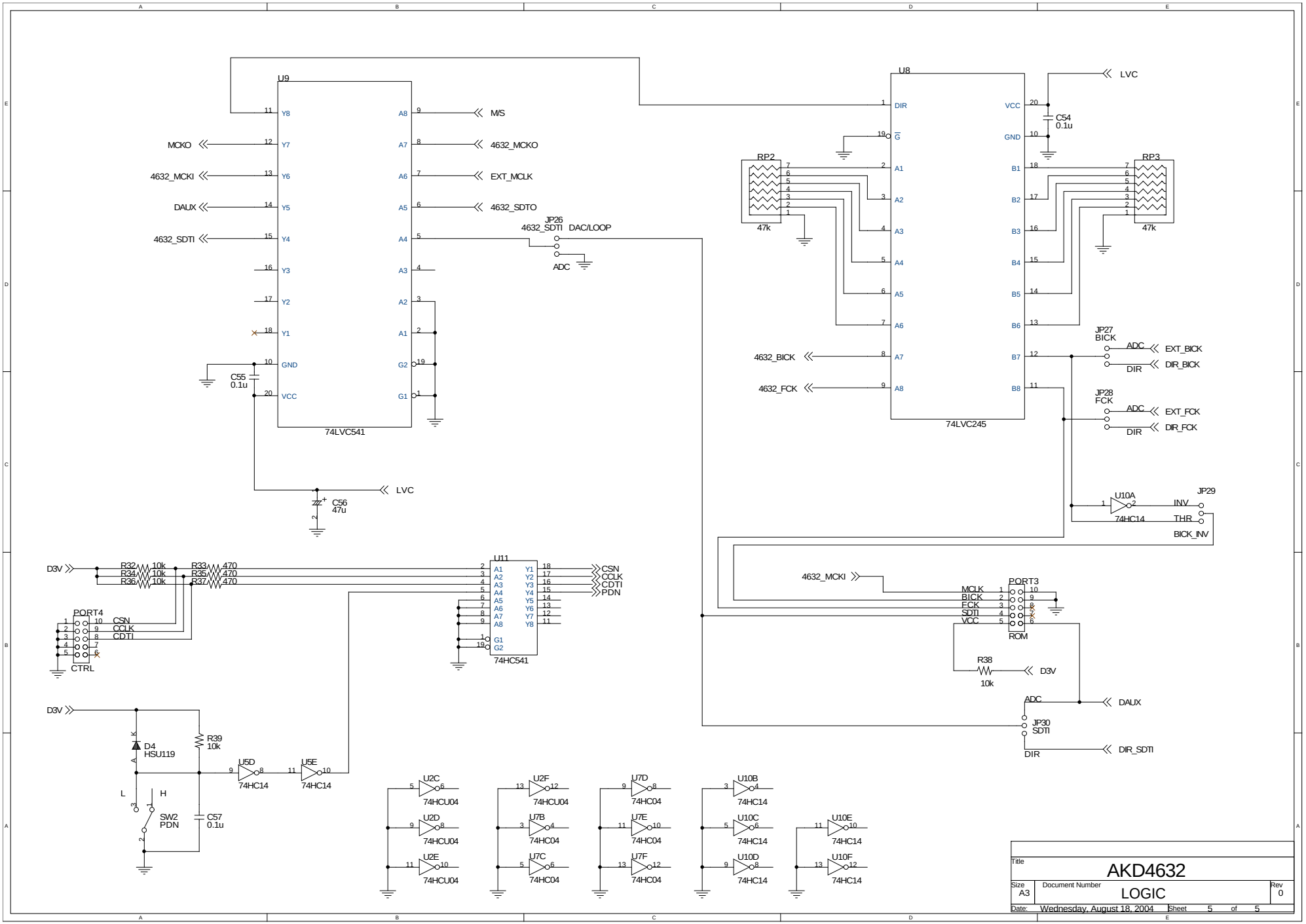

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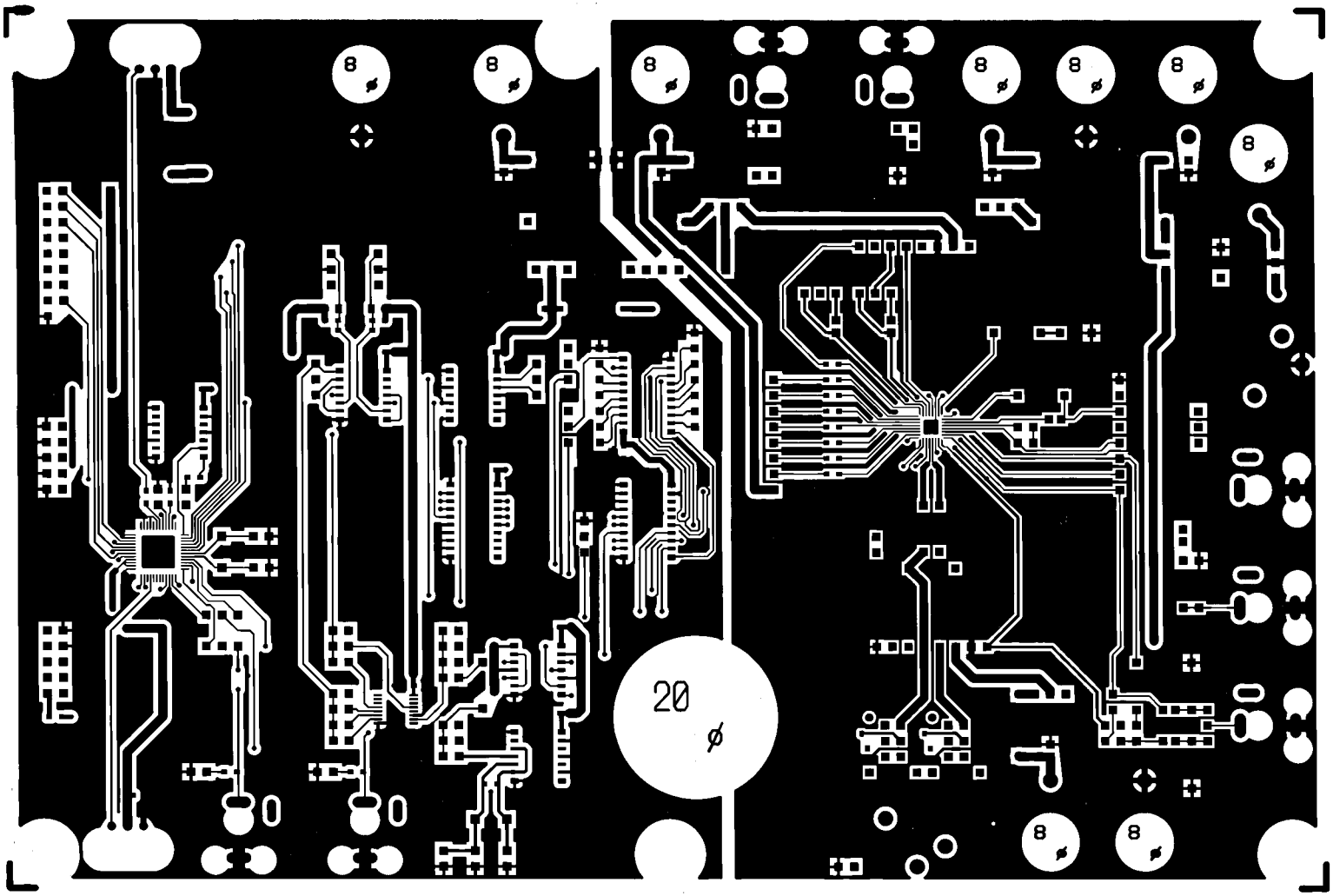

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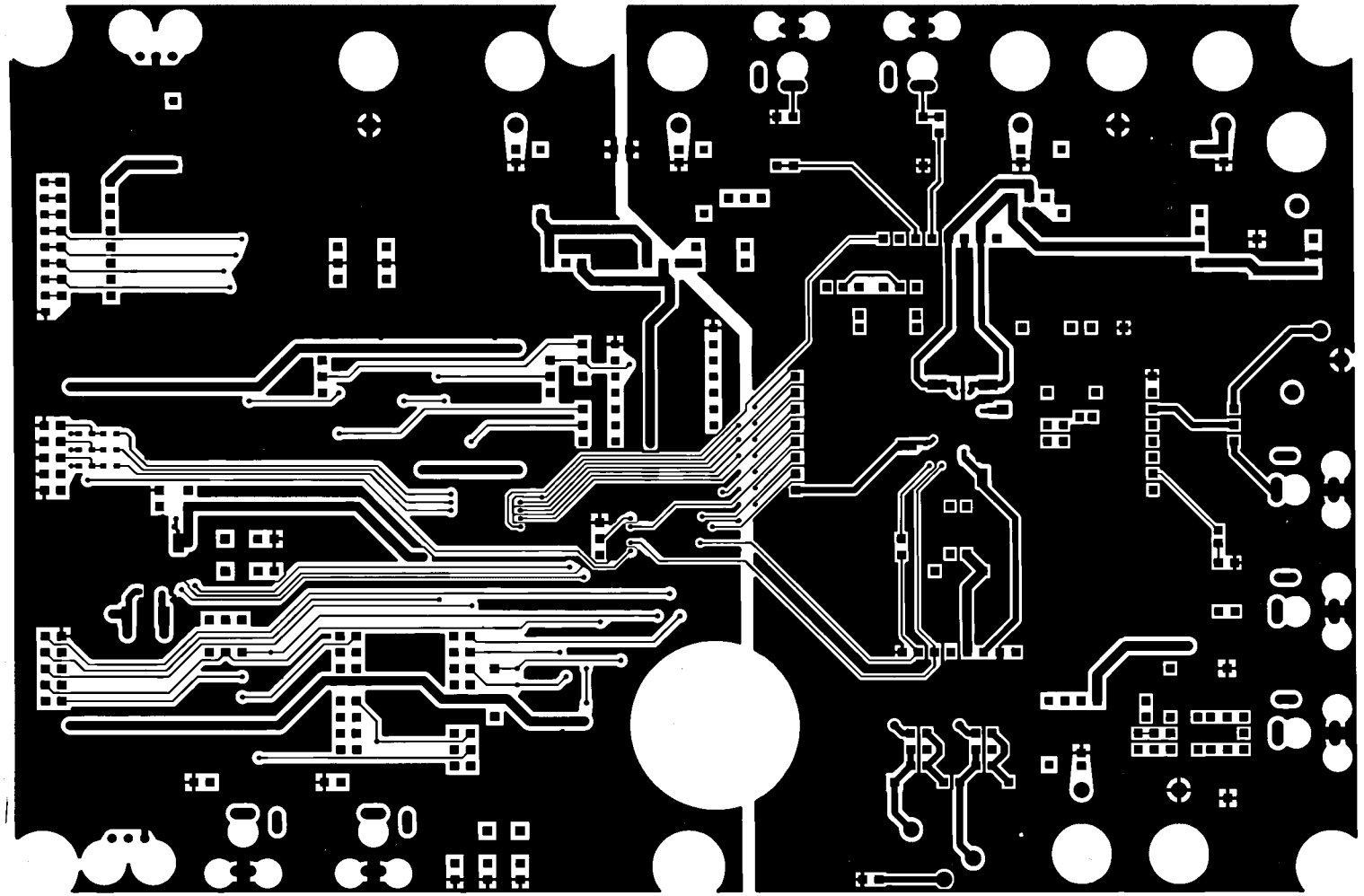

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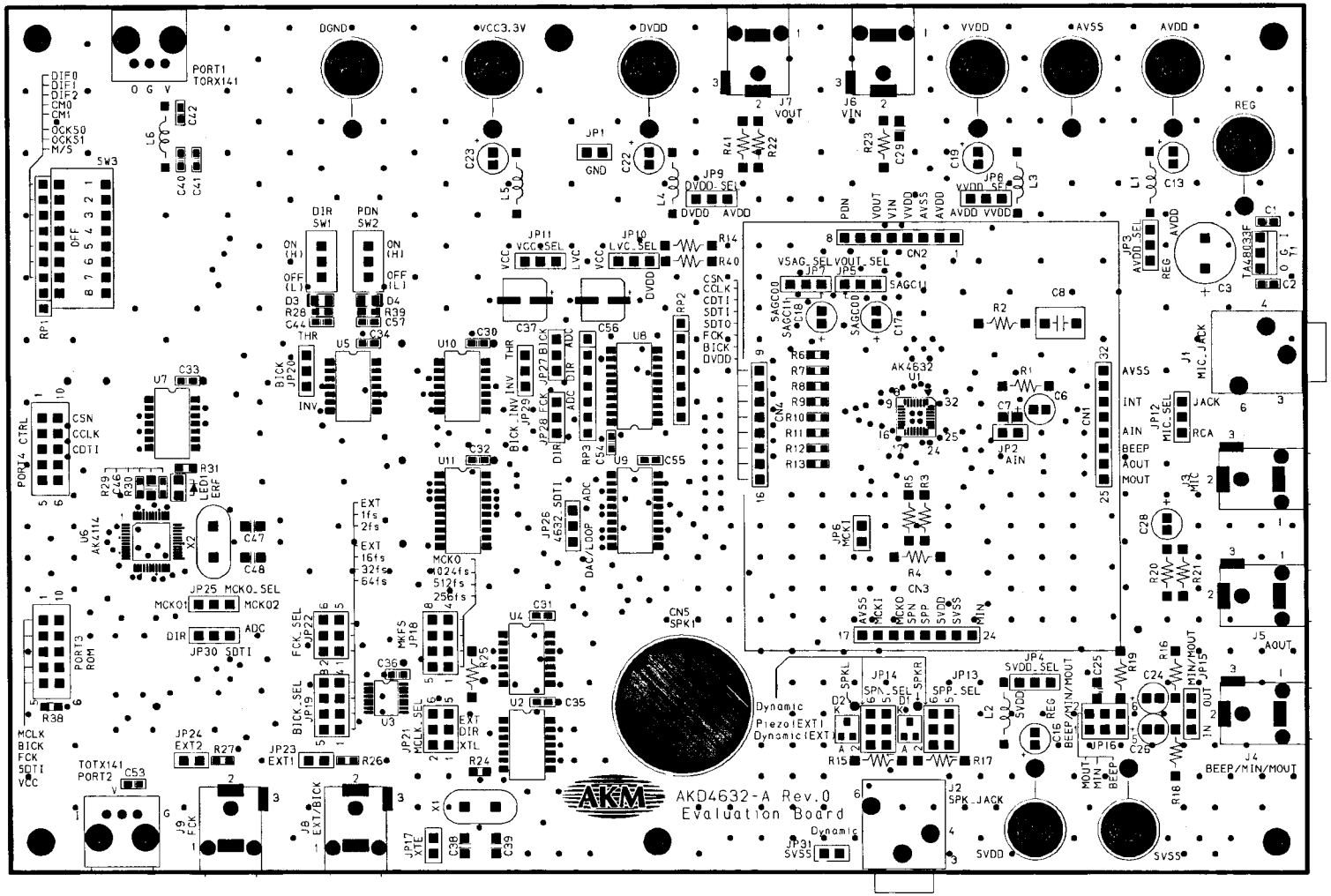

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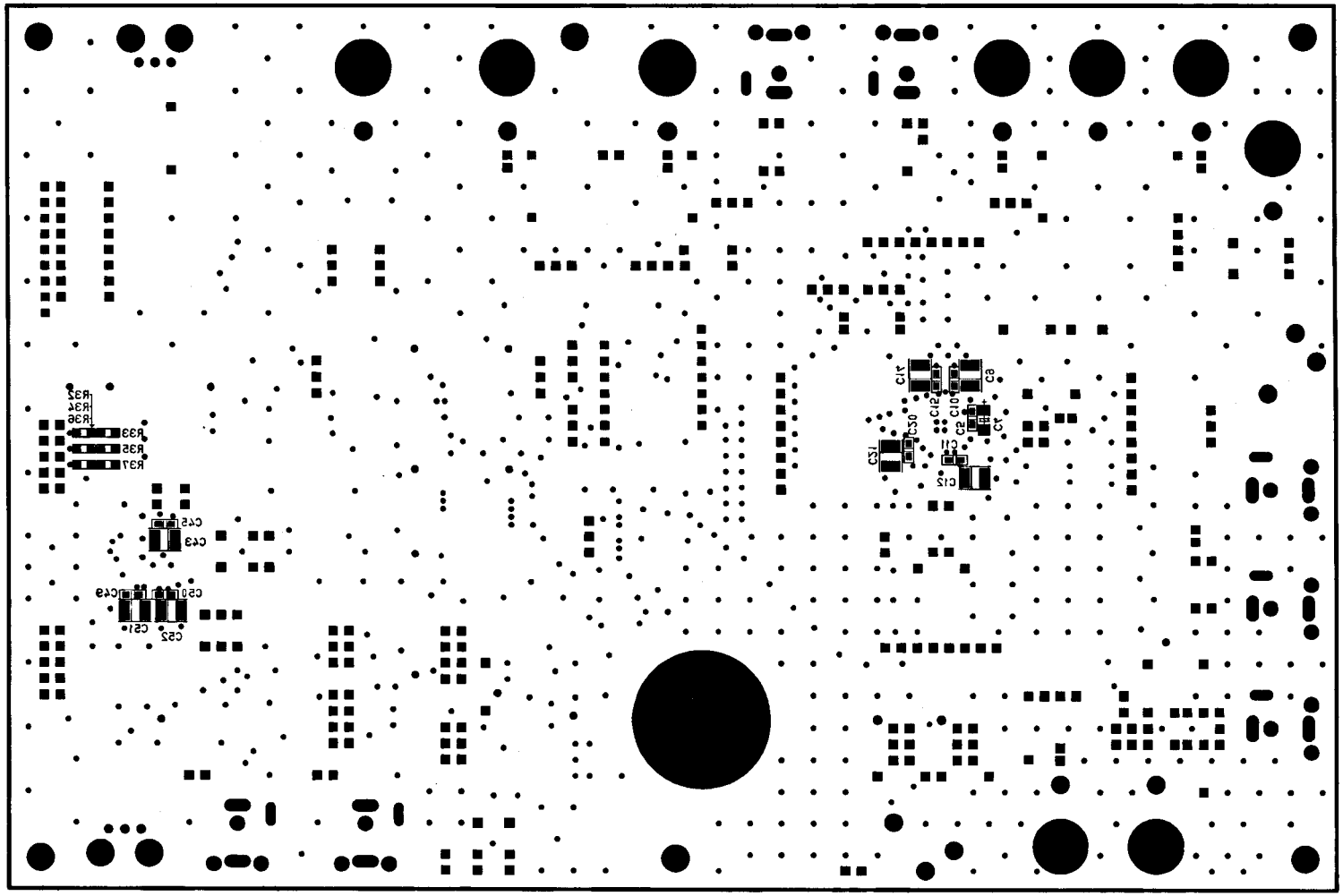

AKD4632-A L2_SILK