EiceDRIVER™ - Safe

High voltage gate driver IC with reinforced isolation

1EDS-SRC

Real-time adjustable gate current control IC
1EDS20I12SV

EiceDRIVER™

Target datasheet

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22	Inserted new parameter “Quiescent current output side VEE2”
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1	corrected sales code
20	Insert note on derating for power dissipation
27	UL 1577 recognition

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EiceDRIVER™ Safe

Real-time adjustable gate current control IC 1EDS20I12SV

1 Overview

PG-DSO36

Main features

- Single-channel isolated IGBT Driver
- Supports IGBT up to 1200 V
- IGBT off-state: 2 A rail to rail
- Overcurrent protection for sense IGBTs and conventional IGBTs
- Desaturation detection
- Soft turn-off shut down
- Two-level turn-off
- Operation at high ambient temperature up to 105°C
- Compatible inputs for 3.3 V, 5 V, and 15 V logic voltages

Product highlights

- Optimized short circuit control for 3-level inverters
- Online adjustable current source slew rate control during IGBT turn-on
- Reinforced isolation according VDE 0884-10

Typical applications

- AC and brushless DC motor drives
- High-voltage DC/DC converters
- UPS systems
- Welding
- Servo drives

Description

The 1EDS20I12SV is a single-channel IGBT driver in a PG-DSO-36-64 package with a reinforced galvanically isolated barrier. The driver IC controls up to three external p-channel MOSFET as a controlled current source during turn-on. The IC is therefore able to control precisely the turn-on process in order to avoid excessive d*v*/dt or d*i*/dt transients. The IC has a peak sinking capability of 2A for turning off the IGBT. An external PNP transistoror is required to support IGBT with currents ratings higher than 75 A.

The logic input pins are 3.3 V, 5 V, and 15 V CMOS-compatible. The data transfer across the galvanic isolation barrier is accomplished with an integrated coreless transformer technology. The 1EDS20I12SV provides several protection features such as IGBT desaturation shut down protection for IGBT, overcurrent protection for sense IGBT, soft turn-off shut down, and two-level turn-off.

2 Block diagram

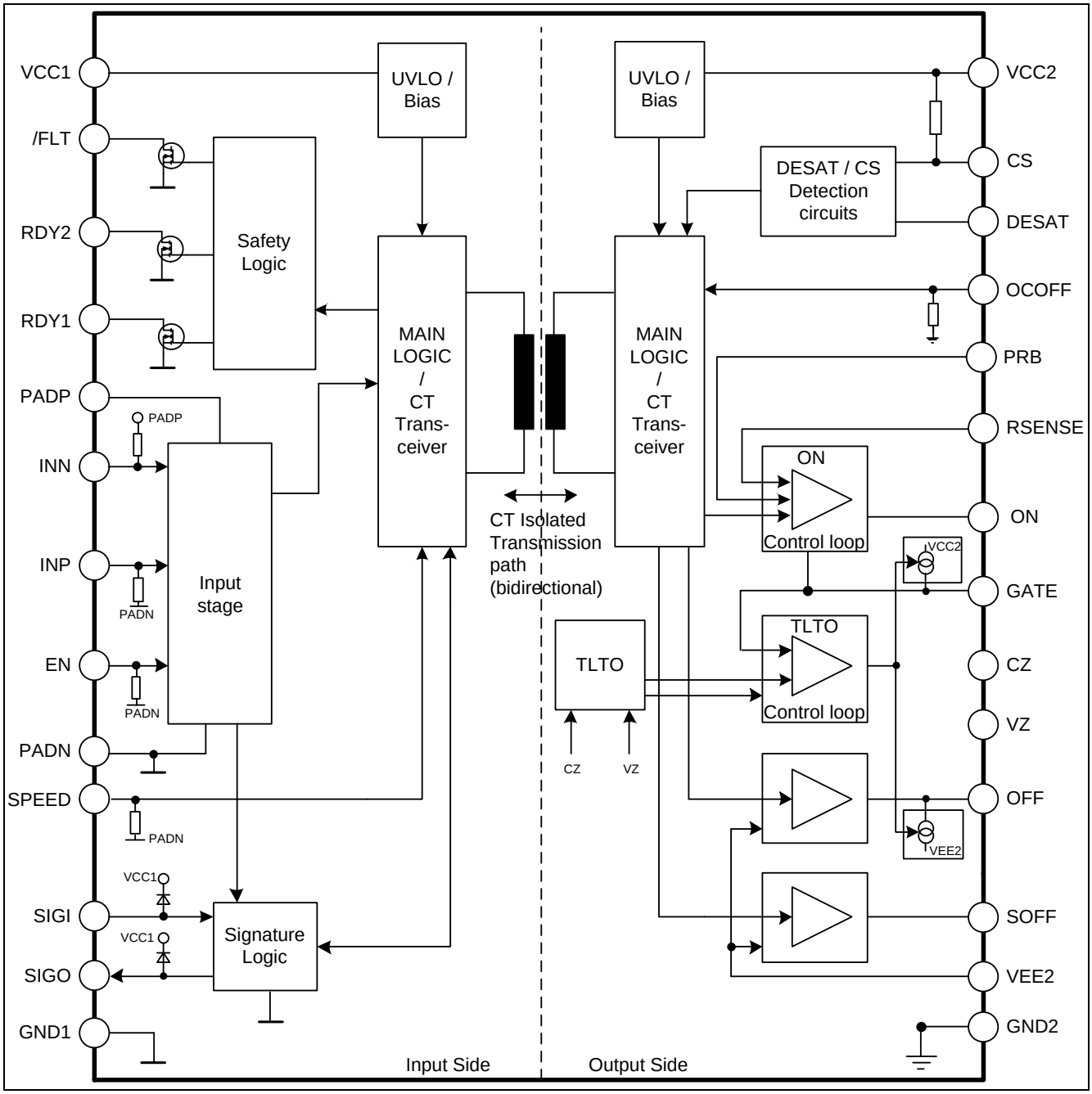


Figure 1 Block diagram for 1EDS20I12SV

3 Pin configuration, description, and functionality

3.1 Terminal configuration

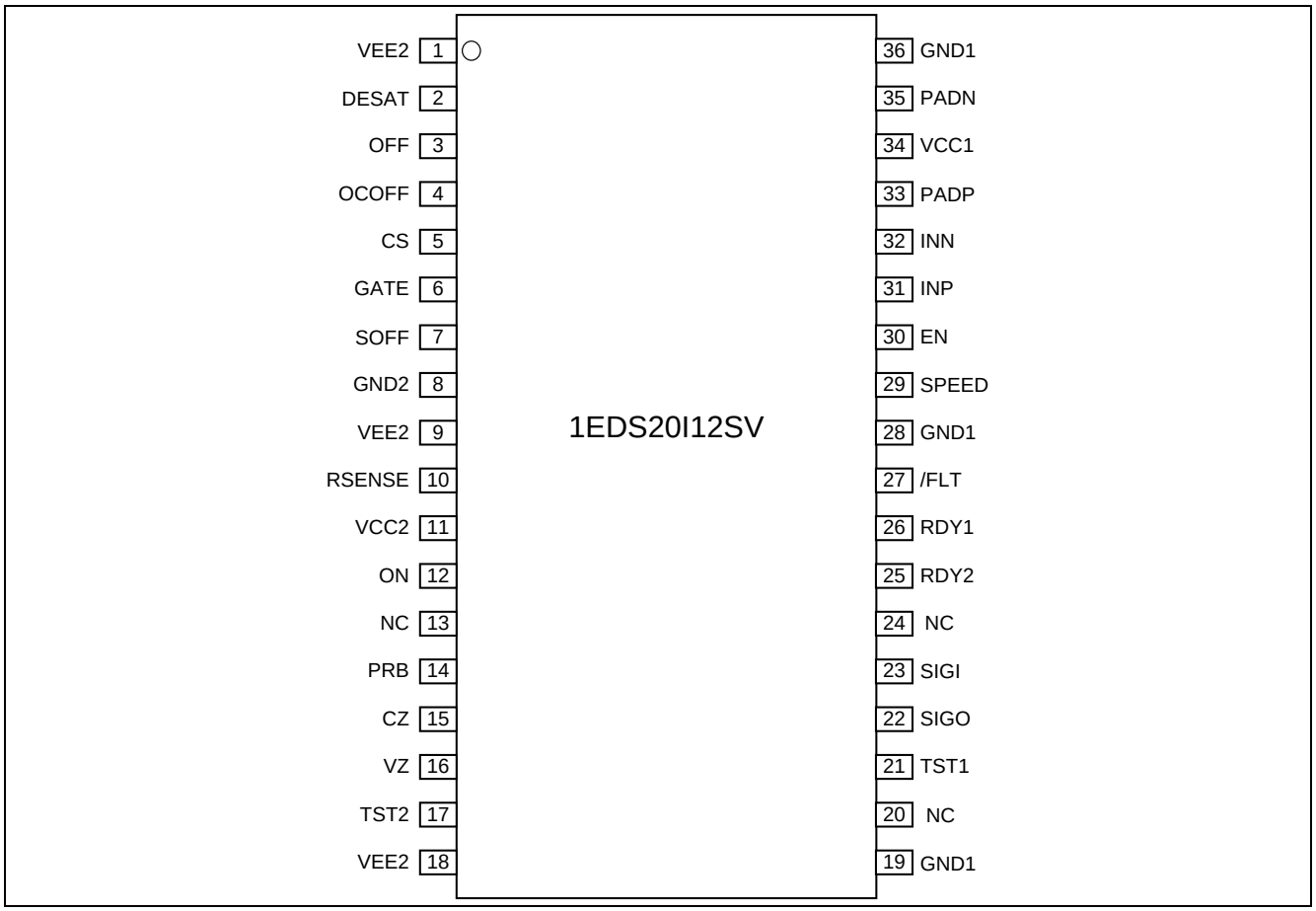


Figure 2 Terminal configuration of 1EDS20I12SV (Top View)

Table 1 Terminal Description

Terminal number	Terminal name	Description
1	VEE2	Negative power supply, output side
2	DESAT	Desaturation shut down protection
3	OFF	Gate turn-off
4	OCOFF	Overcurrent protection on/off
5	CS	Sense IGBT overcurrent
6	GATE	IGBT gate connection
7	SOFF	Gate soft turn-off
8	GND2	Signal ground, output side
9	VEE2	Negative power supply, output side
10	RSENSE	Sense resistor input
11	VCC2	Positive power supply, output side

Table 1 Terminal Description

Terminal number	Terminal name	Description
12	ON	Driver output ON terminal, MOSFET connection
13	NC	Not connected, GND2 recommended
14	PRB	Preboost current adjust
15	CZ	Two-level turn-off time set
16	VZ	Two-level turn-off voltage set
17	TST2	Reserved terminal, to be connected to VEE2 during operation
18	VEE2	Negative power supply, output side
19	GND1	Ground, input side
20	NC	Not connected
21	TST1	Reserved terminal, to be connected to GND1 during operation
22	SIGO	Signature test output
23	SIGI	Signature test input
24	NC	Not connected, GND1 recommended
25	RDY2	Ready signal, output side
26	RDY1	Ready signal, input side
27	/FLT	Fault output
28	GND1	Ground, input side
29	SPEED	IGBT gate current setting (analog)
30	EN	Enable, shutdown, and fault reset input
31	INP	Inverted driver input
32	INN	Non-inverted driver input
33	PADP	Input side logic reference voltage
34	VCC1	Positive power supply, input side
35	PADN	Input side logic reference ground
36	GND1	Ground, input side

3.2 Terminal functionality

GND1

Logic ground terminal of the input side.

PADN

Input side logic reference ground. Direct connection to GND1 is required.

VCC1

5 V power supply for the input side.

PADP

3.3 V, 5 V or 15 V input side logic reference voltage.
The reference terminal for PADP is PADN.

INN inverting driver input

INN control signal for the driver output while INP is set to high. The IGBT is turned on, if INN is set to low, and is turned off, if INN is set to high, respectively. A minimum pulse width is required to prevent from glitches while controlling the IGBT. An internal pull-up resistor ensures that the IGBT is kept in off-state, if terminal INN is left unconnected.

The reference terminal for INN is PADN.

INP non-inverting driver input

INP control signal for the driver output while INN is set to low. The IGBT is turned on, if INP is set to high, and is turned off, if INP is set to low, respectively. A minimum pulse width is required to suppress glitches while controlling the IGBT. An internal pull-down resistor ensures that the IGBT is kept in off-state, if terminal INP is left unconnected.

The reference terminal for INP is PADN.

EN input

Terminal EN needs to be set high for INP and INN to control the IGBT switching.

The EN input terminal serves two purposes:

Feature 1: Enable / shutdown of the output side. The IGBT is turned off by a soft turn-off, if terminal EN is set to low. A minimum pulse width is defined to help suppress glitches on terminal EN.

The IGBT is switched on without preboost on the rising edge of terminal EN, if terminal INP is set high and terminal INN is set low before activating EN.

Feature 2: Resets the desaturation or overcurrent condition signaled on terminal /FLT, if terminal EN is set to low for more than 800 ns. A reset is asserted at the rising edge of terminal EN.

The reference terminal for EN is PADN.

SPEED

IGBT on-state gate current setting sent from input side. This is an analog input terminal. The reference voltage of the internal ADC is PADP.The reference terminal for SPEED is PADN.

/FLT fault output

Open-drain output terminal to signal desaturation of conventional IGBTs or overcurrent of sense IGBTs. Terminal /FLT is set low, if desaturation or overcurrent occurs. The /FLT terminal must be connected via a pull-up resistor to PADP.

The reference terminal for /FLT is GND1.

RDY1 ready status

Open-drain output to signal the proper operation of the input side. RDY1 is set to high if the input side terminals VCC1 and PADP are above their respective undervoltage thresholds. The RDY1 terminal should be connected a via pull-up resistor to PADP.

The reference ground terminal for RDY1 is GND1.

RDY2 ready status

Open-drain output to signal the proper operation of the output side. RDY2 is set to high, if the output side supply is above the UVLO2 level and the internal chip data transmission is operating properly. The RDY2 terminal should be connected via a pull-up resistor to PADP.

The reference ground terminal for RDY2 is GND1.

SIGI

I/O signature check input terminal (5 V, CMOS-compatible)

The reference terminal for SIGI is GND1.

SIGO

I/O signature check output terminal (5 V, CMOS-compatible)
The reference terminal for SIGO is GND1.

TST1

Terminal TST1 is a reserved terminal and has to be connected to GND1.

TST2

TST2 is a reserved terminal and has to be connected to VEE2.

VEE2

Negative power supply terminal for the output side: All VEE2 terminals must be connected to GND2, if no separate negative supply voltage is required.

DESAT

Monitoring of the IGBT saturation voltage $V_{CE(sat)}$ to detect desaturation caused by a short: The IGBT is shut down by activating soft turn-off, if the voltage at this pin is above a given threshold. Two additional filters provide a large robustness against noise and coupling effects. One of these filters is adjustable in terms of the filter time.
The reference terminal for DESAT is GND2.

OFF

Gate turn-off terminal in normal operation mode
The reference terminal for OFF is VEE2.

OCOFF

Input terminal to inhibit the automatic turn-off of the IGBT in case of a desaturation or current sense failure. The fault status continues to be signaled on terminal /FLT. This feature is deactivated (internal pull-down resistor to GND2), if the terminal is left open.
The reference terminal for OCOFF is GND2

CS

Current sense comparator input terminal for sense IGBTs or standard IGBTs with external emitter shunts.
The reference terminal for CS is GND2. If this terminal is connected to GND2, this feature is deactivated.

GATE

Input terminal for sensing the gate voltage at resistor ROFF according to Figure 3.
The reference terminal for GATE is GND2.

PRB

For preboost current adjustment connect a voltage divider between GND2 and VEE2 for a bipolar supply and VCC2 and VEE2 for unipolar supply.
The reference terminal for PRB is VEE2.

SOFF

Output terminal for IGBT soft turn-off in case of short circuit or overcurrent events
The reference terminal for SOFF is VEE2.

GND2

Reference ground terminal of the output side.

RSENSE

Current sense feedback input of the turn-on gate current control loop.

The reference terminal for RSENSE is VCC2.

VCC2

Positive power supply terminal of the output side.

ON

Terminal for the connection to the gate terminal of an external P-channel OptiMOS™ BSD314SPE boost transistor. This transistor is used to drive the IGBT turn-on.

The reference terminal for ON is VCC2.

CZ

This terminal sets the two-level turn-off timing via an external capacitor against VEE2. A short between terminals CZ and VEE2 deactivates the two-level turn-off.

The reference terminal for CZ is VEE2.

VZ

Voltage adjustment terminal for the two-level turn-off feature: This terminal can be connected to VEE2 via a resistor (9.5 V), shorted against VEE2 (11.7 V), or left floating (10.6 V).

The reference terminal for VZ is VEE2.

4 Functional description

4.1 Introduction

The 1EDS20I12SV is an advanced IGBT gate driver with various control and protection features to allow the design of highly reliable systems. The integrated circuit consists of two reinforced isolated sides, called input side and output side. The input side is typically interfaced with a CMOS-compatible standard DSP or a microcontroller. The galvanically isolated output side is connected to the high voltage domain. The adjustable gate current source allows the tuning of the IGBT turn-on slew rate to limit the EMI radiation.

The turn-off process is accomplished with an internal MOSFET stage capable of driving 2 A. An internal MOSFET switch capable of driving 1 A is connected to an external high-impedance gate resistor and prevents from an overvoltage at the IGBT in case of a short or an overcurrent.

The driver also includes IGBT desaturation protection for conventional IGBTs and overcurrent protection for sense IGBTs with the fault status output terminal. Two ready status output terminals indicate whether the driver is properly supplied and operates normally. A two-level turn-off feature with adjustable delay protects against excessive overvoltage at turn-off in case of an overcurrent or a short. The same delay is applied at turn-on to prevent pulse width distortions.

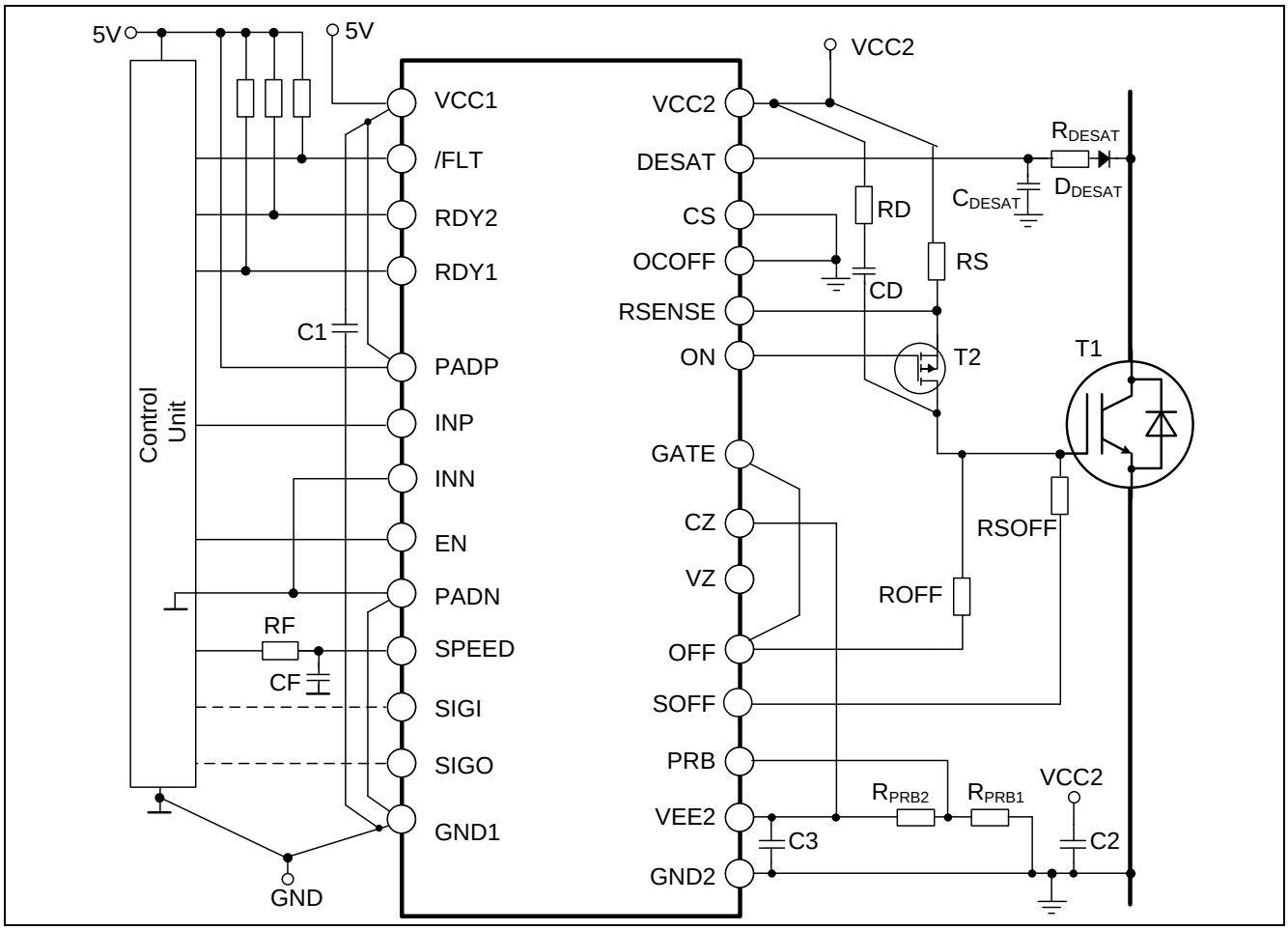


Figure 3 Typical application

4.2 IC Supply

The start up of the input section and the output section of the 1EDS02I12SV needs approx. tbd µs for the VCC1/ PADP domains and tbd µs for the VCC2 domain. However, the IC is in a safe state in any case, meaning that the gate drive outputs are never activated before each part of the IC is ready to operate. The startup times are given in section 5.3.1.

4.2.1 Input side

The driver is supplied with 5 V between terminals VCC1 to GND1. This supply voltage manages the basic functions of the control side. The control side contains a second voltage domain for the logic input signals INP, INN, and EN. This special voltage domain is supplied by the terminals PADP and PADN and can range from 3.3V over 5V to 15V. It is mandatory to connect directly the terminals PADN and GND1. It is important to note, that the voltage domains VCC1 and PADP have independent undervoltage lockout levels and both domains must be supplied appropriately for operation.

VCC1 can be shorted to GND1 in order to deactivate the driver. No turn-on signals will be transmitted from the input to the output side even if terminal VCC1 is left floating. Therefore, the IGBT won't be turned on.

4.2.2 Output side

The EiceDRIVER™ 1EDS20I12SV is designed to support both bipolar and unipolar power supply configurations. The driver IC is typically supplied with a positive voltage of 15 V on terminal VCC2 and a negative voltage of -8 V on terminal VEE2, if configured for bipolar supply. The driver IC is typically supplied with a positive voltage of 15 V on terminal VCC2 for a unipolar supply configuration. VEE2 and GND2 have to be connected together as short as possible in this case.

4.3 Non-inverting and inverting input terminals INP and INN

There are two input modes to control the IGBT. In non-inverting mode, terminal INP controls the driver output while terminal INN is set to low. In inverting mode, terminal INN controls the driver output while terminal INP is set to high. A low signal at terminal INN will activate the output ON. A minimum input pulse width is defined to suppress potential glitches.

4.4 Driver output terminal ON

The output stage consists of the internal regulation circuit inside the driver, an external sense resistor R_{SENSE}, and up to three external P-channel transistors placed in parallel. The recommended P-channel transistor is a BSD314SPE (OptiMOS™-P 3, 30 V, 140 mΩ).

After a short propagation delay, the IGBT is switched on by a regulated current source. The entire turn-on procedure is separated into three phases according to Figure 4: the preboost, the turn-on, and the VCC2 clamping phase.

The preboost phase controls a high current to drive the gate of the IGBT. This brings the gate voltage from its negative level to a voltage slightly lower than the gate-emitter threshold voltage if the IGBT, i.e. $V_{GATE} < V_{GE(th)}$, within a period of typ. 135 ns. The value of the preboost current I_{PRB} is proportional to the voltage V_{PRB} at terminal PRB. The maximum voltage V_{PRB} against VEE2 is 5 V. The preboost current I_{PRB} is defined as:

$$I_{PRB} = \left|\frac{2 \cdot V_{PRB}}{3 \cdot RS}\right| \quad (1)$$

The change from the preboost phase into the turn-on phase needs less than 25 ns. This time must be considered for the setting of the preboost current amplitude in order not to overcharge the gate during the preboost phase.

The gate current during the turn-on phase can be selected out of 11 levels for the proper adjustment of the turn-on transition. The fine granularity between levels 1 and 10 allows accurate slope control. It behaves similar as a traditional driver at level 11. The driver controls the voltage drop across the sense resistor RS. The corresponding gate current I_{gg} is

$$I_{gg} = \frac{V_{RSENSE}}{R_{SENSE}} \quad (2)$$

The selection of the gate current for the turn-on phase is accomplished with terminal SPEED on the input side. Terminal SPEED is an input terminal with voltage levels between 0 V and 3.3 V. The lowest voltage at terminal SPEED corresponds with the highest gate current level, e.g. by connecting SPEED to GND1.

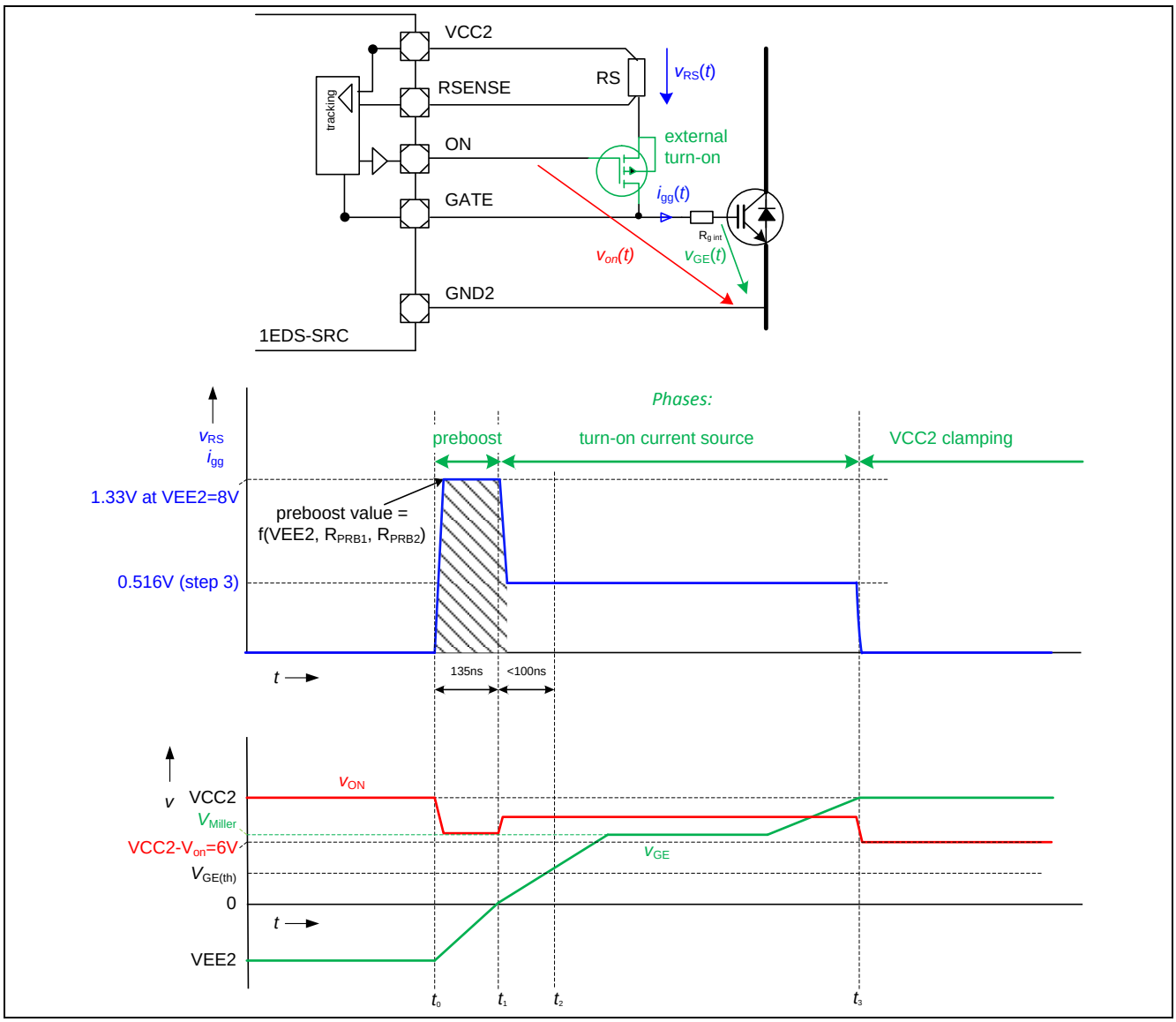


Figure 4 Timing diagram for turn-on

Finally, the IGBT gate voltage saturates at VCC2 in the VCC2 clamping phase. The driver clamps the gate voltage of the external P-channel transistor 6 V below VCC2 according to Figure 4. This provides a low-ohmic connection between the gate of the IGBT and VCC2

It is good board layout engineering to keep tight proximity of the control loop consisting of driver IC, sense resistor, and p-channel MOSFET to avoid oscillations.

4.5 Preboost setting

The preboost timer is always active, both in bipolar or unipolar power supply configuration. The only exception is if the IGBT is turned on via EN according to section 4.7

The preboost current may be set by a simple voltage divider for bipolar gate supply as well as for unipolar supply. In case of bipolar power supply, connect the voltage divider between GND2, PRB, and VEE2. In case of a unipolar power supply, use VCC2, PRB, and VEE2 according to Figure 5.

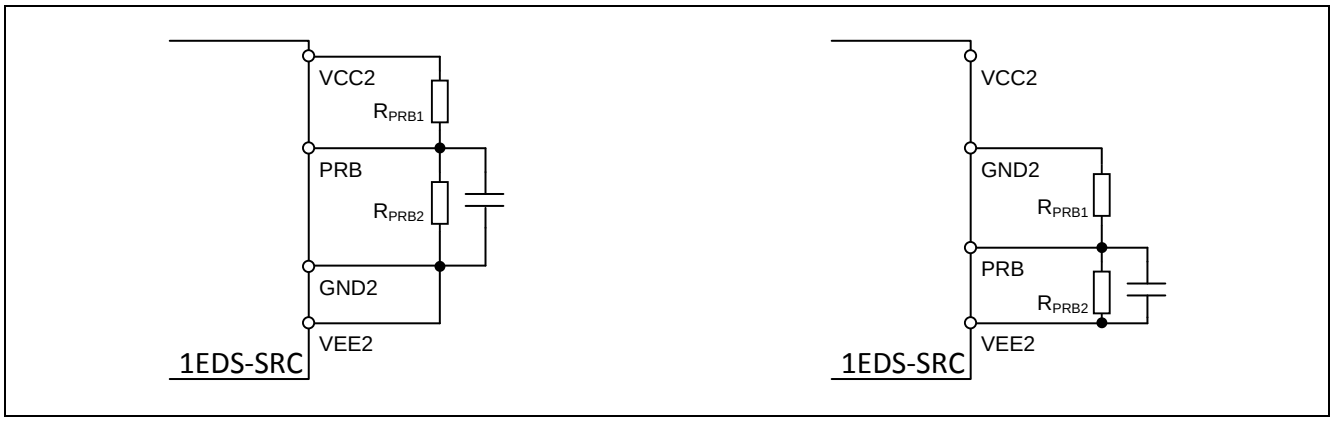


Figure 5 External circuit for setting of preboost current (left: unipolar supply; right: bipolar supply)

The selected preboost current amplitude should charge the IGBT gate from the negative voltage VEE2 to a value between 0 V and $V_{GE(th)}$ of the IGBT within 135 ns. The corresponding IGBT gate charge curves should be consulted for the various collector-emitter voltages V_{CE} for best accuracy.

4.6 Gate turn-off terminal OFF

The driver IC is able to sink a minimum gate current of 1.5A peak. The closed loop controlled sink MOSFET establishes the two-level turn-off function according to section 4.8.6 by controlling the second level during the turn-off process for an adjustable time period T_{TLSET}. An external turn-off boost transistor is recommended for larger sink current capability.

4.7 Terminal EN

Terminal EN is used to enable the input side for normal operation. A soft turn-off is always initiated, when the signal at terminal EN is logic low regardless of the status of signals at terminals INP and INN. The status of EN is dominant over all communications over the insulation barrier. If therefore a shutdown is initiated via terminal EN during normal operation and an overcurrent is detected simultaneously, the IGBT is turned off via soft turn-off. However, /FLT is not activated as the chip is already being reset. /FLT will be activated after IC enable, if the overcurrent still exists on the next IGBT turn-on command.

Signals on terminal EN have also priority over INN and INP. The signals at terminal EN must also pass a noise filter. The EN signal is suppressed, if the pulse duration is shorter than the filter time.evaluated and the driver reacts as described in Table 2.

Table 2 Driver IC status for EN, INP, and INN

EN	INP	INN	Result
high	high	high	regular turn-off / soft off*
high	low	low	regular turn-off / soft off*
high	high ↑	low	turn-on
high	high	low ↓	turn-on
high ↑	high	low	turn-on without preboost

* soft turn-off only in case of simultaneous CS / DESAT event

A second function of the EN terminal is to reset the driver IC after an overcurrent event, which was triggered by the DESAT or CS function. The IC is reset by holding EN low for 800 ns or longer. The fault indication at terminal /FLT follows on the next rising edge of signal EN

4.8 Protection and diagnosis features

4.8.1 Undervoltage lockout (UVLO)

The device is equipped with a system of defined undervoltage lockout (UVLO) levels on both the input and output side to ensure proper operation of the IGBT.

Any triggering of UVLO will turn-off the IGBT by means of the soft turn-off function. All signals at INP and INN are ignored until the voltage at terminals VCC1 recovers above V_{UVLOH1} at terminals VCC1 and V_{UVLOH3} at terminal PADP.

The IGBT is switched off via terminal OFF only in case of an UVLO event at pin VCC2. Signals from the input side are ignored until VCC2 recovers to the power-up level of V_{UVLOH2}. The IC will perform an immediate turn-on after recovery of VCC2 according to Table 3.

4.8.2 Ready and status output terminals

The ready signal RDY1 for the control side covers the following conditions:

- UVLO status of the control side supply voltage domains at terminals VCC1 and PADP
- Establishment of correct signal transmission from input side to output side across the insulation barrier

The ready signal RDY2 for the output side indicates after a short delay:

- UVLO status of the output side supply voltage VCC2
- Establishment of bidirectional signal transmission across the insulation barrier

Both signals are monitoring signals only and need not to be reset actively.

Table 3 Driver IC status UVLO at VCC1, VCC2 and PADP (EN = high)

VCC1	VCC2	PADP	RDY1	RDY2	Result
UVLO ↓	good	good	low	X	SOFF and 5µs watchdog
UVLO ↑	good	good	high	high	acc. INP / INN (turn-on with preboost)
UVLO ↑	good	UVLO	low	high	OFF
X	UVLO ↓	X	X	low	activate OFF and SOFF simultaneously
good	UVLO ↑	good	high	high	acc. INP / INN (turn-on with preboost)
UVLO	UVLO ↑	good	low	high	OFF
X	X	UVLO ↓	low	high	SOFF and 5µs watchdog
good	good	UVLO ↑	high	high	acc. INP / INN (turn-on with preboost)

4.8.3 Fault indication (terminal /FLT)

Terminal /FLT is the indicator for a triggered DESAT or CS event. It is pulled low by an internal FET. The /FLT function is reset by means of a low signal at terminal EN for more than $t_{EN,RST}$ = tbd ns

4.8.4 Watchdog

The bidirectional signal transmission across the insulation barrier is monitored by watchdogs on the input and output side. These are the most important ones:

- The IGBT is switched off via terminal SOFF and additionally switched off via terminal OFF, if the transmission fails for a given duration.
- Another watchdog activates the terminal OFF after 5 µs in any case of a soft turn-off event.

4.8.5 I/O signature check

The I/O signature check is a feature that allows the confirmation of switching commands sent by the microcontroller to the driver IC. The SIGO output terminal is an exclusive-or (XOR) combination of the terminals

INN, INP and EN according to Figure 6. The desaturation status on terminal DESAT and the correct voltage at terminal PADP are also monitored.

To save PCB space, the SIGI and SIGO terminals of a series of drivers can be interconnected via a daisy chain. In this case, terminal SIGI of the first driver in the daisy chain should be connected to VCC1 or GND1. Terminal SIGI of the next driver should be connected to terminal SIGO of the previous driver. Terminal SIGO of the last driver in the daisy chain should be connected to the microcontroller.

The I/O signature check does not monitor the status of the IGBT.

Monitored status

- INN / INP and EN
- DESAT
- PADP undervoltage

The reference terminals are VCC1 and GND1.

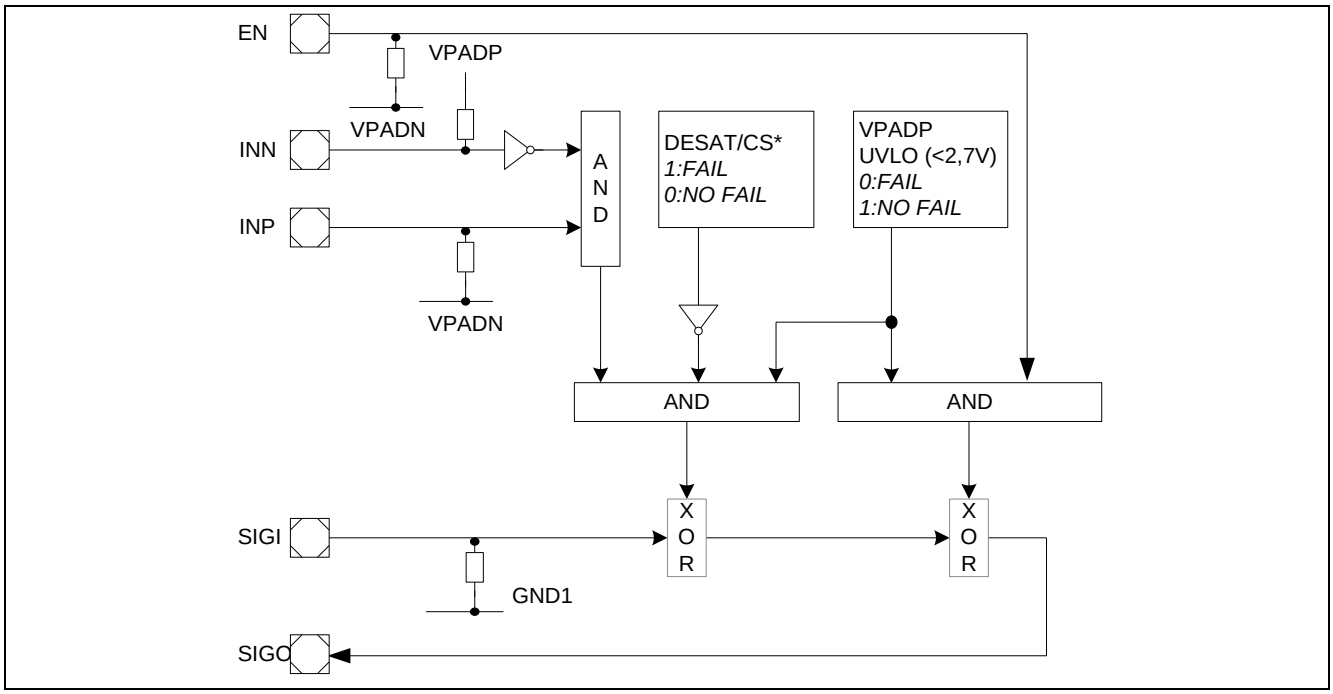


Figure 6 I/O signature check

4.8.6 Two-level turn-off (TLTO)

The TLTO function is activated, if a capacitor is applied between terminal CZ and terminal VEE2. It affects any turn-on and turn-off process, which is either initiated by the input signals INP, INN or EN or by any protection function on the output side. Connecting terminal CZ with terminal VEE2 will deactivate the two-level turn-off function.

The two-level turn-off introduces a second (lower) gate voltage level during the turn-off process according to Figure 16This additional level ensures lower collector-emitter voltage overshoots during turn-off. The second gate voltage level reduces the collector current of the IGBT when reaching this level. The obtained di_C/dt is therefore slower and generates less induced overvoltage. The required timing, which can be adjusted by the capacitance value at terminal CZ, depends on stray inductance and overcurrent at the beginning of the two-level turn-off period.

Three voltage levels are available:

- The voltage level is set to 11.7 V, if terminal VZ is connected to VEE2,
- the voltage level is set to 10.6 V, if terminal VZ is floating,
- the voltage level is set to 9.5 V, if terminal VZ is connected to VEE2 via a 27 kΩ resistor

The second voltage level is set in a way that turn-off losses are the same as during normal turn-off for nominal current values. The turn-on signal is delayed by the duration of the two-level turn-off in order to achieve identical pulse lengths.

The duration of the plateau is set by the capacitor connected between terminals CZ and VEE2.

The IC starts charging the capacitance on CZ for obtaining the two-level set time T_{TLSET}, when a turn-on signal is given. The IC starts the turn-on sequence and resets the capacitor at terminal CZ as soon as the voltage at terminal CZ exceeds 3 V.

The IC activates additionally a soft turn-off sequence, if a turn-off is initiated due to a desaturation condition on terminal DESAT.

4.8.7 Desaturation shut down protection

Desaturation protection ensures the protection of the IGBT in case of a short. When the desaturation voltage on terminal DESAT rises and reaches 9 V, the output is driven low by soft turn-off and the /FLT output terminal is activated. The blanking time is determined by the combination of the highly precise internal current source and an external capacitor. Desaturation protection is only set active 400ns after the preboost phase.

4.8.8 IGBT overcurrent detection

The IGBT overcurrent detection is a protection feature that senses the emitter current on current-sense IGBTs or standard IGBTs via using an emitter shunt resistor. The voltage is measured by a comparator that triggers at 0.35 V. The current sense signal at terminal CS is ignored while the IGBT is off. An external blanking circuit is necessary to prevent false tripping during turn-on. With non-sensing IGBT types, a low resistance shunt is used to sense the emitter current. When a short is detected, the IGBT is switched off by a soft turn-off. Both the desaturation and the current sense features can be used at the same time. The fault status is signaled on terminal /FLT. The fault status has to be reset via terminal EN. IGBT overcurrent detection is only active 400ns after the preboost phase.

4.8.9 Overcurrent protection ON/OFF

If terminal OCOFF is connected to GND2 or left unconnected, the IGBT is switched off via a soft turn-off in case of a CS or DESAT event. If terminal OCOFF is connected to VCC2, the IGBT is not switched off in such cases. The IGBT can be turned off externally instead, e.g. via control input EN. However, the signaling of CS or DESAT events to output /FLT is done in any case.

4.8.10 Soft turn-off

The IGBT can be turned off smoothly via an external higher-ohmic gate resistor attached to terminal SOFF. The soft turn-off speed can be adjusted by selecting the appropriate resistor value. The soft turn-off reduces the voltage overshoot considerably and may be used in combination with the two-level turn-off function of the IC. The regular turn-off function at terminal OFF supports the soft turn-off as soon as the voltage between terminals GATE and VEE2 drops below 3 V. An additional safety feature is installed by means of a watchdog timer, which starts at the same time the soft turn-off is triggered. The watchdog turns off the IGBT in any case via terminal OFF after 5 µs. If the soft-off function is not used, both the terminals SOFF and OFF can be combined to increase the turn-off current capability of the IC.

Trigger conditions for a soft turn-off:

- Desaturation condition at terminal DESAT
- Overcurrent condition at terminal CS
- Driver Enable OFF (EN equals GND1)
- UVLO1 of the input side supply VCC1
- UVLO of the input side logic reference PADP
- Internal signal transmission error

5 Electrical parameters

5.1 Absolute maximum ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all parameters refer to GND1 and to T_A =25°C.

Table 4 Abs. maximum ratings

Parameter	Symbol	Min.	Max.	Unit
Positive power supply input side	V_{VCC1}	-0.3	6.5	V
PADP voltage	V_{PADP}	-0.3	16.05	
PADN voltage	V_{PADN}	-0.3	0.3	
Voltage at terminals INN, INP, EN, RDY1, RDY2, /FLT, **EN** Voltage at terminals SIGI, SIGO, SPEED	$V_{TERMINAL}$	-0.3 -0.3	V_{PADP} V_{VCC1}	
Voltage at terminals DESAT[1] Voltage at terminals GATE [2], Voltage at terminals OCOFF[1], RSENSE [2], **OFF [2], SOFF [2]** Voltage at terminals CS [1], VZ [2], CZ [2], PRB [2]		-5 -0.3 -0.3 -0.3	V_{VCC2} V_{VCC2} V_{VCC2} 5.5	
Positive power supply output side [1]	V_{VCC2}	-0.3	20.3	
Negative power supply output side [1]	V_{VEE2}	-12	0.3	
Maximum power supply voltage output side (V_{VCC2} - V_{VEE2})	V_{max2}	–	28	
Open drain output current (/FLT, RDY2, RDY1)	I_{OD}	–	10	mA
Output current at terminals SIGO	I_{SIGO}	-6	6	
Peak output current at terminal ON (t_p = 2 µs, f = 20 kHz)	$I_{ON,pk}$	–	50	
DC output current at terminal ON (V_{CC2} = 20 V)	$I_{ON,DC}$	–	10	
Peak output current at terminal OFF (t_p = 2 µs, , f = 20 kHz)	I_{OFF}	–	2.4	A
Peak output current at terminal SOFF (t_p = 2 µs, , f = 20 kHz)	I_{SOFF}	–	1.05	
Junction temperature	T_J	-40	125	°C
Storage temperature	T_S	-55	125	
Total power dissipation [3]	$P_{D,tot}$	–	980	mW
Thermal resistance (Both chips active), T_A = 25 °C	$R_{th(j-a)}$	–	102	K/W
ESD Capability HBM [4]	V_{ESD}	–	tbd	kV
CDM [5]			tbd	
Common mode transient immunity	$\|dV_{ISO}/dt\|$	50	–	kV/µs

[1] with respect to terminal GND2

[2] with respect to terminal VEE2

[3] Power dissipation is derated linearly with 9.8 mW/°C above an ambient temperature of T_A = 25°C. See Figure 18 for reference layouts for these thermal data. Thermal performance may change significantly with layout and heat dissipation of components in close proximity.

[4] According to EIA/JESD22-A114-B

[5] According to EIA/JESD22-C101

5.2 Operating range

Note: The IC operates as described in the functional description within the operating range. Unless otherwise noted all parameters refer to terminal GND1 *and (T_A = 25°C).*

Table 5 Operating parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Positive power supply input side	V_{VCC1}	4.75	5	5.5	V
Input side logic reference voltage V_{PADP} - V_{PADN} V_{PADP} =3.3V	ΔV_{PAD}	3	3.3	5.5	
Input side logic reference voltage V_{PADP} - V_{PADN} V_{PADP} = 15V		7	15	15.75	
weitere Parameter aus abs max. ratings					
Control voltage by terminal SPEED at terminal RSENSE	$V_{IN,RSENSE}$	V_{VCC2}-1.7	–	V_{VCC2}-0.2V	
Voltage at terminal SPEED [2]	V_{SPEED}	0	–	3.3	
Positive power supply output side [1]	V_{VCC2}	–	15	20	
Negative power supply output side [1]	V_{VEE2}	-12	-8	0	
Power supply voltage output side (V_{VCC2} - V_{VEE2})	V_{max2}	–	–	25	
Output current at terminal SIGO	I_{SIGO}	-5	–	5	mA
Ambient temperature	T_A	-40	–	105	°C

1) With respect to terminal GND2.
2) With respect to terminal PADN
3) With respect to terminal VEE2

5.3 Electrical characteristics

Note: The electrical characteristics include the spread of values in supply voltages, load and junction temperatures given below. Typical values represent the median values at T_A = 25°C, V_{VCC1} = V_{PADP} = 5V, V_{PADN} = V_{GND1} =, V_{VCC2} = 15V, V_{VEE2} = -8V and the given test conditions. Unless otherwise noted all voltages are given with respect to their respective reference terminal (GND1 for terminals 19 to 36, GND2 for terminals 1 to 18).

5.3.1 Voltage supply

Table 6 Voltage supply

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
UVLO threshold for VCC1 power up	V_{UVLOH1}	–	–	tbd	V	V_{RDY1} > tbd
UVLO threshold for VCC1 power down	V_{UVLOL1}	tbd	–	–		V_{RDY1} < tbd
UVLO hysteresis VCC1 (V_{UVLOH1} - V_{UVLOL1})	$V_{UVLO1,hys}$	0.15		–		
UVLO threshold VCC2 power up	V_{UVLOH2}	–	–	12.6		V_{RDY2} > tbd
UVLO threshold VCC2 power down	V_{UVLOL2}	10.4	–	–		V_{RDY2} < tbd
UVLO hysteresis VCC2 (V_{UVLOH2} - V_{UVLOL2})	$V_{UV,hys2}$	tbd	0.9	–		
UVLO threshold for PADP power up	V_{UVLOH3}	tbd	–	tbd		V_{RDY1} > tbd
UVLO threshold for PADP power down	V_{UVLOL3}	tbd	–	tbd		V_{RDY1} < tbd
UVLO hysteresis PADP (V_{UVLOH3} - V_{UVLOL3})	$V_{UVLO3,hys}$	tbd	0.75			
Quiescent current input side	I_{Q1}	–	tbd	tbd	mA	V_{INP} = V_{PADP}, V_{INN} = V_{PADN} V_{RDY1} = V_{RDY2} = V_{FLT} = V_{PADP}
Quiescent current input side		–	tbd	tbd		V_{INP} = V_{PADP} = V_{FLT} = V_{RDY1} = V_{RDY2} = 15V, V_{INN} = V_{PADN}
Quiescent current output side VCC2	I_{Q2}	–	7	tbd		V_{INP} = V_{PADP}, V_{INN} = V_{PADN} V_{RDY1} = V_{RDY2} = V_{FLT} = V_{PADP}
Quiescent current output side	$I_{Q2,UVLO}$	–	tbd	tbd		tbd.
Quiescent current output side VEE2	I_{Q3}		tbd			tbd.
Quiescent current PADP	I_{Q4}					V_{INP} = V_{PADP}, V_{INN} = V_{PADN} V_{RDY1} = V_{RDY2} = 5 V V_{FLT} = 5 V

5.3.2 Logic input and output

Table 7 Logic input and output

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
Low level input voltage terminals INP, INN, EN	V_{IL}	tbd	1.7	–	V	

Table 7 Logic input and output

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
High level input voltage terminals INP, INN, EN	V_{IH}	–	3.3	tbd		
Low level input voltage terminal SIGI	$V_{IL,SIGI}$	tbd	1.8	tbd	V	
High level input voltage terminal SIGI	$V_{IH,SIGI}$	tbd	2.75	tbd		
Low level output voltage terminal SIGO	$V_{OL,SIGO}$	V_{GND1}	0.2	0.5		$I_{IL,SIGO}$ = 5mA
High level output voltage terminal SIGO	$V_{OH,SIGO}$	4.3	4.7	V_{VCC1}		$I_{IL,SIGO}$ = - 5mA
Low level output voltage terminals /FLT, RDY1, RDY2	$V_{OL,FLT}$, $V_{OL,RDY1}$, $V_{OL,RDY2}$	–	0.15	tbd		$I_{IL,pin}$ = 5 mA
Input bias current INP	$I_{IH,INP}$	tbd	55	tbd	µA	V_{INP} = 5 V
Input bias current EN	$I_{IH,EN}$	tbd	55	tbd		V_{EN} = 5 V
Input bias current INN	$I_{IL,INN}$	tbd	-740	tbd		V_{INN} = 0 V
Input bias current SPEED	$I_{IH,SPEED}$	tbd	5.6	tbd		V_{SPEED} = 5 V
Input filter time terminals INP, INN, SIGI	T_{FILIN}	tbd	–	–	ns	$V_{TERMINAL}$ = 5 V
Input filter time terminal EN	T_{FILEN}	tbd	–	–		V_{EN} = 5 V
Fault reset duration terminal EN	$T_{EN,RST}$	tbd	–	tbd		V_{EN} = 0 V
Propagation delay EN	$T_{EN,ON}$			tbd		neuer Parameter !
Shut down propagation delay EN to SOFF	$T_{EN,SOFF}$			tbd		neuer Parameter !

5.3.3 Gate driver

Table 8 Gate driver

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
Input voltage terminal RSENSE	$V_{IN,RSENSE}$	V_{VCC2}-1.7	–	V_{VCC2}-0.2V	V	IC in control mode
Detection of gate current level 1	V_{RSENSE}	tbd	V_{VCC2}-0.2	tbd		3.03V ≤ V_{SPEED} ≤ 3.3V
Detection of gate current level 2		tbd	V_{VCC2}-0.29	tbd		2.75V≤V_{SPEED}≤3.03 V
Detection of gate current level 3		tbd	V_{VCC2}-0.38	tbd		2.48V≤V_{SPEED}≤2.75 V
Detection of gate current level 4 [1)]		tbd	V_{VCC2}-0.47	tbd		2.2V≤V_{SPEED}≤2.48V
Detection of gate current level 5	V_{RSENSE}	tbd	V_{VCC2}-0.56	tbd		1.93V≤V_{SPEED}≤2.2V
Detection of gate current level 6		tbd	V_{VCC2}-0.64	tbd		1.65V≤V_{SPEED}≤1.93 V
Detection of gate current level 7		tbd	V_{VCC2}-0.73	tbd		1.38V≤V_{SPEED}≤1.65 V
Detection of gate current level 8		tbd	V_{VCC2}-0.82	tbd		1.11V≤V_{SPEED}≤1.38 V

Table 8 Gate driver

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
Detection of gate current level 9		tbd	V_{VCC2}-0.91	tbd		0.83V≤V_{SPEED}≤1.11 V
Detection of gate current level 10		tbd	V_{VCC2}-1.0	tbd	V	0.55V≤V_{SPEED}≤0.83 V
Detection of gate current level 11		tbd	V_{VCC2}-1.57	tbd		0V≤V_{SPEED}≤0.55V
V_{RSENSE} hyseresis		tbd		tbd	mV	
Low level output voltage terminal OFF	V_{OFFL}	–	–	V_{EE2}+tbd	V	I_{OFFL} = 20 mA
		–	V_{EE2}+0.3	V_{EE2}+tbd		I_{OFFL} = 200 mA
		–	V_{EE2}+2.3	V_{EE2}+tbd		I_{OFFL} = 1 A
		–	V_{EE2}+7	–		I_{OFFL} = 2 A [2]
Low level output voltage terminal SOFF	V_{SOFFL}	–	–	V_{EE2}+tbd		I_{SOFFL} = 20 mA
		–	V_{EE2}+0.3	V_{EE2}+tbd		I_{SOFFL} = 200 mA
		–	V_{EE2}+7.3	V_{EE2}+tbd		I_{SOFFL} = 1 A
Input voltage terminal ON	$V_{OH,ON}$	tbd	–	–		I_on = 8 mA
	$V_{OL,ON}$					I_on = -8 mA
Turn-on clamping voltage terminal ON	$V_{ON,ON}$	–	V_{VCC2}-tbd	V_{VCC2}-tbd		
Turn-off threshold voltage terminal GATE	$V_{GATE,th}$	–	3	–		
Preboost time	T_{PRB}	–	135	tbd	ns	
Speed setting propagation delay [2]	T_{SPEED}	–	–	120	µs	IGBT is turn on
Fall time	T_{FALL}	–	tbd	tbd		
Turn-on propagation delay without PMOS	T_{PDON}	–	460	tbd	ns	T_A = 25°C
Turn-off propagation delay	T_{PDOFF}	–	460	tbd		T_A = 25°C
Turn-on propagation delay variation over junction temperature [2]	T_{PDONt}	tbd	–	tbd		
Turn-off propagation delay variation over junction temperature [2]	T_{PDOFFt}	–	–	tbd		
Matching delay (T_{PDON} - T_{PDOFF})	MT	–	–	tbd		T_A = 25°C
Matching delay over temperature (T_{PDONt} - T_{PDOFFt}) [2]	MT_t	–	–	tbd		

1) Default state after power on (V_{VCC1} > V_{UVLOH1})

2) The Parameter is not subject to production test - verified by design / characterization

5.3.4 Desaturation protection (DESAT)

Table 9 Desaturation protection

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
Desaturation trigger level	V_{DESAT}	tbd	9	tbd	V	
Blanking capacitor charge current	$I_{DESAT,C}$	tbd	500	tbd	µA	V_{DESAT} = 2 V
Blanking capacitor discharge current	$I_{DESAT,D}$	–	12	–	mA	V_{DESAT} = 6 V
Desaturation leading edge blanking time	$T_{DESATleb}$	–	tbd	–	ns	
Desaturation filter time [1]	$T_{DESATFIL}$	–	tbd	–		
DESAT shut down propagation delay to SOFF	T_{SOFF}	–	350	tbd		tbd
DESAT shut down propagation delay to OFF	$T_{DESATOFF}$	–	5	tbd	µs	OCOFF = high
DESAT to /FLT propagation delay	$T_{DESATFLT}$	–	700	tbd	ns	

1) The Parameter is not subject to production test

5.3.5 Overcurrent protection disable (OCOFF)

Table 10 Overcurrent protection disable

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
High level input voltage terminal OCOFF	$V_{IH,OCOFF}$	0.7 x V_{VCC2}	–	–	V	
Low level input voltage terminal OCOFF	$V_{IL,OCOFF}$	–	–	0.3 x V_{VCC2}		
Input bias current OCOFF	$I_{IH,OCOFF}$	–	140	tbd	µA	V_{OCOFF} = 15 V

5.3.6 Current sense (CS)

Table 11 Current sense

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
Current sense trigger threshold	V_{CS}	tbd	350	tbd	V	V_{SOFF} < 4 V
Input bias current CS	$I_{IH,CS}$	tbd	-115	tbd	µA	V_{CS} = 0 V
Over current detection blanking time [1]	$T_{CS,blank}$	–	tbd	–	ns	
Shut down propagation delay CS to SOFF	T_{CS}	–	400	tbd		tbd
Propagation delay CS to /FLT	$T_{CS,FLT}$	–	700	tbd		

1) The parameter is not subject to production test

5.3.7 Two-level turn-off (CZ, VZ, GATE)

Table 12 Two-level turn-off

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
Two-level voltage terminal VZ	V_{TLTO}	Tbd	11.7	Tbd	V	Terminal VZ connected to VEE2
		Tbd	10.6	Tbd		VZ open connected to VEE2
		Tbd	9.5	Tbd		R_{VZ} = 27 kΩ connected to VEE2
Two-level turn-off threshold voltage [1]	$V_{TLTO,th}$	–	3	–		
Two-level turn-off charging current	I_{CZ}	tbd	1000	tbd	µA	$V_{CZ} = V_{EE2}$ + 1V
Two-level turn-off time limitation	T_{TLLIM}	Tbd	5	tbd	µs	
Two-level voltage slope [2]	dV_{TLTO}/dt		15		V/µs	

1) Referenced to VEE2

2) The parameter is not subject to production test - verified by design / characterization

6 Insulation characteristics

6.1 Reinforced insulation requirements according to VDE 0884-10 (pending)

Table 13 Reinforced insulation

Parameter	Symbol	Characteristic	Unit
Installation classification per EN 60664-1, Table 1 For rated mains voltage ≤ 150 V_{rms} For rated mains voltage ≤ 300 V_{rms} For rated mains voltage ≤ 600 V_{rms} For rated mains voltage ≤ 1000 V_{rms}		Rated Impulse Voltage I-IV = 4000 V I-IV = 6000 V I-IV = 8000 V I-III = 8000 V	
Climatic Classification according to IEC 68		40 / 105 / 21	
Pollution degree (EN 60664-1)		2	
Minimum external clearance	CLR	8.2	mm
Minimum external creepage	CPG	8.2	
Minimum Comparative Tracking Index	CTI	>400	
Maximum Repetitive Insulation Voltage	V_{IORM}	1420	V_{pk}
Input to output test voltage, method b V_{IORM} * 1.875 = V_{PR}, productive test, t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	2662	
Highest allowable overvoltage	V_{IOTM}	8000	
Maximum withstanding insulation voltage, 1 min	V_{ISO}	5000	V_{rms}
Insulation resistance at T_s, V_{IO} = 500 V	R_{IO}	> 10^9	Ω

Notes

This coupler is suitable for "reinforced insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

6.2 Recognized under UL 1577 (pending)

Table 14 Recognized under UL 1577

Parameter	Symbol	Characteristic	Unit
Insulation withstand voltage / 1 min	V_{ISO}	5000	V_{RMS}
Insulation test voltage / 1 s	V_{ISO}	6000	V_{RMS}

7 Timing diagrams

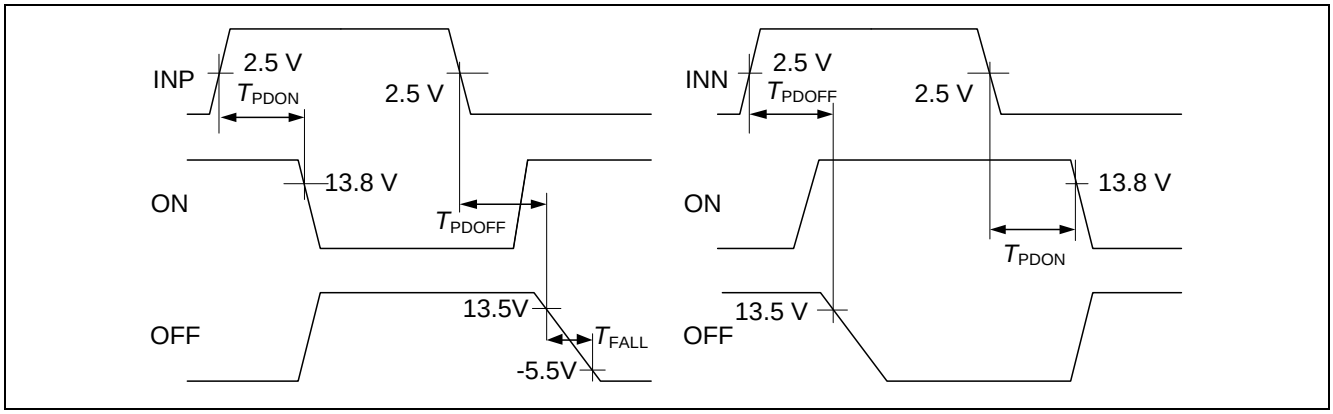


Figure 7 Timing of turn-on and turn-off propagation delay without two-level turn-off mode

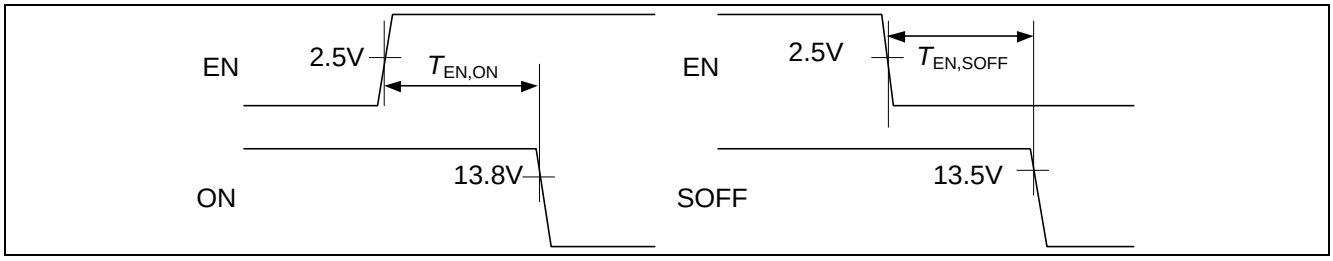


Figure 8 Timing of EN turn-on and shut down propagation delay

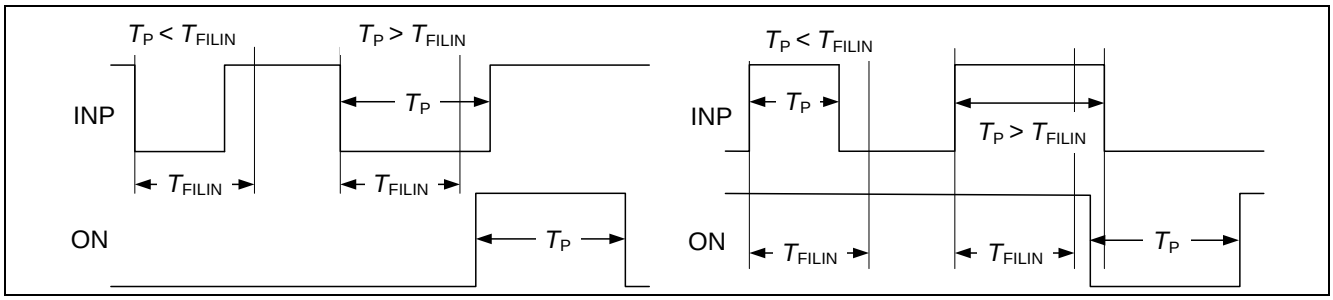


Figure 9 Timing of short pulse suppression terminal INP

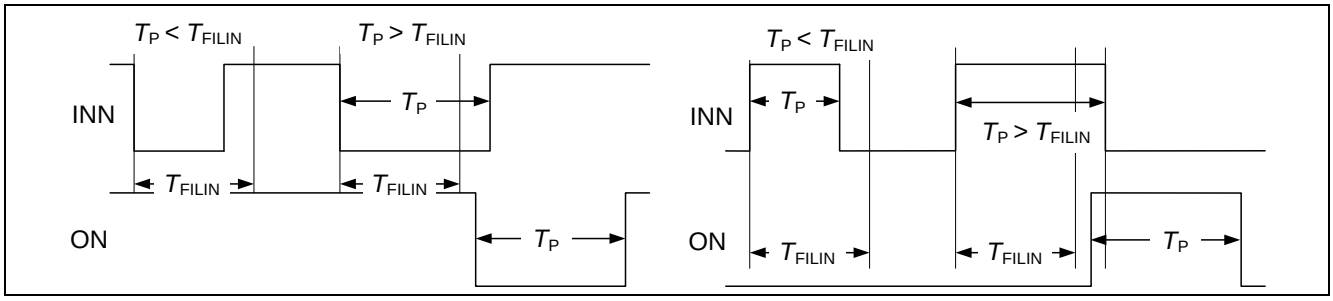


Figure 10 Timing of short pulse suppression terminal INN

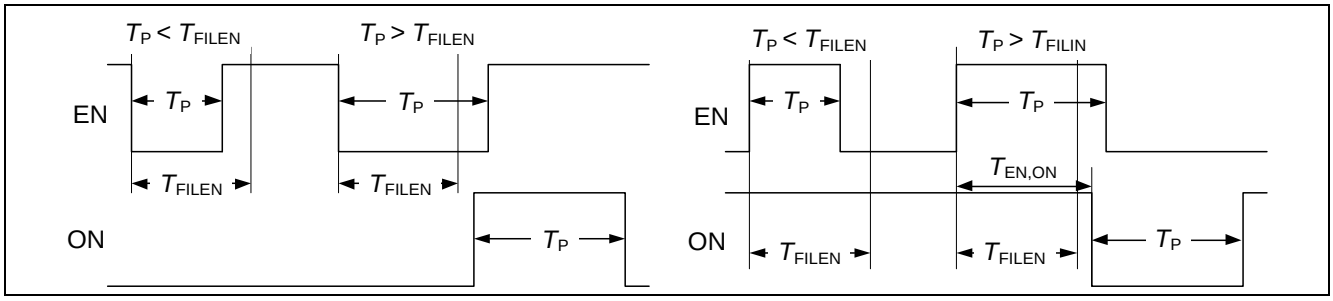


Figure 11 Timing of short pulse suppression terminal EN and EN propagation delay to turn-on

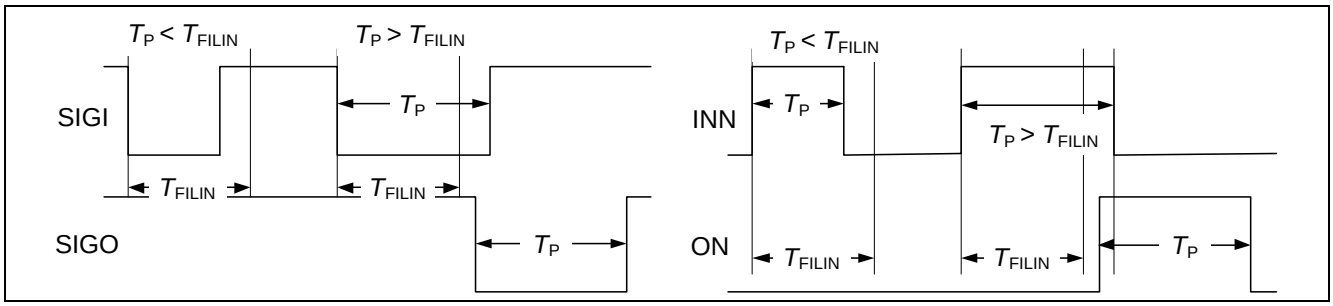


Figure 12 Timing of short pulse suppression terminal SIGI

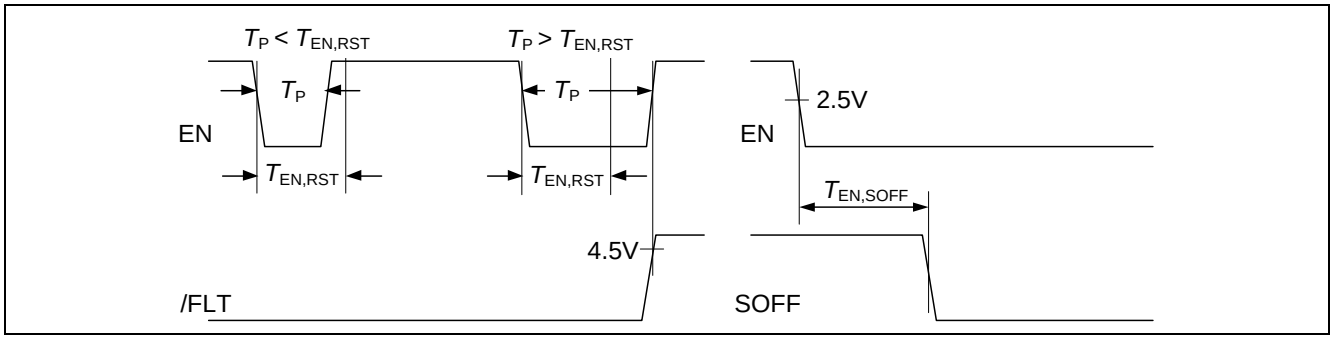


Figure 13 Timing for fault reset at terminal EN (left) and EN shut down time to soft turn-off (right)

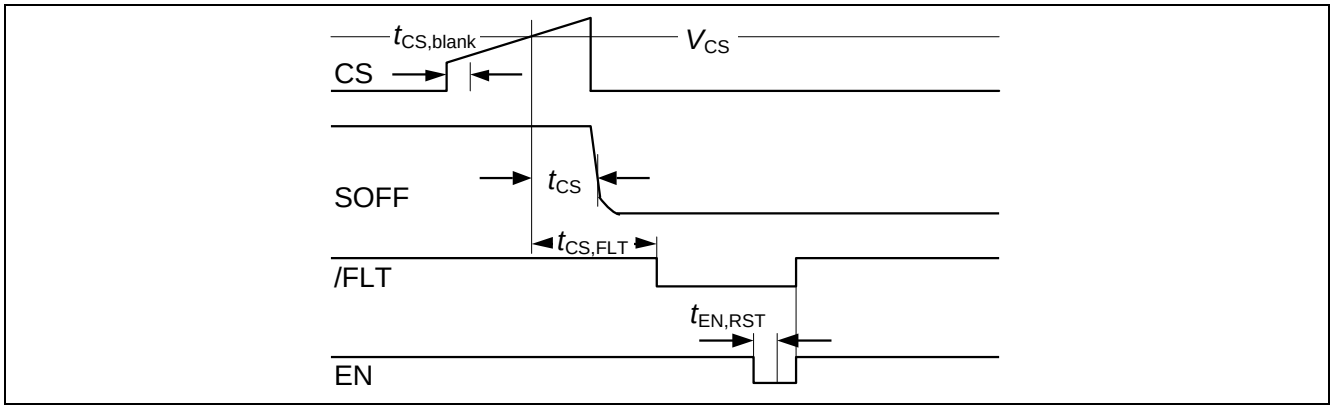


Figure 14 Timing of CS events incl. terminals SOFF, /FLT and EN

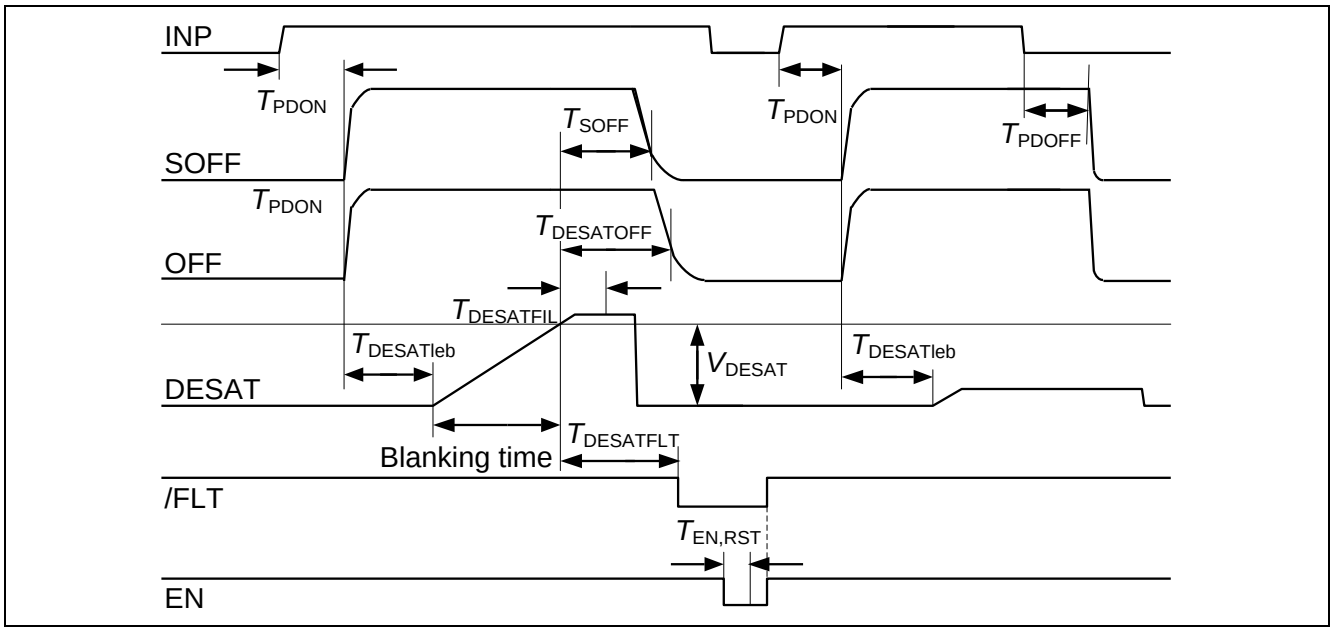


Figure 15 Timing for DESAT events incl. terminals SOFF, /FLT and EN

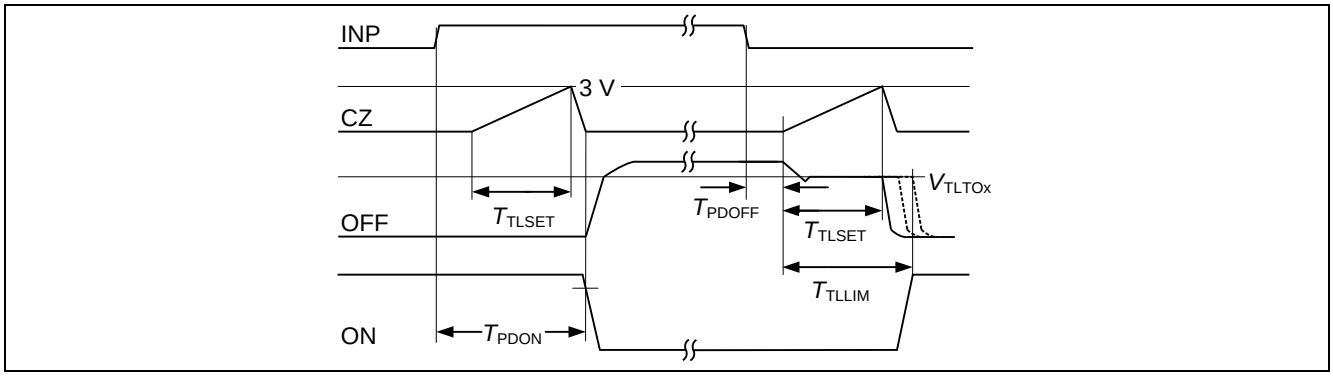
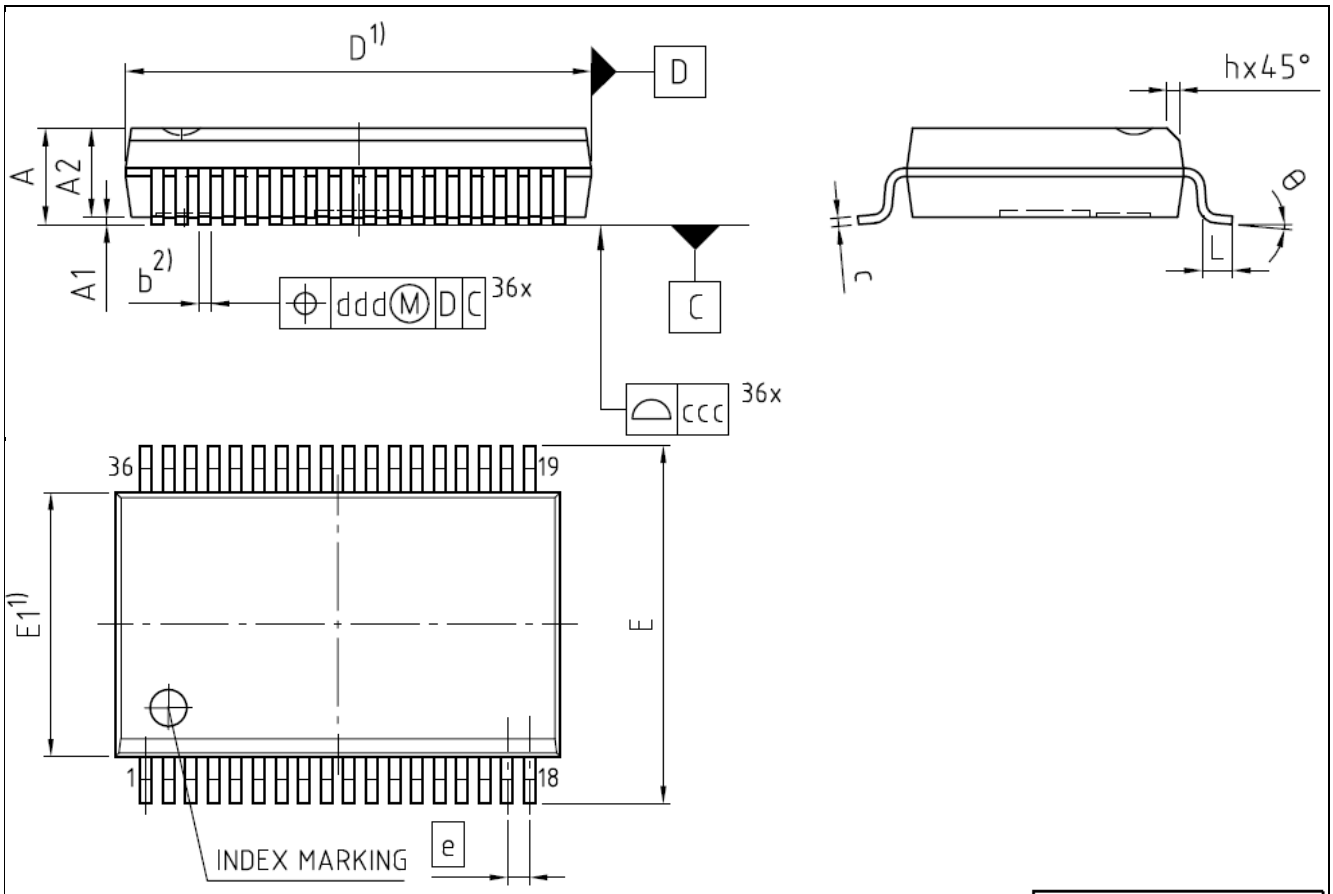


Figure 16 Timing for two-level turn-off incl. terminals CZ and OFF

8 Package

8.1 PG-DSO-36



1) DOES NOT INCLUDE PLASTIC OR METAL PROTRUSIONS OF MAX 0.15MM PER SIDE.
2) DOES NOT INCLUDE DAMBAR PROTRUSION OF MAX 0.10MM.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	2.65	-	0.104
A1	0.10	0.30	0.004	0.012
A2	2.05	2.55	0.081	0.100
b	0.22	0.41	0.009	0.016
c	0.23	0.32	0.009	0.013
D	12.60	13.00	0.496	0.512
E	10.00	10.65	0.394	0.419
E1	7.40	7.60	0.291	0.299
e	0.65 BSC		0.026 BSC	
N	36		36	
L	0.40	1.27	0.016	0.050
h	0.25	0.75	0.010	0.030
Θ	0°	8°	0°	8°
ccc	0.10		0.004	
ddd	0.18		0.007	

DOCUMENT NO.
Z8B00168162

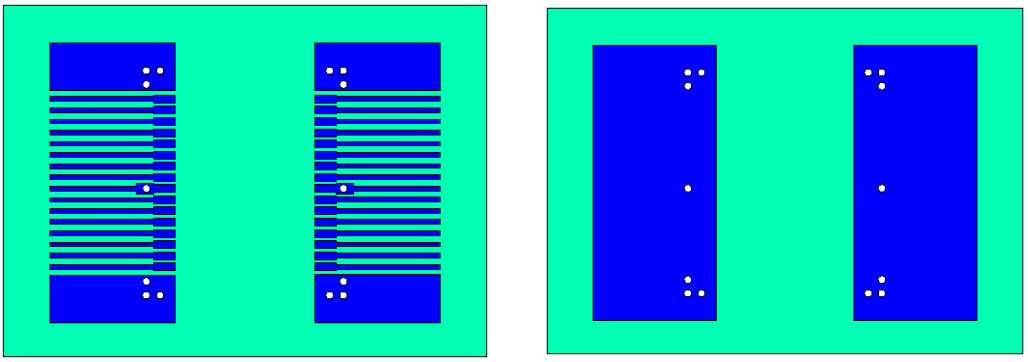
SCALE 0 2 0 2 4mm

EUROPEAN PROJECTION

ISSUE DATE
14.05.2014

REVISION
02

Figure 17 Package drawing



Dimension [mm³]	25.0 × 31.5 × 1.5	λ_{therm} [W/m·K]
Material	FR4	0.3
Metalization [µm]	35	388
Vias	∅ = 0.3 mm; plating 25 µm; 14 pcs.	
Package Attach [50µm]	Solder	55

Figure 18 PCB reference layout (left: top layer, right: bottom layer)

Thermal performance may change significantly with layout and heat dissipation of components in close proximity.

w w w . i n f i n e o n . c o m

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