Mixed-Mode Clock Manager (MMCM) Module (v1.00a)

DS737 June 24, 2009 **Product Specification**

Introduction

The MMCM primitive in Virtex-6 parts is used to generate multiple clocks with defined phase and frequency relationships to a given input clock. The MMCM module is a wrapper around the MMCM_ADV primitive that allows the MMCM to be used in the EDK tool suite.

Features

- Wrapper around the MMCM_ADV primitive
- Configurable BUFG insertion
- Supports all MMCM_BASE and some MMCM_ADV features, as applicable to embedded system designs

LogiCORE™ IP Facts				
Core Specifics				
Supported Device Family	Virtex®-6®			
Resources Used	I/O	LUTs	FFs	Block RAMs
	N/A	N/A	N/A	N/A
Version of core	1.00a			
Provided with Core				
Documentation	Product Specification			
Design File Formats	VHDL			
Constraints File	None			
Verification	None			
Instantiation Template	None			
Design Tool Requirements				
Xilinx Implementation Tools	ISE® 11x			
Verification	ModelSim PE/SE 6.4b or later			
Simulation	ModelSim PE/SE 6.4b or later			
Synthesis	XST			
Support				
Provided by Xilinx, Inc.				

Functional Description

The MMCM Module takes an input clock named CLKIN1, and generates several output clocks, each of which can be configured to have a different frequency that is dependent on the input clock frequency. The MMCM Module encapsulates the MMCM_ADV primitive. The MMCM_ADV primitive is described in the *Virtex-6 Libraries Guide* that is provided as part of the ISE tools documentation. Detailed information about the usage of the MMCM_ADV primitive is available in the *Virtex-6 User Guide*.

The MMCM Module provides optional buffers for the CLKIN1 input, and the CLKOUTn and CLKFBOUT outputs. CLKOUTn represents the seven clock outputs CLKOUT0 through CLKOUT6. The second clock input of the MMCM_ADV primitive is not used, and the clock input select input of the MMCM_ADV primitive is connected to a constant to always select the CLKIN1 signal. The dynamic reconfiguration inputs and outputs of the MMCM_ADV primitive are hidden/terminated within the MMCM module. All other inputs and outputs of the MMCM_ADV primitive are inputs and outputs of the MMCM module, with optional buffering.

In the context of an embedded processor system, the recommended usage of the MMCM module is to take a single reference clock input, and configure one or more CLKOUTn signals to produce the different clock frequencies and phases required, with the CLKOUTn and CLKFBOUT signals buffered as needed, and the CLKFBOUT signal connected back to the CLKFBIN input.

The output clock frequencies are derived from the input clock frequency, and the values of the C_DIVCLK_DIVIDE, C_CLKFBOUT_MULT and C_CLKOUTn_DIVIDE parameters, as described in the *Virtex-6 Libraries Guide*.

MMCM Module Parameters

The MMCM module is configured by selecting appropriate values for its configuration parameters, described in Table 1.

Table 1: **Configuration Parameters for MMCM Module**

Parameter Name	Description	Allowed Values	Default Value	Type
C_BANDWIDTH	This parameter passes the value to the equivalent attribute of the MMCM_ADV	Same as MMCM_ADV	OPTIMIZED	string
C_CLKFBOUT_BUF	If C_CLKFBOUT_BUF = true, a BUFG is inserted between the CLKFBOUT pin of the MMCM_ADV primitive and CLKFBOUT output	true, false	false	Boolean
C_CLKFBOUT_ USE_FINE_PS	This parameter passes the value to the equivalent attribute of the MMCM_ADV	true, false	false	Boolean
C_CLKFBOUT_MULT_F	This parameter passes the value to the equivalent attribute of the MMCM_ADV	Same as MMCM_ADV	1.000	real
C_CLKFBOUT_PHASE	This parameter passes the value to the equivalent attribute of the MMCM_ADV	Same as MMCM_ADV	0.000	real
C_CLKIN1_BUF	If C_CLKIN1_BUF = true, a BUFG is inserted between the CLKIN1 input and the CLKIN1 pin of the MMCM_ADV primitive	true, false	false	Boolean

Table 1: **Configuration Parameters for MMCM Module *(Cont'd)***

Parameter Name	Description	Allowed Values	Default Value	Type
C_CLKIN1_PERIOD	This parameter passes the value to the equivalent attribute of the MMCM_ADV	Same as MMCM_ADV	0.000	real
C_CLKOUT0_BUF... C_CLKOUT6_BUF	If C_CLKOUTn_BUF = true, a BUFG is inserted between the CLKOUTn pin of the MMCM_ADV primitive and CLKOUTn output	true, false	false	Boolean
C_CLKOUT0_USE_FINE_PS... C_CLKOUT6_USE_FINE_PS	This parameter passes the value to the equivalent attribute of the MMCM_ADV	true, false	false	Boolean
C_CLKOUT0_DIVIDE_F	This parameter passes the value to the equivalent attribute of the MMCM_ADV	Same as MMCM_ADV	1.000	real
C_CLKOUT1_DIVIDE... C_CLKOUT6_DIVIDE	This parameter passes the value to the equivalent attribute of the MMCM_ADV	Same as MMCM_ADV	1	integer
C_CLKOUT0_DUTY_CYCLE... C_CLKOUT6_DUTY_CYCLE	This parameter passes the value to the equivalent attribute of the MMCM_ADV	Same as MMCM_ADV	0.500	real
C_CLKOUT0_PHASE... C_CLKOUT6_PHASE	This parameter passes the value to the equivalent attribute of the MMCM_ADV	Same as MMCM_ADV	0.000	real
CLKOUT4_CASCADE	This parameter passes the value to the equivalent attribute of the MMCM_ADV	true, false	false	Boolean
C_COMPENSATION	This parameter passes the value to the equivalent attribute of the MMCM_ADV	Same as MMCM_ADV	ZHOLD	string
C_DIVCLK_DIVIDE	This parameter passes the value to the equivalent attribute of the MMCM_ADV	Same as MMCM_ADV	1	integer
C_REF_JITTER1	This parameter passes the value to the equivalent attribute of the MMCM_ADV	Same as MMCM_ADV	0.010	real
CLOCK_HOLD	This parameter passes the value to the equivalent attribute of the MMCM_ADV	true, false	false	Boolean
STARTUP_WAIT	This parameter passes the value to the equivalent attribute of the MMCM_ADV	true, false	false	Boolean
C_EXT_RESET_HIGH	IF C_EXT_RESET_HIGH = 0, the RST signal is inverted before connecting to the MMCM_ADV	0,1	1	integer
C_FAMILY	Target FPGA family	virtex6	virtex6	string

Allowable Parameter Combinations

The MMCM module has the same restrictions on parameter combinations that are documented for the MMCM_ADV primitive in the *Virtex-6 User Guide and* Virtex-6 Libraries Guide.

Note: The MMCM Module wrapper does not perform any error checking to enforce the design rules and restrictions described in the *Virtex-6 User Guide*.

MMCM Module I/O Signals

The input and output signals of the MMCM module are described in Table 2.

Table 2: **MMCM Module Input and Output Signals**

Signal	Signal Direction	Default Value	Description
CLKFBOUT	Output		Feedback clock output (typically to be connected to CLKFBIN)
CLKFBOUTB	Output		Inverted feedback clock output
CLKOUT0... CLKOUT6	Output		Clock output
CLKOUT0B... CLKOUT3B	Output		Inverted clock output
LOCKED	Output		MMCM Locked signal
CLKFBSTOPPED	Output		Status pin indicating that the feedback clock has stopped
CLKINSTOPPED	Output		Status pin indicating that the input clock has stopped
PSDONE	Output		Phase shift done
CLKFBIN	Input	Same as MMCM_ADV primitive	Clock feedback input
CLKIN1	Input		Primary clock input
RST	Input		Asynchronous global reset signal
PWRDWN	Input		MMCM global power down pin
PSCLK	Input		Phase shift clock
PSEN	Input		Phase shift enable
PSINCDEC	Input		Phase shift Increment/Decrement control

Register Descriptions

Not Applicable.

Timing Diagrams

See the *Virtex-6 User Guide* for more information.

Design Constraints

None.

Design Implementation

Target Technology

This module is intended for use on Virtex-6 devices.

Device Utilization and Performance Benchmarks

Core Performance

This module uses one MMCM primitive and one BUFG primitive for each clock input and output that is buffered.

Specification Exceptions

USB 2.0

Not Applicable.

Reference Documents

1. Virtex-6 User Guide
2. *Virtex-6 Libraries Guide for HDL Designs*

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
6/24/09	1.0	Initial Xilinx release.

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