KERSMI ELECTRONIC CO.,LTD. **800V**

Description

This MOSFETS use advanced trench technology and design to provide excellent RDS(on) with low gate charge. It can be used in a wide variety of applications.

SYMBOL	PARAMETER	MAX	MAX	MAX	UNIT
	-----	TYN610	TYN612	TYN812	
V_{DRM}	Repetitive peak off-state	600	600	800	V
ID	RMS on-state current	10	12	12	A

Features

1) Low gate charge.
2) Green device available.
3) Advanced high cell denity trench technology for ultra RDS(ON)
4) Excellent package for good heat dissipation.

TO-220

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance ,Junction to Case1	60	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient1	2.5	

Package Marking and Ordering Information

Part NO.	Marking	Package
TYN812	TYN812	TO-220

Notes:

1. The data tested by surface mounted on a 1 inch² FR-4 board 2OZ copper.
2. The data tested by pulse width≤300us,duty cycle≤2%
3. The EAS data shows Max.rating.The test condition is V_{DD}=25v,V_{GS}=10V,L=0.1mH,i_{AS}=17.8A
4. The power dissipation is limited by 150℃ junction temperature.

Typical Characteristics T_J=25℃ unless otherwise noted

Table 3: Absolute Ratings (limiting values)

Symbol	Parameter			Value		Unit
				TN12-G TYN12	TN12-B/H TS12-B/H	
$I_{T(RMS)}$	RMS on-state current (180° conduction angle)		T_c = 105°C	12		A
$IT_{(AV)}$	Average on-state current (180° conduction angle)		T_c = 105°C	8		A
I_{TSM}	Non repetitive surge peak on-state current	t_p = 8.3 ms	T_j = 25°C	145	115	A
		t_p = 10 ms		140	110	
I^2t	I^2t Value for fusing	t_p = 10 ms	T_j = 25°C	98	60	A^2s
dI/dt	Critical rate of rise of on-state current I_G = 2 x I_{GT} , t_r ≤ 100 ns	F = 60 Hz	T_j = 125°C	50		A/µs
I_{GM}	Peak gate current	t_p = 20 µs	T_j = 125°C	4		A
$P_{G(AV)}$	Average gate power dissipation		T_j = 125°C	1		W
T_{stg} T_j	Storage junction temperature range Operating junction temperature range			- 40 to + 150 - 40 to + 125		°C
V_{RGM}	Maximum peak reverse gate voltage (for **TN12** & **TYN12** only)			5		V

■ SENSITIVE

Symbol	Test Conditions			TS1220	Unit
I_{GT}	V_D = 12 V R_L = 140 Ω		MAX.	200	µA
V_{GT}			MAX.	0.8	V
V_{GD}	$V_D = V_{DRM}$ R_L = 3.3 kΩ R_{GK} = 1 kΩ	T_j = 125°C	MIN.	0.1	V
V_{RG}	I_{RG} = 10 µA		MIN.	8	V
I_H	I_T = 50 mA R_{GK} = 1 kΩ		MAX.	5	mA
I_L	I_G = 1 mA R_{GK} = 1 kΩ		MAX.	6	mA
dV/dt	V_D = 65 % V_{DRM} R_{GK} = 220 Ω	T_j = 125°C	MIN.	5	V/µs
V_{TM}	I_{TM} = 24 A tp = 380 µs	T_j = 25°C	MAX.	1.6	V
V_{t0}	Threshold voltage	T_j = 125°C	MAX.	0.85	V
R_d	Dynamic resistance	T_j = 125°C	MAX.	30	mΩ
I_{DRM} I_{RRM}	$V_{DRM} = V_{RRM}$ R_{GK} = 220 Ω	T_j = 25°C	MAX.	5	µA
		T_j = 125°C		2	mA

■ STANDARD

Symbol	Test Conditions			TN1215		TYN		Unit
				B / H	G	x12T	x12	
I_{GT}	V_D = 12 V R_L = 33 Ω		MIN.	2		0.5	2	mA
			MAX.	15		5	15	
V_{GT}			MAX.	1.3				V
V_{GD}	$V_D = V_{DRM}$ R_L = 3.3 kΩ	T_j = 125°C	MIN.	0.2				V
I_H	I_T = 500 mA Gate open		MAX.	40	30	15	30	mA
I_L	I_G = 1.2 I_{GT}		MAX.	80	60	30	60	mA
dV/dt	V_D = 67 % V_{DRM} Gate open	T_j =125°C	MIN.	200		40	200	V/µs
V_{TM}	I_{TM} = 24 A t_p = 380 µs	T_j = 25°C	MAX.	1.6				V
V_{t0}	Threshold voltage	T_j = 125°C	MAX.	0.85				V
R_d	Dynamic resistance	T_j = 125°C	MAX.	30				mΩ
I_{DRM} I_{RRM}	$V_{DRM} = V_{RRM}$	T_j = 25°C	MAX.	5				µA
		T_j = 125°C		2				mA

Symbol	Parameter			Value	Unit
$R_{th(j-c)}$	Junction to case (DC)			1.3	°C/W
$R_{th(j-a)}$	Junction to ambient (DC)	S = 0.5 cm²	DPAK	70	°C/W
		S = 1 cm²	D^2PAK	45	
			IPAK	100	
			TO-220AB	60	

S = Copper surface under tab.

Figure 1: Maximum average power dissipation versus average on-state current

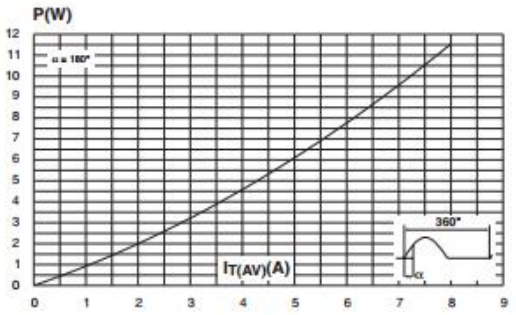

Figure 2: Average and D.C. on-state current versus case temperature

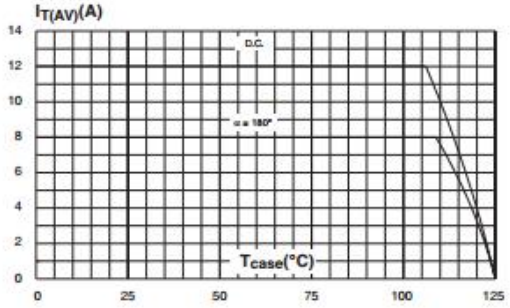

Figure 3: Average and D.C. on-state current versus ambient temperature (device mounted on FR4 with recommended pad layout) (DPAK)

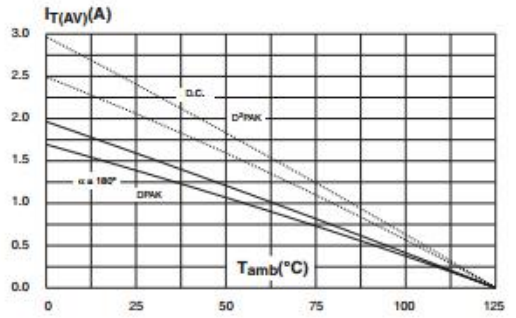

Figure 4: Relative variation of thermal impedance junction to case versus pulse duration

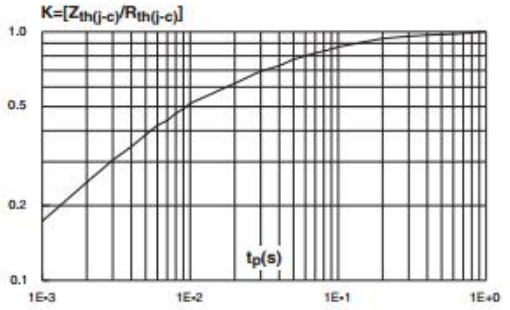

Figure 5: Relative variation of thermal impedance junction to ambient versus pulse duration (recommended pad layout, FR4 PC board for DPAK)

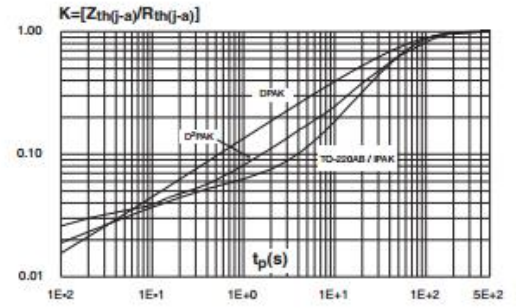

Figure 6: Relative variation of gate trigger current and holding current versus junction temperature for TS8 series

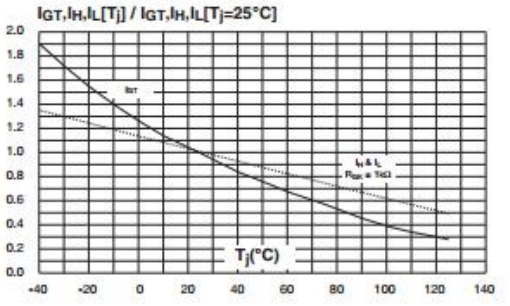

Figure 7: Relative variation of gate trigger current and holding current versus junction temperature for TN8 & TYN08 series

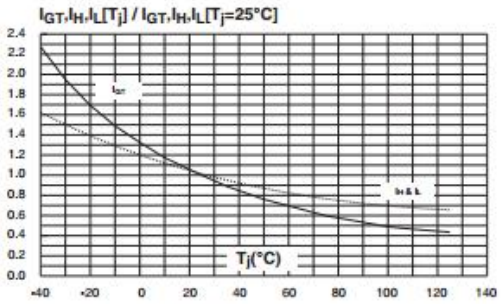

Figure 8: Relative variation of holding current versus gate-cathode resistance (typical values) for TS8 series

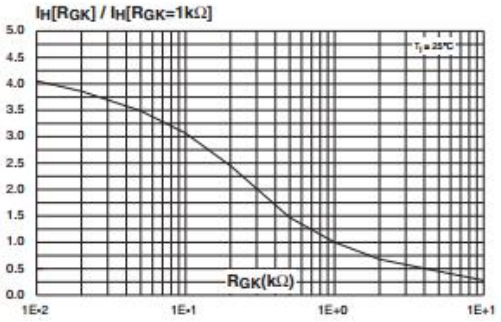

Figure 9: Relative variation of dV/dt immunity versus gate-cathode resistance (typical values) for TS8 series

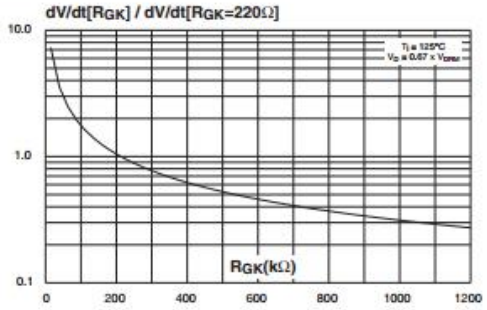

Figure 10: Relative variation of dV/dt immunity versus gate-cathode capacitance (typical values) for TS8 series

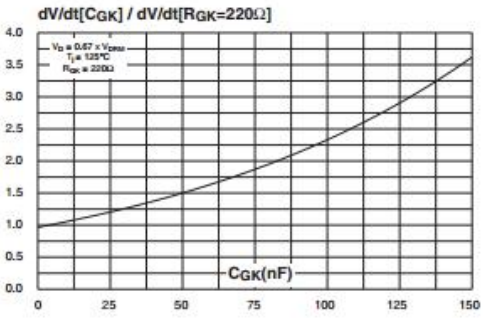

Figure 11: Surge peak on-state current versus number of cycles

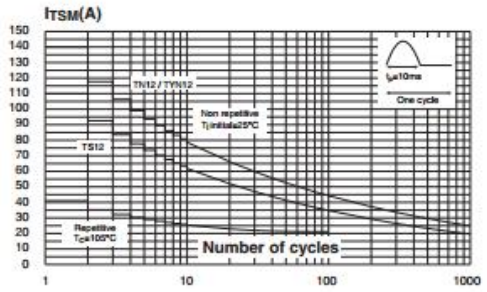

Figure 12: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp < 10 ms, and corresponding values of I²t