

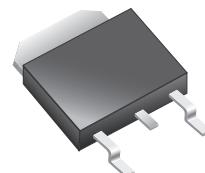
RoHS Compliant Product  
A suffix of "-C" specifies halogen free

## DESCRIPTION

SSD14N02E is the best-performance trench N-ch MOSFETs with extreme high cell density, which provides excellent  $R_{DS(ON)}$  and gate charge for most of the synchronous buck converter applications.

SSD14N02E meets the RoHS and Green Product requirement with full function reliability approved.

**TO-252(D-Pack)**



## FEATURES

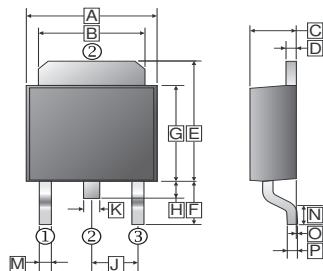
- Advanced high cell density Trench technology
- Super low gate charge
- Excellent CdV/dt effect decline
- ESD protection
- Green device available

## MARKING

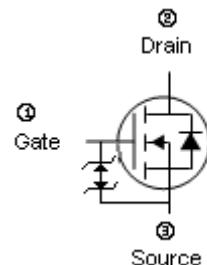


## PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.35	6.90	J	2.336	REF.
B	4.95	5.50	K	0.89	REF.
C	2.10	2.50	M	0.50	1.14
D	0.43	0.9	N	1.3	1.8
E	6.0	7.5	O	0	0.13
F	2.90	REF.	P	0.58	REF.
G	5.40	6.40			
H	0.60	1.20			



## ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current@ $V_{GS}=4.5\text{V}^1$	$I_D$	14.7	A
$T_A=70^\circ\text{C}$		11.6	
Pulsed Drain Current <sup>3</sup>	$I_{DM}$	20	A
Total Power Dissipation@ $T_A=25^\circ\text{C}$	$P_D$	6.3	W
Thermal Resistance from Junction to Ambient <sup>1</sup>	$R_{\theta JA}$	20	$^\circ\text{C} / \text{W}$
Steady State		62.5	
Thermal Resistance from Junction to Ambient		110	
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~150	°C

**ELECTRICAL CHARACTERISTICS** ( $T_J=25^\circ\text{C}$  unless otherwise specified)

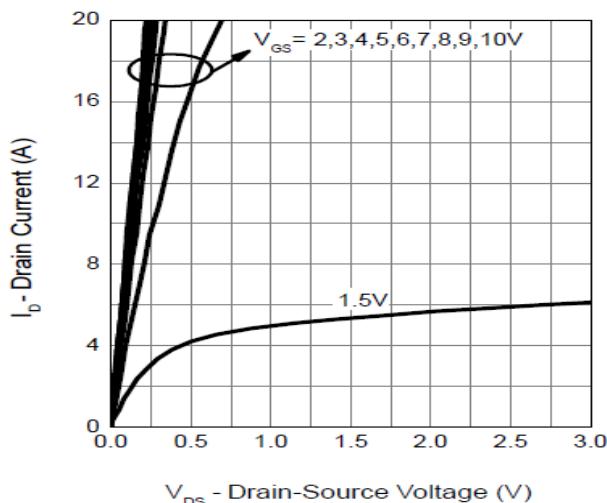
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	20	-	-	V	$\text{V}_{\text{GS}}=0, \text{I}_D=250\mu\text{A}$
Drain-Source Leakage Current	$\text{I}_{\text{DSS}}$	-	-	1	$\mu\text{A}$	$\text{V}_{\text{DS}}=16\text{V}, \text{V}_{\text{GS}}=0, \text{T}_J=25^\circ\text{C}$
		-	-	30		$\text{V}_{\text{DS}}=16\text{V}, \text{V}_{\text{GS}}=0, \text{T}_J=85^\circ\text{C}$
Gate-Source Leakage Current	$\text{I}_{\text{GSS}}$	-	-	$\pm 10$	$\mu\text{A}$	$\text{V}_{\text{DS}}=0\text{V}, \text{V}_{\text{GS}}= \pm 10\text{V}$
Gate-Threshold Voltage	$\text{V}_{\text{GS}(\text{th})}$	0.5	0.7	1.2	V	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_D=250\mu\text{A}$
Static Drain-Source On-Resistance <sup>2</sup>	$\text{R}_{\text{DS}(\text{ON})}$	-	-	19.5	$\text{m}\Omega$	$\text{V}_{\text{GS}}=4.5\text{V}, \text{I}_D=10\text{A}$
		-	-	26.5		$\text{V}_{\text{GS}}=2.5\text{V}, \text{I}_D=5\text{A}$
Input Capacitance	$\text{C}_{\text{iss}}$	-	630	-	$\text{pF}$	$\text{V}_{\text{DS}}=15\text{V}$ $\text{V}_{\text{GS}}=0$ $f=1\text{MHz}$
Output Capacitance	$\text{C}_{\text{oss}}$	-	105	-		
Reverse Transfer Capacitance	$\text{C}_{\text{rss}}$	-	100	-		
Total Gate Charge	$\text{Q}_g$	-	12	-	$\text{nC}$	$\text{V}_{\text{DS}}=10\text{V}$ $\text{V}_{\text{GS}}=4.5\text{V}$ $\text{I}_D=10\text{A}$
Gate-Source Charge	$\text{Q}_{\text{gs}}$	-	1.4	-		
Gate-Drain ("Miller") Charge	$\text{Q}_{\text{gd}}$	-	4.4	-		
Turn-on Delay Time	$\text{T}_{\text{d}(\text{on})}$	-	5	-		
Rise Time	$\text{T}_r$	-	9	-	$\text{nS}$	$\text{V}_{\text{DD}}=10\text{V}$ $\text{V}_{\text{GS}}=4.5\text{V}$ $\text{R}_G=6\Omega$ $\text{R}_L=10\Omega$ $\text{I}_D=1\text{A}$
Turn-off Delay Time	$\text{T}_{\text{d}(\text{off})}$	-	25	-		
Fall Time	$\text{T}_f$	-	5	-		
Source-Drain Diode Characteristics						
Diode Forward Voltage <sup>2</sup>	$\text{V}_{\text{SD}}$	-	-	1.3	V	$\text{I}_s=1.3\text{A}, \text{V}_{\text{GS}}=0$
Continuous Source Current <sup>1,4</sup>	$\text{I}_s$	-	-	14.7	A	$\text{V}_G=\text{V}_D=0\text{V}, \text{Force Current}$
Pulsed Source Current <sup>2,4</sup>	$\text{I}_{\text{SM}}$	-	-	20	A	
Reverse Recovery Time	$\text{T}_{\text{RR}}$	-	16	-	nS	$\text{I}_F=10\text{A}, \text{dI}/\text{dt}=100\text{A}/\mu\text{s}, \text{T}_J=25^\circ\text{C}$
Reverse Recovery Charge	$\text{Q}_{\text{RR}}$	-	10	-	nC	

Notes:

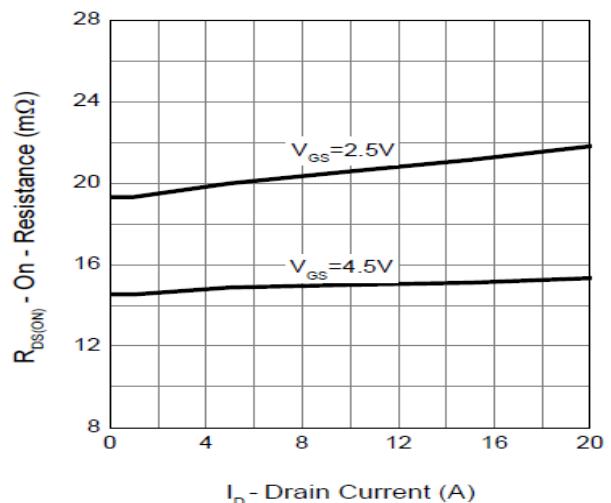
1. The data is tested when the surface of the device is mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data is tested by the pulse: Pulse width $\leq 300\mu\text{s}$ , duty cycle $\leq 2\%$ .
3. The Power dissipation is limited by 150°C junction temperature.
4. The data is theoretically the same as  $\text{I}_D$  and  $\text{I}_{\text{DM}}$ , in real applications, the data should be limited by the total power dissipation.

## CHARACTERISTIC CURVE

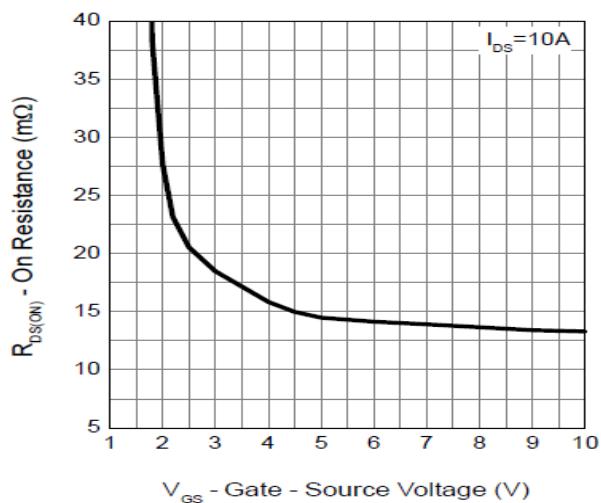
Output Characteristics



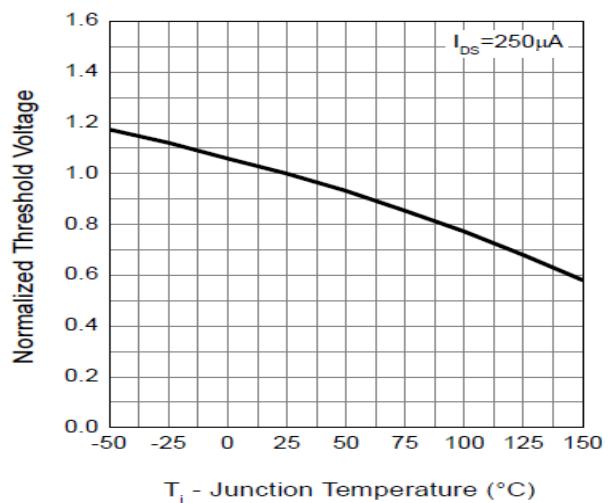
Drain-Source On Resistance



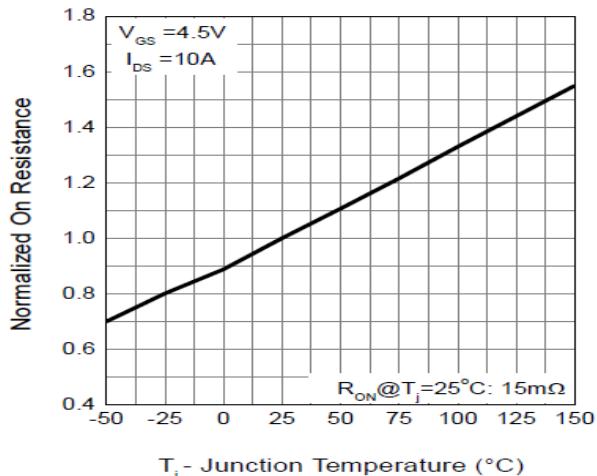
Gate-Source On Resistance



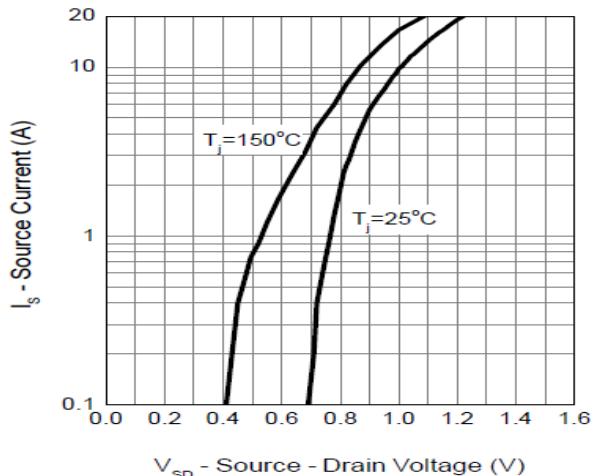
Gate Threshold Voltage



Drain-Source On Resistance

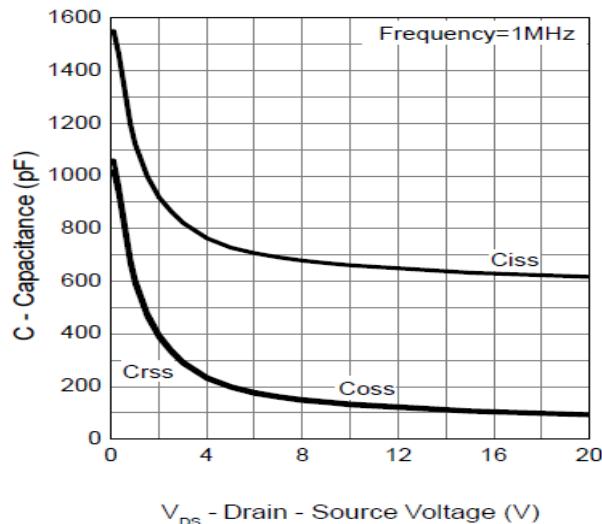


Source-Drain Diode Forward

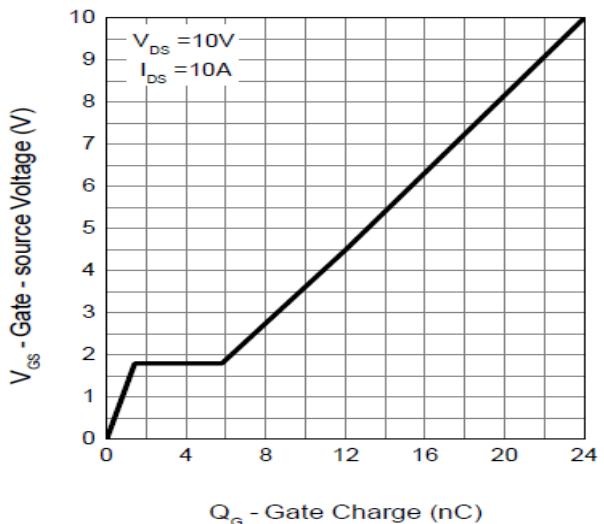


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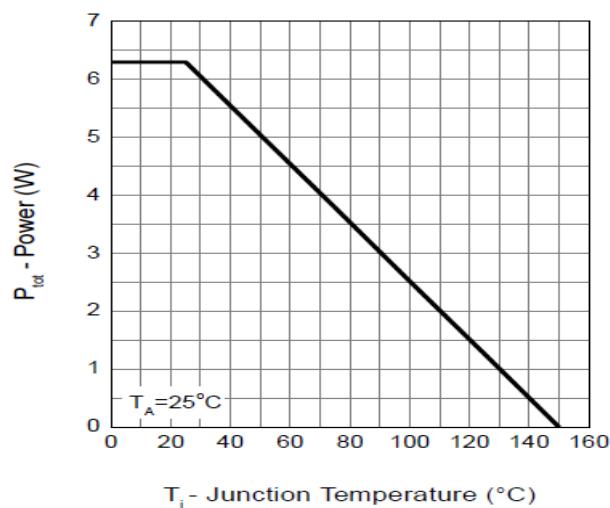
### Capacitance



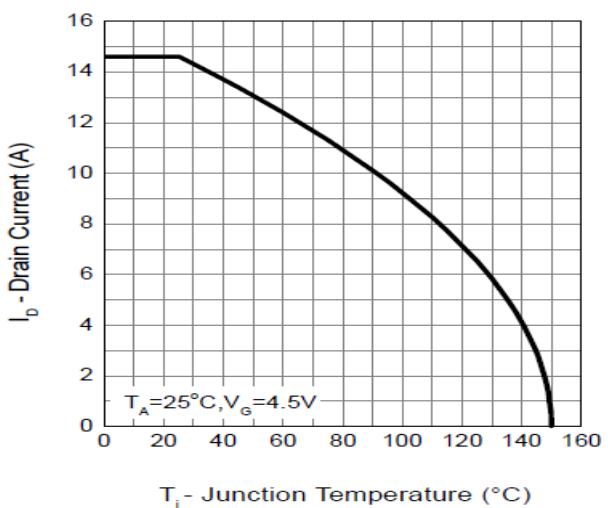
### Gate Charge



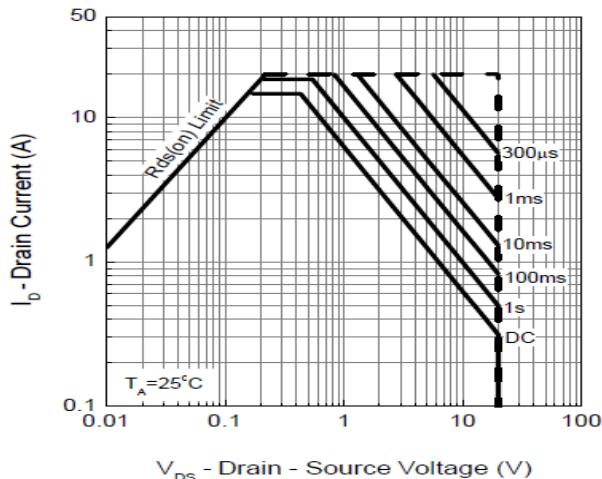
### Power Dissipation



### Drain Current



### Safe Operation Area



### Thermal Transient Impedance

