To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS FIELD EFFECT TRANSISTOR
μPA2706GR

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The μPA2706GR is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

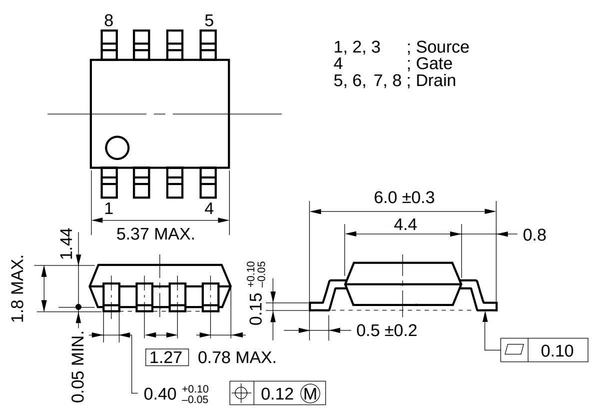
FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 15 mΩ MAX. (V_{GS} = 10 V, I_D = 5.5 A)
  $R_{DS(on)2}$ = 22.5 mΩ MAX. (V_{GS} = 4.5 V, I_D = 5.5 A)
- Low C_{iss}: C_{iss} = 660 pF TYP. (V_{DS} = 10 V, V_{GS} = 0 V)
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA2706GR	Power SOP8

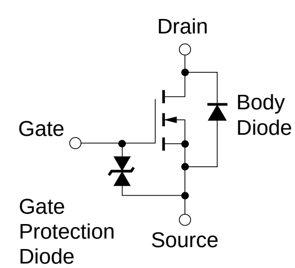
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±11	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±44	A
Total Power Dissipation (T_A = 25°C) Note2	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to + 150	°C
Single Avalanche Current Note3	I_{AS}	11	A
Single Avalanche Energy Note3	E_{AS}	12.1	mJ

EQUIVALENT CIRCUIT



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%
2. Mounted on ceramic substrate of 1200 mm^2 x 2.2 mm
3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω, L = 100 μH, V_{GS} = 20 → 0 V

Caution Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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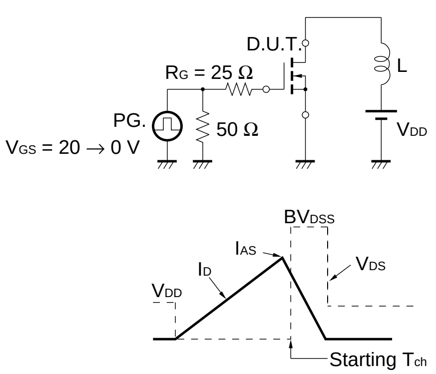
Date Published April 2003 NS CP(K)
Printed in Japan

ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

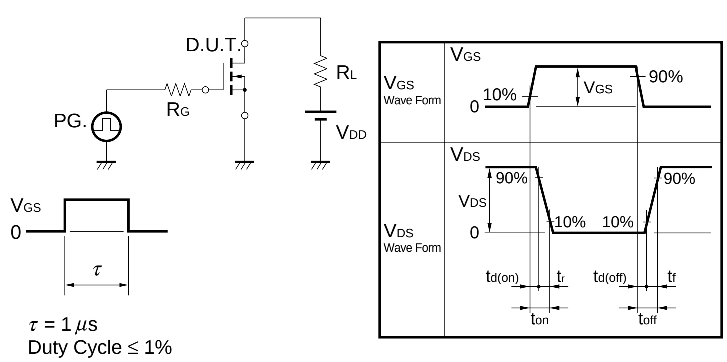
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5		2.5	V
Forward Transfer Admittance Note	$\| y_{fs} \|$	V_{DS} = 10 V, I_D = 5.5 A	4.5			S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 5.5 A		11	15	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 5.5 A		16	22.5	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.0 V, I_D = 5.5 A		19	29	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		660		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		270		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		83		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15 V, I_D = 5.5 A		9		ns
Rise Time	t_r	V_{GS} = 10 V		5		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		29		ns
Fall Time	t_f			6		ns
Total Gate Charge	Q_G	V_{DD} = 15 V		7.1		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 5 V		2.1		nC
Gate to Drain Charge	Q_{GD}	I_D = 11 A		3.1		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 11 A, V_{GS} = 0 V		0.84		V
Reverse Recovery Time	t_{rr}	I_F = 11 A, V_{GS} = 0 V		25		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		17		nC

Note Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2%

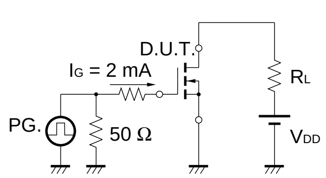
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

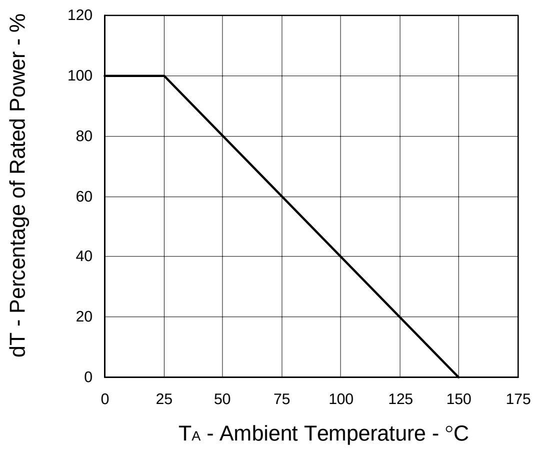


TEST CIRCUIT 3 GATE CHARGE

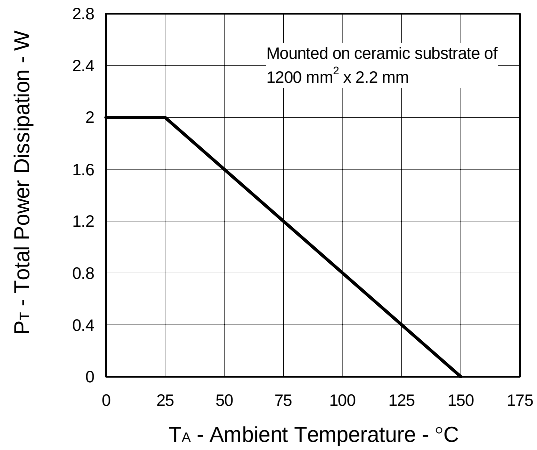


TYPICAL CHARACTERISTICS (T_A = 25°C)

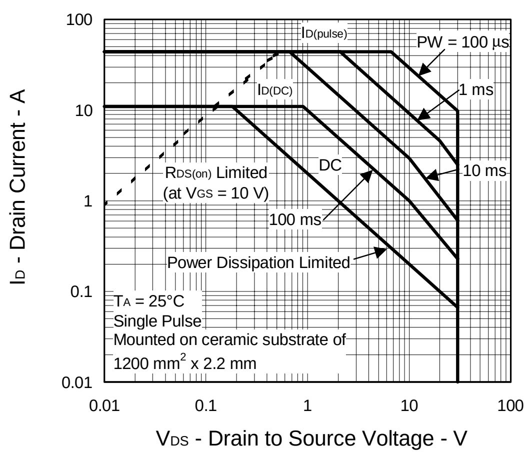
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



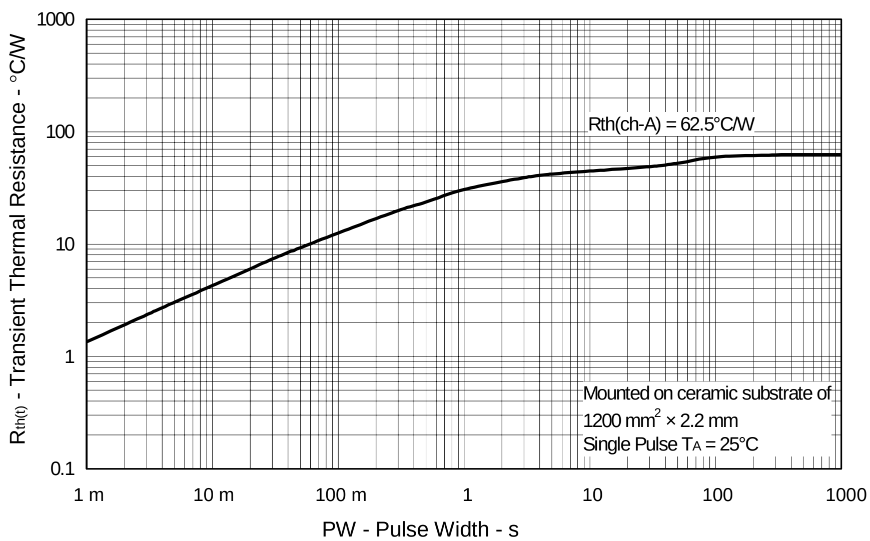
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



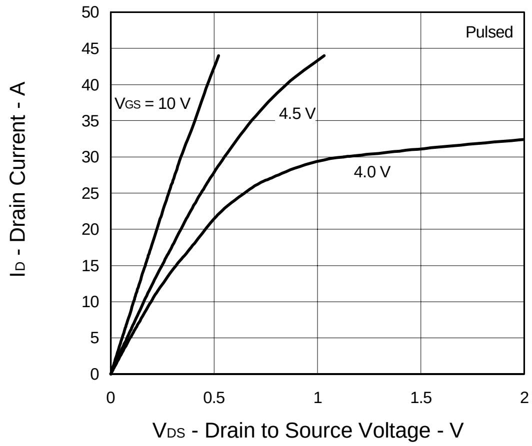
FORWARD BIAS SAFE OPERATING AREA



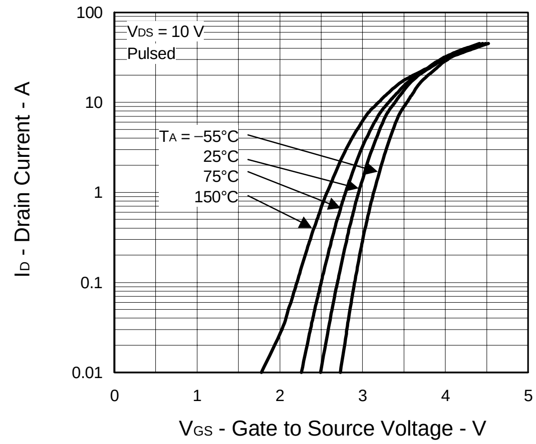
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



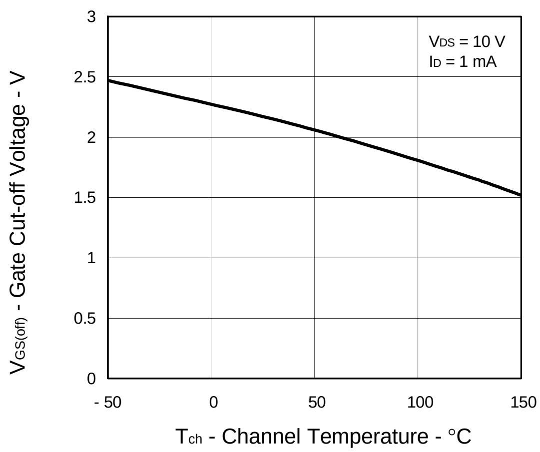
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



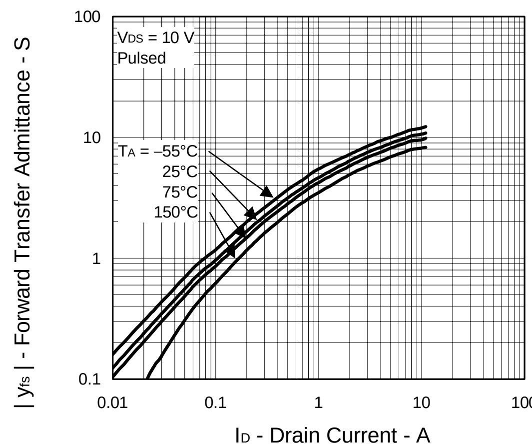
FORWARD TRANSFER CHARACTERISTICS



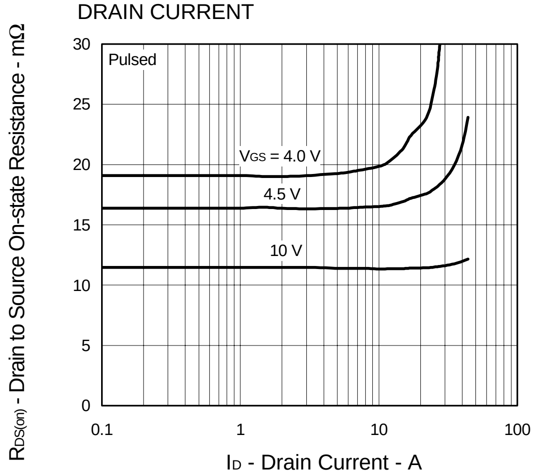
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



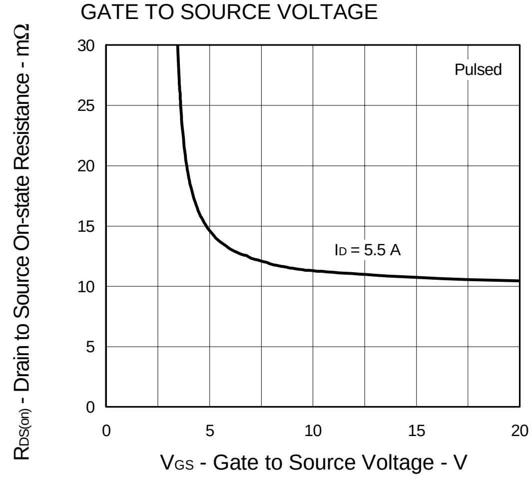
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



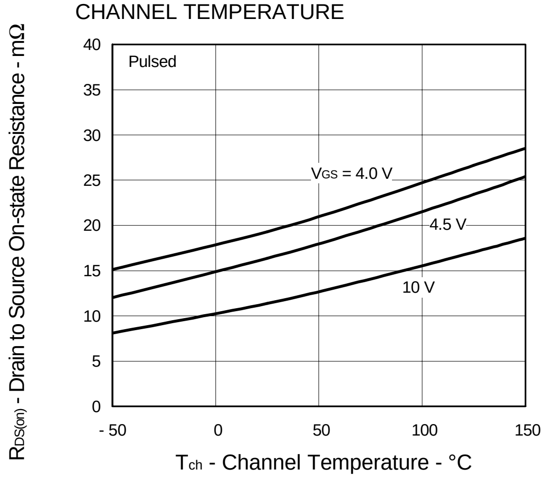
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



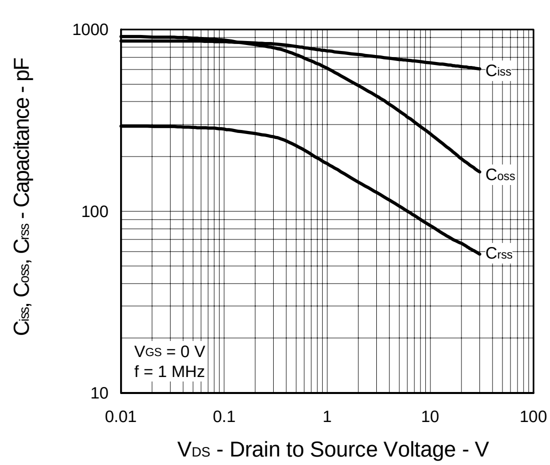
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



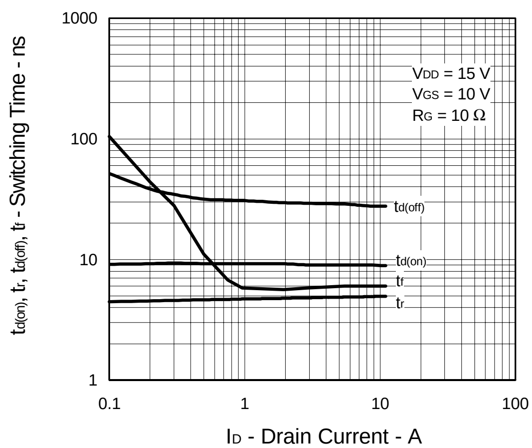
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



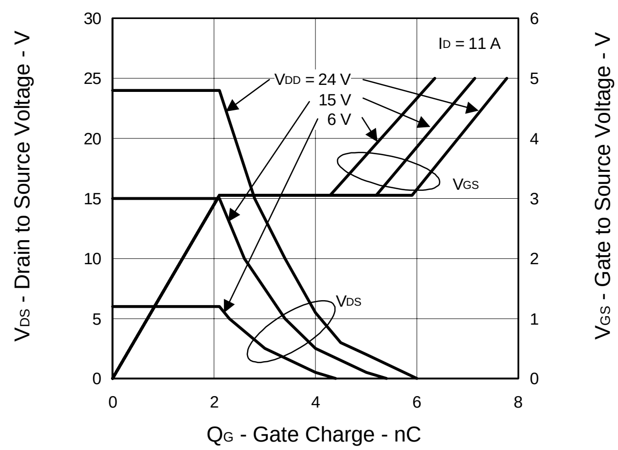
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



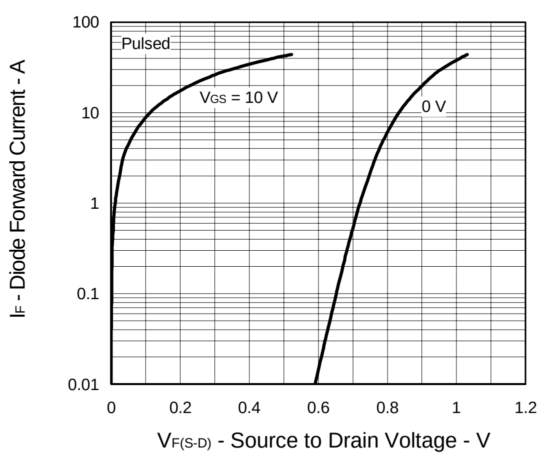
SWITCHING CHARACTERISTICS



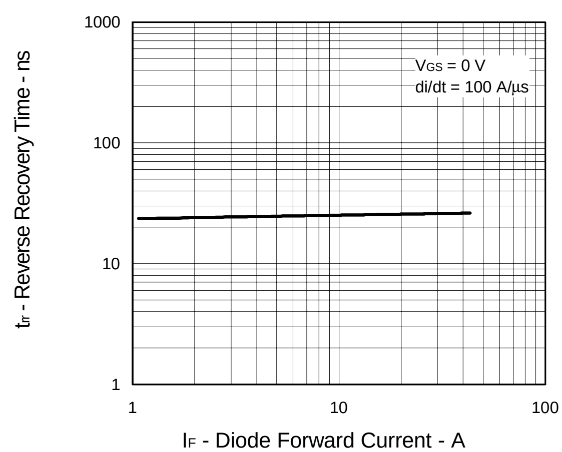
DYNAMIC INPUT/OUTPUT CHARACTERISTICS

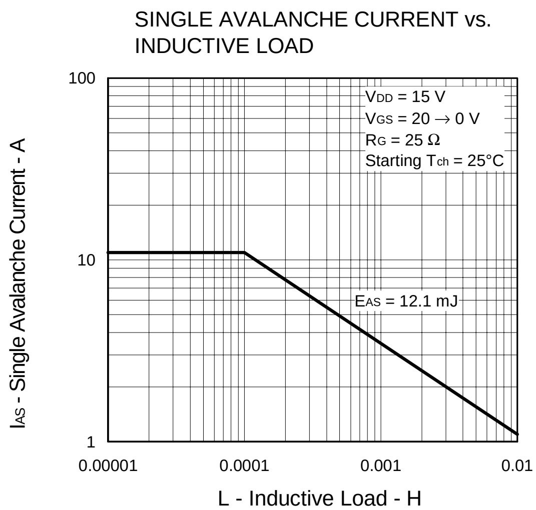


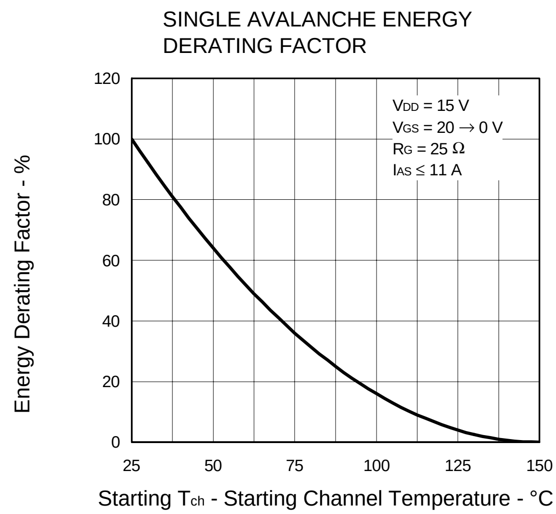
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT




SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD
VDD = 15 V
VGS = 20 → 0 V
RG = 25 Ω
Starting Tch = 25°C
EAS = 12.1 mJ
IAS - Single Avalanche Current - A
100
10
1
0.00001
0.0001
0.001
0.01
L - Inductive Load - H


SINGLE AVALANCHE ENERGY
DERATING FACTOR
VDD = 15 V
VGS = 20 → 0 V
RG = 25 Ω
IAS ≤ 11 A
Energy Derating Factor - %
120
100
80
60
40
20
0
25
50
75
100
125
150
Starting Tch - Starting Channel Temperature - °C