## FEATURES

- Ideal for Server Memory applications using +5V
- Fixed 5V Gate Drive
- Large drivers designed to drive 3nF in ≤ 15ns with +5V drive
  - Low-side driver – 2A source/4A sink
  - High-side driver – 2A source/2A sink
  - Transitions times & Propagation delays ≤ 15ns
- Integrated bootstrap diode
- Capable of high switching frequencies from 200kHz up to greater than 1MHz
- Compatible with IR's patented Active Tri-Level (ATL) PWM for fastest response to transient overshoot
- Non-overlap and under voltage protection
- Thermally enhanced 10-pin DFN package
- Lead free RoHS compliant package
- Low Quiescent power to optimize efficiency

## APPLICATIONS

- Multiphase synchronous buck converter for Server CPUs and DDR Memory VR solutions
- High efficiency and compact VRM
- Optimized for Sleep state S3 systems using +5VSB
- Notebook Computer and Graphics VR solutions

## DESCRIPTION

The CHL8505 MOSFET is a high-efficiency gate driver which can switch both high-side and low-side N-channel external MOSFETs in a synchronous buck converter. It is intended for use with IR Digital PWM controllers to provide a total voltage regulator (VR) solution for today's advanced computing applications.

The CHL8505 driver is capable of rapidly switching large MOSFETs with low $R_{dson}$ and large input capacitance used in high-efficiency designs. It is uniquely designed to operate from a 5V source such as a system 5V or 5V standby voltages in sleep states.

The CHL8505 has a unique circuit which improves drive strength to the external MOSFETs even with just 5V supplied at the VDRV pin. This insures faster switching comparable to drivers designed for +12V drive operation. The integrated boot diode reduces external component count. The CHL8505 also features an adaptive non-overlap control for shoot-through protection.

The CHL8505 is configured to drive both the high and low-side switches from the patented IR fast Active Tri-Level (ATL) PWM signal, which will optimize the turn off time of individual phases, optimizing transient performance.

## BASIC APPLICATION

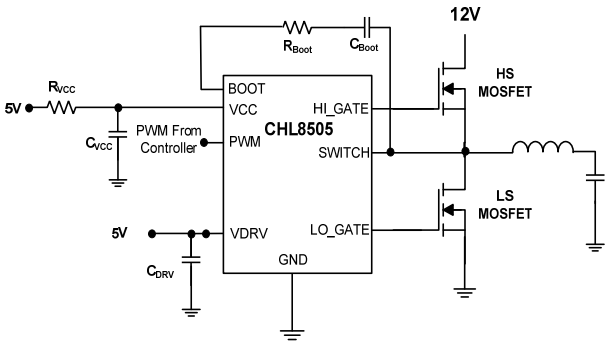



Figure 1: CHL8505 Basic Application Circuit

## PIN DIAGRAM

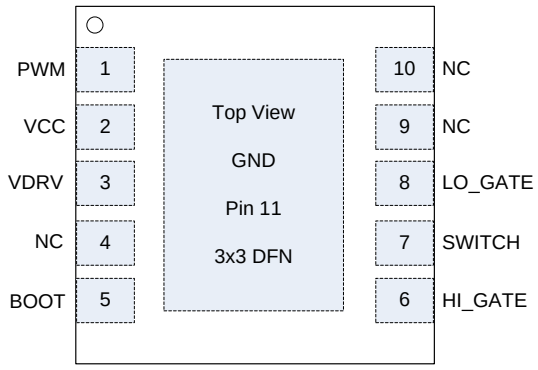
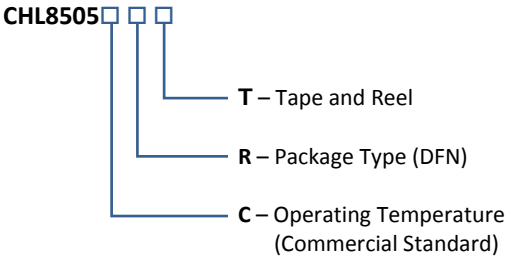



Figure 2: CHL8505 Package Top View

## ORDERING INFORMATION




| Package | Tape & Reel Qty | Part Number |
|---|---|---|
| **DFN** | 3000 | **CHL8505CRT** |

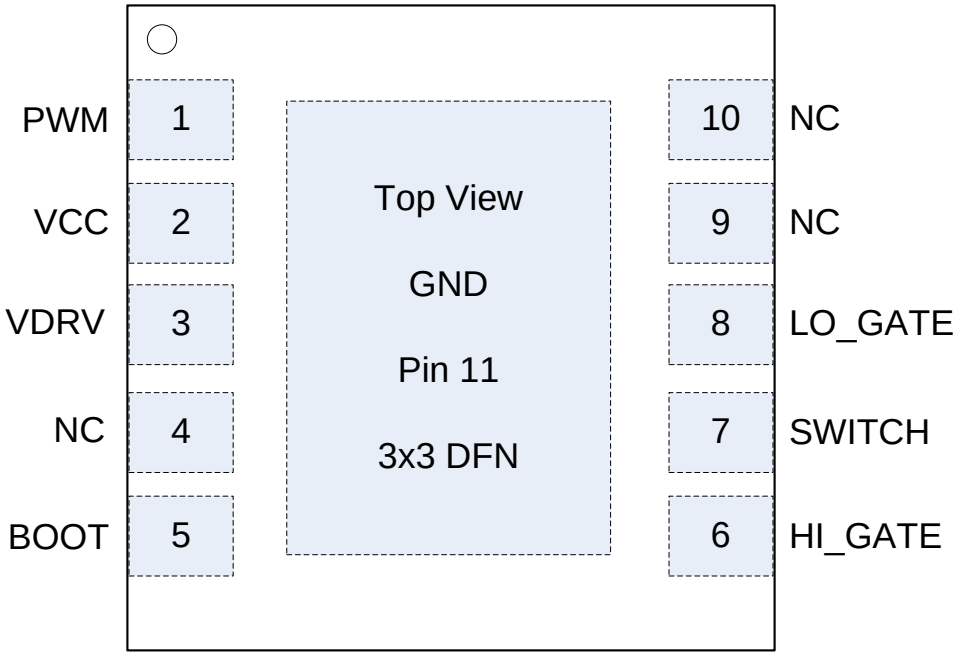



**Figure 3: CHL8505 Pin Diagram Enlarged**

## FUNCTIONAL BLOCK DIAGRAM

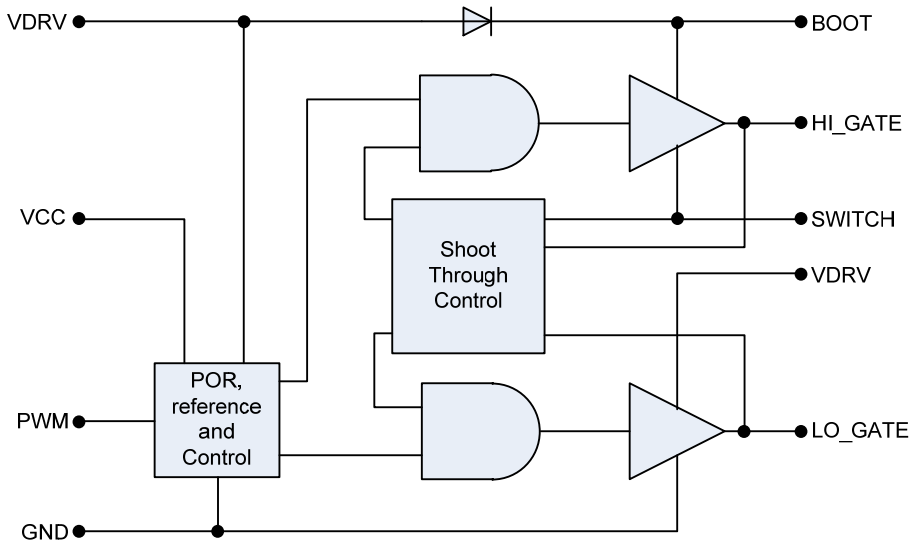
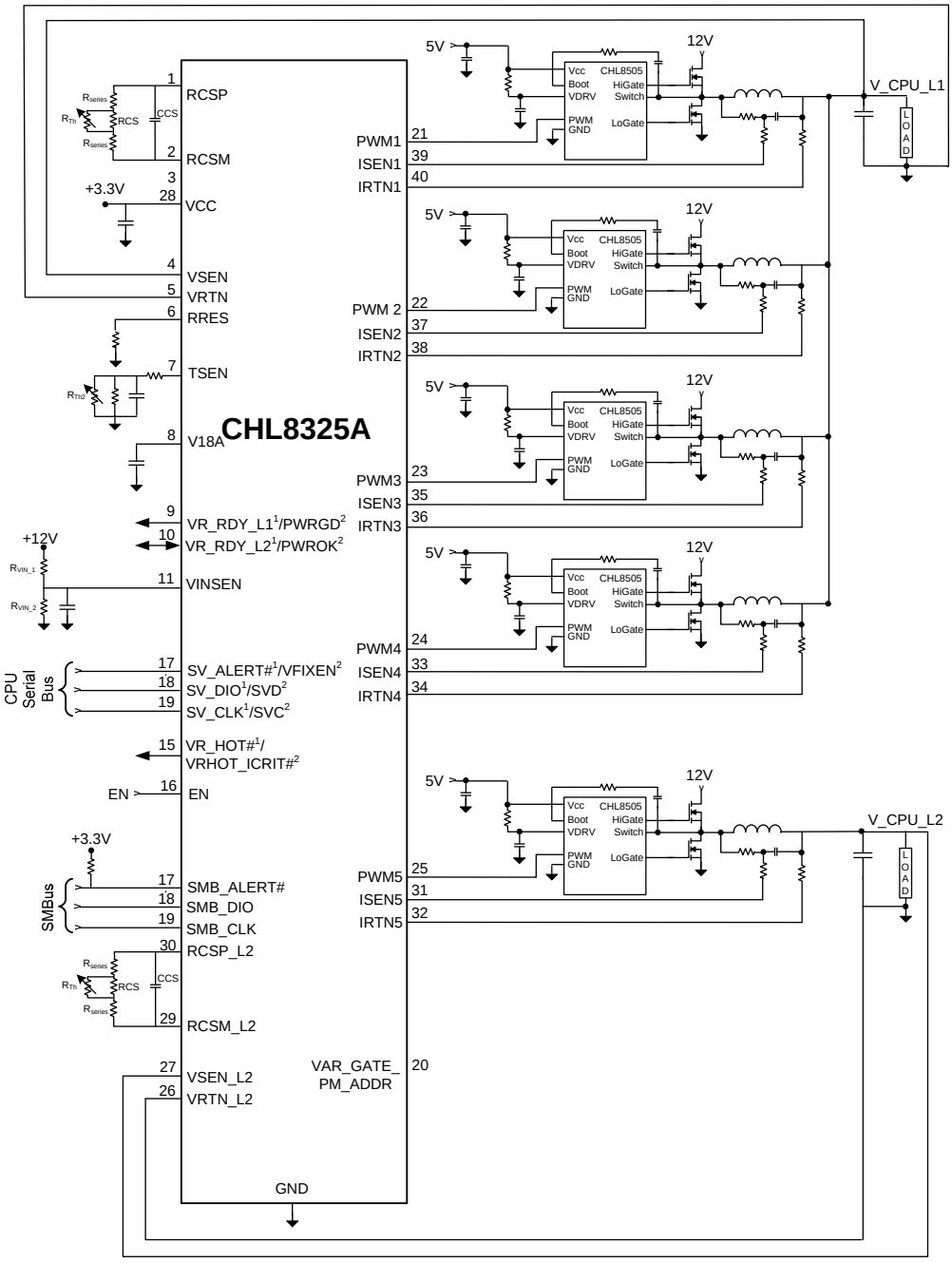



**Figure 4: CHL8505 Simplified Functional Block Diagram**

## TYPICAL APPLICATION DIAGRAM




**Notes**
[1] Pin definition in Intel & MPoL modes
[2] Pin definition in AMD mode

**Figure 5: 4+1 CPU VR solution using CHL8505 MOSFET Drivers & CHL8325A Controller**

## PIN DESCRIPTIONS

| PIN# | PIN NAME | PIN DESCRIPTION |
|---|---|---|
| 1 | PWM | The PWM signal is the control input for the driver from a 1.8V IR ATL-based PWM signal. Connect this pin to the PWM output of the controller. |
| 2 | VCC | Connect this pin to a +5V bias supply. Place a high quality low ESR ceramic capacitor from this pin to GND. |
| 3 | VDRV | Connect this pin to a separate supply voltage between 4.0V and 13.2V to vary the drive voltage on the low-side MOSFETs. Place a high quality low ESR ceramic capacitor from this pin to GND. |
| 4 | NC | Leave this pin floating. |
| 5 | BOOT | Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the SWITCH pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Internal Bootstrap Device section under DESCRIPTION for guidance in choosing the capacitor value. |
| 6 | HI_GATE | Upper gate drive output. Connect to gate of high-side power N-Channel MOSFET. |
| 7 | SWITCH | Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET. This pin provides a return path for the upper gate drive |
| 8 | LO_GATE | Lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET. |
| 9 | NC | Leave this pin floating. |
| 10 | NC | Leave this pin floating. |
| PAD (11) | GND | Bias and reference ground. All signals are referenced to this node. It is also the power ground return of the driver. |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| VCC, VDRV | -0.3V to +7.0V |
| PWM, OTSET, OT# | -0.3V to +7.0V |
| BOOT-GND, BOOT-SWITCH | -0.3V to +35.0V, -0.3V TO +7V |
| LO_GATE | -0.3V to VDRV + 0.3V, <200ns: -5V to VDRV + 0.3V |
| HI_GATE | SWITCH – 0.3V to VBOOT + 0.3V, <20ns: SWITCH –5V to VBOOT + 0.3V |
| SWITCH | -0.3V to +35.0V, <200ns, -8V |
| ESD | HBM 250V JEDEC Standard |
| **Thermal Information** | |
| Thermal Resistance ($\theta_{JC}$) | 3°C/W |
| Thermal Resistance ($\theta_{JA}$)[1] | 45°C/W |
| Maximum Operating Junction Temperature | 150°C |
| Maximum Storage Temperature Range | -65°C to 150°C |
| Maximum Lead Temperature (Soldering 10s) | 300°C |

**Note:** 1. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

# ELECTRICAL SPECIFICATIONS

## RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

| | |
|---|---|
| Recommended Operating Ambient Temperature Range | -40°C to 85°C |
| Recommended Maximum Operating Junction Temperature | 125°C |
| Supply Voltage Range | +5V ± 10% |

The electrical characteristics table lists the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C, unless otherwise specified. VCC = 5.0V, HVCC = 7.0V, LVCC = 5.0V.

## ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| Idle Supply Bias Current | $I_{VCC} + I_{VDRV}$ | PWM input tri-stated | - | 2.3 | - | mA |
| Active Supply Bias Current | $I_{VCC}$ | VCC = 5V | 2.7 | 3.1 | 3.5 | mA |
| VCC Rising Threshold for POR | | | 3.5 | 3.7 | 3.9 | V |
| VCC Falling Threshold for POR | | | 3.2 | 3.4 | 3.6 | V |
| **PWM Input IR ATL Mode** | | | | | | |
| PWM Input High Threshold | $V_{IH(C\_PWM)}$ | | - | 1.0 | - | V |
| PWM Input Low Threshold | $V_{IL(C\_PWM)}$ | | - | 0.8 | - | V |
| PWM Input Tri-level High Threshold | $V_{TL(C\_PWM)}$ | | - | 2.5 | -- | V |
| PWM Input Tri-level Low Threshold | $V_{TH(C\_PWM)}$ | | - | 2.3 | - | V |
| PWM Input Current Low | $I_{C\_PWM}$ | $V_{PWM}$ = 0V | - | 1.0 | - | mA |
| PWM Input Current High | | $V_{PWM}$ = 1.8V | - | 1.0 | - | mA |
| **High-side Gate Driver** | | | | | | |
| Transition Time – Rise | $t_{R(HS)}$ | 3nF Load, 10% – 90% | - | 10 | - | ns |
| Transition Time – Fall | $t_{F(HS)}$ | 3nF Load, 10% – 90% | - | 8 | - | ns |
| Propagation Delay – Turn-on | $t_{PDH(HS)}$ | 3nF Load, Adaptive | - | 19 | - | ns |
| Propagation Delay – Turn-off | $t_{PDL(HS)}$ | 3nF Load | - | 20 | - | ns |
| Propagation Delay – Exit Tri-state | $t_{PDTS(HS\_en)}$ | 3nF Load | - | 35 | - | ns |
| Propagation Delay – Enter Tri-state | $t_{PDTS(HS\_dis)}$ | 3nF Load | - | 20 | - | ns |
| Source Current | $I_{HS\_SOURCE}$ | 3nF Load | - | 2 | - | A |
| Output Impedance Sourcing | $R_{HS\_SOURCE}$ | Sink Current at 100mA | - | 1.4 | - | Ω |
| Sink Current | $I_{HS\_SINK}$ | 3nF Load | - | 2 | - | A |
| Output Impedance – Sinking | $R_{HS\_SINK}$ | Sink Current at 100mA | - | 0.7 | - | Ω |
| **Low-side Gate Driver** | | | | | | |
| Transition Time – Rise | $t_{F(LS)}$ | 3nF Load, 10% – 90% | - | 10 | - | ns |
| Transition Time – Fall | $t_{R(LS)}$ | 3nF Load, 10% – 90% | - | 7 | - | ns |

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Propagation Delay – Turn-on | $t_{PDH(LS)}$ | 3nF Load, Adaptive | - | 9 | - | ns |
| Propagation Delay – Turn-off | $t_{PDL(LS)}$ | 3nF Load | - | 25 | - | ns |
| Propagation Delay – Exit Tri-state | $t_{PDTS(LS\_en)}$ | 3nF Load | - | 36 | - | ns |
| Propagation Delay – Enter Tri-state | $t_{PDTS(LS\_dis)}$ | 3nF Load | - | 22 | - | ns |
| Source Current | $I_{LS\_SOURCE}$ | 3nF Load | - | 2 | - | A |
| Output Impedance Sourcing | $R_{LS\_SOURCE}$ | Sink Current at 100mA | - | 1.5 | - | Ω |
| Sink Current | $I_{LS\_SINK}$ | 3nF Load | - | 4 | - | A |
| Output Impedance – Sinking | $R_{LS\_SINK}$ | Sink Current at 100mA | - | 0.4 | - | Ω |

**Note:** [1] Guaranteed by design

## TIMING DIAGRAM

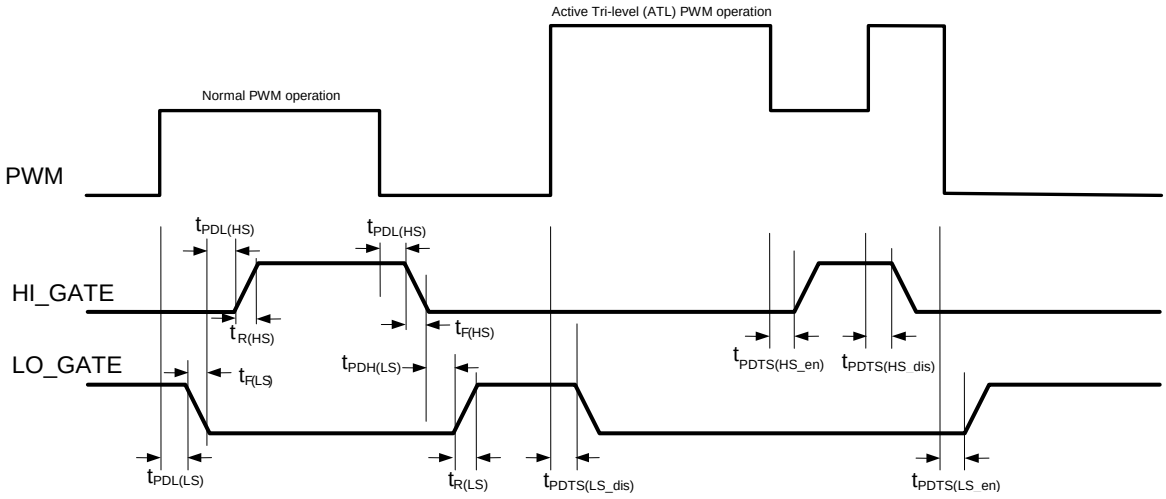



**Figure 6: IR Active Tri-Level (ATL) mode PWM, HI_GATE and LO_GATE signals**

## GENERAL DESCRIPTION

The CHL8505 is a high efficiency, fast MOSFET driver with large source and sink current capability. It can reliably drive the external high- and low-side N-channel MOSFETs with large input capacitance at switching frequencies up to 1MHz. The patented IR Active Tri-Level (ATL) feature allows complete control over enable and disable of both MOSFETs using the PWM input signal from the controller. The timing and voltage levels of ATL are shown in Figure 6.

During normal operation the PWM transitions between low and high voltage levels to drive the low- and high-side MOSFETs. The PWM signal falling edge transition to a low voltage threshold initiates the high-side driver turn off after a short propagation delay, $t_{PDL(HS)}$. The dead time control circuit monitors the HI_GATE and switch voltages to ensure the high-side MOSFET is turned off before the LO_GATE voltage is allowed to rise to turn on the low-side MOSFET.

The PWM rising edge transition through the high-side turn on threshold, initiates the turn off of the low-side MOSFET after a small propagation delay, $t_{PDL(LS)}$. The adaptive dead time circuit provides the appropriate dead time by determining if the falling LO_GATE voltage threshold has been crossed before allowing the HI_GATE voltage to rise and turn on the high-side MOSFET, $t_{PDH(HS)}$.

.

# THEORY OF OPERATION

## POWER-ON RESET (POR)

The CHL8505 incorporates a power-on reset feature. This ensures that both the high- and low-side output drivers are made active only after the device supply voltage has exceeded a certain minimum operating threshold. The $V_{cc}$ and $V_{drv}$ supply is monitored and both the drivers are set to the low state, holding both external MOSFETs off. Once $V_{cc}$ and $V_{drv}$ crosses the rising POR threshold, the CHL8505 is reset and the outputs are held in the low state until a transition from tri-state to active operation is detected at the PWM input. During normal operation the drivers continue to remain active until the $V_{cc}$ and $V_{drv}$ falls below the falling POR threshold.

## INTEGRATED BOOTSTRAP DIODE

The CHL8505 features an integrated bootstrap diode to reduce external component count. This enables the CHL8505 to be used effectively in cost and space sensitive designs.

The bootstrap circuit is used to establish the gate voltage for the high-side driver. It consists of a diode and capacitor connected between the SWITCH and BOOT pins of the device. Integrating the diode within the CHL8505, results in the need for an external boot capacitor only. The bootstrap capacitor is charged through the diode and injects this charge into the high-side MOSFET input capacitance when PWM signal goes high.

## IR ACTIVE TRI-LEVEL (ATL) PWM INPUT SIGNAL

The CHL8505 gate drivers are driven by a patented tri-level PWM control signal provided by the IR digital PWM controllers. During normal operation, the rising and falling edges of the PWM signal transitions between 0V and 1.8V to switch the LO_GATE and HI_GATE. To force both driver outputs low simultaneously, the PWM signal crosses a tri-state voltage level higher than the tri-state HI_GATE threshold. This threshold based tri-state results in a very fast disable for both the drivers, with only a small tri-state propagation delay. MOSFET switching resumes when the PWM signal falls below the tri-state threshold into the normal operating voltage range.

This fast tri-state operation eliminates the need for any tri-state hold-off time of the PWM signal to dwell in the shutdown window. Dedicated disable or enable pins are not required which simplifies the routing and layout in applications with a limited number of board layers. It also provides switching free of shoot through for slow PWM transition times of up to 20ns. The CHL8505 is therefore tolerant of stray capacitance on the PWM signal lines.

The CHL8505 provides a 1.0mA typical pull-up current to drive the PWM input to the tri-state condition of 3.3V when the PWM controller output is in its high impedance state. The 1.0mA typical current is designed for driving worst case stray capacitances and transition the CHL8505 into the tri-state condition rapidly to avoid a prolonged period of conduction of the high- or low-side MOSFETs during faults. Immediately after the driver is driven into the tri-state mode, the 1mA current is disables such that power is conserved.

## DIODE EMULATION DURING LOAD RELEASE

One advantage of this fast tri-state scheme is the ability to quickly turn-off all low-side MOSFETs during a load release event. This is known as diode emulation since all the load current is forced to flow momentarily through the body diodes of the MOSFETs. This results in a much lower overshoot on the output voltage as can be seen in Figure 7 below.

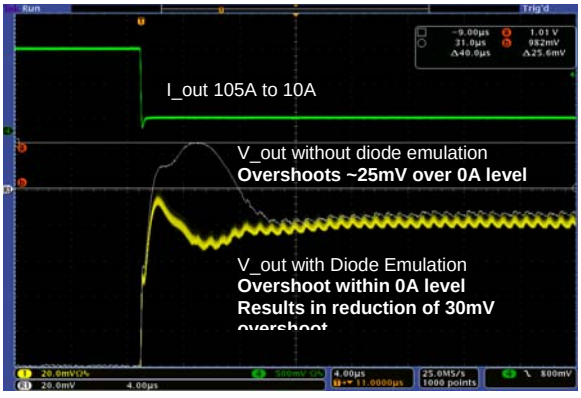



**Figure 7: Output Voltage Overshoot Reduction with Diode Emulation**

## START UP

During initial startup, the CHL8505 holds both high- and low-side drivers low even after POR threshold is reached. This mode is maintained while the PWM signal is pulled to the tri-state threshold level greater than the tri-state HI_GATE threshold and until it transitions out of tri-state. It is this initial transition out of the tri-state which enables both drivers to switch based on the normal PWM voltage levels.

This startup also ensures that any undetermined PWM signal levels from a controller in pre-POR state will not result in high- or low-side MOSFET turn on until the controller is out of its POR.

## HIGH-SIDE DRIVER

The high-side driver drives an external floating N-channel MOSFET which can be switched at 1MHz. An external bootstrap circuit referenced to the SWITCH node, consisting of a boot diode and capacitor is used to bias the external MOSFET gate. When the SWITCH node is at ground, the boot capacitor is charged to near the supply voltage using the boot diode and this stored charge is used to turn on the external MOSFET when the PWM signal goes high. Once the high-side MOSFET is turned on, the SWITCH voltage raises to the supply voltage and the boot voltage to twice the supply voltage.

When the PWM signal goes low, the MOSFET is turned off by pulling the MOSFET gate to the SWITCH voltage.

## LOW-SIDE DRIVER

The CHL8505 low-side driver is designed to drive an external N-channel MOSFET referenced to ground at 1MHz. The low-side driver is connected internally to the supply voltage to turn the MOSFET on.

When the low-side MOSFET is turned on the SWITCH node is pulled to ground. This allows charging of the boot capacitor to the supply voltage ready to drive the high-side MOSFET based on the PWM signal level.

## ADAPTIVE DEAD TIME ADJUSTMENT

In a synchronous buck configuration dead time between the turn off of one gate and turn on of the other is necessary to prevent simultaneous conduction of the external MOSFETS. It prevents a shoot-through condition which would result in a short of the supply voltage to ground. A fixed dead time does not provide optimal performance over a variety of MOSFETs, converter duty cycles and board layouts.

The CHL8505 provides an ‘adaptive’ dead time adjustment. This feature minimizes dead time to an optimum duration which allows for maximum efficiency. The ‘break before make’ adaptive design is achieved by monitoring gate and SWITCH voltages to determine OFF status of a MOSFET. It also provides zero-voltage switching (ZVS) of the low-side MOSFET with minimum current conduction through its body-diode.

When the PWM is switching between 1.8V and 0V, its falling edge transition from high to low will turn off the high-side gate driver. The adaptive dead time circuit monitors the HI_GATE and the SWITCH node voltages during the high-side MOSFET turn off. When the HI_GATE falls below 1.7V above the SWITCH node potential or the SWITCH node voltage drops below 0.8V the high-side MOSFET is determined to be turned off and the LO_GATE turn on is initiated. This turns on the external low-side MOSFET. The rising edge transition of the PWM signal from low to high voltage causes the low-side gate driver to turn off. The adaptive circuit monitors the voltage at LO_GATE and when it falls below 1.7V, the low-side MOSFET is determined to be turned off and the high-side MOSFET turn on is initiated.

# APPLICATION INFORMATION

## BOOT STRAP CIRCUIT

Once the high-side MOSFET selection is made, the bootstrap circuit can be defined. The integrated boot diode of the CHL8505 reduces the external component count for use in cost and space sensitive designs. For ultra high efficiency designs, an external boot strap diode is recommended.

The bootstrap capacitor $C_{Boot}$ stores the charge and provides the voltage required to drive the external high-side MOSFET gate. The minimum capacitor value can be defined by:

$$C_{Boot} = Q_{HS\ MOSFET\_gate} / \Delta V_{Boot}$$

where,

- $Q_{HS\ MOSFET\_gate}$ is the total gate charge of the high-side external MOSFET(s)
- $\Delta V_{Boot}$ is the droop allowed on the boot capacitor voltage (at the high-side MOSFET gate)

A series resistor, 1Ω to 4Ω, may be added to customize the rise time of the high-side output. Slowing down this output allows setting the phase node rising slew rate and limits the surge current into the boot capacitor on start-up.

## SUPPLY DECOUPLING CAPACITOR

VCC decoupling to the IR3598 is provided by a 0.1uF bypass capacitor $C_{Vcc}$ located close to the supply input pin. A series resistor Rvcc, typically 10Ω, is added in series with the supply voltage to filter high frequency ringing and noise. A 1.0uF or higher capacitor is recommended for the VDRV decoupling capacitor, CDRV.

## PCB LAYOUT CONSIDERATIONS

PCB layout and design is important to driver performance in voltage regulator circuits due to the high current slew rate (di/dt) during MOSFET switching.

- Locate all power components in each phase as close to each other as practically possible in order to minimize parasitics and losses, allowing for reasonable airflow.
- Input supply decoupling and bootstrap capacitors should be physically located close to their respective IC pins.
- High current paths like the gate driver traces should be as wide and short as practically possible.
- Trace inductances to the high- and low-side MOSFETs should be minimized.
- The ground connection of the IC should be as close as possible to the low-side MOSFET source.
- Use of a copper plane under and around the IC and thermal vias to connect to buried copper layers improves the thermal performance.

MOSFET stages should be well bypassed with capacitors placed between the drain of the HIGH-side MOSFET and the source of the LOW-side MOSFET.

## MARKING INFORMATION

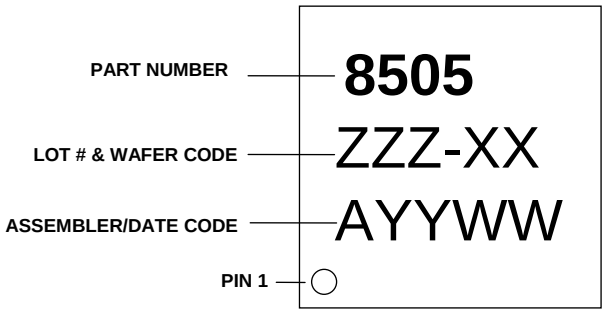



Figure 8: Package Marking

## PACKAGE INFORMATION

DFN 3x3mm, 10 pin

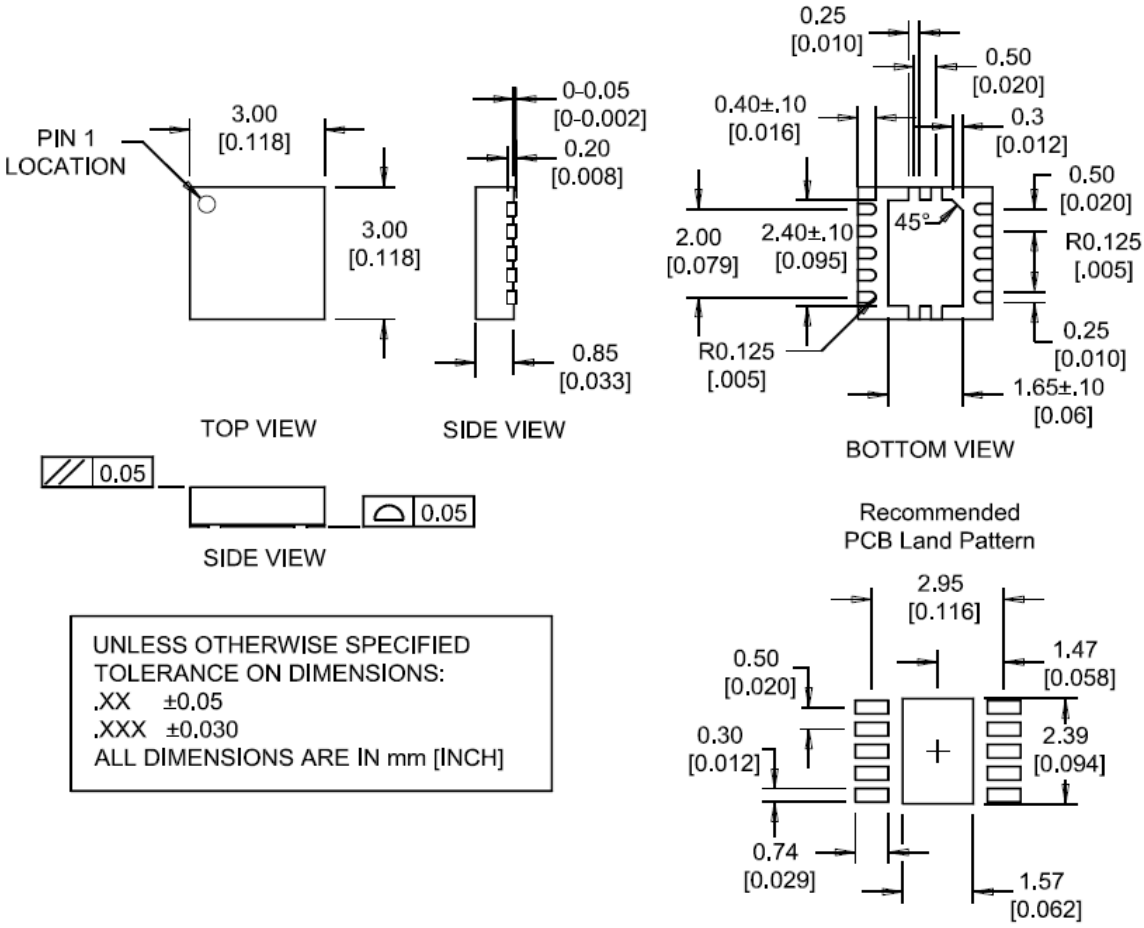



Figure 9: Package Dimensions

Data and specifications subject to change without notice.
This product will be designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.
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