AN11486

GreenChip SSL8516T PFC and flyback controller

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Document information

Info	Content
Keywords	GreenChip, SSL8516T, PFC, flyback, high-efficiency, LED driver
Abstract	The SSL8516T is a member of the new generation of combined Power Factor Correction (PFC) and flyback controller ICs, used for efficient Switched-Mode Power Supplies (SMPS). The PFC enables low Total Harmonic Distortion (THD) performance over a wide input voltage and output power range. The SSL8516T has a high level of integration allowing cost-effective design of power supplies using a minimal number of external components. The SSL8516T is designed in a Silicon-On-Insulator (SOI) process, enabling it to operate at a wide voltage range.

Revision history

Rev	Date	Description
v.1	20140717	first issue

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1. Introduction

The SSL8516T is an integrated PFC and flyback controller in an SO16 package. Both controllers operate in Quasi-Resonant (QR) mode and in Discontinuous Conduction Mode (DCM) with valley detection. They are independently switched.

The PFC output power is on-time controlled for simplicity. Sensing the phase of the mains voltage is not required. The flyback output power is current-mode controlled providing good input voltage ripple suppression.

The integrated communication circuitry between the controllers does not require adjustment.

Remark: The voltage and current levels contained in this application note are typical values. The specification of the pin level spreading is given in the *SSL8516T data sheet*.

Remark: If a parameter value in this application note is different from the value in the applicable data sheet, the data sheet is leading.

This application note describes the functionality of the SSL8516T and the adjustments required within the power converter application.

The large signal parts of the PFC/flyback power stages and the coil/transformer design and data are not included in this application note.

2. Features

The GreenChip features allow the design of reliable, cost-effective and efficient Switched-Mode Power Supplies (SMPS) using a minimal number of external components.

2.1 Key features

- PFC and flyback controllers integrated in one SO16 package
- PFC and flyback controllers operate at independent switching frequencies
- No external hardware required for the communication between the controllers
- High level of integration, resulting in a low external component count
- Integrated mains voltage enable and brownout protection
- Fast-latch reset function implemented
- Power-down functionality for low standby mode power requirements

2.2 System features

- Safe restart mode for system fault conditions
- High-voltage start-up current source (5 mA)
- Reduction of HV current source (1 mA) in safe restart mode
- Wide V_{CC} range (13.4 V to 38 V)
- V_{CC} UnderVoltage LockOut protection (UVLO)
- MOSFET driver voltage limited

- Easy control of start-up behavior and V_{CC} circuit
- General-purpose input for latched protection
- Internal IC OverTemperature Protection (OTP)
- Accurate PFC switch-on/switch-off control using flyback switching frequency measurement
- One high-voltage spacer between the HV pin and the next active pin
- Open pin protection on the VINSENSE, VOSENSE, PFCAUX, FBCTRL, and FBAUX pins

2.3 PFC features

- Fixed output voltage boost converter
- QR/DCM operation with valley switching
- Frequency limitation at 400 kHz to minimize mains current harmonics
- t_{on} controlled
- Mains input voltage compensation for control loop to achieve a good transient response
- OverCurrent Protection (OCP)
- Soft-start and soft-stop
- Open/short-circuit detection for PFC feedback loop: no external OverVoltage Protection (OVP) circuit required
- Adjustable PFC switch-off delay
- PFC switch-on/switch-off overriding functionality

2.4 Flyback features

- FR/QR/DCM operation with valley switching
- Frequency Reduction (FR) with an adjustable minimum peak current and valley switching to maintain high efficiency at low output power levels
- Frequency limitation (130 kHz) to reduce switching losses and ElectroMagnetic Interference (EMI)
- Current mode controlled
- Overcurrent protection
- Soft-start
- Accurate OVP through auxiliary winding
- Time-out protection for output overloads and open feedback loop, available as safe restart protection

3. SSL8516T schematic

Figure 1 and Figure 2 show the schematic diagrams of a typical application for a constant current output application.

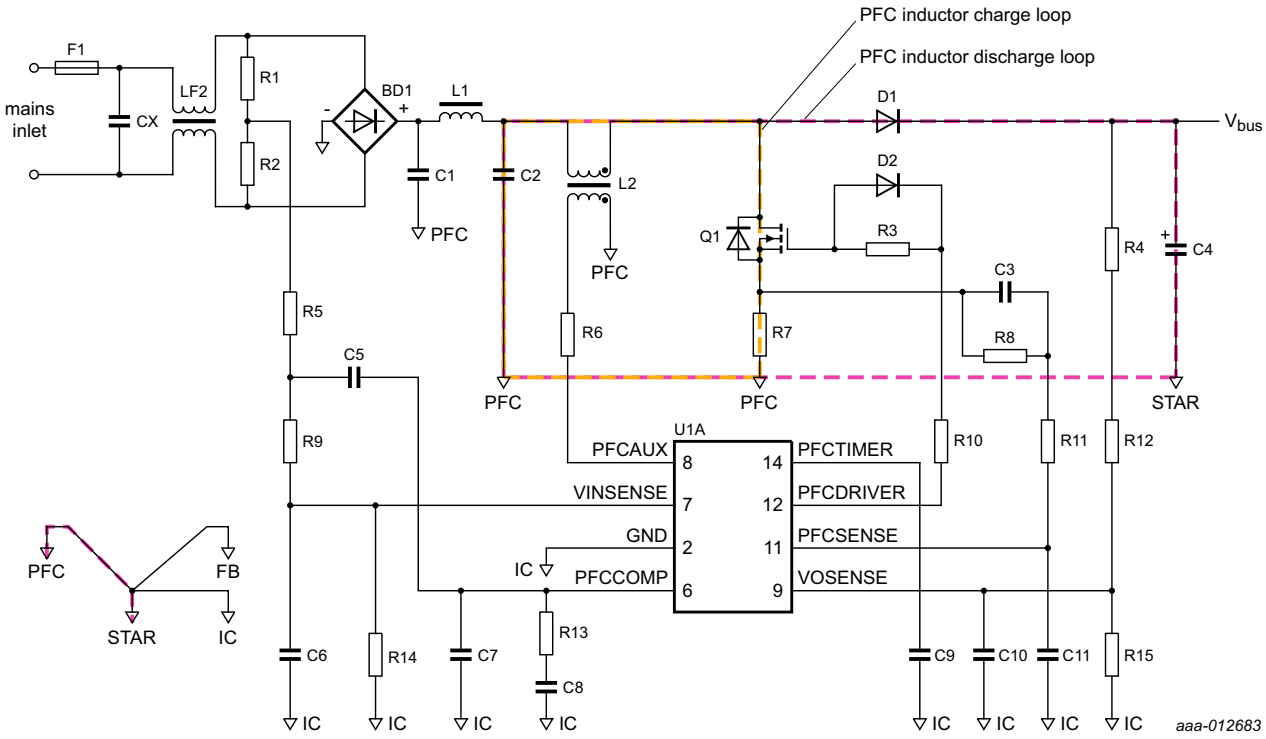


Fig 1. SSL8516T schematic including EMI filter and PFC part

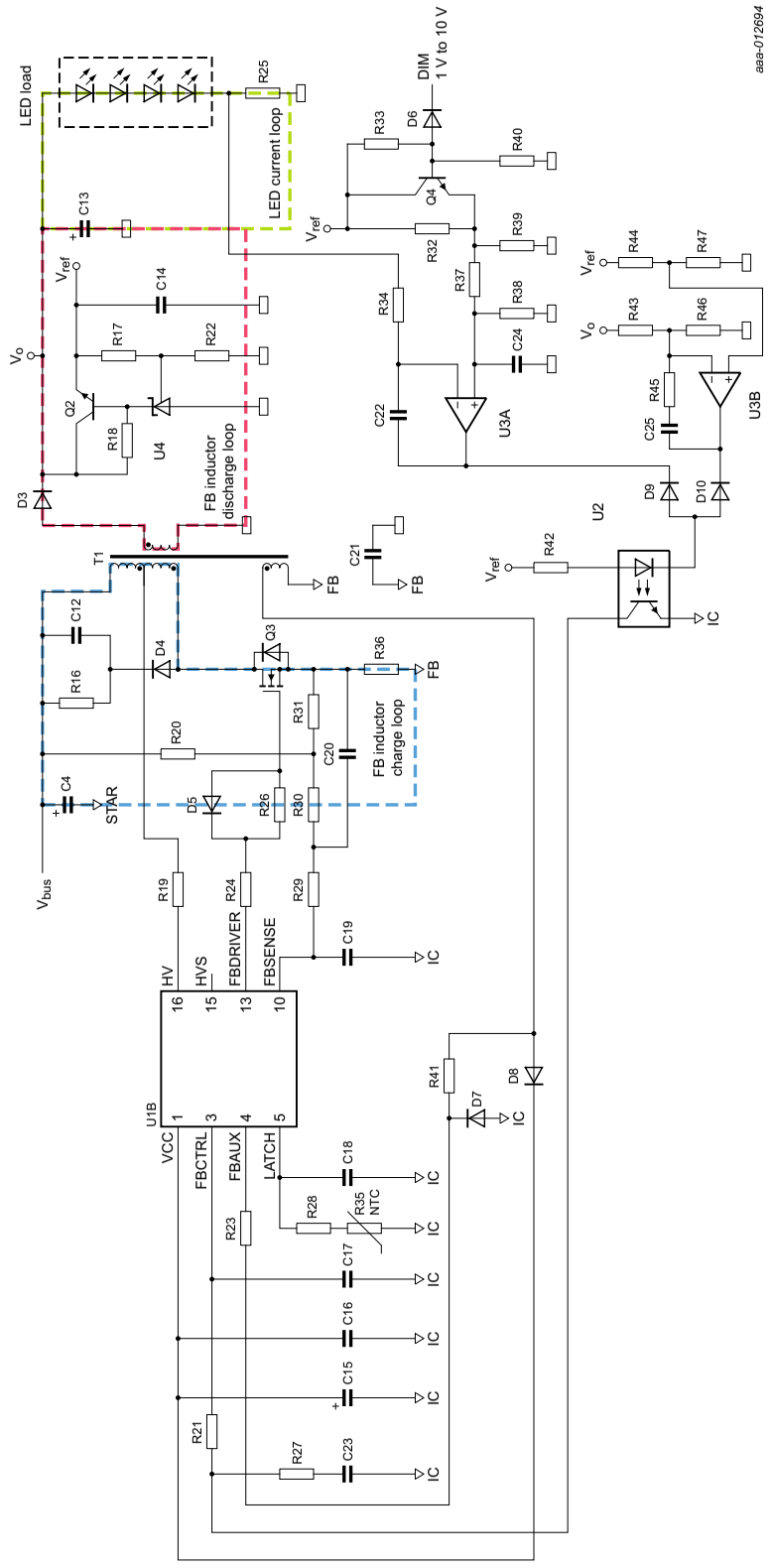


Fig 2. SSL8516T schematic including flyback and output part

4. Pin description

4.1 Pinning diagram

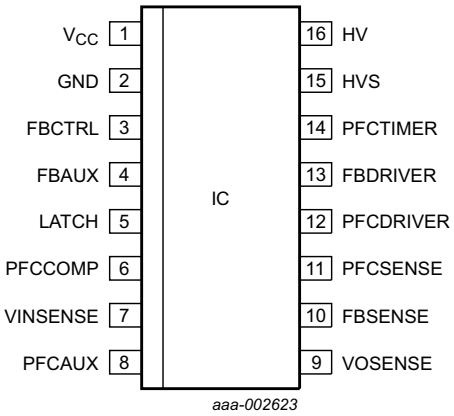


Fig 3. SSL8516T pinning diagram

4.2 Pin descriptions

Table 1. SSL8516T pin description

Pin number	Pin name	Functional description summary
1	V_{CC}	Supply voltage: V_{trip} = 0.6 V; $V_{startup}$ = 22.3 V; $V_{th(UVLO)}$ = 13.4 V When mains voltage is applied, the V_{CC} pin capacitors are charged to $V_{startup}$ by the internal HV current source I_{HV}. When $V_{CC} < V_{trip}$, I_{HV} is limited to 1.1 mA. This feature prevents that the IC overheats when the V_{CC} pin is short-circuited. When $V_{trip} < V_{CC} < V_{startup}$, the initial I_{HV} is 5 mA to enable a fast start-up. During safe restart, when $V_{th(UVLO)} < V_{CC} < V_{startup}$, I_{HV} is limited to 1 mA again to reduce the safe restart duty cycle. The lower duty cycle results in reduced input power during fault conditions. When $V_{startup}$ is reached, I_{HV} is pinched off and V_{CC} is regulated to $V_{startup}$ until the flyback starts. See Section 5.2 for a complete description of the start-up sequence.
2	GND	Ground connection
3	FBCTRL	Control input for flyback for direct connection of the optocoupler When $V_{FBCTRL} > 4.9$ V, the flyback delivers maximum power. The flyback enters FR mode when 0.54 V < V_{FBCTRL} < 4.0 V. The flyback driver stops switching when $V_{FBCTRL} < 0.54$ V. The built-in logic controls an internal 29 μA current source $I_{to(FBCTRL)}$ that is connected to the pin. $I_{to(FBCTRL)}$ can be used to implement a time-out function for detecting an open control loop or a short circuit of the flyback output. For testing purposes, the time-out function can be disabled by connecting a 180 kΩ resistor between pin FBCTRL and ground.
4	FBAUX	Input for flyback auxiliary winding for transformer demagnetization detection, OverVoltage Protection (OVP) of the flyback, and, if necessary, mains dependent OverPower Protection (OPP). The demagnetization detection on the FBAUX pin and the valley detection on the HV pin determine the flyback switch-on timing in the valley. A flyback OVP is detected at $I_{FBAUX} > 300$ μA (into the IC). Internal filtering prevents false detection of an OVP. The flyback OPP starts at $I_{FBAUX} > 100$ μA (out of the IC).

Table 1. SSL8516T pin description *...continued*

Pin number	Pin name	Functional description summary
5	LATCH	General-purpose latched protection input When V_{CC} reaches $V_{startup}$, the LATCH pin capacitor is charged to 582 mV before the PFC and flyback controllers can be switched on. The latched protection is triggered when V_{LATCH} < 494 mV. The PFC and the flyback are then switched off. The internal logic controls an internal 30.5 μA current source $I_{O(LATCH)}$ which connects to the pin. With $I_{O(LATCH)}$, connecting a Negative Temperature Coefficient (NTC) resistor to the LATCH pin enables an optional latching temperature protection.
6	PFCCOMP	Frequency compensation pin for the PFC control loop Input for on-time modulation of the PFC gate drive signal. When PFC is off, the PFCCOMP pin is clamped to a low voltage of 3.32 V or 1.18 V (determined by $V_{th(sel)clmp}$) on the VINSENSE pin) and an upper voltage of 3.75 V.
7	VINSENSE	Sense input for mains voltage The VINSENSE pin has several functions: • Mains voltage start level: $V_{start(VINSENSE)}$ = 1.16 V • Mains voltage stop level (brownout): $V_{stop(VINSENSE)}$ = 0.89 V • Mains voltage compensation for the PFC control-loop gain bandwidth • Fast-latch reset: V_{flr} = 0.75 V • PFCCOMP clamp select threshold: $V_{th(sel)clmp}$ = 2.0 V • Enter standby mode: $V_{th(pd)}$ = 385 mV • Exit standby mode: $V_{th(pd)exit}$ = 460 mV The $V_{VINSENSE}$ must be an averaged DC value, representing the AC line voltage. The VINSENSE pin is not used for sensing the phase of the mains voltage.
8	PFCAUX	Input from an auxiliary winding of the PFC coil for demagnetization timing and valley detection to determine the PFC switch-on timing To prevent pin damage due to lighting surges, always connect a 5 kΩ series resistor between the auxiliary winding and this pin.
9	VOSENSE	Sense input for the PFC output voltage, open-loop and short-circuit detection: • PFC output voltage start level $V_{th(start)VOSENSE}$ = 0.5 V • PFC output voltage stop level $V_{th(stop)(VOSENSE)}$ = 0.4 V • PFC output voltage regulation; $V_{reg(VOSENSE)}$ = 2.5 V • PFC soft OVP (cycle-by-cycle): $V_{ovp(VOSENSE)}$ = 2.62 V

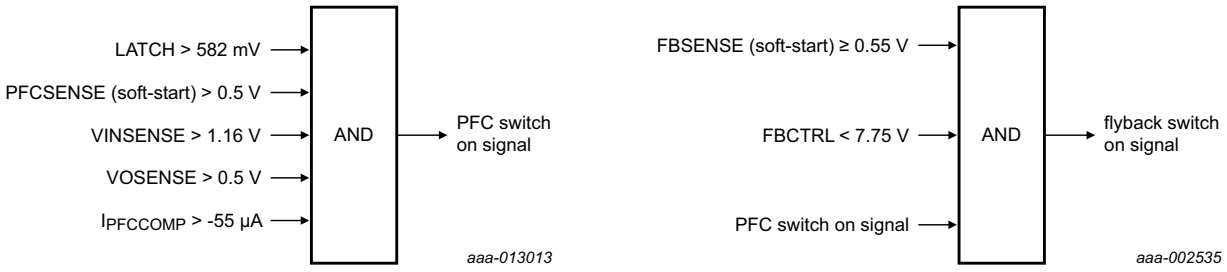
Table 1. SSL8516T pin description *...continued*

Pin number	Pin name	Functional description summary
10	FBSENSE	Flyback current sense input On this pin, the sum of three voltages is measured. The voltages are: • Flyback current × sense resistor • $I_{adj(FBSENSE)}$ × series resistance • Delay compensation voltage Selecting the proper resistor values for the FBSENSE circuit: • Prevents or minimizes the risk of flyback transformer saturation • Allows some adjustment for switching on or switching off the PFC controller • Allows a system that operates line voltage independently $V_{sense(fb)max}$ = 545 mV at dV/dt = 0 mV/μs. $V_{sense(fb)min}$ = 232 mV at dV/dt = 0 mV/μs. $V_{sense(fb)min}$ is related to the adjustable peak current through the flyback transformer when flyback is operating in frequency reduction mode. There are two internal current sources connected to this pin: • $I_{start(soft)fb}$ = 60 μA • $I_{adj(FBSENSE)}$ = 2.1 μA The internal logic controls $I_{start(soft)fb}$ which is intended to implement a soft-start function for the flyback controller. The flyback driver only starts when $I_{start(soft)fb}$ can charge the soft-start capacitor to a voltage > 0.55 V. A minimum soft-start resistance of 15 kΩ is required to ensure that the flyback controller is switched on. $I_{adj(FBSENSE)}$ is intended to support the switch-on/switch-off adjustment of the PFC.
11	PFCSENSE	PFC overcurrent protection input The PFCSENSE pin limits the maximum peak current in the PFC transformer. It is a cycle-by-cycle protection. The PFC MOSFET switches off when $V_{PFCSENSE}$ > 495 mV (at dV/dt = 0 mV/μs). The logic controls a 60 μA current source $I_{start(soft)PFC}$ which connects to this pin. $I_{start(soft)PFC}$ is used to implement a soft-start and soft-stop function for the PFC to prevent audible noise. The PFC driver only starts when $I_{start(soft)PFC}$ can charge $V_{PFCSENSE}$ > 0.5 V. The soft-start resistance must exceed 15 kΩ to ensure PFC start-up.
12	PFCDRIVER	PFC MOSFET gate-driver output
13	FBDRIVER	Flyback MOSFET gate-driver output
14	PFCTIMER	The PFC switch-on/switch-off control and timing The PFC is switched on without delay. The timer delays the switch-off of the PFC when the load of the flyback is removed or minimized. Switch-off is triggered when two conditions are met: • The filtered flyback operating frequency < 53 kHz (FR mode only) • $V_{PFCTIMER}$ > 3 V An externally applied voltage on the PFCTIMER pin can overrule the automatic PFC switch-on/switch-off: • $V_{PFCTIMER}$ < 1.03 V: PFC is on • $V_{PFCTIMER}$ > 4.4 V: PFC is off
15	HVS	High-voltage safety spacer; not connected
16	HV	High-voltage input for the internal start-up current source (to charge V_{CC}) and valley sensing input of the flyback Valley detection input: The combination of demagnetization detection at the FBAUX pin and valley detection at the HV pin determine the switch-on timing of the flyback MOSFET in the valley.

5. System description and calculation

5.1 PFC and flyback start conditions

Figure 4 shows the enable conditions of the PFC and the flyback during initial start-up. If start-up problems occur, check these conditions with an oscilloscope to find the cause of the problem. The conditions rely on dynamic signals (see Figure 5).



a. PFC

b. Flyback

Fig 4. Controller enable conditions at initial start-up

5.2 Initial start-up sequence

At initial power-on, the IC has the following start-up sequence (see Figure 5):

1. The HV current source I_{HV} is set to 1.1 mA and the V_{CC} pin capacitance is charged to 0.60 V to allow short-circuit detection at the V_{CC} pin.
2. At V_{CC} = 0.60 V, I_{HV} set to 5 mA and the V_{CC} pin capacitance is quickly charged to $V_{startup}$.
3. At $V_{startup}$, I_{HV} is pinched off. The 30.5 µA LATCH pin current source $I_{O(LATCH)}$ is switched on to charge the LATCH pin capacitance. The PFCSENSE and FBSENSE soft-start current sources are switched on.
4. When the LATCH pin capacitance is charged to 582 mV, the PFC can start switching when $V_{VOSENSE}$ > 0.5 V and $V_{VINSENSE}$ > 1.16 V.
5. Two additional conditions that must be met to enable the PFC driver are:
   - The PFCSENSE pin soft-start capacitor is charged to 0.5 V
   - The PFCCOMP pin capacitance is charged to either 1.19 V or 3.32 V, depending on $V_{VINSENSE}$ ($V_{th(sel)clmp}$) and $I_{PFCCOMP}$ > −55 µA
6. Conditions to enable the flyback driver are:
   - The PFCSENSE pin soft-start capacitor is charged to 0.5 V
   - The PFCCOMP pin capacitance is charged to either 1.19 V or 3.32 V, depending on $V_{VINSENSE}$ ($V_{th(sel)clmp}$) and $I_{PFCCOMP}$ > −55 µA
7. When flyback increases its output voltage, the auxiliary winding takes over the V_{CC} supply.
8. If the flyback feedback loop signal is open (due to a fault), the time-out protection on pin FBCTRL is triggered. Both converters are switched off, V_{CC} drops to $V_{th(UVLO)}$, and the IC performs a safe restart. During safe restart I_{HV} is set to 1 mA to charge the V_{CC} pin capacitance.

9. At $V_{CC} = V_{th(UVLO)}$, $I_{ch(low)}$ charges the V_{CC} pin capacitance to $V_{startup}$. The sequence is continued at step 3 above.

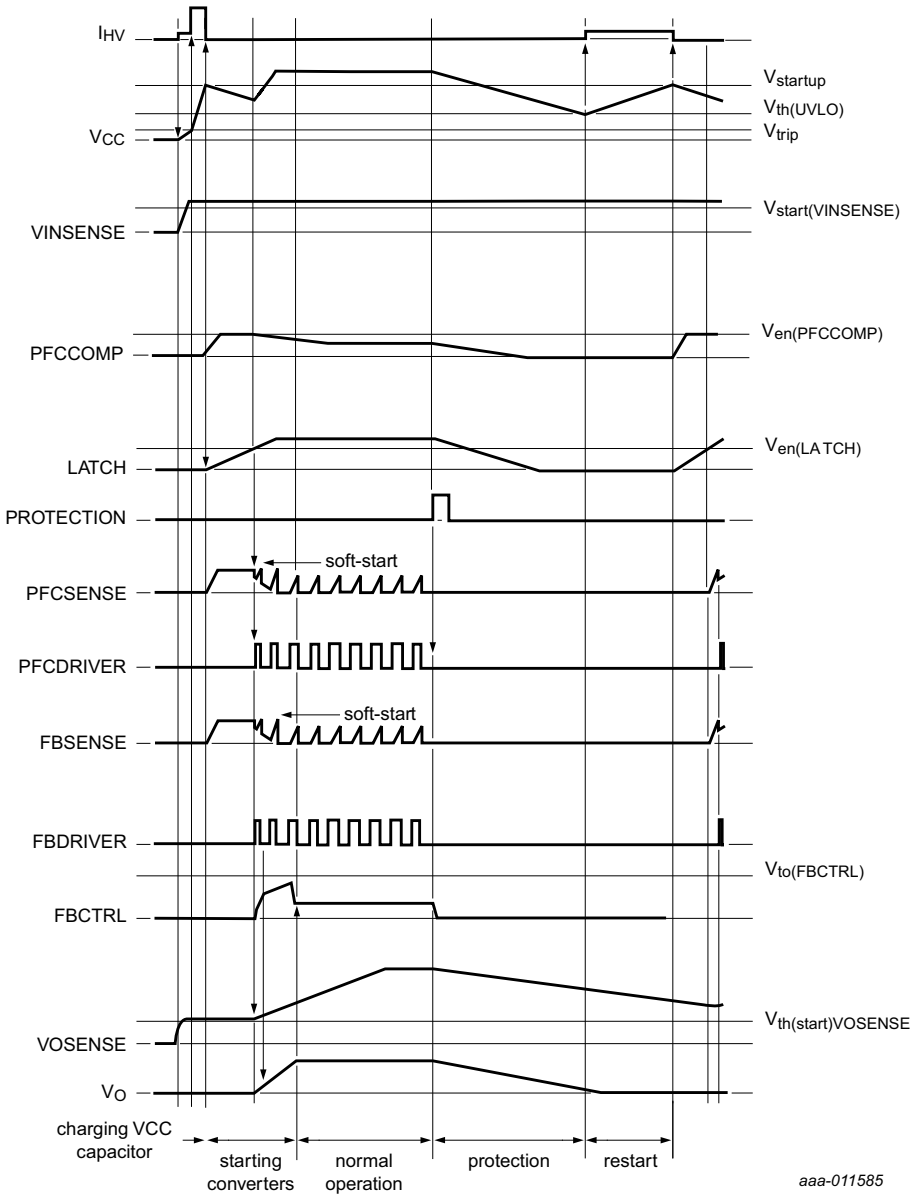


Fig 5. Start-up, normal operation and restart sequence

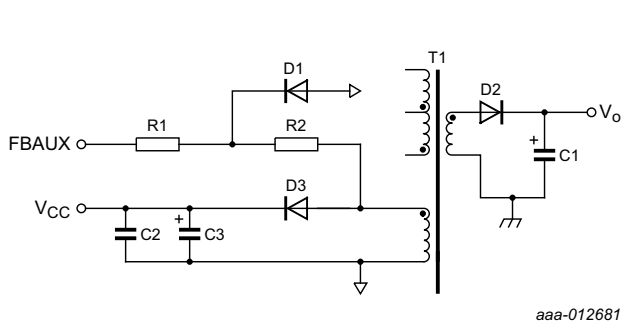
In safe restart mode, the controller goes through the steps 3 to 9 as described in Section 5.2. The PFC and flyback soft-start capacitors can be chosen independently to set the soft-start time.

5.3 V_{CC} supply

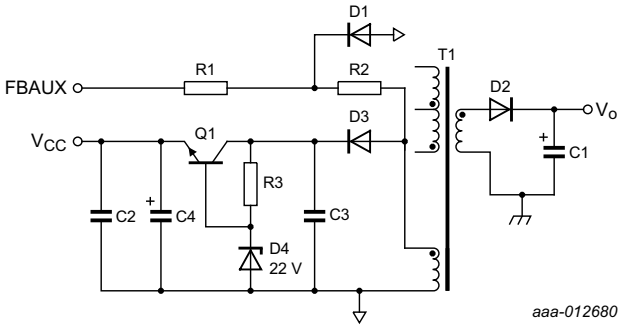
In a constant current output LED driver, the output voltage can vary from $V_{o(min)}$ to $V_{o(max)}$ with a ratio of 3. The V_{CC} is derived from the auxiliary winding of the flyback transformer, which can cause high power dissipation in case of no-load.

Figure 6 shows options for V_{CC} generation to supply the SSL8516T:

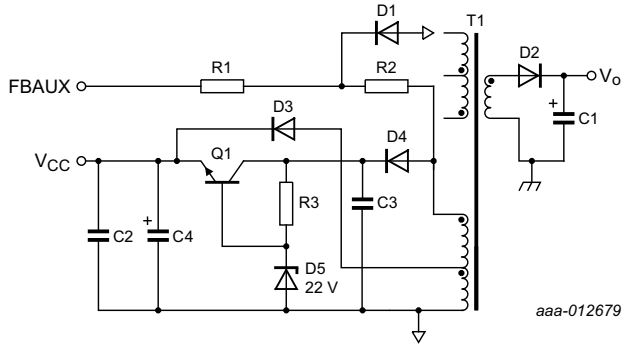
- Basic application for fixed output voltage applications (see Figure 6 (a))
- V_{CC} application for an LED driver with large V_o range support (see Figure 6 (b))
- Reduced standby power compared to Figure 6 (b), V_{CC} takeover in case of no-load by diode D3 (see Figure 6 (c)).
- When PFC is always enabled, the bus voltage can be used as fixed reference during the primary stroke of the flyback (see Figure 6 (d)).



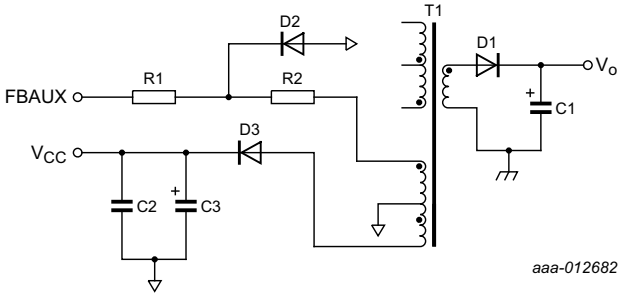
a. Fixed output voltage example



b. Linear regulator example



c. Takeover by D3 at $V_o = V_{o(max)}$



d. Using primary stroke with PFC always on

Fig 6. V_{CC} supply circuit diagrams

5.4 Mains voltage sensing and brownout

The VINSENSE pin senses the mains input voltage. When $V_{VINSENSE} > V_{start(VINSENSE)}$ and all the other start conditions are met (see Section 5.1), the PFC starts switching.

When $V_{VINSENSE} < V_{stop(VINSENSE)}$, the PFC stops switching. The flyback driver continues switching until the maximum flyback on-time protection $t_{on(fb)} > t_{on(fb)max}$ is triggered. When this protection is triggered, the IC stops switching and enters safe restart mode.

$V_{VINSENSE}$ must be an average DC value, representing the mains input voltage. The system works optimally using a time constant of approximately 150 ms for the VINSENSE pin RC filter.

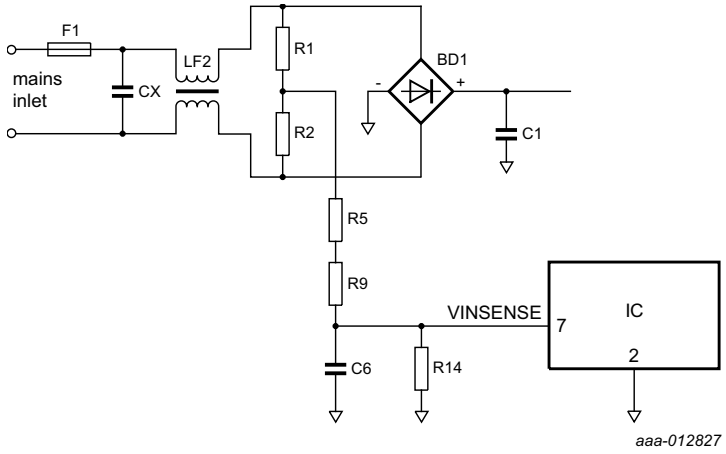


Fig 7. VINSENSE circuit

5.4.1 Discharging the mains input capacitor

For safety reasons, discharge the ElectroMagnetic Compatibility (EMC) input filter X-capacitors CX with a time constant of $\tau < 1$ s.

The replacement resistor R_V and CX determine the time constant.

$$\tau_{VINSENSE} = R_V \cdot CX \quad (1)$$

RV can be calculated with Equation 2:

$$R_V = R1 + \frac{R1 \cdot (R5 + R9 + R14)}{R1 + R5 + R9 + R14} \quad (2)$$

Where:

- R1 = R2

5.4.2 Brownout voltage adjustment

The rectified input voltage is measured using resistors R1 and R2. R1 must be equal to R2. The average rectified line voltage is calculated with Equation 3:

$$V_{ac(avg)} = \frac{2\sqrt{2}}{\pi} V_{ac(rms)} \quad (3)$$

The brownout level is calculated with Equation 4:

$$V_{bo} = \frac{\pi}{2\sqrt{2}} \cdot V_{stop(VINSENSE)} \cdot \frac{R_V + R5 + R9 + R14}{R14} \quad (4)$$

Where:

- $V_{stop(VINSENSE)}$ = 0.89 V
- V_{bo} is the RMS AC mains voltage at which the PFC converter stops

At a brownout threshold of 68 V (AC) and in compliance to IEC-60950 chapter 2.1.1.7 discharge of capacitors in equipment (Ref. 3). Example values are shown in Table 2.

Table 2. VINSENSE component values

CX total	R1	R2	R5 + R9	R14
220 nF	2 MΩ	2 MΩ	560 kΩ	47 kΩ
330 nF	1.5 MΩ	1.5 MΩ	820 kΩ	47 kΩ
470 nF	1 MΩ	1 MΩ	1.1 MΩ	47 kΩ

3.3 µF for capacitor C6 and 47 kΩ for resistor R14, sets the recommended ~150 ms time constant for the VINSENSE pin filter.

5.5 Internal OverTemperature Protection (OTP)

The IC has an internal temperature protection to protect the IC from overheating. The IC stops switching when the junction temperature exceeds the thermal shutdown temperature. As long as the OTP is active, the V_{CC} capacitor is not recharged from the HV mains. When the V_{CC} supply voltage is not sufficient, the OTP circuit is supplied from the HV pin. The internal OTP is not a latched protection. A safe restart is performed when the internal OTP is released.

5.6 LATCH pin

The LATCH pin is a general-purpose input pin which can be used to disable and latch both converters. The pin sources a bias current $I_{O(LATCH)}$ of 30.5 µA for the connection of an NTC resistor. When $V_{LATCH} < V_{prot(LATCH)}$, switching of both converters is stopped immediately. V_{CC} starts cycling between $V_{th(UVLO)}$ and $V_{startup}$ without a restart at $V_{startup}$. A mains power cycle (switch-off/switch-on) triggers the fast-latch reset circuit using the VINSENSE pin and resets the latch.

At start-up, the LATCH pin capacitance is charged above $V_{en(LATCH)}$ before both converters are enabled. The LATCH pin is charged when V_{CC} reaches $V_{startup}$.

A 10 nF capacitor is placed between the LATCH pin and the IC GND pin to prevent false triggering. When the LATCH pin function is not used, place a 10 nF capacitor on the pin.

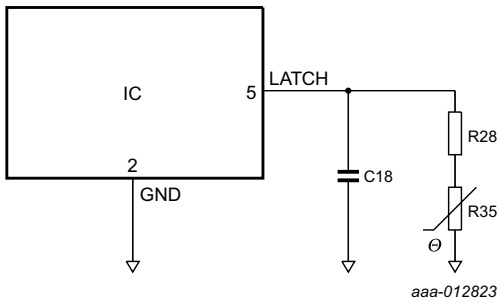


Fig 8. Usage of the LATCH pin protection

Latching on application overtemperature occurs when R_{otp} < 16.2 kΩ.

$$R_{otp} = \frac{V_{prot(LATCH)}}{I_{O(LATCH)}} = \frac{494\ mV}{30.5\ \mu A} = 16.2\ k\Omega \quad (5)$$

Where:

- R_{otp} is R28 + R35

5.7 Fast latch reset

A power cycle (switch-off/switch-on) resets the latched protection. After the input voltage is switched off, $V_{VINSENSE}$ decreases. When $V_{VINSENSE} < V_{flr}$ the fast-latch reset circuit is triggered but does not reset the latched protection. After the mains input voltage is applied, the $V_{VINSENSE}$ increases again. The latch is only reset when $V_{VINSENSE} > (V_{flr} + V_{flr(hys)})$. The system restarts when the V_{CC} pin is charged to $V_{startup}$.

6. PFC description

The PFC controller operates in either QR mode or DCM mode with valley detection to reduce the switch-on losses. The maximum switching frequency $f_{sw(PFC)max}$ of the PFC is limited to 400 kHz. One or more valleys are skipped to keep the frequency below $f_{sw(PFC)max}$.

The PFC is designed as a fixed boost converter. The resistors connected to the VOSENSE pin set the PFC output voltage.

The PFC is switched off automatically with a delay (default PFCTIMER pin application) to ensure high efficiency at low output currents. The switch off delay prevents audible noise caused by PWM / dynamic loads. After switch-off, the electrolytic bus capacitor voltage V_{bus} drops to the peak of the mains voltage.

6.1 PFC output voltage and voltage control

The PFC control in the SSL8516T is on-time controlled. The IC does not require mains phase angle sensing. To obtain a good Power Factor (PF), Total Harmonic Distortion (THD), and a class-C Mains Harmonics Reduction (MHR), the on-time is kept constant during the half sine wave.

The VOSENSE pin senses the PFC output voltage. The pin is the input of a transconductance error amplifier with a reference voltage of $V_{reg(VOSENSE)}$. The error signal (2.5 V − $V_{VOSENSE}$) amplified by 77 μA/V (g_m) to a current in the PFCCOMP pin. $V_{PFCCOMP}$ and $V_{VINSENSE}$ determine the PFC on-time.

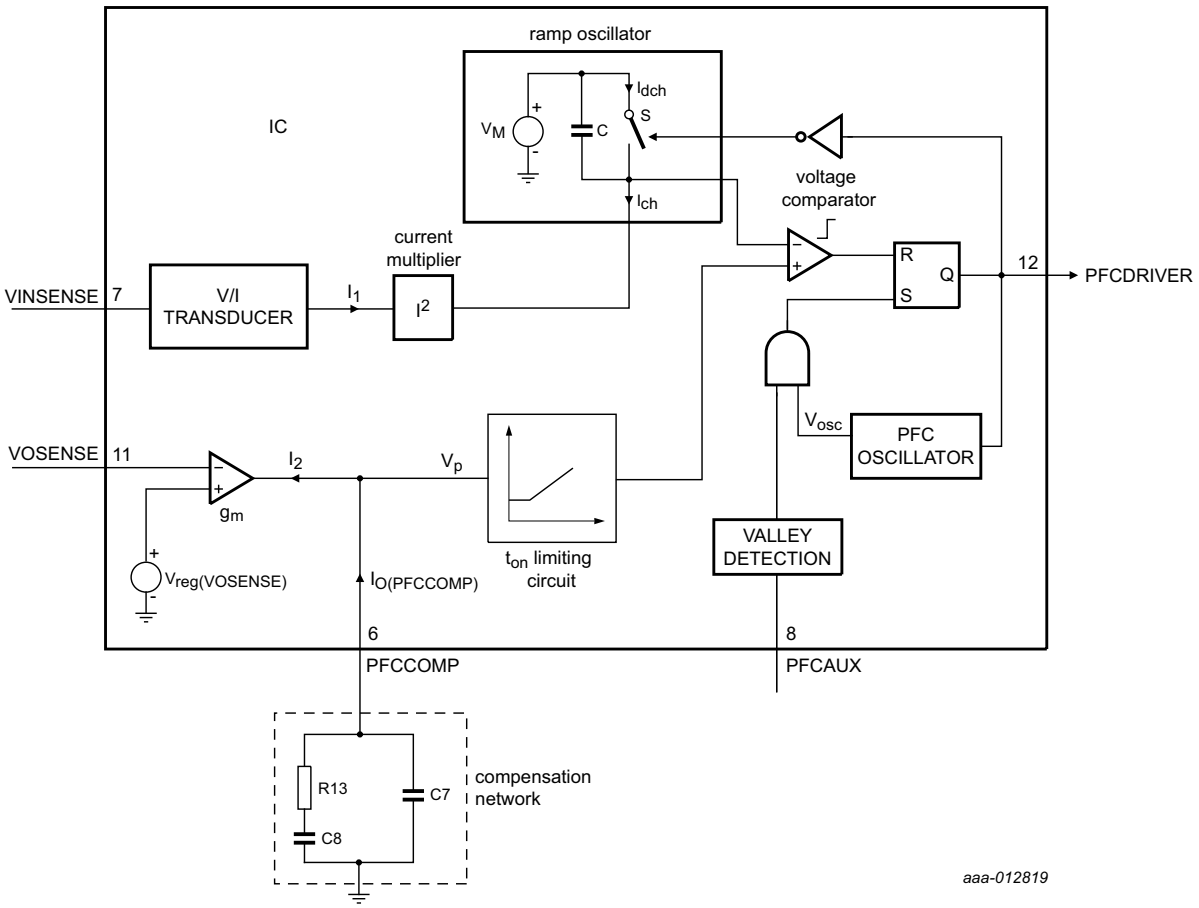


Fig 9. PFC converter on-time control

R13, C8, and C7 at the PFCCOMP pin are intended to stabilize the PFC control loop. The equation for a boost converter transfer function contains the square of the mains input voltage. In competitor controllers without mains compensation, the result is a low regulation bandwidth for low mains input voltages and a high regulation bandwidth for high input voltages. The result can be that at high mains input voltages, it is difficult to meet the MHR requirements. The SSL8516T uses the mains input voltage measured through the VINSENSE pin to compensate the control loop gain as a function of the mains input voltage. As a result the gain is constant over the entire mains input voltage range.

$V_{VINSENSE}$ must be an average DC value, representing the mains input voltage. The system works optimally with a time constant of ~150 ms on the VINSENSE pin RC filter.

During low-power mode operation and start-up, the PFCCOMP pin is clamped to a minimum voltage of 3.32 V or 1.18 V and a maximum voltage of 3.75 V. The minimum clamp voltage depends on $V_{th(sel)clmp}$ on the VINSENSE pin. This clamp limits the maximum power that is delivered when the PFC switches on. The maximum clamp voltage ensures that the PFC returns from low-power mode to its normal regulation point in a limited time.

6.2 Mains Current Harmonics (MHR)

For lighting applications, the mains current harmonics MHR must comply with class C requirements of IEC 61000-3-2. It is important to achieve a good THD over a wide input voltage range and output power range.

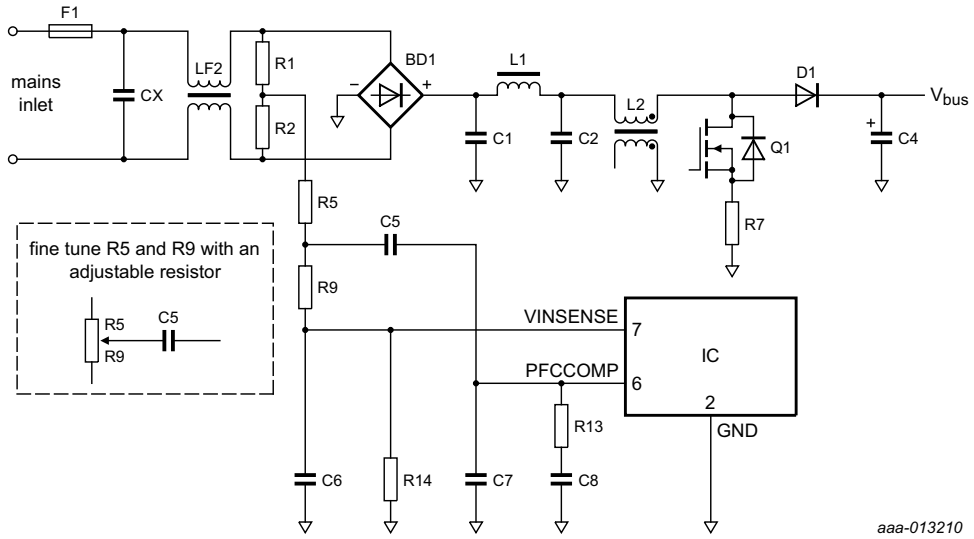


Fig 10. MHR optimization

There are multiple causes why the mains current is distorted.

6.2.1 Residual C1 voltage

Residual voltage on capacitor C1 can cause the diode bridge current to stop. The residual voltage depends on the load and the value of the capacitance (C1 + C2) after the bridge diode. Light load conditions leave more energy in the C1 capacitor.

$$V_{mains(t)} + 2 \cdot V_{f(bridge)} < V_{C1(t)} \quad (6)$$

Where:

- $V_{mains(t)}$ is the momentary mains voltage
- $V_{f(bridge)}$ is the forward voltage of a bridge diode

6.2.2 PFC inductor energy too low

Near the mains voltage, zero crossing, the energy in the PFC inductor is not sufficient to charge the Q1 drain capacitance and transfer energy to the bus capacitor C4. Certain offset energy in the PFC inductor is required.

$$\frac{1}{2} \cdot L_{PFC} \cdot I_{pk(PFC)}^{2} = \frac{1}{2} \cdot C_{d(PFC)} \cdot V_{bus}^{2} \quad (7)$$

Where:

- L_{PFC} is the PFC inductance
- $I_{pk(PFC)}$ is the peak current set by the actual PFC on-time
- $C_{d(PFC)}$ is the total capacitance on the drain of Q1 (C_{oss} + C_{stray})
- V_{bus} is the actual bus voltage

6.2.3 Bus voltage ripple

The bus voltage ripple with a frequency of $2 \times f_{ac}$ causes a modulation of the $t_{on(PFC)}$ because of the VOSENSE pin error amplifier. The $2 \times f_{ac}$ ripple voltage is out of phase with the mains current, causing the mains current to be slightly asymmetrically distorted.

6.2.4 Valley hopping

At the maximum PFC frequency of 400 kHz, the PFC controller enters DCM and it starts valley hopping. When the PFC controller transits from the first valley to the second, the mains current drops because the PFCDRIVER duty cycle decreases with a discrete step. This discrete step increases the THD.

6.2.5 MHR improvement guidelines

In order to improve the THD, the following measures must be taken:

- The total capacitance (C1 + C2) after the bridge must be small to minimize residual voltage.
- To reduce capacitance after the bridge, consider to move the differential mode EMI PI filter (C1, L1, C2) before the bridge diodes.
- To modulate $t_{on(PFC)}$, add capacitor C5 in the circuit. As a consequence $I_{pk(PFC)}$ from Equation 7 increases near the zero crossing and energy is transferred to C4.
- The PFC NMOST drain capacitance $C_{d(PFC)}$ must be minimal
- Choose a relatively slow PFCCOMP time constant (10 Hz) for minimum distortion from the $2 \times f_{ac}$ bus voltage ripple.
- To use the full frequency operating range of the PFC controller, choose the highest possible for L_{PFC}. Move the valley hopping angle towards the zero crossings. The frequency at low mains and high mains must not cause ringing of the EMI filter.

6.3 PFC output voltage

The PFC output voltage $V_{bus(avg)PFCon}$ is set using a resistor divider between V_{bus} and the VOSENSE pin. In normal operation mode, V_{bus} is regulated so that $V_{VOSENSE}$ equals $V_{reg(VOSENSE)}$ at 2.5 V.

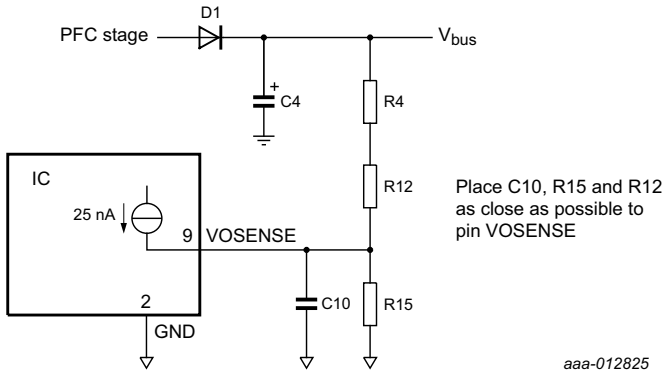


Fig 11. PFC output voltage setting

The VOSENSE pin has an integrated protection circuit and current $I_{prot(VOSENSE)}$ to detect an open circuit pin.

The bus electrolytic capacitor voltage $V_{bus(avg)PFCon}$ can be calculated with Equation 8:

$$V_{bus(avg)PFCon} = V_{reg(VOSENSE)}\left(\frac{R4 + R12 + R15}{R15} + 1\right) = 2.5\left(\frac{R4 + R12 + R15}{R15} + 1\right) \quad (8)$$

Where:

- $I_{prot(VOSENSE)}$ = 25 nA is neglected
- R15 advised < 120 kΩ

The PFC converter only operates nicely when:

$$V_{bus(avg)PFCon} > V_{mains}\ (RMS) \cdot \sqrt{2} + 10\ V \quad (9)$$

Always keep the bus voltage ripple below the bus capacitors voltage rating.

Capacitor C10 filters noise and prevents false triggering of protection modes because of MOSFET switching noise. False triggering of the $V_{ovp(VOSENSE)}$ protection can cause audible noise and disturbance of the AC mains input current.

A time constant between 500 μs and 1 ms at the VOSENSE pin is sufficient:

$$500\ \mu s < R15 \cdot C10 < 1\ ms \quad (10)$$

Place resistors R15 and R12 and capacitor C10 as close as possible to pin VOSENSE. Use the IC GND for resistor R15 and capacitor C10.

The OVP level is 5 % above regulation level which allows the average bus voltage to be close to the voltage rating of the capacitor. However, the allowed ripple on the bus capacitor is limited because of the OVP level. The minimum bus capacitor value is:

$$C4_{min} = \frac{V_{o(max)} \cdot I_{o(max)}}{4 \cdot \pi \cdot f_{ac(min)} \cdot V_{bus(avg)PFCon}^{2} \cdot \eta_{total}} \cdot \frac{V_{reg(VOSENSE)}}{V_{ovp(VOSENSE)} - V_{reg(VOSENSE)}} \quad (11)$$

6.4 Calculation of the PFC soft-start components

Soft-start and soft-stop are implemented using the R8 and C3 network that is connected to the PFCSENSE pin.

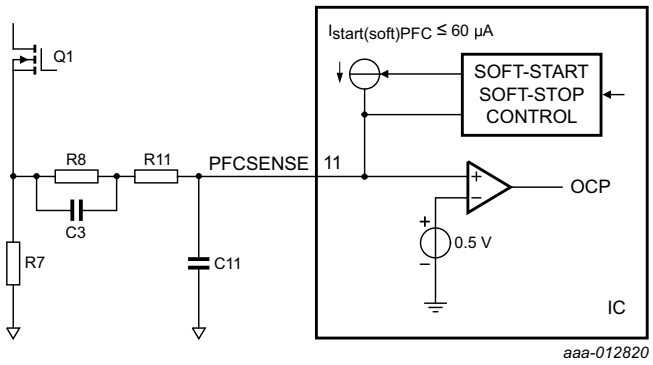


Fig 12. PFC soft-start and soft-stop

To enable PFC start-up, the total series resistance must be > 15 kΩ, so $V_{start(soft)PFC}$ = 0.5 V is reached.

$$R7 + R8 + R11 > 15\ k\Omega \quad (12)$$

The total soft-start time or soft-stop time is:

$$V_{start(soft)PFC} = R8 \cdot C3 \quad (13)$$

The PFCTIMER pin switching off PFC always ends with a soft-stop. However, there is an exception to this rule: no soft-stop occurs when $V_{ovp(VOSENSE)}$ is triggered.

Keep $t_{start(soft)PFC}$ within a range between 2 ms and 5 ms:

$$2\ ms < R8 \cdot C3 < 5\ ms \quad (14)$$

6.5 PFC demagnetization and valley detection

The PFC MOSFET is switched on after the PFC transformer is demagnetized. The internal circuitry connected to the PFCAUX pin detects the end of the secondary stroke. It also detects the voltage across the PFC MOSFET. The next primary stroke is started when the voltage across the PFC MOSFET is at its minimum level. Switching at the minimum voltage level (valley switching) reduces switching losses and EMI.

The maximum switching frequency of the PFC converter is limited to 400 kHz. One or more valleys are skipped to keep the frequency < 400 kHz.

When the PFCAUX pin does not detect demagnetization, the controller generates a Zero-Current Signal (ZCS) 48 µs (= $t_{to(demag)PFC}$) after the last PFC gate signal. When a valley signal is not detected on this pin, the controller generates a valley signal 4.2 µs (= $t_{to(vrec)PFC}$) after demagnetization was detected.

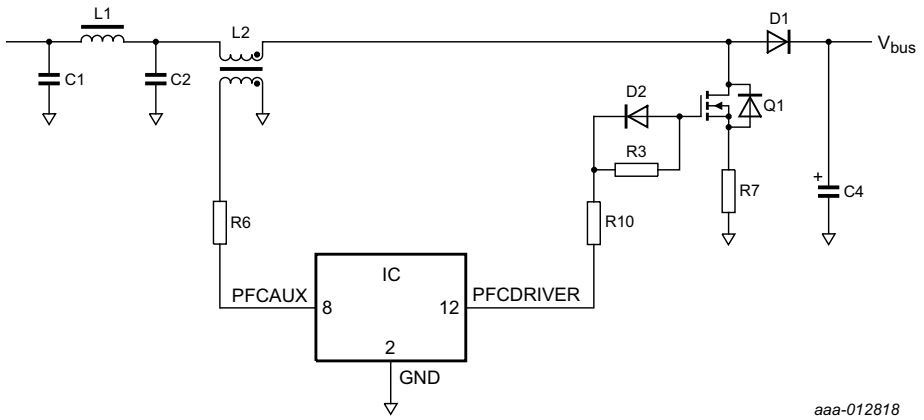


Fig 13. PFCAUX circuitry

6.5.1 PFCAUX winding and circuit design

V_{PFCAUX} must be as close as possible to the absolute maximum voltage rating of ±25 V of the PFCAUX pin. This setting ensures valley detection at low ringing amplitudes.

The maximum number of turns of the PFCAUX winding is calculated with Equation 15:

$$N_{aux(PFC)} < \frac{V_{PFCAUX(max)}}{V_{L(PFC)max}} \cdot N_{p(PFC)} \quad (15)$$

Where:

- $V_{PFCAUX(max)}$ is the absolute maximum rating of the PFCAUX pin (±25 V)
- $V_{L(PFC)max}$ is the maximum voltage across the PFC primary winding
- $N_{p(PFC)}$ is the number of turns of the PFC primary winding

The PFC output voltage V_{bus} during the PFC OVP conditions determines the maximum voltage across the PFC primary winding and is calculated with Equation 16:

$$V_{L(PFC)max} = \frac{V_{ovp(VOSENSE)}}{V_{reg(VOSENSE)}} \cdot V_{bus(avg)PFCon} = \frac{2.62\ V}{2.5\ V} \cdot V_{bus(avg)PFCon} = 1.048 \cdot V_{bus(avg)PFCon} \quad (16)$$

Where:

- $V_{bus(avg)PFCon}$ is the average bus voltage when the PFC is enabled

Place a resistor voltage divider between the auxiliary winding and the PFCAUX pin when a PFC coil with a higher number of auxiliary turns is used. The total resistive value of the divider must be < 10 kΩ to prevent a valley detection delay due to parasitic capacitance.

The polarity of the signal at the PFCAUX pin is reversed compared to the PFC MOSFET drain signal.

To protect against electrical overstress during lightning surge events, always add a 5 kΩ resistor between the PFC auxiliary winding and the PFCAUX pin. To prevent incorrect valley switching of the PFC because of external disturbances, place the resistor as close as possible to the IC.

6.6 PFC on/off

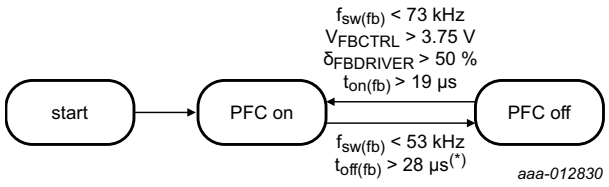
The advantages of PFC on/off functionality are:

- Disabled: improvement of overall efficiency at low output power
- Enabled: improvement of power factor and harmonics of the line current

In FR mode, the auto PFC on/off control mainly depends on $f_{sw(fb)}$. $f_{sw(fb)}$ is a result of:

- Primary flyback inductance
- Output power
- Output voltage

Figure 14 shows the conditions to switch on/off the PFC (FR mode only).



* For this condition the PFCTIMER is ignored. V_{FBCTRL} > 3.75 V overrules this condition.

Fig 14. Automatic PFC on/off state transition

The application can overrule the automatic PFC on/off (see Section 6.6.1.2).

Remark: $V_{VINSENSE} < V_{stop(VINSENSE)}$ disables PFC switching anytime.

$L_{p(fb)}$ must not exceed $L_{p(fb)max}$ to ensure active PFC at output power $P_{o(PFC)swon}$.

$$L_{p(fb)max} = \frac{1}{\left[\sqrt{\left(\frac{2 \cdot P_{o(PFC)swon} \cdot f_{sw(fb)swon(PFC)}}{\eta_{fb}}\right)}\left(\frac{1}{V_{bus(min)PFCoff}} + \frac{1}{N_{fb}V_o}\right) + f_{sw(fb)swon(PFC)}\pi\sqrt{C_{d(fb)}}\right]^2} \quad (17)$$

Where:

- $f_{sw(fb)swon(PFC)}$ is 73 kHz
- η_{fb} is the flyback controller efficiency, typically 0.95
- $V_{bus(min)PFCoff}$ is the minimum mains voltage (AC) when the PFC is off
- N_{fb} is flyback turns ratio $N_{p(fb)}/N_{s(fb)}$
- V_o is the output voltage
- $P_{o(PFC)swon}$ is the output power at which the PFC must be enabled
- $C_{d(fb)}$ is the total capacitance on the drain of the flyback switch

In a typical LED driver, the V_o varies from $V_{o(min)}$ to $V_{o(max)}$. $f_{sw(fb)swon(PFC)}$ is lower at $V_{o(min)}$ because of the longer $t_{off(fb)}$ time. $N_{fb}V_{o(min)}$ must be used in Equation 17.

If the PFC is off, the peak of $V_{mains(min)}$ must trigger PFC on transition. In Figure 15 the expected bus voltage waveform is shown for $P_{o(PFC)swon}$ at $V_{mains(rms)min}$ = 85 V (AC).

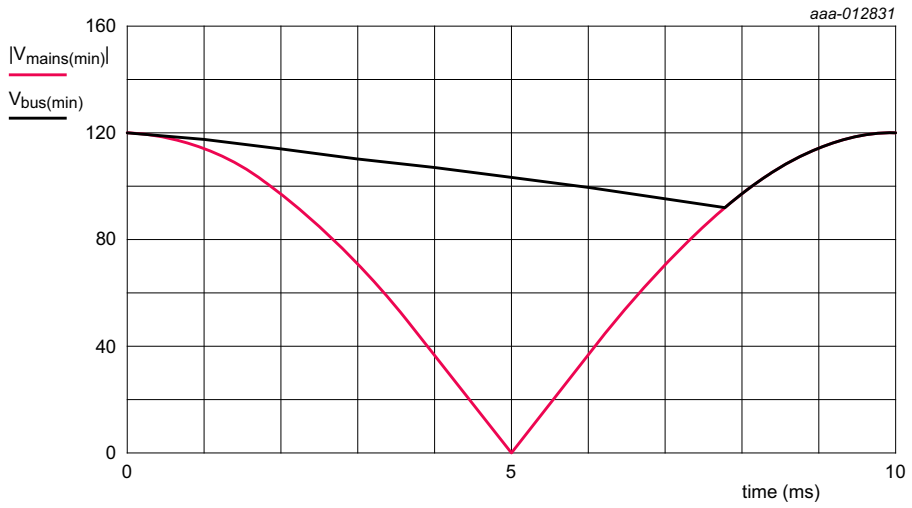


Fig 15. $V_{bus(min)}$ waveform with PFC disabled at $P_{o(PFC)swon}$

Substitution of the known variables results in Equation 18 for $L_{p(fb)max}$.

$$L_{p(fb)max} = \frac{1}{\left[\left(\sqrt{\frac{2 \cdot 73\ kHz \cdot P_{o(PFC)on}}{\eta_{fb}}}\right) \cdot \left(\frac{1}{V_{mains(rms)min}\sqrt{2}} + \frac{1}{N_{fb}V_{o(min)}}\right) + 73\ kHz \cdot \pi \cdot \sqrt{C_{d(fb)}}\right]^2} \quad (18)$$

Where:

- $V_{mains(rms)min}$ is the minimum RMS mains voltage (AC)
- $V_{o(min)}$ is the minimum output voltage

The primary inductance must be:

$$L_{p(fb)} < L_{p(fb)max} \quad (19)$$

6.6.1 PFCTIMER pin circuit

When the output power drops to below the PFC switch-off level, the PFCTIMER pin delays the PFC switch-off. The switch-off delay prevents that the PFC repeatedly switches on and off due to fast, large, dynamic load changes. It results in reduced audible noise.

Different pin applications can overrule the PFCTIMER pin switching on/off automatically.

6.6.1.1 Automatic PFC on/off

The default application of the SSL8516T enables automatic PFC on/off functionality.

A capacitor connected to an internal current source determines the PFC switch-off delay time $t_{d(PFC)swoff}$. Capacitor C9 is charged from 0 V to 3 V during the delay time. The PFC typically switches off using a soft-stop when $V_{PFCTIMER}$ > 3 V.

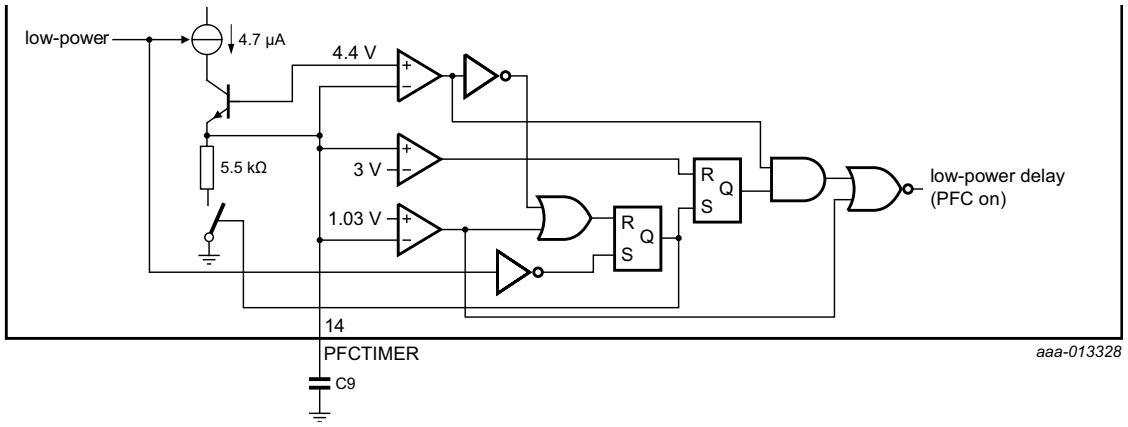


Fig 16. PFCTIMER pin circuit

Equation 20 shows how to calculate $t_{d(PFC)swoff}$:

$$t_{d(PFC)swoff} = C9\frac{V_{stop(PFCTIMER)}}{I_{source(PFCTIMER)}} = C9\frac{3\ \text{V}}{4.7\ \mu A} \quad (20)$$

Where:

- The PFCTIMER capacitor C9 must be > 1 nF

When the PFC is switched on, the IC discharges capacitor C9.

An output power below the $P_{o(PFC)swoff}$ level for a short time results in the charging of capacitor C9. However, if $V_{PFCTIMER}$ remains under 3 V, the capacitor immediately discharges when $P_o > P_{o(PFC)swoff}$. The PFCDRIVER signal operates continuously during these load changes at the output (see Figure 17).

When $P_o < P_{o(PFC)swoff}$ during a time that allows $V_{PFCTIMER}$ to exceed 3 V, the PFC switches off.

When $P_o > P_{o(PFC)swon}$, the PFC switches on immediately and capacitor C9 is discharged.

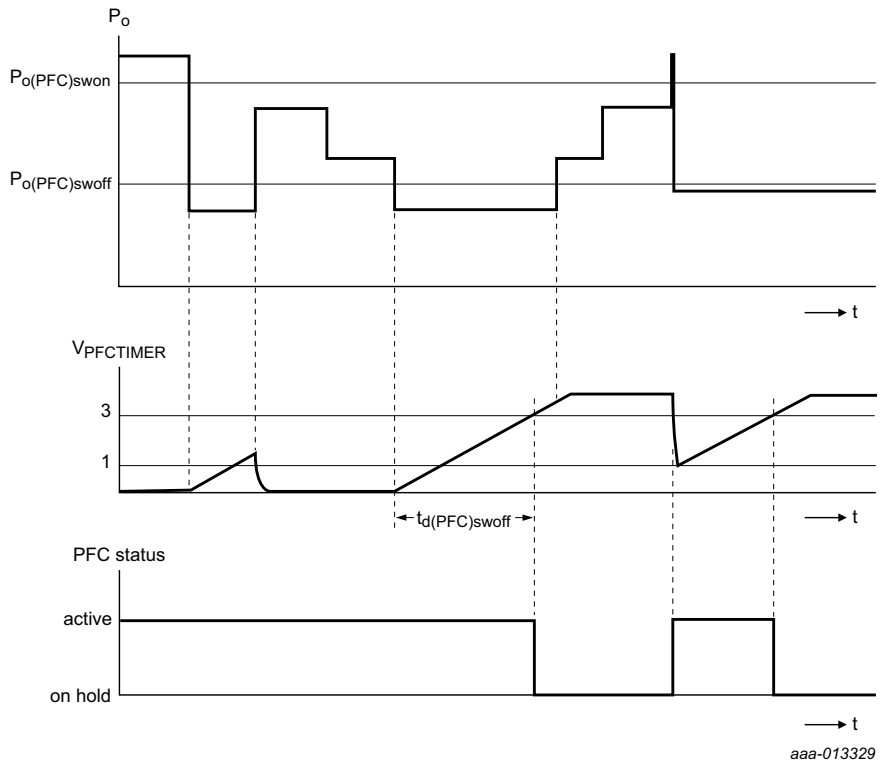


Fig 17. PFCTIMER pin waveform

6.6.1.2 Overruling automatic PFC on/off

The PFC controller is typically switched on or switched off using the filtered flyback operating frequency. However, if necessary, the PFCTIMER allows override of this functionality. The conditions for overruling the PFCTIMER are:

- $V_{PFCTIMER}$ < 1.0 V: PFC is on
- $V_{PFCTIMER}$ > 4.4 V: PFC is off

For applications that require the PFC to be on all the time, a 0 Ω resistor can replace capacitor C9.

If a dynamic control signal is used to operate the PFCTIMER pin, the recommended C9 capacitor value is 1 nF. This value results in the shortest PFCTIMER pin response time to an external control signal. Correct timing is important if an external dynamic signal is used to override the PFC, especially when switching on the PFC.

Operate $V_{PFCTIMER}$ close to 4.6 V ($V_{th(off)PFCTIMER(max)}$) when the PFC is switched off. It minimizes the external driver current required to override the PFC and it allows a fast response to the external PFC switch-on signal.

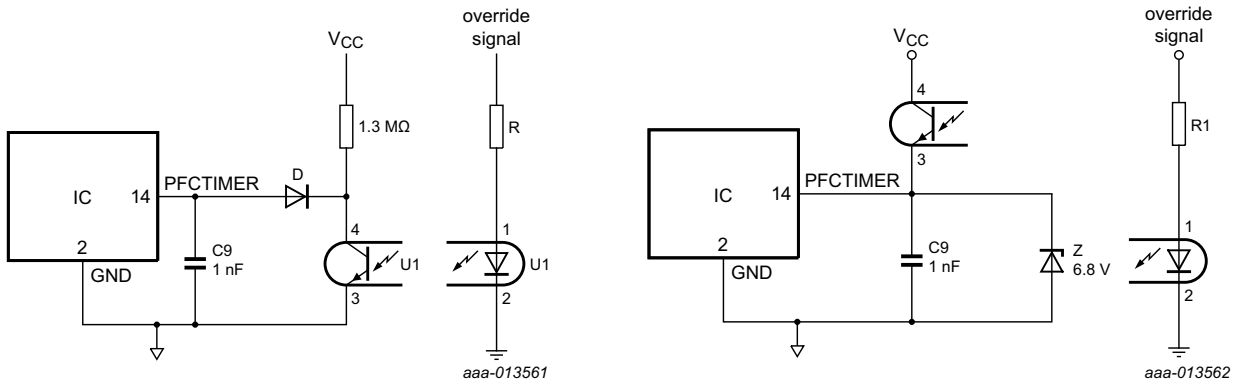
To force PFC on, sink current out of PFCTIMER pin:

$$I_{PFCTIMER} \gg 4.7\ \mu A \tag{21}$$

To force a PFC switch-off, source current into PFCTIMER pin:

$$I_{PFCTIMER} > \frac{V_{th(off)PFCTIMER(max)}}{R_{sink(PFCTIMER)min}} \Rightarrow I_{PFCTIMER} > \frac{4.6\ V}{4\ k\Omega} \Rightarrow I_{PFCTIMER} > 1.15\ mA \quad (22)$$

Figure 18 shows two example circuits to overrule the auto PFC on/off functionality. The optocoupler transistor operates as a current source. The constant current through the optocoupler diode determines its output transistor current setting. Both examples can handle optocoupler dark current up to 10 μA.



a. Force PFC on

b. Force PFC off

Fig 18. PFC override control examples

7. Protections

7.1 VOSENSE OverVoltage Protection (OVP)

V_{bus} overshoot occurs on C4 at the initial start-up and in case of large load steps. The relative slow response of the PFC control loop causes this overvoltage. The PFC control loop response must be slow to guarantee a good power factor and MHR performance. The VOSENSE pin OVP limits the overvoltage on C4.

If $V_{ovp(VOSENSE)}$ is triggered, the PFC MOSFET is switched off immediately regardless of the on-time setting. The switching of the PFC MOSFET is inhibited until $V_{VOSENSE}$ < 2.62 V. OVP is triggered when the resistor between the VOSENSE pin and ground is open (due to a fault). The maximum bus voltage $V_{bus(max)}$ during overshoot is:

$$V_{bus(max)} = \frac{V_{ovp(VOSENSE)}}{V_{reg(VOSENSE)}} \cdot V_{bus(avg)PFCon} = \frac{2.62\ V}{2.5\ V} \cdot V_{bus(avg)PFCon} = 1.048 \cdot V_{bus(avg)PFCon} \quad (23)$$

Where:

- $V_{bus(avg)PFCon}$ is the average bus voltage when the PFC is on.

7.2 VOSENSE open and short pin detection

The VOSENSE pin has an integrated protection circuit to detect an open and short circuited pin. The VOSENSE pin also senses open resistors in the voltage divider. It is not required to add an external OVP circuit for the PFC.

When the pin is open, an internal current source $I_{prot(VOSENSE)}$ charges the VOSENSE pin. The PFC stops switching when $V_{VOSENSE} > V_{ovp(VOSENSE)}$. An internal voltage clamp limits $V_{VOSENSE}$. The same condition applies when only resistor R15 is open.

The PFC is not switching when $V_{VOSENSE} < V_{th(stop)VOSENSE}$. This condition is applicable when the VOSENSE pin is shorted to ground or if resistor R4 or R12 is open.

7.3 VINSENSE open pin detection

The VINSENSE pin has a protection circuit to detect an open pin. An internal current source $I_{I(VINSENSE)}$ pulls down the pin < $V_{stop(VINSENSE)}$ when the pin is open.

7.4 OverCurrent Protection (OCP)

The overcurrent protection limits the maximum current through the PFC MOSFET. The current is sensed with resistor R7 in series with the MOSFET source. The MOSFET is switched off immediately when $V_{PFCSENSE} > V_{sense(PFC)max}$. OCP is a cycle-by-cycle protection.

To avoid false triggering of the PFC OCP by the flyback converter switching noise, keep a margin of 100 mV. False triggering of PFC OCP causes disturbance to the AC mains input current. To suppress any external disturbance, place a small capacitor C11 of between 100 pF and 220 pF next to the PFCSENSE pin.

$$100\ pF < C11 < 220\ pF \tag{24}$$

The current sense resistor R7 can be calculated with Equation 25:

$$R7 = \frac{V_{sense(PFC)max} - V_{margin}}{I_{pk(PFC)max}} = \frac{0.495\ V - 0.1\ V}{I_{pk(PFC)max}} \tag{25}$$

Where:

- $I_{pk(PFC)max}$ is the maximum PFC peak current at the high output load and low mains while the PFC operates in QR mode.

The maximum peak current for the PFC operating in Quasi-Resonant (QR) mode is calculated using Equation 26:

$$I_{pk(PFC)max} = \frac{2\sqrt{2}P_{i(max)} \cdot 1.1}{V_{mains(rms)min}} = \frac{2\sqrt{2}\frac{P_{o(max)}}{\eta_{total}} \cdot 1.1}{V_{mains(rms)min}} \tag{26}$$

Where:

- $P_{o(max)}$ is the maximum output power of the flyback.
- A factor 1.1 is used to compensate the dead time between zero-current in the PFC inductor at the end of the secondary stroke and the detection of the first valley in quasi-resonant mode.
- η_{total} is the expected efficiency of the total converter at maximum output power at low mains. Use 90 % for the initial design.
- $V_{mains(rms)min}$ is the minimum RMS mains input voltage.

8. Flyback description

8.1 Flyback operation modes

At initial start-up, the flyback controller starts at the maximum output power. So the system starts in Quasi-Resonant (QR) mode. The flyback controller passes through three operation modes from maximum to minimum output power (see Figure 19):

- Quasi-Resonant (QR) mode
- Discontinuous Conduction Mode (DCM)
- Frequency Reduction (FR) mode

The internal demagnetization detection and valley switching circuitry is active in all operating modes.

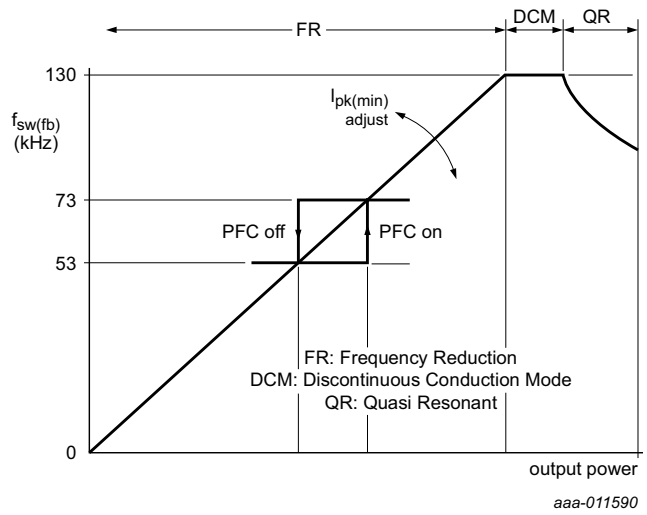


Fig 19. Flyback operation modes

The SSL8516T flyback controller waits until the transformer is demagnetized and at least one valley has appeared before it is magnetized again for the next cycle.

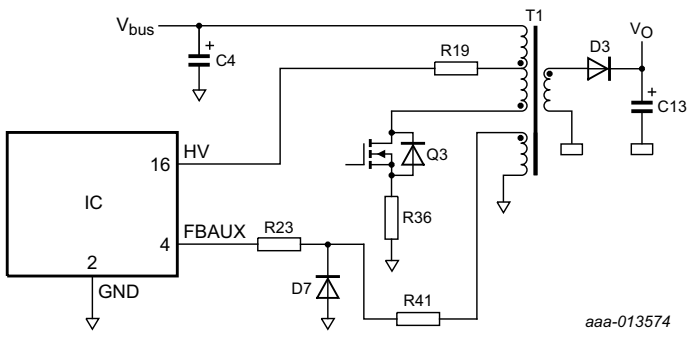


Fig 20. HV pin and FBAUX pin

The FBAUX pin detects demagnetization via the auxiliary winding. The HV pin detects the bottom of the valley via the drain of the MOSFET or the central tap of the primary winding.

The power conversion can be calculated with Equation 27:

$$P_o = \frac{1}{2} \cdot L_{p(fb)} \cdot I_{pk(fb)}^{2} \cdot f_{sw(fb)} \cdot \eta_{fb} \quad (27)$$

Where:

- $L_{p(fb)}$ is the flyback transformer primary inductance
- $I_{pk(fb)}$ is the flyback transformer primary peak current
- $f_{sw(fb)}$ is the flyback controller operating frequency
- η_{fb} is the flyback controller efficiency

$L_{p(fb)}$ is selected at the start of the design. $I_{pk(fb)}$ is regulated to meet the output power demand in QR and DCM mode. The switching frequency $f_{sw(fb)}$ is a result of external application parameters and IC parameters.

External application parameters:

- Transformer turns ratio N_{fb}
- Primary inductance $L_{p(fb)}$
- Drain source capacitance of the flyback switch $C_{d(fb)}$
- Input voltage V_{bus} of the flyback stage
- Output voltage V_o
- Control loop feedback signal V_{FBCTRL}

IC parameters:

- Oscillator setting
- Peak current setting
- Demagnetization detection
- Valley detection

8.1.1 Quasi-Resonant (QR) mode

The flyback operates in QR mode at high and maximum output power. The peak current control sets the output power P_o. Reducing $I_{pk(fb)}$ results in a lower P_o and a higher operating frequency until $f_{sw(fb)max}$ is reached. QR mode can easily be recognized. The primary switching cycle starts at the bottom of the first valley and $V_{sense(fb)} > 232$ mV.

The V_{FBCTRL} pin sets the primary peak current $I_{pk(fb)}$ limit level $V_{sense(fb)}$.

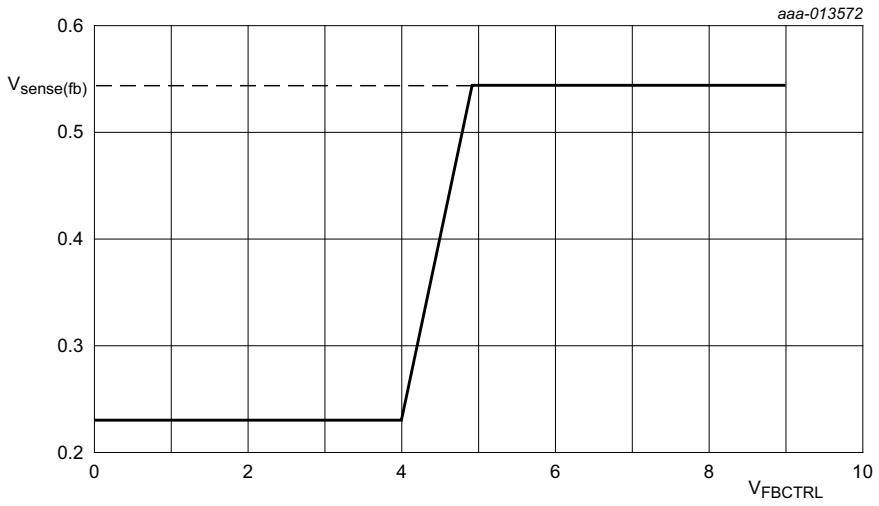


Fig 21. $V_{sense(fb)}$ setting as function of V_{FBCTRL}

In QR mode, the PFC switch-off timer is never started.

Equation 28 shows the relationship between the $V_{sense(fb)}$ voltage and the flyback peak current:

$$I_{pk(fb)} = \frac{V_{R36}}{R36} = \frac{V_{sense(fb)} - V_{R29} - V_{R30} - V_{R31}}{R36}$$
$$\Rightarrow I_{pk(fb)} = \frac{V_{sense(fb)} - I_{adj(FBSENSE)}(R29 + R30) - (I_{adj(FBSENSE)} + I_{R20}) \cdot R31}{R36} \quad (28)$$

Where:

- $V_{sense(fb)}$ varies between 232 mV and 545 mV
- $I_{adj(FBSENSE)}$ is a 2.1 μA current source inside the IC; connected to pin FBSENSE
- $I_{R20} \approx V_{bus} / R20$

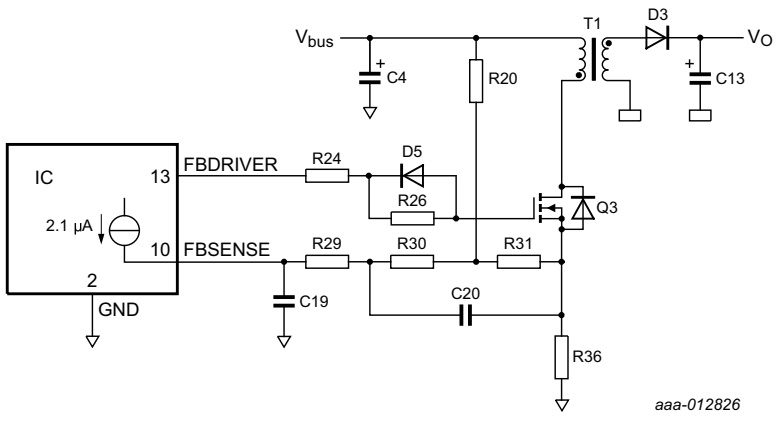


Fig 22. Flyback adjustment circuit

8.1.2 Discontinuous Conduction Mode (DCM)

P_o decreases when $I_{pk(fb)}$ is reduced and more than one valley is skipped. It results in $f_{sw(fb)}$ operating just below $f_{sw(fb)max}$ (130 kHz). The operating mode switches from DCM to FR mode at V_{FBCTRL} equals $V_{start(red)f}$ (4.0 V).

Sometimes DCM is not reached when the selected primary inductance of the inductor is high. In this case, flyback skips DCM when it is reducing power. It jumps directly from QR mode to FR mode.

In DCM, the PFC switch-off timer is not started.

8.1.3 Frequency reduction and PFC on/off control

At medium and low output power, $I_{pk(fb)}$ is fixed. The operating frequency controls P_o. P_o and $f_{sw(fb)}$ are linearly related during this type of control. In this application note, it is called operating in Frequency Reduction (FR) mode. The minimum switching frequency in FR mode is 0 Hz.

In FR mode, V_{FBCTRL} does not set the peak current. It sets the operating frequency. The minimum primary peak current $I_{pk(fb)min}$ through the $L_{p(fb)}$ is kept constant in FR mode.

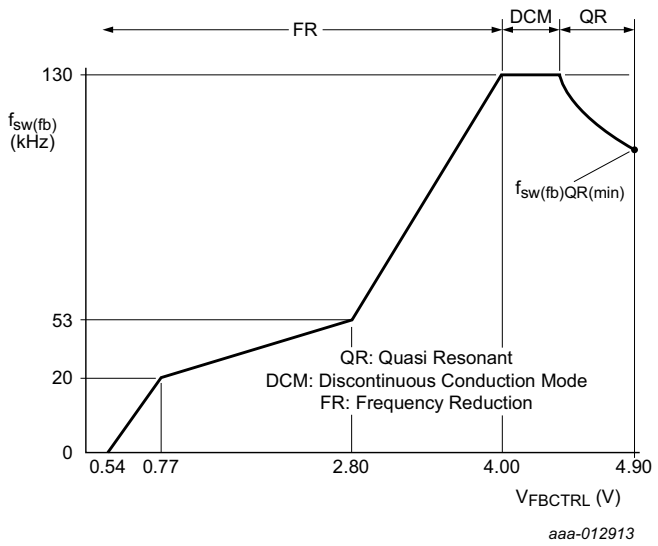


Fig 23. Flyback frequency control

The ratio $I_{pk(fb)min}$: $I_{pk(fb)max}$ mainly depends on the sense resistor R36 and R30 assuming that the core does not saturate at $I_{pk(fb)max}$. Decreasing the output power reduces the operating frequency. As a result of the frequency limit, more valleys are skipped.

Only in FR mode, $f_{sw(fb)}$ determines when the PFC is on or off.

8.2 Flyback protections

8.2.1 Short circuit at the FBCTRL pin

If the FBCTRL pin is shorted to ground, switching of the flyback controller is inhibited.

8.2.2 Open FBCTRL pin

Pin FBCTRL connects to an internal 7 V voltage source (see Figure 24) via an internal 13.2 kΩ resistor and a series switch. When V_{FBCTRL} > 5.5 V, the series switch opens and the 13.2 kΩ resistor disconnects. Pin FBCTRL is biased with 29 μA $I_{to(FBCTRL)}$.

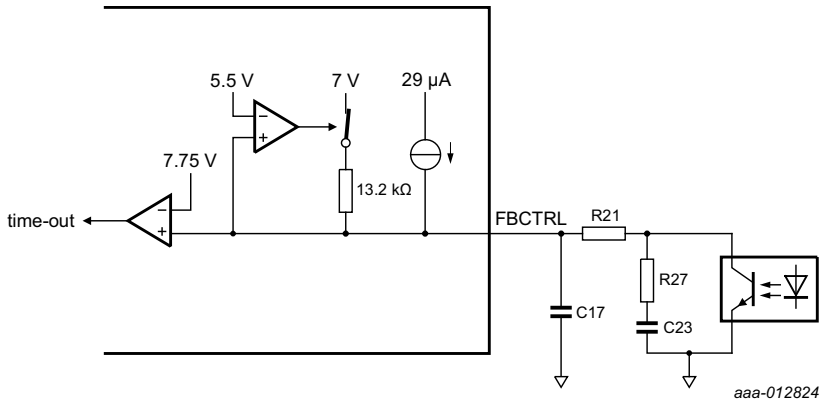
When V_{FBCTRL} > 7.75 V, a fault is assumed. The flyback and PFC switches are switched off and a safe restart is initiated. An internal pull-down switch on the FBCTRL pin is activated during the safe restart.

8.2.3 Time-out flyback control loop

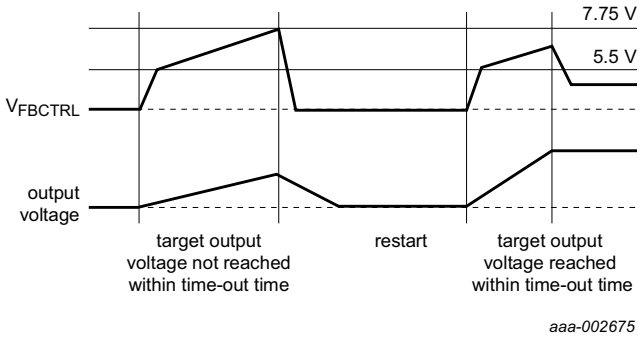
A time-out function is set using resistor R27 and capacitor C23 to protect against the following faults:

- Output short circuit at initial start-up
- Open flyback control loop

The time-out protection initiates a safe restart.



a. Circuit diagram



b. Timing diagram

Fig 24. Flyback time-out protection

A noise filter (C17 = 220 pF; R21 = 10 Ω) located close to pin FBCTRL avoids interference by PFC MOSFET switching or HF noise (e.g. GSM phone). Resistor R27 and capacitor C23 set the time delay for V_{FBCTRL} to reach 7.75 V. Resistor R27 is required to separate the relatively high-value time-out capacitor C23 from the control loop response. The value of resistor R27 must be > 30 kΩ.

The flyback time-out time $t_{to(fb)}$ can be calculated with Equation 29:

$$t_{to(fb)} = C23 \cdot \frac{\Delta V_{to(FBCTRL)}}{I_{to(FBCTRL)}} - R27 \cdot C23 \cdot ln\left(\frac{I_{to(FBCTRL)} \cdot R27}{V_{to(FBCTRL)en}}\right) \quad (29)$$

Where:

- $\Delta V_{to(FBCTRL)} = V_{to(FBCTRL)trip} - V_{to(FBCTRL)en} = 7.75 - 5.5 = 2.25$ V

If the flyback time-out protection is not required (e.g. for testing or debugging purposes), it can be disabled. Place a 180 kΩ resistor between pin FBCTRL and ground.

8.2.4 Flyback OverVoltage Protection (OVP)

To disable both controllers when overvoltage is detected at the output of the flyback, the IC has an internal OVP circuit.

The voltage on the flyback transformer secondary winding during the secondary stroke is a reflection of the output voltage plus the voltage of the secondary rectifier.

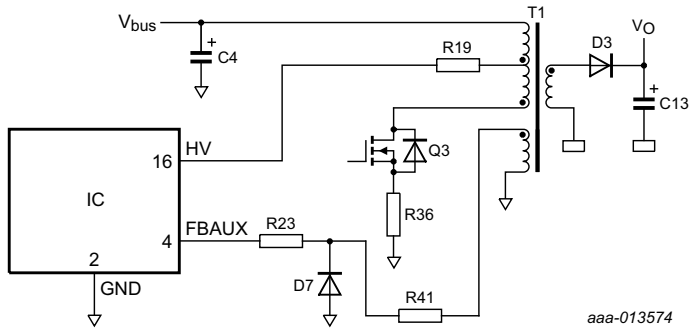
During the secondary stroke, the voltage on the auxiliary $V_{aux(T1)}$ winding equals:

$$V_{aux(T1)} = (V_o + V_{rectifier}) \cdot \frac{N_{aux(fb)}}{N_{s(fb)}} \quad (30)$$

Where:

- V_o is the output voltage
- $V_{rectifier}$ is the voltage across the output rectifier when conducting
- $N_{aux(fb)}$ is the number of auxiliary turns
- $N_{s(fb)}$ is the number of secondary turns

The total series resistance R23 + R41 located between the auxiliary winding and the FBAUX pin converts $V_{aux(T1)}$ to current in pin FBAUX.



R_{ovp} = R23 + R41

Fig 25. Flyback OVP circuit

An internal integrator filters noise and spikes. The output of the integrator connects to a counter. The counter prevents false OVP detection which can occur during ESD or lightning events.

The OVP condition is met when I_{FBAUX} > 300 μA. If the internal integrator detects OVP, the counter increases by one. If OVP is detected during the next switching cycle, the counter increases by one again. If no OVP is detected during the next switching cycle, the counter decreases by two. (The minimum value is zero.) If the counter reaches six, the IC assumes a true overvoltage.

Both converters are switched off immediately and a safe restart is initiated.

The OVP level can be calculated with Equation 31:

$$R23 + R41 = \frac{\left(\frac{N_{aux(fb)}}{N_{s(fb)}}\right) \cdot (V_{o(ovp)} + V_{rectifier}) - V_{clamp(FBAUX)}}{I_{ovp(FBAUX)}}$$

$$\Rightarrow R41 = \frac{\left(\frac{N_{aux(fb)}}{N_{s(fb)}}\right) \cdot (V_{o(ovp)} + V_{rectifier}) - 0.92}{300\ \mu A} - 10\ k\Omega \quad (31)$$

Where:

- $N_{s(fb)}$ is the number of turns on the secondary winding
- $N_{aux(fb)}$ is the number of turns on the flyback transformer auxiliary winding
- $V_{o(ovp)}$ is the output voltage OVP level
- $V_{rectifier}$ is the forward voltage of the secondary rectifier (0.6 V for diode)
- $V_{clamp(FBAUX)}$ is pin FBAUX positive clamp voltage 0.92 V
- $I_{ovp(FBAUX)}$ is the OVP protection level
- R23 is 10 kΩ placed close to the IC pin

To avoid OVP triggering in normal operation, take the tolerances on $I_{ovp(FBAUX)}$ into account for $V_{o(ovp)}$ calculation.

The maximum series resistance calculation is based on the demagnetization threshold.

$$R_{ovp} < \frac{V_{th(comp)FBAUX(min)}}{I_{prot(FBAUX)min}} = \frac{60\ mV}{65\ nA} = 923\ k\Omega \quad (32)$$

Keep some margin and keep R_{ovp} < 650 kΩ. Higher values can cause slow output voltage rise during initial start-up which can trigger the time-out protection because the demagnetization function is disturbed.

8.2.5 OverPower Protection (OPP)

The SSL8516T is a fixed boost PFC controller. So the OPP is not required when using the default application where $V_{bus(avg)PFCon}$ is fixed over the full mains voltage range. Diode D7 and resistor R23 disable the OPP (see Figure 26). The current flowing out of pin FBAUX is limited to < 100 μA.

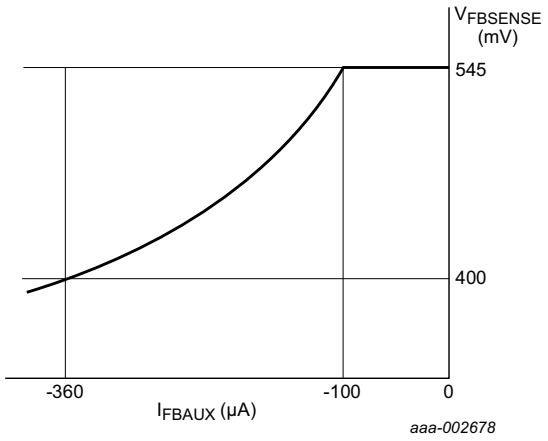


Fig 26. OPP level adjustment

9. Large signal component values calculation

Table 3 shows the initial requirements of an LED driver as example.

Table 3. Initial design requirements

Requirement	Symbol	Choice	Example
low input voltage	$V_{ac(rms)min}$	90 V (AC)	100 V; −10 % margin
high input voltage	$V_{ac(rms)max}$	305 V (AC)	277 V; +10 % margin THD at 305 V (AC) can be compromised when a 450 V bus capacitor is used
output voltage	$V_{o(min)}$ $V_{o(max)}$	16 V 48 V	$V_{o(max)} : V_{o(min)} = 3 : 1$
output current	$I_{o(min)}$ $I_{o(max)}$	160 mA 1.6 A	75 W; 10 % dimmable LED driver
holdup time	t_{holdup}	0 ms	lower output capacitance and bus capacitance can be used when no hold up time is required
flyback MOSFET voltage rating	$V_{DS(fb)max}$	800 V	allows high $N_{fb}V_o$: • lower voltage stress on the secondary rectifier • less turn on losses due to deeper valley
fast transient support	-	no (CC output)	a smaller C_{bus} can be used when no transient support is required when PFC is switched off

9.1 Bus capacitor

For the bus capacitor value calculation, several constraints apply:

- Voltage rating
- OVP level on the VOSENSE pin
- Holdup time
- Auto PFC on/off with load step support

9.1.1 Voltage rating

The target is to use a single 450 V bus capacitor C4.

- $V_{C4(max)} = 450\ V$
- $V_{bus(avg)PFCon} = V_{mains(rms)max} \cdot \sqrt{2} = 305\sqrt{2} = 431\ V$
- $V_{bus(ripple)pp(max)} = 2(V_{C4(max)} - V_{bus(avg)PFCon}) = 38\ V$

The minimum bus capacitance due to the allowed voltage ripple based on the C4 voltage rating is:

$$C4_{rating} = \frac{V_{o(max)} \cdot I_{o(max)}}{2 \cdot \pi \cdot f_{ac(min)} \cdot V_{bus(ripple)pp(max)} \cdot V_{bus(avg)PFCon} \cdot \eta_{total}}$$

$$\Rightarrow C4_{rating} = \frac{48 \cdot 1.6}{2 \cdot \pi \cdot 50 \cdot 38 \cdot 431 \cdot 0.9} = 16.6\ \mu F \quad (33)$$

Where:

- $f_{ac(min)}$ is the minimum mains frequency 50 Hz
- η_{total} is the total efficiency

9.1.2 OVP level on the VOSENSE pin

The minimum bus capacitance due to OVP on the VOSENSE pin is:

$$C4_{ovp} = \frac{V_{o(max)} \cdot I_{o(max)}}{4 \cdot \pi \cdot f_{ac(min)} \cdot V_{bus(avg)PFCon}^{2} \cdot \eta_{total}} \cdot \frac{V_{reg(VOSENSE)}}{V_{ovp(VOSENSE)} - V_{reg(VOSENSE)}}$$
$$\Rightarrow C4_{ovp} = \frac{48 \cdot 1.6}{4 \cdot \pi \cdot 50 \cdot 431^{2} \cdot 0.9} \cdot \frac{2.5}{2.62 - 2.5} = 15.3\ \mu F \quad (34)$$

9.1.3 Holdup time

The minimum capacitance due to the holdup time requirement is:

$$C4_{holup} = \frac{\frac{2 \cdot V_{o(max)} \cdot I_{o(max)}}{\eta_{fb}} \cdot t_{holdup}}{\left(V_{bus(avg)PFCon} - \frac{V_{bus(ripple)pp(max)}}{2}\right)^{2} - V_{bus(holdup)min}^{2}}$$
$$\Rightarrow C4_{holdup} = \frac{\frac{2 \cdot 48 \cdot 1.6}{0.95} \cdot 0}{\left(431 - \frac{38}{2}\right)^{2} - 100^{2}} = 0\ \mu F \quad (35)$$

Where:

- $V_{bus(holdup)min}$ is the minimum bus voltage at which the flyback stage can still transfer $P_{o(max)}$, typically between 60 V and 100 V
- η_{fb} is the flyback efficiency (assumption: 0.95)

9.1.4 Auto PFC on/off

Here is a rule of thumb for the minimum bus capacitance supporting auto PFC on/off function and wide mains applications with certain load step requirements:

- Constant current LED drivers 0.3 µF/W (smooth load steps):

  $C4_{PFConoff} = 0.3\ \mu F \cdot P_{o(max)}$

- Constant voltage LED drivers 1.0 µF/W (large load steps):

  $C4_{PFConoff} = 1.0\ \mu F \cdot P_{o(max)}$

Transient step response support is not required (see Table 3):

$$\Rightarrow C4_{PFConoff} = 0.3\ \mu F \cdot P_{o(max)} = 0.3 \cdot 48 \cdot 1.6 = 23\ \mu F \quad (36)$$

$$C4 > max(C4_{ripple}, C4_{ovp}, C4_{holdup}, C4_{PFConoff})$$
$$\Rightarrow C4 > max(16.6, 15.3, 0, 23) > 23\ \mu F \quad (37)$$

The value chosen for capacitor C4 is 22 μF.

The recalculated peak-to-peak bus voltage ripple with the selected bus capacitor C4 is:

$$V_{bus(ripple)pp} = \frac{P_{o(max)}}{2 \cdot \pi \cdot f_{ac(min)} \cdot C4 \cdot V_{bus(avg)PFCon} \cdot \eta_{total}}$$
$$\Rightarrow V_{bus(ripple)pp} = \frac{48 \cdot 1.6}{2 \cdot \pi \cdot 50 \cdot 22\ \mu F \cdot 431 \cdot 0.9} = 28.6\ V \quad (38)$$

The final bus voltage with the selected bus capacitor C4 can be set:

$$V_{bus(nom)} = V_{c4(max)} - \frac{V_{bus(ripple)pp}}{2} = 450 - \frac{28.6}{2} = 435\ V \quad (39)$$

9.2 PFC inductance

The minimum PFC switching frequency requirement at full load determines the maximum PFC inductance. At low line, the primary stroke is dominant and at high mains the secondary stroke is dominant, both conditions must be checked:

$$L_{PFC(lowline)} = \frac{V_{mains(rms)min}^{2} \cdot (V_{bus(nom)} - \sqrt{2} \cdot V_{mains(rms)min})}{2 \cdot f_{sw(PFC)min} \cdot \frac{P_{o(max)}}{\eta_{total}} \cdot V_{bus(nom)}}$$
$$\Rightarrow L_{PFC(lowline)} = \frac{90^2 \cdot (435 - \sqrt{2} \cdot 90)}{2 \cdot 20\ kHz \cdot \frac{48 \cdot 1.6}{0.9} \cdot 435} = 1.679\ mH \quad (40)$$

Where:

- $f_{sw(PFC)min}$ (minimum PFC switching frequency) = 20 kHz

$$L_{PFC(highline)} = \frac{V_{mains(rms)max}^{2} \cdot (V_{bus(nom)} - \sqrt{2} \cdot V_{mains(rms)max})}{2 \cdot f_{sw(PFC)min} \cdot \frac{P_{o(max)}}{\eta_{total}} \cdot V_{bus(nom)}}$$
$$\Rightarrow L_{PFC(highline)} = \frac{300^2 \cdot (435 - \sqrt{2} \cdot 300)}{2 \cdot 20\ kHz \cdot \frac{48 \cdot 1.6}{0.9} \cdot 435} = 803\ \mu H \quad (41)$$

$$L_{PFC} < min(L_{PFC(lowline)}, L_{PFC(highline)}) < 803\ \mu H \quad (42)$$

9.3 Reflected output voltage

The reflected output voltage V_r (equals $N_{fb}V_o$) is a compromise between the flyback MOSFET voltage rating $V_{DS(fb)max}$ and secondary rectifier reverse voltage rating.

- High N_{fb}: More voltage stress on the flyback MOSFET
- Low N_{fb}: More voltage stress on secondary rectifier

The leakage inductance of the flyback transformer generates a ringing voltage on the drain at switch-off. Allow at least 20 % of the $V_{DS(fb)max}$ margin as starting point.

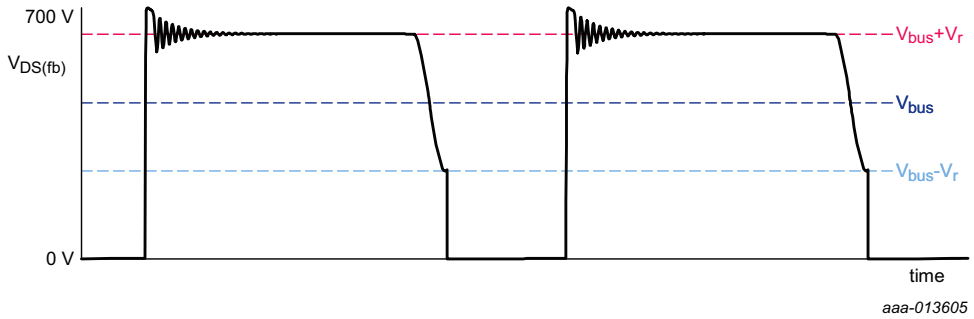


Fig 27. Flyback MOSFET drain voltage $V_{DS(fb)}$ with ringing

The reflected output voltage V_r is super-imposed on the V_{bus} during the secondary stroke.

$$0.8 \cdot V_{DS(fb)max} = V_{bus(max)} + V_r = V_{bus(max)} + N_{fb} \cdot V_{o(max)} = V_{bus(max)} + \frac{N_{p(fb)}}{N_{s(fb)}} \cdot V_{o(max)} \quad (43)$$

Where:

- $V_{DS(fb)max}$ is the flyback MOSFET maximum drain source voltage
- $V_{bus(max)}$ is the maximum bus voltage
- V_r is the reflected output voltage
- $V_{o(max)}$ is the maximum output voltage

The peak voltage during ringing in applications can be minimized with the flyback clamp circuit with diode D4, resistor R16, and capacitor C12.

9.3.1 Primary flyback inductance ($L_{p(fb)}$)

At full power, the system must operate in QR mode at the highest efficiency possible. The results is an optimized transformer design with accompanying $I_{sat(fb)}$, $L_{p(fb)}$, and $f_{sw(fb)QR(min)}$. So, the flyback inductance is selected based on the desired minimum operating frequency in QR mode at $P_{o(max)}$.

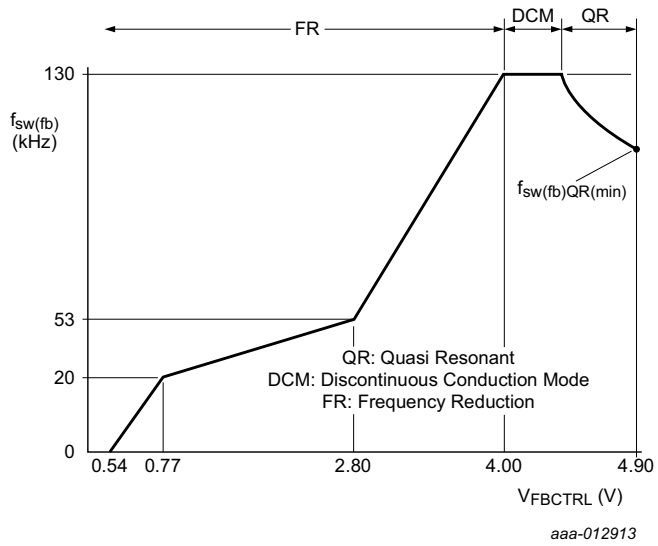


Fig 28. Minimum frequency in QR mode

The equation for the primary flyback inductance is:

$$L_{p(fb)} = \frac{1}{\left[\left(\sqrt{\frac{2 \cdot P_{o(max)} \cdot f_{sw(fb)QR(min)}}{\eta_{fb}}}\right) \cdot \left(\frac{1}{V_{bus(min)}} + \frac{1}{N_{fb} V_o}\right) + f_{sw(fb)QR(min)} \cdot \pi \cdot \sqrt{C_{d(fb)}}\right]^2} \quad (44)$$

Where:

- $f_{sw(fb)QR(min)}$ minimum flyback switching frequency in QR mode
- η_{fb} is the flyback controller efficiency, typically 0.95
- $V_{bus(min)}$ is the expected minimum bus voltage
- N_{fb} is flyback turns ratio $N_{p(fb)}/N_{s(fb)}$
- V_o is the output voltage
- $P_{o(max)}$ is the maximum output power
- $C_{d(fb)}$ is the total capacitance on the drain of the flyback switch

To ensure that the PFC is on at $P_{o(PFC)swon}$, the $L_{p(fb)}$ must not exceed the value $L_{p(fb)max}$ when the auto PFC on/off function is used (See Section 6.6).

$$L_{p(fb)max} = \frac{1}{\left[\left(\sqrt{\frac{2 \cdot 73\ kHz \cdot P_{o(PFC)swon}}{\eta_{fb}}}\right) \cdot \left(\frac{1}{v_{mains(rms)min} \cdot \sqrt{2}} + \frac{1}{N_{fb} V_o}\right) + f_{sw(fb)QR(min)} \cdot \pi \cdot \sqrt{C_{d(fb)}}\right]^2} \quad (45)$$

Where:

- $V_{mains(rms)min}$ is the minimum mains voltage (AC)
- $V_{o(min)}$ is the minimum output voltage
- η_{fb} is the flyback controller efficiency, typically 0.95
- N_{fb} is flyback turns ratio $N_{p(fb)}/N_{s(fb)}$
- $P_{o(PFC)swon}$ is the output power at which the PFC must be enabled
- $C_{d(fb)}$ is the total capacitance on the drain of the flyback switch

The effects of the primary inductance $L_{p(fb)}$ are:

- High value: Small PFC switch on/off hysteresis
- Low value: Lower efficiency due to flyback switching losses

9.3.2 Flyback peak current ($I_{pk(fb)}$)

The output power P_o is calculated with Equation 46:

$$P_o = \frac{1}{2} \cdot L_{p(fb)} \cdot I_{pk(fb)}^{2} \cdot f_{sw(fb)} \cdot \eta_{fb} \quad (46)$$

In QR and DCM modes, V_{FBCTRL} sets the flyback peak current $I_{pk(fb)}$; $f_{sw(fb)}$ is a result.

In FR mode, V_{FBCTRL} sets $f_{sw(fb)}$; $I_{pk(fb)}$ is fixed at its minimum level $I_{pk(fb)min}$.

9.3.2.1 Maximum flyback peak current ($I_{pk(fb)max}$)

To prevent saturation of the flyback transformer, the OverCurrent Protection (OCP) limits $I_{pk(fb)}$. A saturated core deteriorates the overall system performance. Saturation causes more stress, EMI, and, in the worst case, a system failure.

$$I_{sat(fb)} = \frac{N_{p(fb)} \cdot B_{max} \cdot A_e}{L_{p(fb)}} \quad (47)$$

Where:

- $N_{p(fb)}$ is number of primary turns
- B_{max} is maximum flux density at expected high operating temperature
- A_e is effective core area

The flyback transformer must never saturate, not even at high temperatures. To avoid saturation due to component spread, a margin of minimal 10 % must also be applied.

$$0.9 \cdot I_{sat(fb)} > I_{pk(fb)max} \quad (48)$$

9.3.2.2 Minimum flyback peak current ($I_{pk(fb)min}$)

The automatic PFC on/off function is based on $f_{sw(fb)}$. When the automatic on/off function is used, Equation 49 applies:

$$P_{o(PFC)on} = \frac{1}{2} \cdot L_{p(fb)} \cdot I_{pk(fb)min}^{2} \cdot f_{sw(fb)swon(PFC)} \cdot \eta_{fb} \quad (49)$$

$I_{pk(fb)min}$ can be calculated with Equation 50:

$$I_{pk(fb)min} = \sqrt{\frac{2 \cdot P_{o(PFC)on}}{L_{p(fb)} \cdot f_{sw(fb)swon(PFC)} \cdot \eta_{fb}}} \quad (50)$$

Where:

- $f_{sw(fb)swon(PFC)}$ = 73 kHz

The output power level $P_{o(PFC)swoff}$ at which the PFC switches off, is:

$$P_{o(PFC)swoff} = \frac{1}{2} \cdot L_{p(fb)} \cdot I_{pk(fb)min}^{2} \cdot f_{sw(fb)swoff(PFC)} \cdot \eta_{fb} \quad (51)$$

Where:

- $f_{sw(fb)swoff(PFC)}$ = 53 kHz

Furthermore, the ratio between $I_{pk(fb)max}$ and $I_{pk(fb(min)}$ cannot be lower than 2.35:

$$I_{pk(fb)max} > I_{pk(fb)min} \cdot \frac{V_{sense(fb)max}}{v_{sense(fb)min}}$$
$$\Rightarrow I_{pk(fb)max} > I_{pk(fb)min} \cdot \frac{545\ mV}{232\ mV} \Rightarrow \frac{I_{pk(fb)max}}{I_{pk(fb)min}} > 2.35 \quad (52)$$

9.3.3 Flyback adjust by FBSENSE pin circuit

The FBSENSE pin functionality is:

- Set $I_{pk(fb)max}$
- Set $I_{pk(fb)min}$

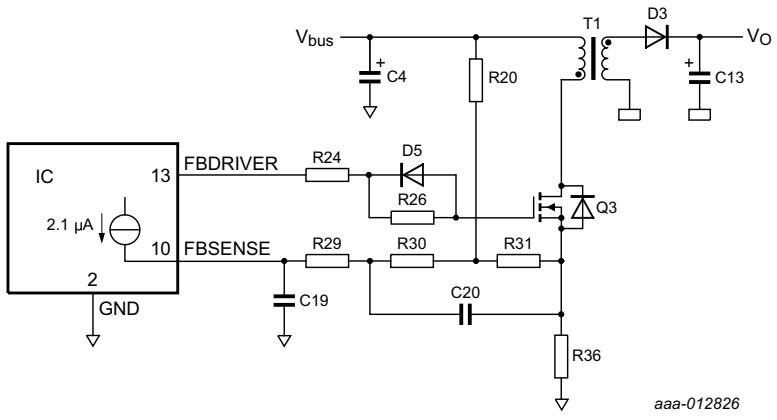


Fig 29. Flyback adjustment circuit

Resistor R29 and capacitor C19 prevent that the FBSENSE pin is charged negative because of disturbances on the sense resistor R36.

9.3.3.1 Flyback current sense resistor R36

The sense resistor R36 can be calculated with Equation 53:

$$R36 = \frac{V_{sense(fb)max} - V_{sense(fb)min}}{I_{pk(fb)max} - I_{pk(fb)min}} = \frac{545\ mV - 232\ mV}{I_{pk(fb)max} - I_{pk(fb)min}} = \frac{313\ mV}{I_{pk(fb)max} - I_{pk(fb)min}} \quad (53)$$

9.3.3.2 FBSENSE noise filter resistor R29 and capacitor C19

The value of resistor R29 is between 680 Ω and 2.2 kΩ. The purpose of resistor R29 is to prevent that capacitor C19 is charged due to negative voltage spikes on resistor R36.

A commonly used time constant for resistor R29 and capacitor C19 is approximately 220 ns. The filter capacitor at the FBSENSE pin can be calculated with Equation 54:

$$C19 = \frac{220\ ns}{R29} \quad (54)$$

The tolerance of capacitor C19 must be 10 % maximum. This tolerance limits the impact on the overall spreading for the $P_{o(PFC)swon}$ and $P_{o(PFC)swoff}$ levels.

9.3.3.3 FBSENSE series resistance $R_{s(FBSENSE)}$

The total series resistance $R_{s(FBSENSE)}$ between the FBSENSE pin and sense resistor R36 determines the static offset voltage on the FBSENSE pin. $R_{s(FBSENSE)}$ is used to adjust the ratio between $I_{pk(fb)min}$ and $I_{pk(fb)max}$.

$$R_{s(FBSENSE)} = R29 + R30 + R31 \quad (55)$$

$$R_{s(FBSENSE)} = \frac{I_{pk(fb)max} \cdot V_{sense(fb)min} - I_{pk(fb)min} \cdot V_{sense(fb)max}}{I_{adj(FBSENSE)} \cdot (I_{pk(fb)max} - I_{pk(fb)min})} \quad (56)$$

Where:

- $I_{adj(FBSENSE)}$ is the 2.1 μA internal current source on the FBSENSE pin

9.3.4 Flyback switch-off delay compensation

Resistors R20 and R31 are intended to compensate the sum of these delays:

- Switch-off internal delay time $t_{d(FBDRIVER)}$ = 80 ns of the IC
- MOSFET switch-off delay time $t_{d(MOSFET)off}$, typically 60 ns
- Delay time caused by resistor R29 and capacitor C19

If these delay times are not compensated, they lead to an increased $I_{pk(fb)}$ value at a high V_{bus}.

$$t_{d(fb)swoff} = t_{d(FBDRIVER)} + t_{d(MOSFET)off} + R29 \cdot C19 \quad (57)$$

The increase of $I_{pk(fb)}$ depends on V_{bus}:

$$\Delta I_{pk(fb)} = \frac{V_{bus}}{L_{p(fb)}} \cdot t_{d(fb)swoff} \quad (58)$$

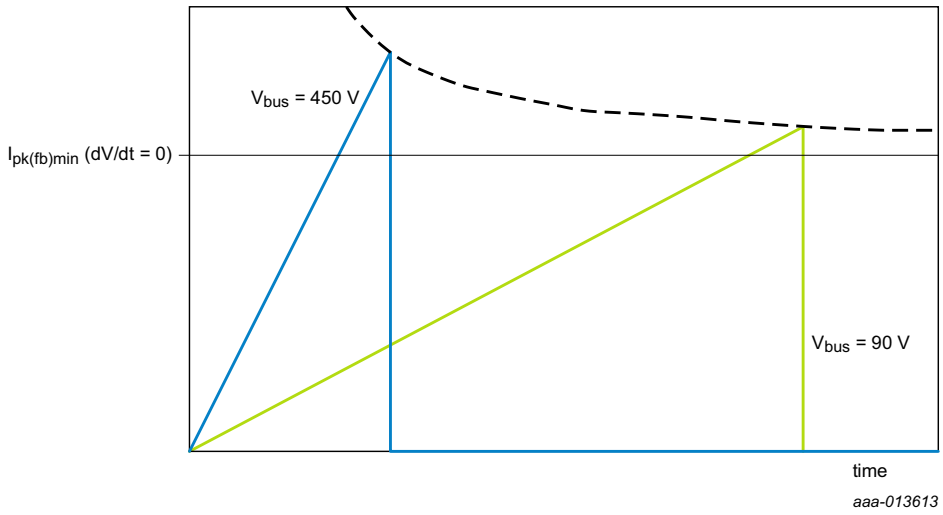


Fig 30. $I_{pk(fb)min}$ increase due to a switch-off delay

$\Delta I_{pk(fb)}$ results in a voltage on resistor R36 which must be compensated as a function of V_{bus} by I_{R20} through resistor R31:

$$I_{R20} \cdot R31 = \Delta I_{pk(fb)} \cdot R36 \Rightarrow \frac{V_{bus}}{R20} \cdot R31 = \Delta I_{pk(fb)} \cdot R36$$
$$\Rightarrow \frac{V_{bus}}{R20} \cdot R31 = \frac{V_{bus}}{L_{p(fb)}} \cdot t_{d(fb)swoff} \cdot R36 \quad (59)$$

V_{bus} drops out of the equation:

$$\frac{R31}{R20} = \frac{t_{d(fb)swoff}}{L_{p(fb)}} \cdot R36 \quad (60)$$

R31 can be calculated once R20 is selected.

$$R31 = \frac{t_{d(fb)swoff}}{L_{p(fb)}} \cdot R20 \cdot R36 \quad (61)$$

R20 sets the current I_{R20} through resistor R31. Choose $I_{R20} > 3 \times I_{adj(FBSENSE)}$:

Assuming $V_{bus} \gg V_{FBSENSE}$:

$$\Rightarrow R20 < \frac{V_{bus(min)}}{3 \cdot I_{adj(FBSENSE)}} \quad (62)$$

To meet the rated resistor voltage, R20 is typically constructed with several 0805 resistors in series.

Remark: Always verify the actual $t_{d(MOSFET)swoff}$ in the application prototype because of different MOSFET types and different gate discharge resistors.

9.3.5 Flyback soft-start

Soft-start is implemented using the RC network connected to the FBSENSE pin.

To ensure that $V_{start(soft)fb}$ is reached and flyback start-up is enabled, the sum of resistors R29, R30, and R31 must be > 15 kΩ.

The flyback soft-start $t_{start(soft)fb}$ must range between 5 ms and 10 ms. Furthermore, $t_{start(soft)fb}$ must be longer than the PFC soft-start time $t_{start(soft)PFC}$.

$$t_{start(soft)fb} > t_{start(soft)PFC} \quad (63)$$

$$t_{start(soft)fb} = 3 \cdot (R30 + R31) \cdot C20 \approx 7\ ms \quad (64)$$

10. PCB layout considerations

A good layout is an important part of the final design. It minimizes many kinds of disturbances and makes the overall performance more robust with less risk of EMI. Guidelines for the PCB layout are:

- Separate large signal grounds from small signal grounds (PFC, FB, and IC).
- Reduce the PCB area within the indicated large signal current loops (PFC inductor and FB inductor currents) to a minimum. Each indicated large signal loop has its own color in Figure 1 and Figure 2. Make the copper tracks as short and as wide as possible.
- The connection between both MOSFETs (PFC and flyback) and the IC driver outputs must be as short as possible. To minimize inductance, use wide tracks. Increase the distance between the copper tracks and/or use a separate guided ground track for both connections. The separated guided ground track minimizes the coupling between the PFCDRIVER and FBDRIVER signals. If it is impossible to place the MOSFET and the IC close to each other, a circuit, like the one in Figure 31, can be added.
- The power ground and small signal ground are only connected with one short copper track (make this track as short and as wide as possible). Preferably, it should become one spot (connection between IC ground and STAR ground at the bus capacitor).
- Use a ground shield underneath the IC, connect this ground shield to the GND pin of the IC.
- Place all series connected resistors that are fixed to an IC pin as close as possible to that pin.
- Heat sink can carry HF currents. Connect heat sinks which are connected to the nearest corresponding ground signal of the component. Make this connection as short as possible. Connect the heat sink of Q1 to the ground PFC and the heat sink of Q3 to the ground FB. In typical applications, all primary components are often mounted on a single heat sink. If so, make one wide copper track that connects all these grounds to each other. Combine in this copper track the ground of the PI filter (capacitors C1 and C2).
- Place capacitors C10 (VOSENSE), C17 (FBCTRL), C19 (FBSENSE), and C11 (PFCSENSE) (in order of priority) as close as possible to the IC. Reduce coupling between the PFC switching signals (PFCDRIVER and PFCAUX) and the flyback sense signals (FBSENSE and FBCTRL) as much as possible. The coupling reduction minimizes the risk of electromagnetic interference and audible noise.

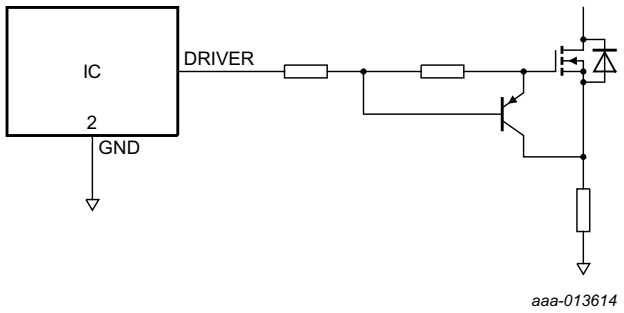


Fig 31. MOSFET local turn-off circuit

11. Abbreviations

Table 4. Abbreviations

Acronym	Description
AC	Alternate Current
DC	Direct Current
DCM	Discontinuous Conduction Mode
EMI	ElectroMagnetic Interference
FR	Frequency Reduction
GND	Ground
GSM	Global System for Mobile communications
HV	High-Voltage
IC	Integrated Circuit
IEC	International Electrotechnical Commission
LED	Light Emitting Diodes
MHR	Mains Harmonics Reduction
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NTC	Negative Temperature Coefficient
OCP	OverCurrent Protection
OPP	OverPower Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
PCB	Printed-Circuit Board
PF	Power Factor
PFC	Power Factor Converter/Controller/Correction
QR	Quasi-Resonant
RMS	Root Mean Square
SMPS	Switched Mode Power Supply
SO	Small Outline
SOI	Silicon-On-Insulator
SSL	Solid-State Lighting
THD	Total Harmonic Distortion
UVLO	UnderVoltage LockOut
ZCS	Zero Current Signal

12. References

[1] SSL8516T data sheet — GreenChip PFC and flyback controller

[2] UM10776 user manual — SSL8516DB1195 75 W 1.6 A dimmable LED driver

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