International
IOR Rectifier

PD-97301B

2N7606U3
IRHLNJ77034
60V, N-CHANNEL
R7 TECHNOLOGY

RADIATION HARDENED LOGIC LEVEL POWER MOSFET SURFACE MOUNT (SMD-0.5)

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D
IRHLNJ77034	100K Rads (Si)	0.035Ω	22A*
IRHLNJ73034	300K Rads (Si)	0.035Ω	22A*

SMD-0.5

International Rectifier's R7™ Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments.The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation.This is achieved while maintaining single event gate rupture and single event burnout immunity.

The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

Features:

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Ceramic Package
- Surface Mount
- Light Weight

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
I_D @ V_{GS} = 4.5V, T_C = 25°C	Continuous Drain Current	22*	A
I_D @ V_{GS} = 4.5V, T_C = 100°C	Continuous Drain Current	20	
I_{DM}	Pulsed Drain Current ①	88	
P_D @ T_C = 25°C	Max. Power Dissipation	57	W
	Linear Derating Factor	0.45	W/°C
V_{GS}	Gate-to-Source Voltage	±10	V
E_{AS}	Single Pulse Avalanche Energy ②	63	mJ
I_{AR}	Avalanche Current ①	22	A
E_{AR}	Repetitive Avalanche Energy ①	5.7	mJ
dv/dt	Peak Diode Recovery dv/dt ③	8.8	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150	°C
	Pckg. Mounting Surface Temp.	300 (for 5s)	
	Weight	1.0 (Typical)	g

* Current is limited by package

For footnotes refer to the last page

12/02/10

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.068	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.035	Ω	V_{GS} = 4.5V, I_D = 20A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	V_{DS} = V_{GS}, I_D = 250μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-4.9	—	mV/°C	
g_{fs}	Forward Transconductance	15	—	—	S	V_{DS} = 10V, I_{DS} = 20A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	μA	V_{DS}= 48V ,V_{GS}=0V
		—	—	10		V_{DS} = 48V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 10V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -10V
Q_g	Total Gate Charge	—	—	34	nC	V_{GS} = 4.5V, I_D = 22A
Q_{gs}	Gate-to-Source Charge	—	—	8.0		V_{DS} = 30V
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	16		
$t_{d(on)}$	Turn-On Delay Time	—	—	26	ns	V_{DD} = 30V, I_D = 22A,
t_r	Rise Time	—	—	110		V_{GS} = 5.0V, R_G = 7.5Ω
$t_{d(off)}$	Turn-Off Delay Time	—	—	54		
t_f	Fall Time	—	—	30		
$L_S + L_D$	Total Inductance	—	4.0	—	nH	Measured from the center of drain pad to center of source pad
C_{iss}	Input Capacitance	—	2015	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	—	488	—		f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	—	4.5	—		
R_g	Gate Resistance	—	1.45	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	22*	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	88		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_j = 25°C, I_S = 22A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	160	ns	T_j = 25°C, I_F = 22A, di/dt ≤ 100A/μs
Q_{RR}	Reverse Recovery Charge	—	—	704	nC	V_{DD} ≤ 25V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

* Current is limited by package

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	2.2	°C/W	

Note: Corresponding Spice and Saber models are available on International Rectifier Web site.

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Upto 300K Rads (Si)[1]		Units	Test Conditions
		Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	—	V	V_{GS} = 0V, I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	1.0	2.0		V_{GS} = V_{DS}, I_D = 250μA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V_{GS} = 10V
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100		V_{GS} = -10V
I_{DSS}	Zero Gate Voltage Drain Current	—	1.0	μA	V_{DS}= 48V, V_{GS}=0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.045	Ω	V_{GS} = 4.5V, I_D = 20A
$R_{DS(on)}$	Static Drain-to-Source On-state ④ Resistance (SMD-0.5)	—	0.035	Ω	V_{GS} = 4.5V, I_D = 20A
V_{SD}	Diode Forward Voltage④	—	1.2	V	V_{GS} = 0V, I_D = 22A

1. Part numbers IRHLNJ77034, IRHLNJ73034

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm^2))	Energy (MeV)	Range (μm)	VDS (V)					
			@VGS= 0V	@VGS= -2V	@VGS= -4V	@VGS= -5V	@VGS= -6V	@VGS= -7V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	60	60	60	60	60	-
62 ± 5%	355 ± 7.5%	33 ± 7.5%	60	60	60	60	-	-
85 ± 5%	380 ± 7.5%	29 ± 7.5%	60	60	60	-	-	-

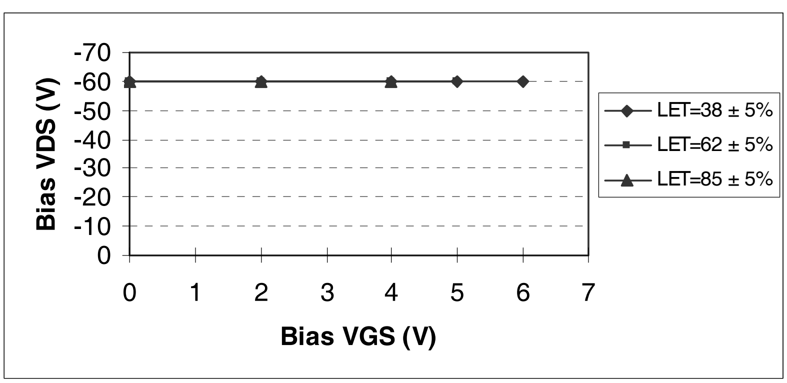


Fig a. Typical Single Event Effect, Safe Operating Area

For footnotes refer to the last page

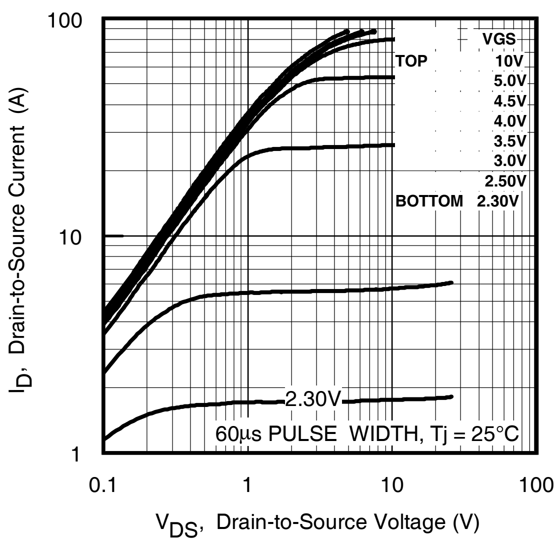


Fig 1. Typical Output Characteristics

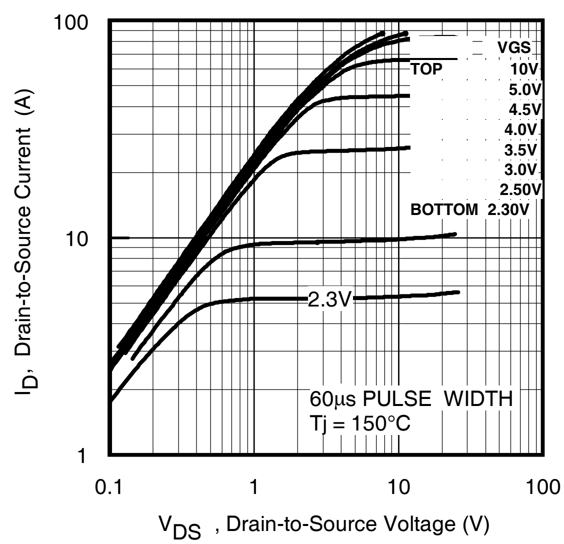


Fig 2. Typical Output Characteristics

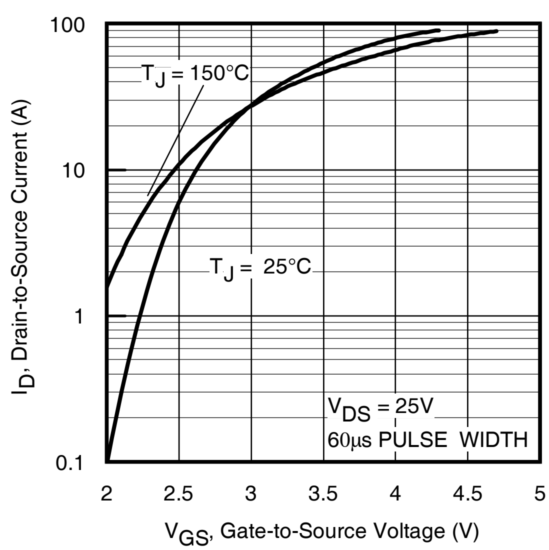


Fig 3. Typical Transfer Characteristics

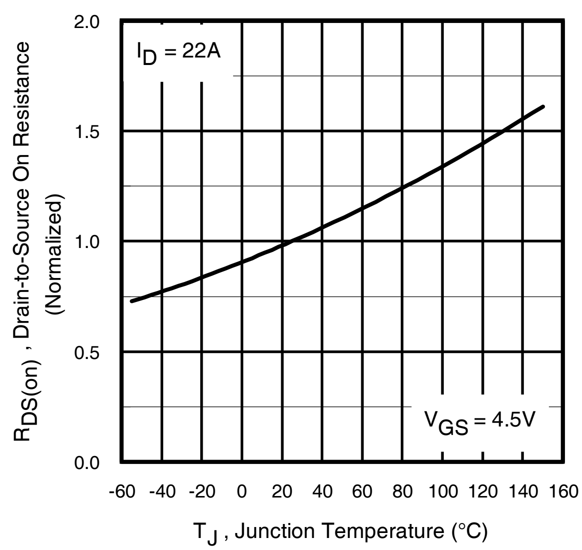


Fig 4. Normalized On-Resistance Vs. Temperature

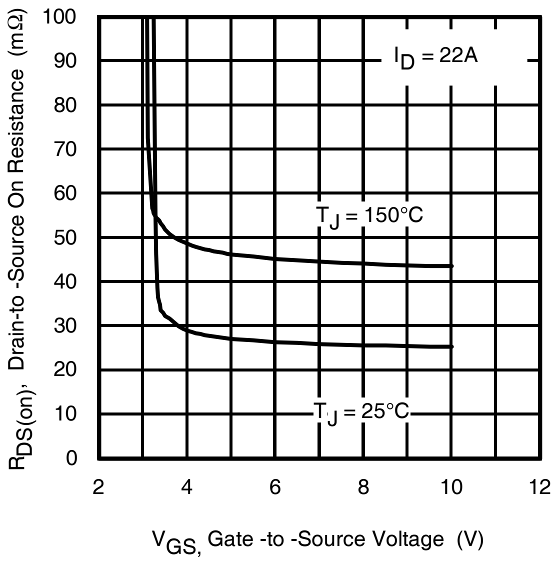


Fig 5. Typical On-Resistance Vs Gate Voltage

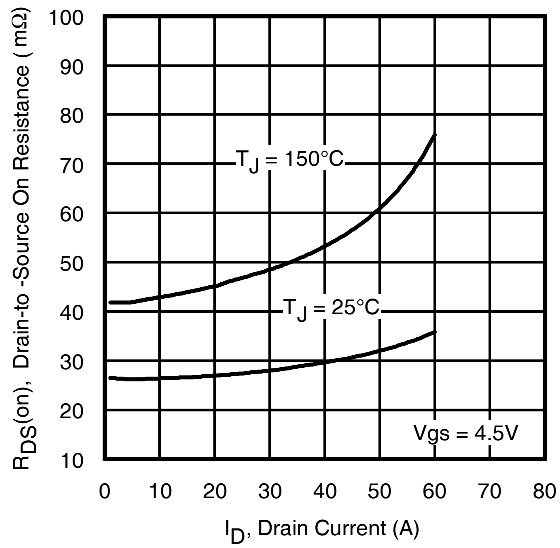


Fig 6. Typical On-Resistance Vs Drain Current

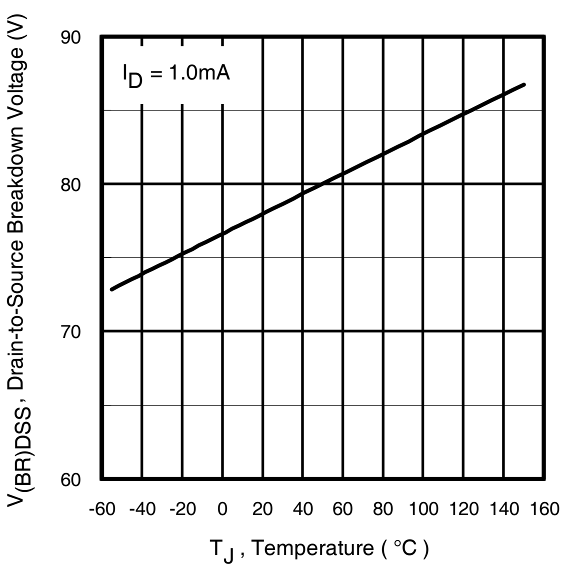


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

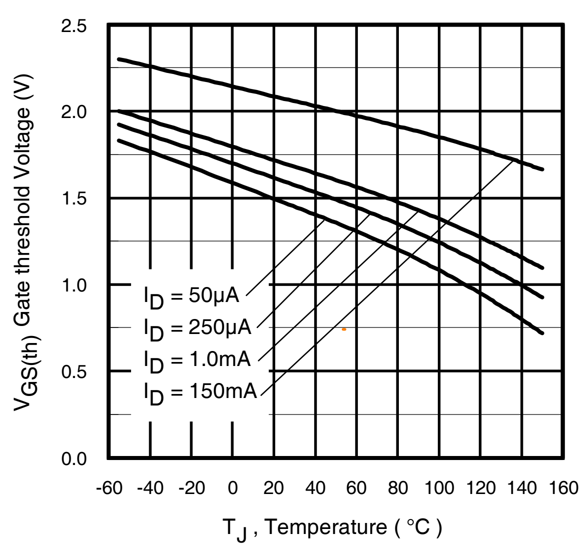


Fig 8. Typical Threshold Voltage Vs Temperature

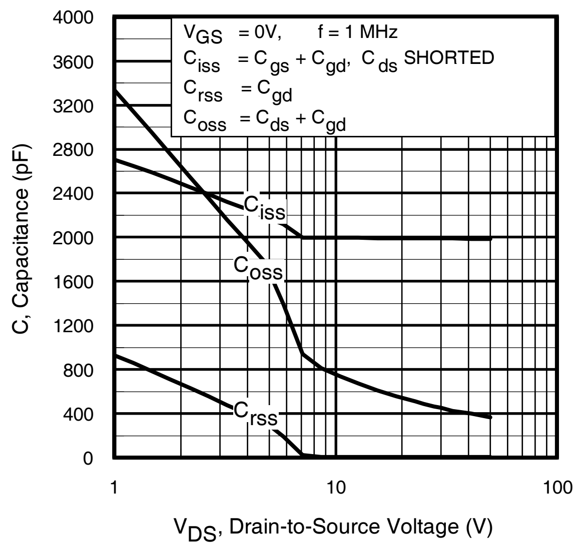


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

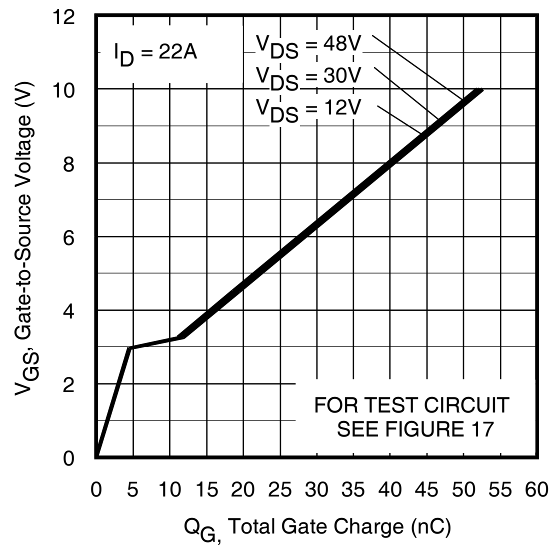


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

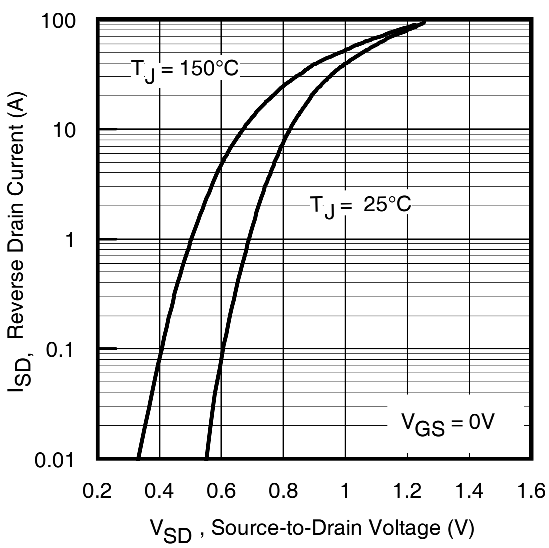


Fig 11. Typical Source-to-Drain Diode Forward Voltage

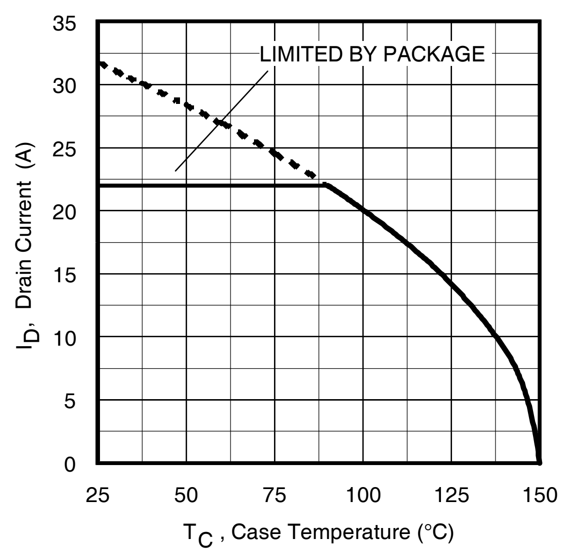


Fig 12. Maximum Drain Current Vs. Case Temperature

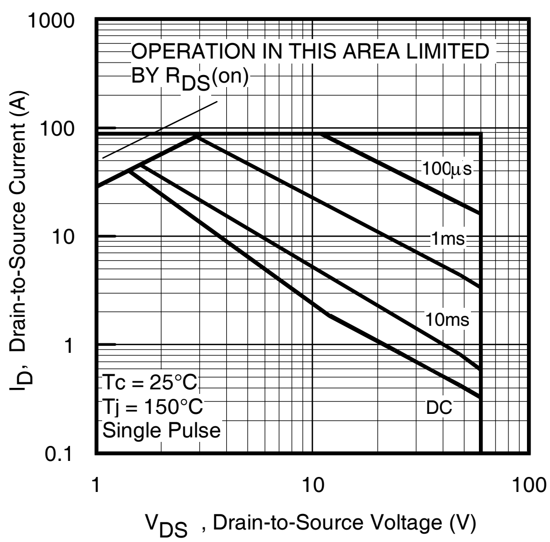


Fig 13. Maximum Safe Operating Area

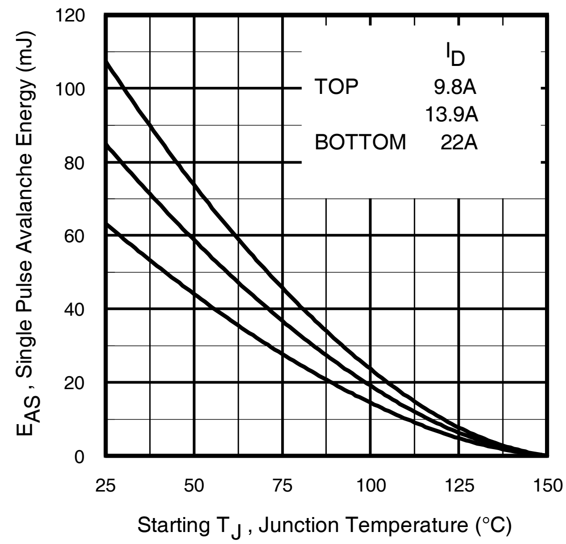


Fig 14. Maximum Avalanche Energy Vs. Drain Current

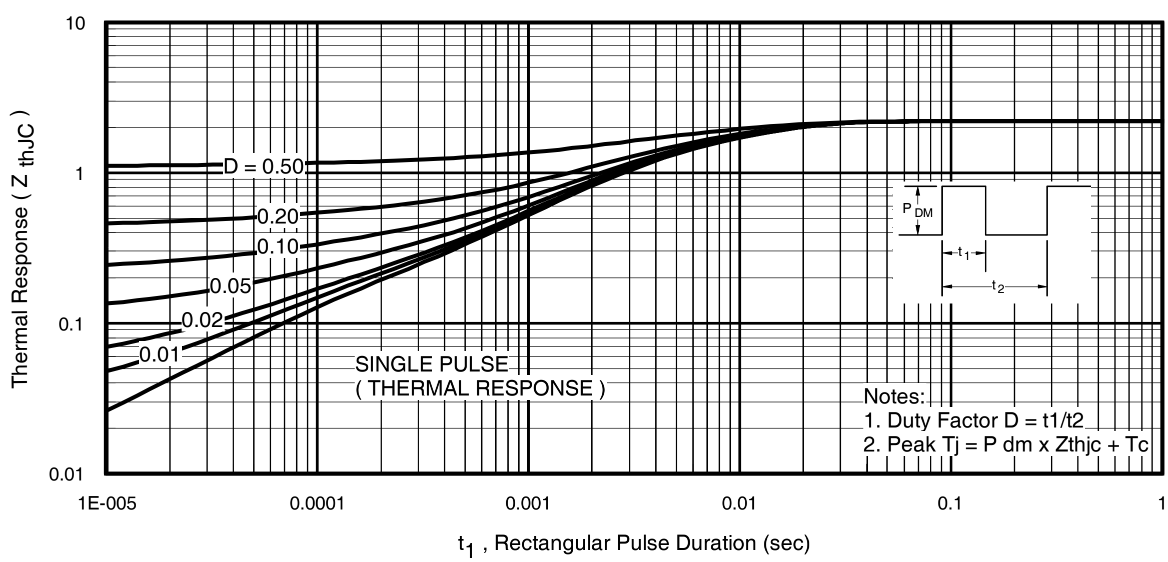


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

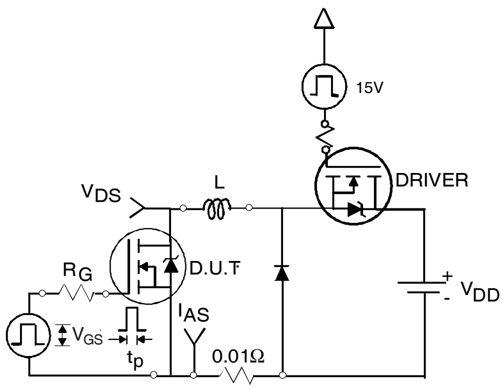


Fig 16a. Unclamped Inductive Test Circuit

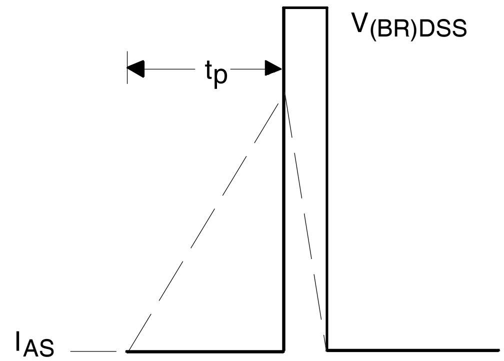


Fig 16b. Unclamped Inductive Waveforms

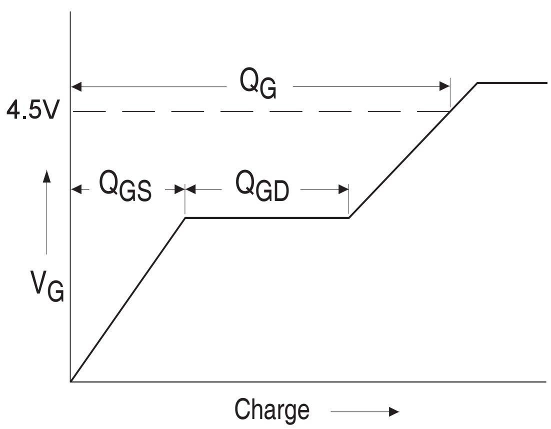


Fig 17a. Basic Gate Charge Waveform

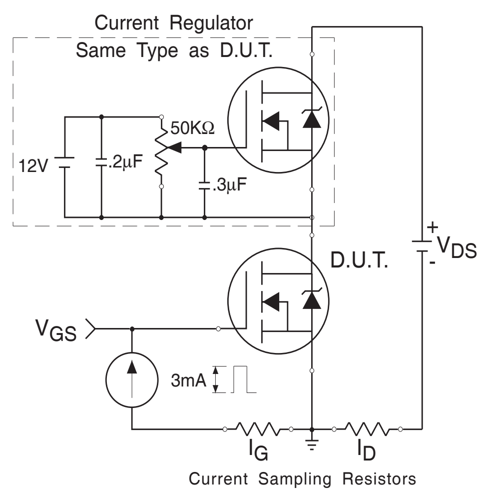


Fig 17b. Gate Charge Test Circuit

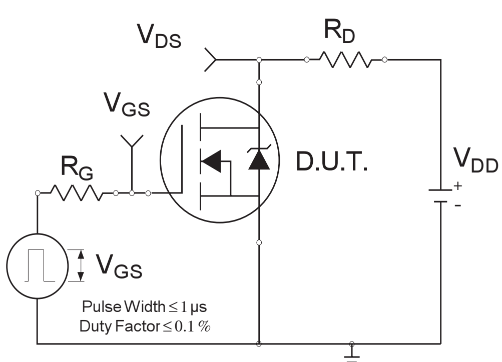


Fig 18a. Switching Time Test Circuit

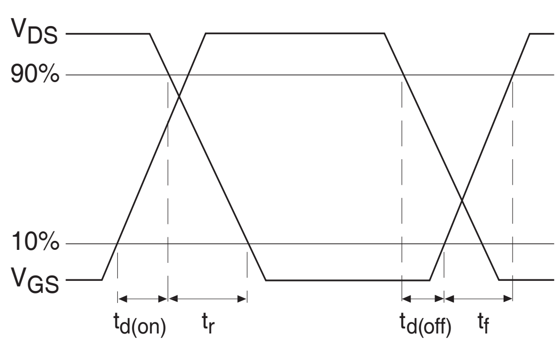


Fig 18b. Switching Time Waveforms

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 25V, starting T_J = 25°C, L= 0.26mH Peak I_L = 22A, V_{GS} = 10V

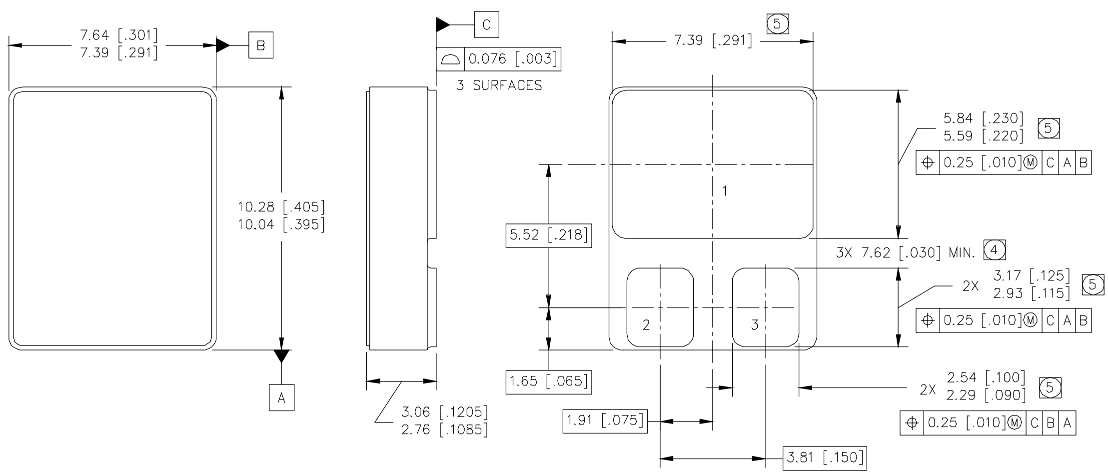
③ $I_{SD} \leq$ 22A, di/dt $\leq$ 328A/µs, $V_{DD} \leq$ 60V, $T_J \leq$ 150°C

④ Pulse width $\leq$ 300 µs; Duty Cycle $\leq$ 2%

⑤ **Total Dose Irradiation with V_{GS} Bias.** 10 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

⑥ **Total Dose Irradiation with V_{DS} Bias.** 48 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — SMD-0.5



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

4 DIMENSION INCLUDES METALLIZATION FLASH.

5 DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

PAD ASSIGNMENTS

1 = DRAIN
2 = GATE
3 = SOURCE

International
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