GENERAL DESCRIPTION

MC7010 provides 9 DOF function with an ultra-small 3x3mm single package for consumer electronic market. It consists of a 3-axis accelerometer, 3-axis magnetometer and a specially designed sensor fusion unit.

Besides the accelerometer and tilt-compensated compass, it integrates the mCube patented iGyro™ engine supported by the optimized sensor fusion unit design, to provide an ultra-low power gyroscope function. Thus, the MC7010 can provide the 9 DOF function for cellphone, tablet, and other consumer electronic devices with competitive performance and ultra-low current.

FEATURES

- Competitive 9 DOF solution
  - 3-axis accelerometer
  - 3-axis magnetometer
  - 3-axis virtual gyroscope function
- 3x3 single package, small footprint
  - 3x3x0.95mm 16pin LGA
  - Industry leading 9DOF package
- Ultra-low power consumption
  - 0.25mA normal 9DOF mode
  - 75% power saving vs. physical gyroscope function
- Flexible pin compatibility
  - mCube 3-axis accelerometer MC325x
  - mCube 6-axis eCompass MC6450
  - One PCB for 3 axis, 6 axis and 9 axis
- Digital interface
  - Dual I2C interface up to 400KHz
  - 1 interrupt for accelerometer
  - 1 interrupt for magnetometer
- Power supply
  - AVDD 1.7-3.6V
  - DVDD 1.7-3.6V

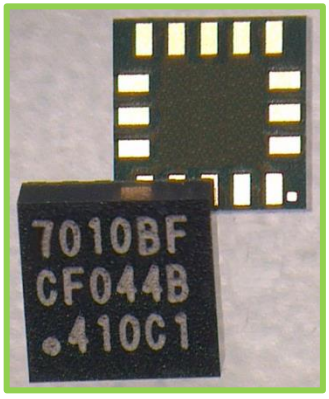


TABLE OF CONTENTS

1 ORDER INFO

Part Number	Order Number	Package	Shipping
MC7010	MC7010	LGA-16	Tape & Reel, 5Ku

2 FUNCTIONAL BLOCK DIAGRAM

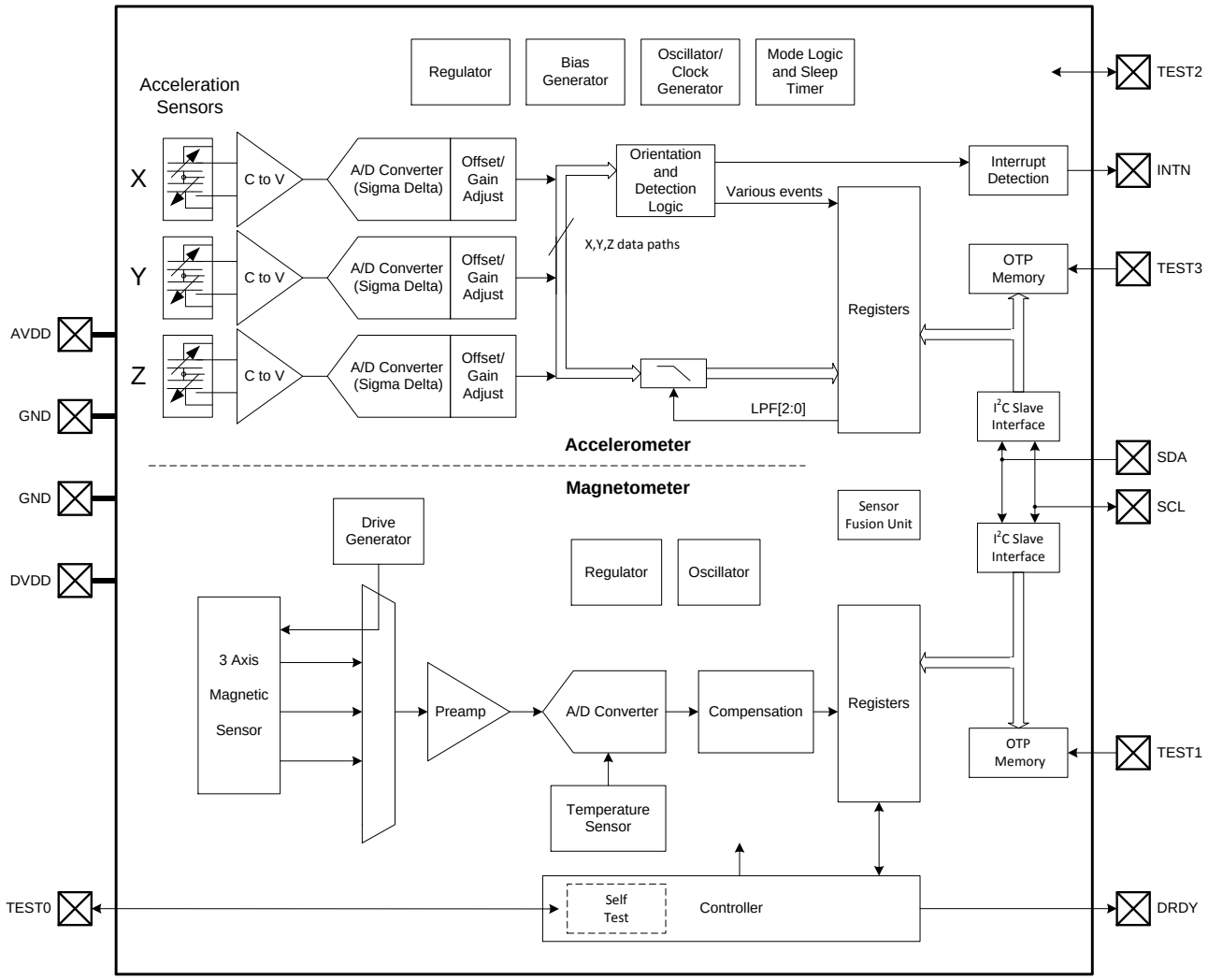


Figure 1. Block Diagram

3 PACKAGING AND PIN DESCRIPTIONS

3.1 Package Orientation

Positive values indicate direction of acceleration force.

The magnetic sensor output value of each axis is positive when turned toward magnetic north.

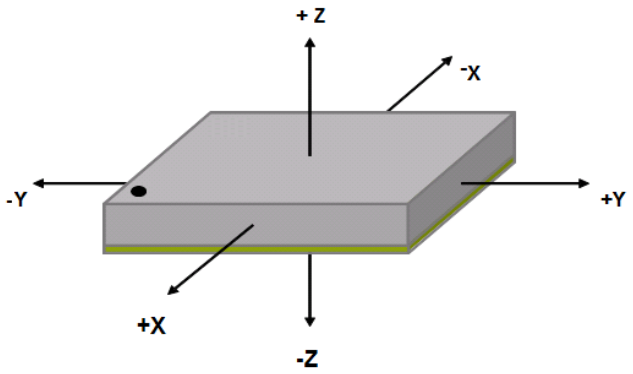


Figure 2. Package Axis Reference – Magnetometer & Accelerometer

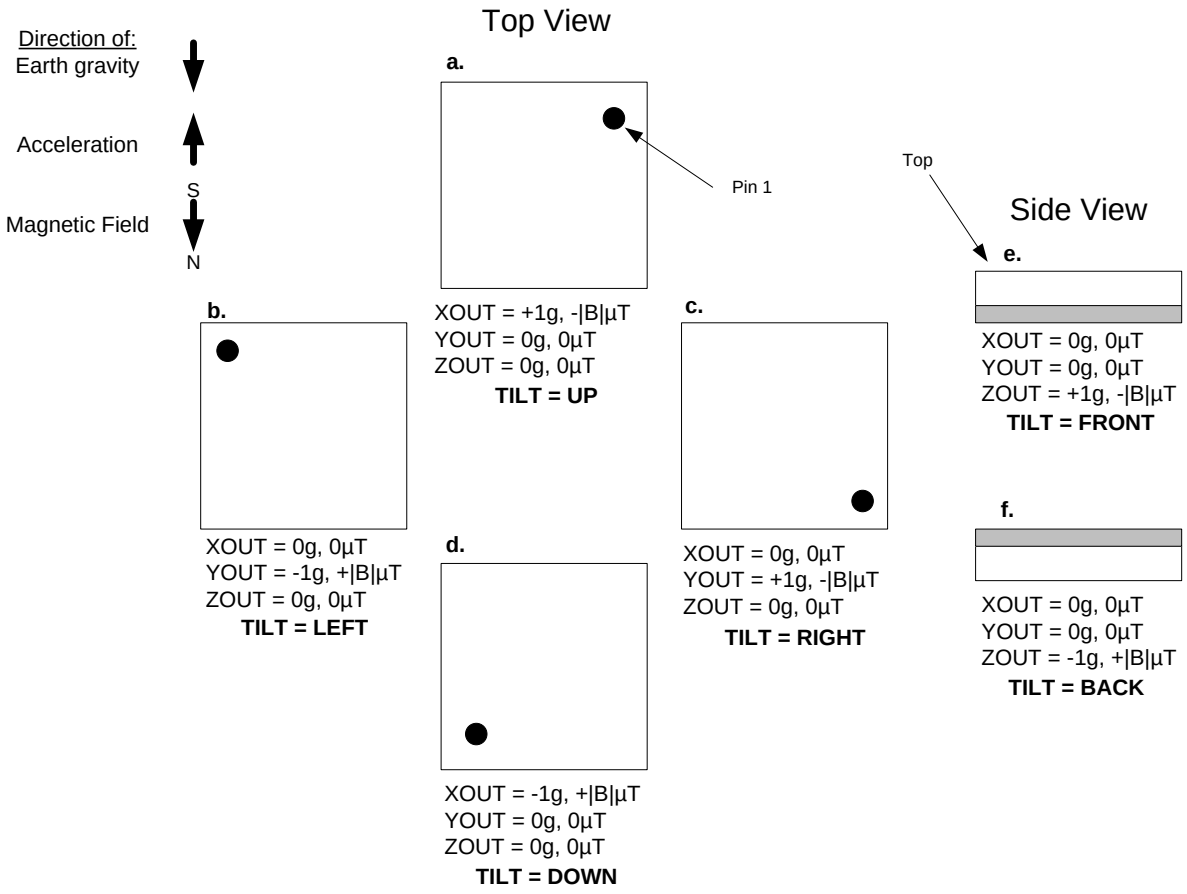


Figure 3. Package Orientation – Accelerometer & Magnetometer

3.2 Package Outline

Dimension in millimeters				Dimension in millimeters			
Ref	Min.	Nom.	Max.	Ref	Min.	Nom.	Max.
A	2.9	3	3.1	E1	0.47	0.50	0.53
B	2.9	3	3.1	E2	---	0.375	---
C	0.90	0.95	1.00	E3	---	0.1	---
C1	0.72	0.77	0.82				
C2	0.13	0.18	0.23				
D1	0.22	0.25	0.28				
D2	0.445	0.475	0.505				
D3	0.47	0.50	0.53				
D4	---	0.875	---				
D5	---	0.1	---				

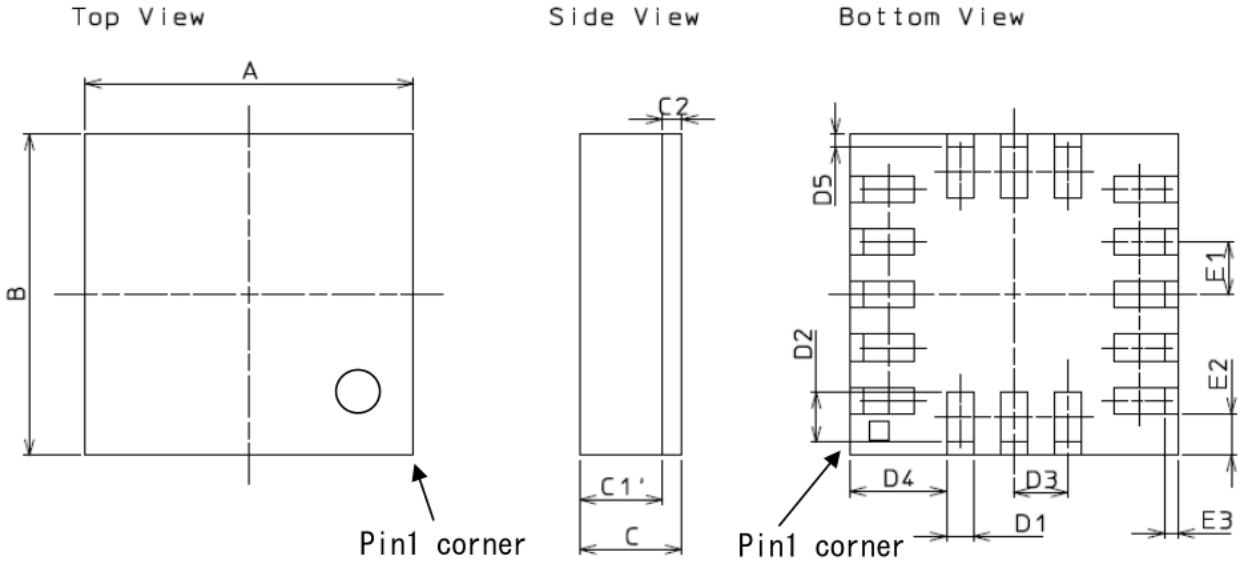


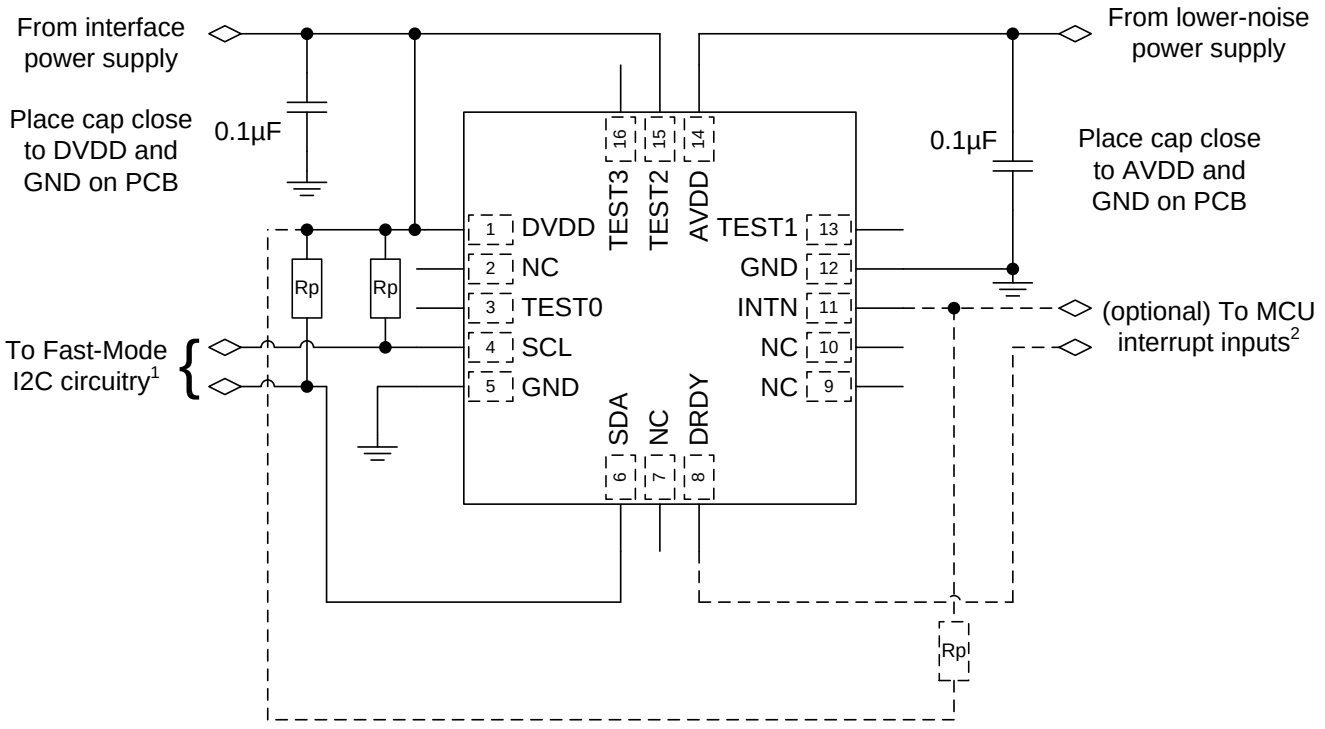
Figure 4. Package Outline Dimensions

3.3 Pin Descriptions

Pin	Name	Function
1	DVDD	Digital Power Supply (to interface circuitry)
2	NC	No connection
3	TEST0	Factory use mag test (no connect, Ground)
4	SCL	I2C Serial Clock Input
5	GND	Ground
6	SDA	I2C Serial Data Input / Output
7	NC	No connection
8	DRDY	Magnetometer Interrupt (no connect, Ground, DVDD)
9	NC	No connection
10	NC	No connection
11	INTN	Accelerometer Interrupt
12	GND	Ground
13	TEST1	Factory use mag program (no connect, Ground, DVDD)
14	AVDD	Analog Power Supply (to internal circuitry)
15	TEST2	Factory use accel test (no connect, Ground, DVDD)
16	TEST3	Factory use accel program (no connect, Ground, DVDD)

Table 1: Pin Descriptions

4 TYPICAL APPLICATION CIRCUIT



NOTE[1]: Rp are typically 4.7 kΩ pull-up resistors to DVDD, per I2C specification. When DVDD is powered down, SDA and SCL will be driven low by internal ESD diodes.
NOTE[2]: Attach typical 4.7 kΩ pull-up resistor if INTN is defined as open-drain.

Figure 5. Typical Application Circuit

In typical applications, the digital power supply may contain significant noise from external sources and other circuits which should be isolated from the sensors. For these applications, a lower-noise power supply to power the AVDD pins may be desirable.

5 SPECIFICATIONS

5.1 Absolute Maximum Ratings

Parameters exceeding the Absolute Maximum Ratings may permanently damage the device.

Rating	Symbol	Minimum / Maximum Value	Unit
Supply voltages	Pins DVDD, AVDD	-0.3 / +3.6	V
Acceleration, any axis, 100 µs	g_{MAX}	10000	g
Magnetic field	H_{MAX}	0.2	T
Storage temperature	T_{STG}	-40 / +125	^{0}C
ESD human body model	HBM	±2000	V
Input voltage to non-power pin	Pins INTN, SCL,SDA, DRDY, TEST0, TEST1, TEST2, TEST3	-0.3 / (DVDD + 0.3) or 3.6, whichever is lower	V

Table 2. Absolute Maximum Ratings

5.2 Magnetometer Sensor Characteristics

Test condition: AVDD = 2.8V, DVDD = 2.8V, T_{op} = 25 ^{0}C unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
Magnetometer Field Range[1]		-2.4		+2.4	mT
Magnetometer Sensitivity1			0.15		µT / LSB
Magnetometer Linearity	±1.2mT	-2		+2	%FS
Magnetometer Sample Rate1	Programmable	0.5		100	Hz

Table 3. Magnetometer Sensor Characteristics

[1] Values are based on device characterization, not tested in production.

5.3 Magnetometer Electrical Characteristics

Test condition: AVDD = 2.8V DVDD = 2.8V, T_{op} = 25 ^{0}C unless otherwise noted

Parameter	Conditions		Symbol	Min	Typ	Max	Unit
Supply voltage			AVDD	1.7		3.6	V
I/O voltage			DVDD	1.7		3.6	V
Standby current[2]			I_{DD0}		3		µA
Continuous State Supply Current	Magnetometer only	Average (ODR = 10 Hz) Maximum peak draw	I_{DD2}		60 2500		µA
Control Timing	Turn On Time (Off to Standby) Turn On Time (Standby to Active) Turn Off Time (Active to Standby)					3 5 5	mSec µSec µSec

Table 4. Magnetometer Electrical Characteristics

[2] Values are based on device characterization, not tested in production.

5.4 Accelerometer Sensor Characteristics

Test condition: AVDD = 2.8V, DVDD=2.8V, T_{op} = 25 ^{0}C unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
Acceleration Range			±8.0		g
Sensitivity			1024		LSB/g
Sensitivity Temperature Coefficient [3]	-40 ≤ T_{op} ≤ +85 ^{0}C		0.02		%/^{0}C
Zero-g Offset			±200 ±50 [4]		mg
Zero-g Offset Temperature Coefficient [3,4]	-40 ≤ T_{op} ≤ +85 ^{0}C		±1		mg/^{0}C
Noise Density [3]			100		µg/√Hz
Nonlinearity [3]	Within ±1g range		1		% FS
Accelerometer Sample Rate			1024		Hz
Cross-axis Sensitivity [3]	Between any two axes		2		%
Operating Temperature		-40	25	85	^{0}C

Table 5. Accelerometer Sensor Characteristics

[3] Values are based on device characterization, not tested in production.
[4]Requires compensation algorithm running on external system.

5.5 Accelerometer Electrical Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Supply Voltage		AVDD	1.7		3.6	V
I/O Voltage		DVDD	1.7		3.6	V
Sample Rate Tolerance		T_{clock}	-5		5	%

Test condition: AVDD = 2.8V, DVDD=2.8V, T_{op} = 25 ^{0}C unless otherwise noted

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Standby Current	AVDD=2.0V AVDD=2.8V AVDD=3.6V	I_{dd0}		3.8 4.9 5.9		µA
WAKE State Supply Current		I_{dd1024}		200		µA
Pad Leakage	Per I/O pad	I_{pad}	-1	0.01	1	µA

Table 6. Accelerometer Electrical Characteristics

5.6 iGyro™ Characteristics

The MC7010 contains the optimized sensor fusion unit that can support the patented mCube iGyro™ engine. Based on the high performance magnetometer and accelerometer, iGyro™ provides virtual 3-axis gyroscope functionality with competitive performance. mCube's proprietary technology employs a corrective trace-distortion capability to counteract interference from high acceleration events in situations where other virtual gyros designs typically do not work well. This patented algorithm provides a good user experience, close to that of a real gyro for gaming.

The specifications of iGyro™ engine can vary according to target system software and capabilities relating to accelerometer & magnetometer performance. The reference specifications are as follows.

Parameter	Value	Unit
500 DPS Linear Rotation Rate Support for Gaming	Yes	Y/N
ZRO	0	Deg/s
ODR	64	Hz
Resolution	1	Deg/s
Accuracy	99	%
Latency	60	ms
Slow-Motion Jitter Noise	2.1	Deg/s
Rotation rate SNR	13.8	N/A
4HZ Bandwidth Support	Yes	Y/N
Anti-Mag Capability	Yes	Y/N
Trace Distortion corrective capability	Yes	Y/N

Table 7. iGyro™ Features and Characteristics

mCube iGyro™ support exists for Android version 4.x.x and beyond. Access to the iGyro™ functionality and data is done via the standard Android APIs, as described in android development website.

http://developer.android.com/guide/topics/sensors/sensors_overview.html

Contact the factory or your local support for information regarding software porting.

5.7 I2C Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
LOW Level Input Voltage	V_{IL}	-0.5	0.3*DVDD	V
HIGH Level Input Voltage	V_{IH}	0.7*DVDD	-	V
Schmitt Trigger Input Hysteresis	V_{hys}	0.05*DVDD	-	V
Output Voltage, Pins INTN, DRDY, $I_{ol} \leq 2$ mA	V_{ol} V_{oh}	0 0	0.4 0.9*DVDD	V V
Output Voltage, Pin SDA (open drain), $I_{ol} \leq 1$ mA	V_{ols}	-	0.1*DVDD	V
Input current, pins SDA, SCL (input voltage between 0.1*DVDD and 0.9*DVDD max)	I_i	-10	10	µA
Capacitance, pins SDA, SCL	C_i	-	10	pF

Table 8. I2C Electrical Characteristics

NOTES:

- If multiple slaves are connected to the I2C signals in addition to this device, only 1 pull-up resistor on each of SDA and SCL should exist.
- Care must be taken to not violate the I2C specification for capacitive loading.
- When DVDD is not powered and set to 0V, INTN, DRDY, SDA and SCL will be held to DVDD plus the forward voltage of the internal static protection diodes, typically about 0.6V.
- When DVDD is disconnected from power or ground (e.g. Hi-Z), the device may become inadvertently powered up through the ESD diodes present on other powered signals.
- Characteristics not tested in production.

5.8 I2C Timing Characteristics

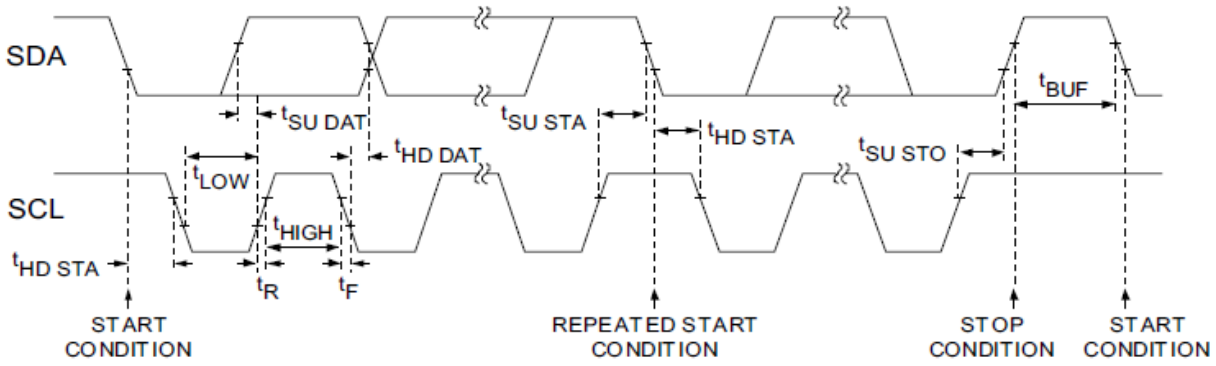


Figure 6.I2C Interface Timing

Parameter	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;\ STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
$t_{HD;DAT}$	Data hold time	5.0	-	-	-	µs
$t_{SU;DAT}$	Data set-up time	250	-	100	-	ns
$t_{SU;STO}$	Set-up time for STOP condition	4.0	-	0.6	-	µs
t_{BUF}	Bus free time between a STOP and START	4.7	-	1.3	-	µs

Table 9.I2C Timing Characteristics

NOTE: Values are based on I2C Specification requirements, not tested in production.

5.9 Power Supply Sequence

The timing and sequence requirements of the power supply pins are shown below.

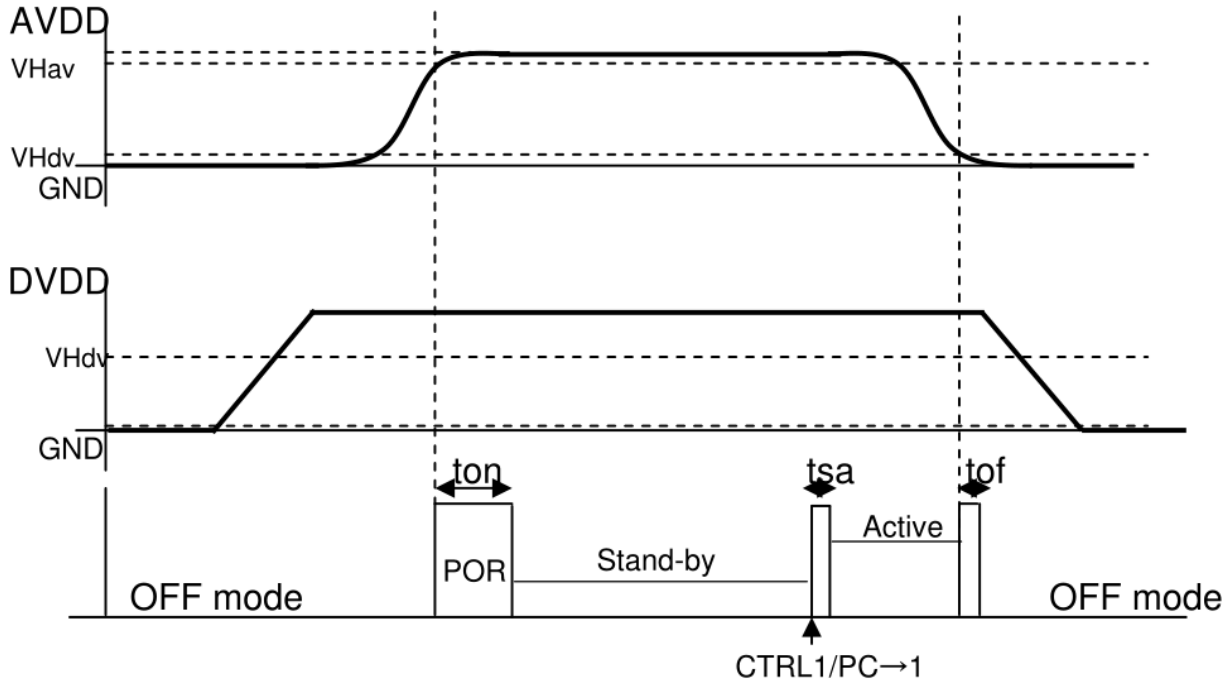


Figure 7 - Power Supply Sequence 1

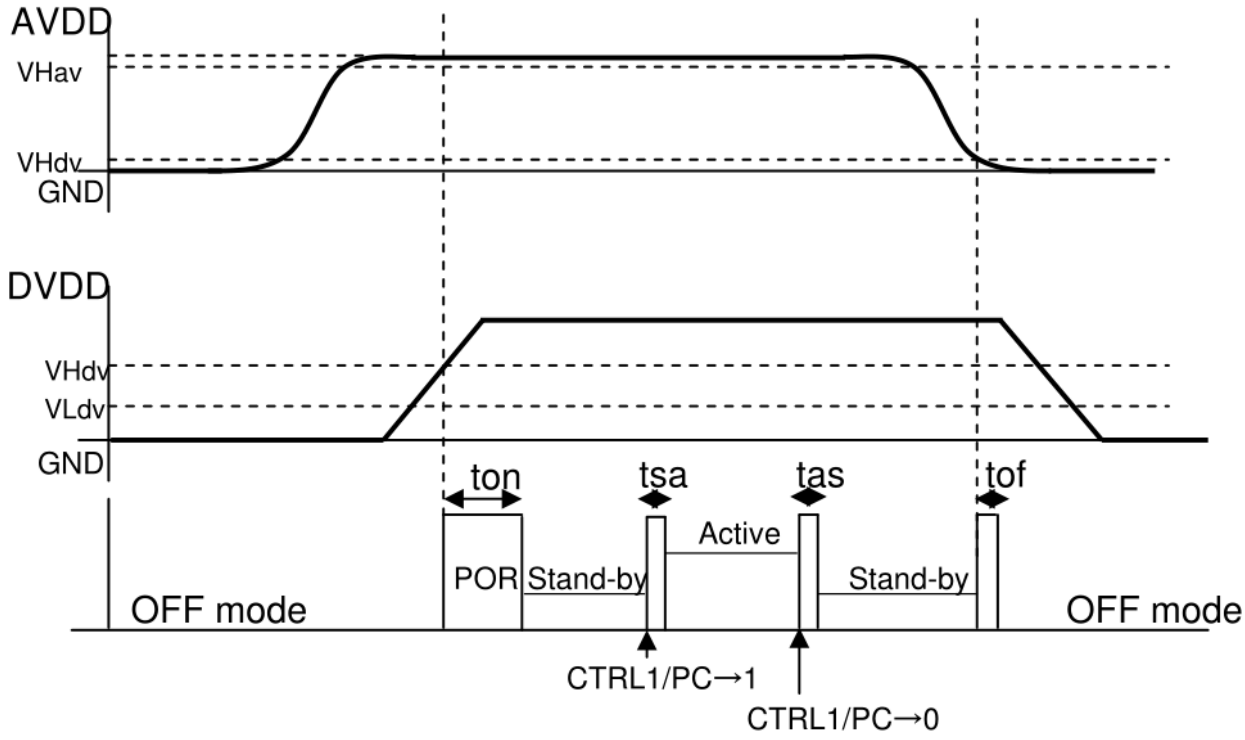


Figure 8 - Power Supply Sequence 2

Parameters on Supply voltage sequence (All Condition)

Transition	Symbol	Typ.	Max.	Unit
OFF→Stand-by	ton	-	3	ms
Stand-by→Active	tsa	-	5	μs
Active→Stand-by	tas	-	5	μs
Active or Stand-by→OFF	tof	-	10	ms

Table 10 - Power Supply Voltage Timing

Parameters on Supply voltage sequence (All Condition)

Characteristics	Symbol	Min.	Max.	Unit
AVDD ON	VHav	1.75	-	V
AVDD OFF	VLav	-	0.17	V
DVDD ON	VHdv	1.53	-	V
DVDD OFF	VLdv	-	0.17	V

Table 11 - Power Supply Voltage Levels (for sequencing purposes only)

- There is no limitation in the turn-on timing of the AVDD and the DVDD voltages.
- Case 1:
  - When the DVDD voltage turns on initially.
  - After the DVDD voltage has risen (reached VHdv).
  - The AVDD's voltage rising slope must rise (reach 0.9*AVDD) within 1.5 [msec].

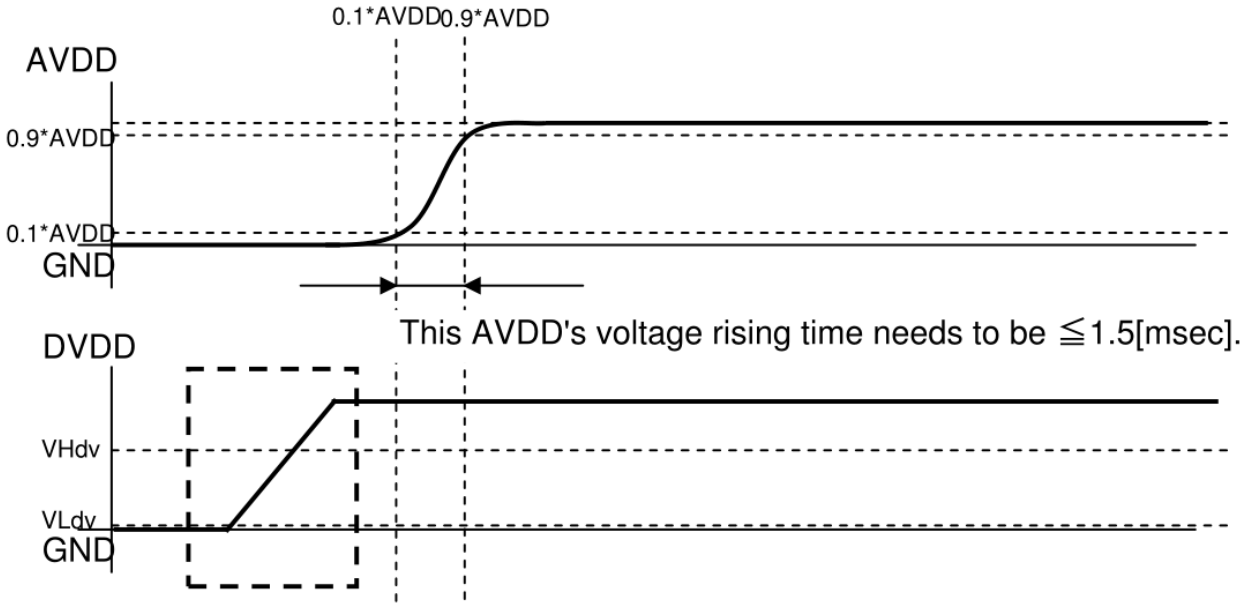


Figure 9- AVDD and DVDD Turn-On Timing

6 MAGNETOMETER OPERATION

6.1 Magnetometer Operational Modes

The various operational modes of the magnetometer are shown below.

Initialization	Power on reset is performed by turning on the power. All circuits and registers are set to default and the mode is set to stand-by mode automatically by POR. Software reset can be performed by writing to a control register. All registers is reloaded from OTP and the internal compensation table is reloaded.
Self-Test	Self-test confirms the operation of the sensor by register command.
Functional Modes	The sensor has stand-by mode and active mode for power control. There are two states in active mode.
Off mode	The sensor is not active when AVDD and/or DVDD are disabled.
Stand-by Mode	Low power state. Stand-by mode can access I2C registers (read / write).
Active Mode	Change from stand-by to active mode by register command to control register.
Force State	Start to measure and output data by register command. Force state is default.
Normal State	Measure sampled magnetometer data by using an internal timer.
Data Ready Function	Occurs when new measured results are updated. The DRDY pin can be used to indicate new sample data is available.
Offset Calibration Function	Sensor offset can be canceled by using internal DAC circuit and digital compensation function.
Offset Drift Function	When magnetic field strength drifts, the output data values can be compensated by writing to the offset value registers.
Temperature Measurement Function	Retrieve temperature data from internal temperature sensor. Temperature data is used for internal compensation of output data.
Temperature Compensation Function	Compensate gain, via digital circuitry, by temperature measurement results.

The magnetometer has several states whose primary purpose is power management. A simplified state diagram is shown below.

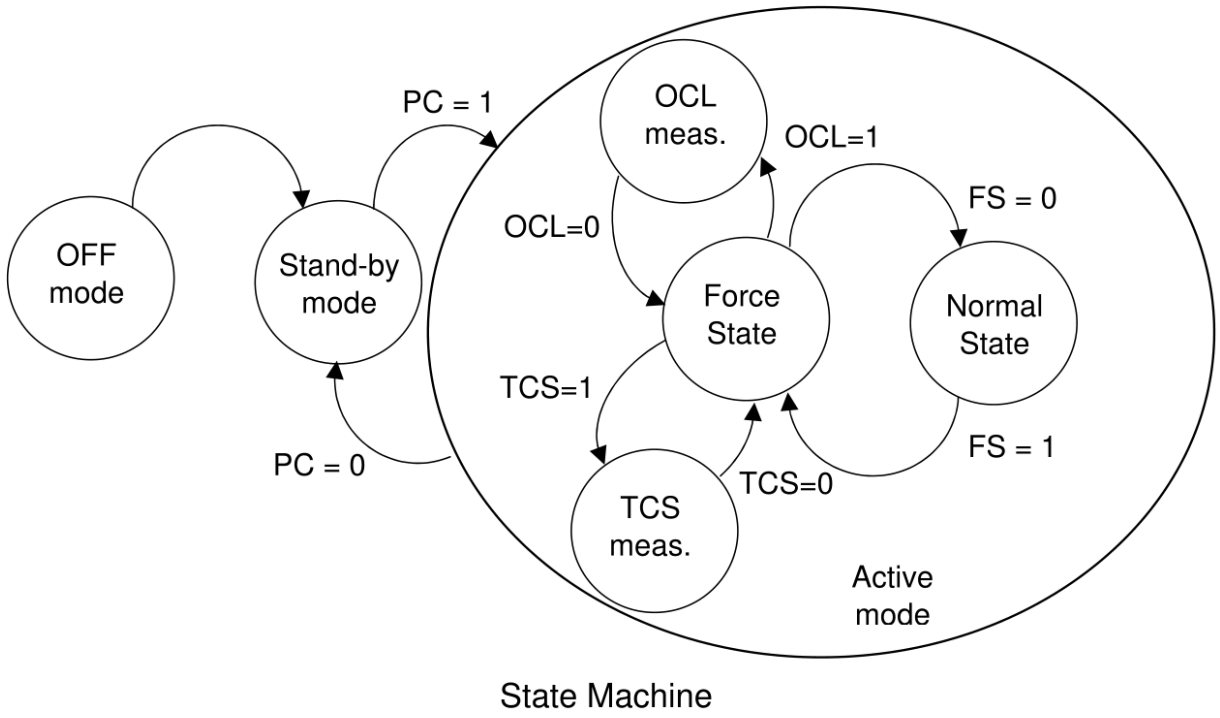


Figure 10. Magnetometer State Diagram

6.2 Initialization

- All internal circuits and all register values are initialized by an internal POR (Power On Reset) circuit after power-on.
- After initialization, the functional mode moves to standby mode automatically.
- The software reset set by the register command SRST=1 sets all register value to defaults and reload the compensation values for internal sensor calculation.

6.2.1 Self-Test

- Self-test can be used to confirm the internal sensor interface and digital logic.
- Self-test is performed by reading the STB register and setting the register command CTRL3 STC bit to Hi.
- The following chart shows the procedure to execute self-test.
- Following a properly function self-test operation, the value of response register STB will be set to 0x55.

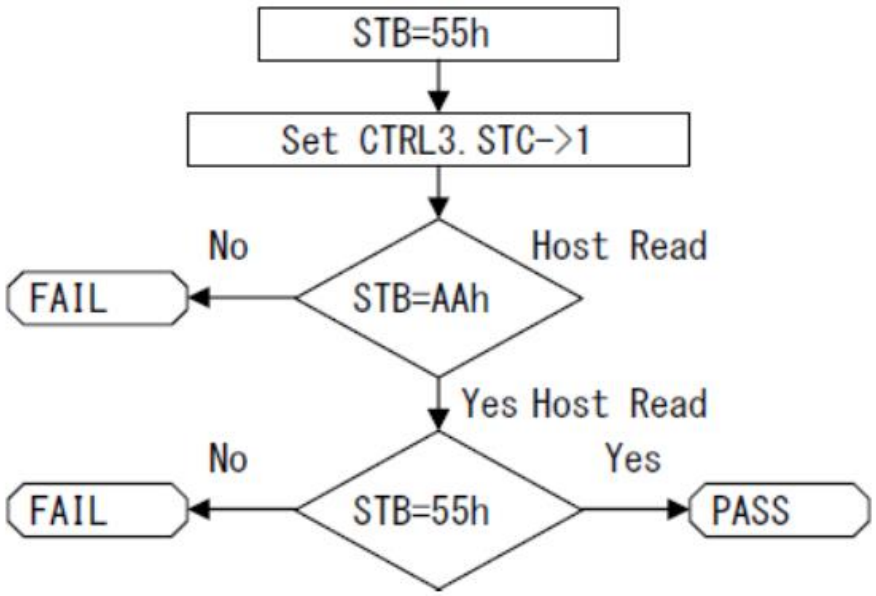


Figure 11 - Self Test Flow Chart

6.3 Modes

6.3.1 OFF mode

The sensor is not active when AVDD and/or DVDD are disabled. The following table shows each status of off mode.

AVDD	DVDD	Operation State
0V	0V	Sensor is not active. There is no activity on the I2C bus.
0V	1.7V to 3.6V	Sensor is not active. There is no activity on the I2C bus.
1.7V to 3.6V	0V	Sensor is not active. There is no activity on the I2C bus.

Table 12. OFF Mode

6.3.2 Stand-by mode

After loading the POR (Power On Reset), internal state is moved to the standby mode automatically.

Read and Write access function is limited to the following in stand-by mode:

- Write: (CTRL3) FORCE, TCS and STC are disabled
- Read: All resisters can be read.
- Register is changed from the Active mode to the Stand-by mode by setting PC=0 (CNTL1).

6.3.3 Active mode

At active mode, each function can be performed by setting control register 3 (CTRL3). To transfer to active mode, set the PC=1 (CTRL1).

- There are two types of measurement state. One is periodical measurement "Normal state," controlled by inner timer, and the other is "Force state," controlled by register command set by I2C access.
- The measurement state is selectable with FS bit on control register 1 (CTRL1).
- The default of measurement state is the force state (FS=1) after POR or reset running.

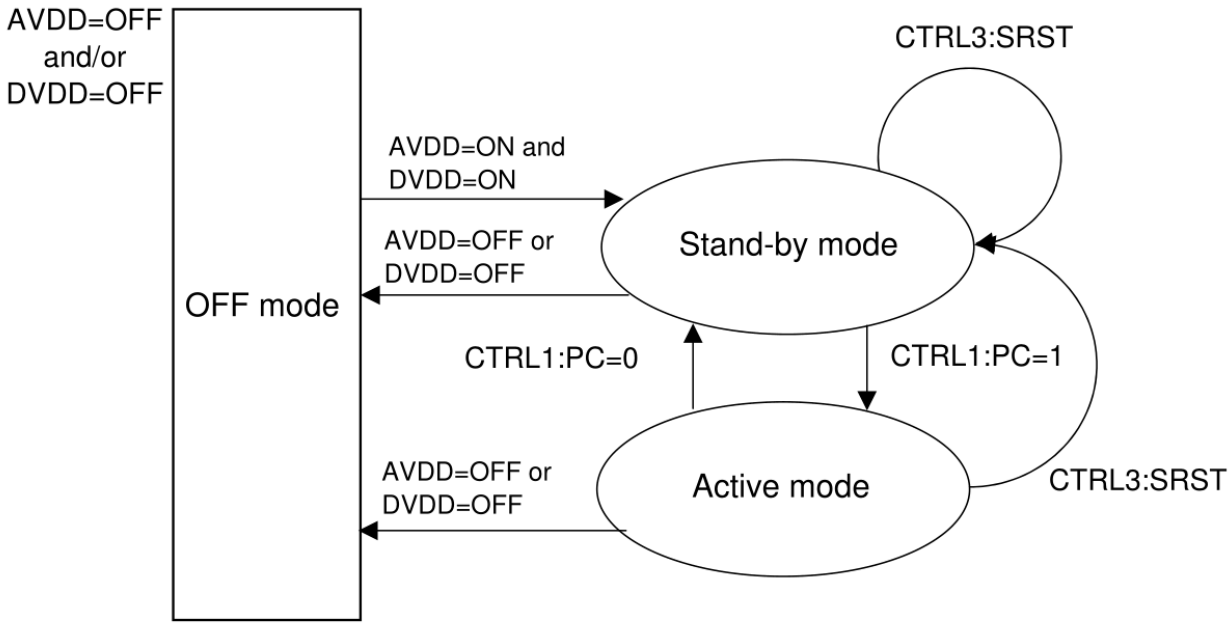


Figure 12 - Transferring Between Modes

6.3.3.1 FORCE STATE

Force State is used for synchronous measurement (selected from register CTRL3, bit FRC). Measurements start after forced register command are written to register via I2C.

- Functional mode changes from Stand-by mode to Active mode by setting register(Control1: bit PC) to "1".
- Force State is set by control register (CNTL1: bit FS) "1".
- Acquired data stored to output register (OUTX, OUTY, OUTZ), and status register(STAT: bit DRDY) is set to "1" and output signal (DRDY PIN) are set to active.
- Output on external DRDY PIN is set by control register (CNTL2).
- During reading data, output register is not updated. After reading is complete, reading data is updated.
- Change of state from Normal to Force is valid after measurement if control register is set during the Active measuring in Normal state.

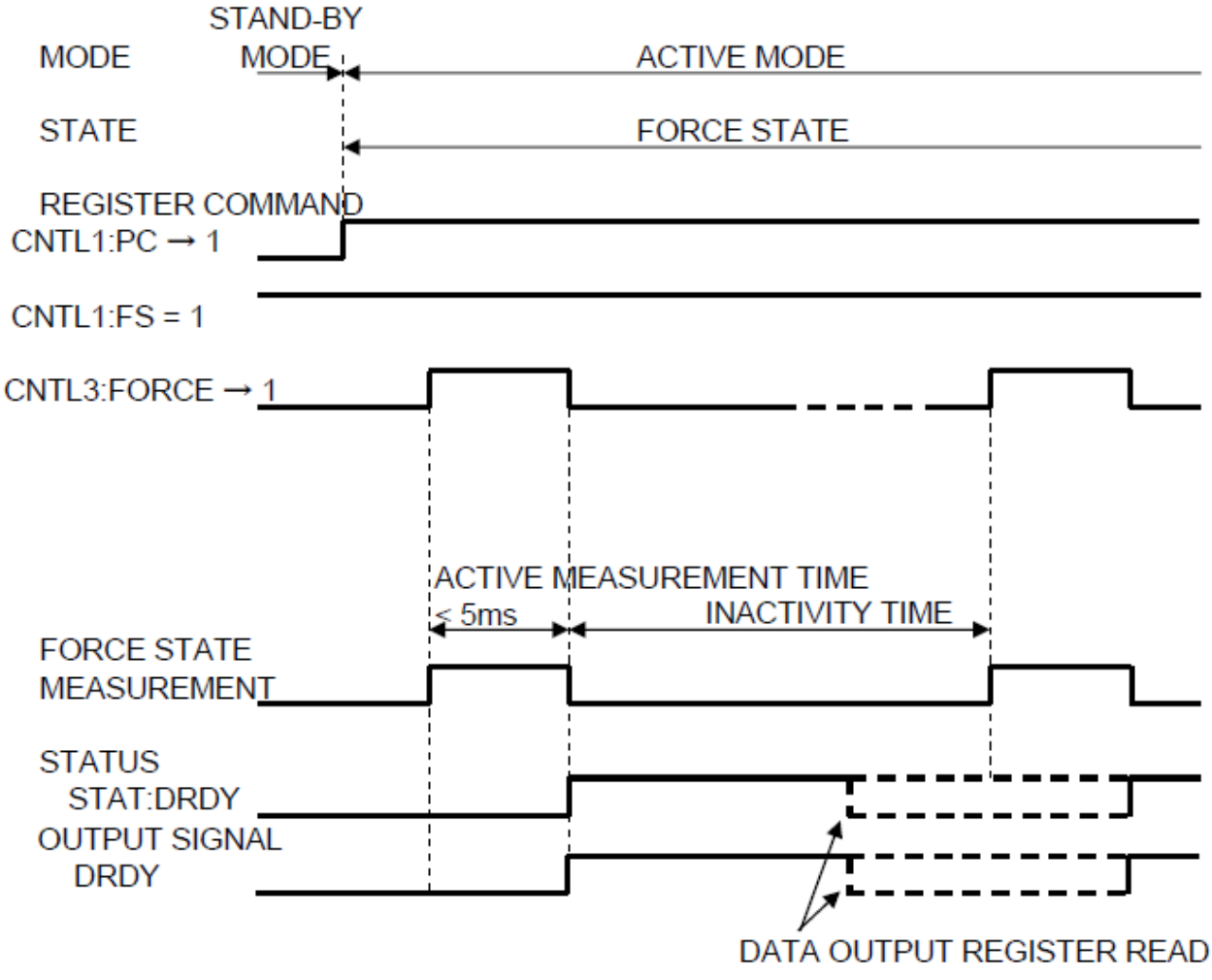


Figure 13 - Measurement Control Timing (Force State)

6.3.3.2 NORMAL STATE

- Normal state is a continuous measurement state, and when Normal state is set by setting “0” to control register (CNTL1: bit FS), a measurement is started.
- Measurement time and interval are managed by an internal clock.
- Functional mode is changed from Stand-by mode to Active mode by setting register (CNTL1: bit PC) to "1".
- Output data rate (ODR) is selectable between 0.5Hz or 100Hz by register (CNTL1: bit ODR).
- Acquired data are stored to register (OUTX, OUTY, OUTZ), status register(STAT: bit DRDY) is set to "1" and output PIN signal are control with (CNTL2:bit DEN).

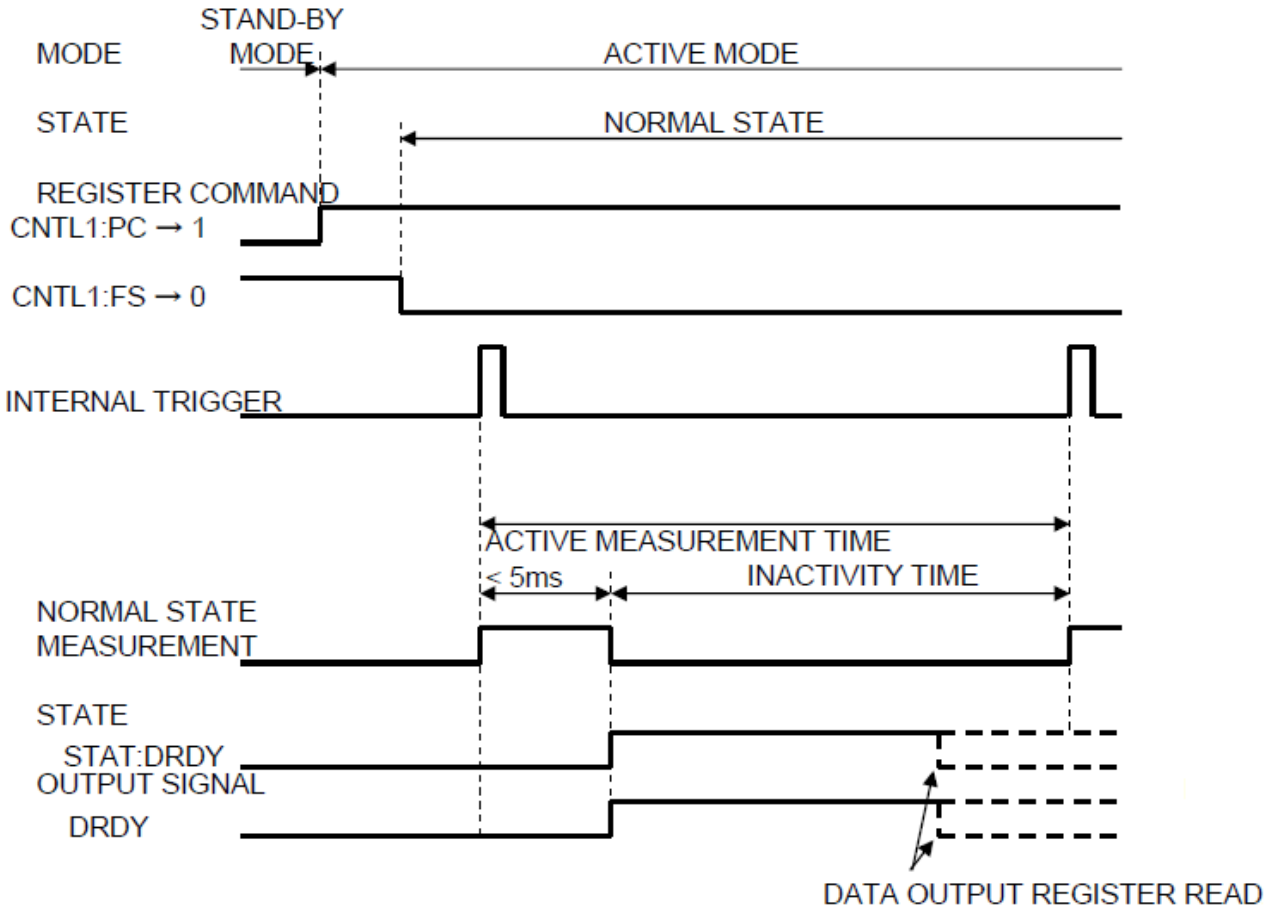


Figure 14 - Measurement Control Timing (Normal State)

6.4 Data Ready Interrupt Output (DRDY pin)

- This function is used to indicate that output sample data has been updated.
- Data ready output is enabled on the DRDY PIN, when the sensor data has been updated.
- The status (active / inactive) of the data ready pin can be read via the status register (STAT).
- DRDY is changed to inactive after reading data on the output register.
- Conditions of data ready function can be set in the control register (CTRL2).

CNRL2 bit	Bit Name	Default	Condition
4	DEN	0	Output control on DRDY PIN 0 = Disable 1 = Enable
3	DRP	1	The polarity setting on DRDY PIN 0 = Active Low 1 = Active High

Table 13 - Control Of DRDY Interrupt Output Pin

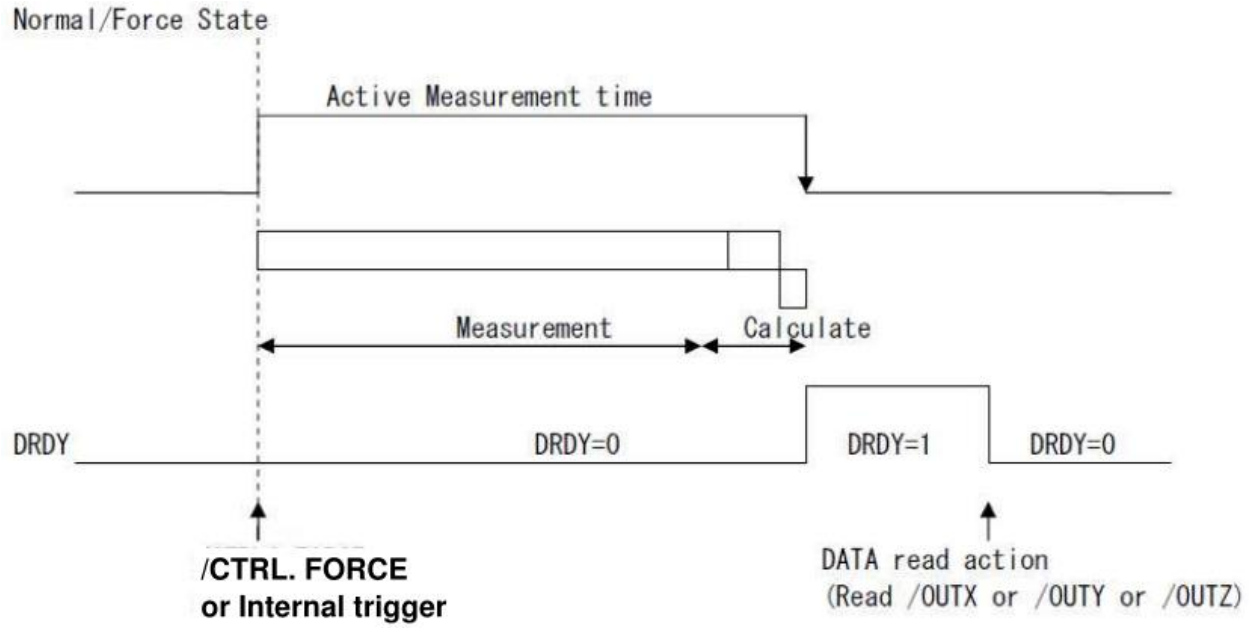


Figure 15 - Data Ready (DRDY) Interrupt Function

6.5 Offset Calibration

- This function is enabled when control register (CNTL3:OCL) is set to Hi during the Force State.
- The offset value for inner ADC output is calculated with the measured sensor offset, and then compensation values for the amplitude offset and the digital offset are set automatically.
- The OCL bit is changed to be low after the compensation offset value is updated, and then the status is back to what it was before measurement.

6.6 Offset Drift

- This function can make the digital compensation output that is add with values wrote by the host CPU on the offset drift register (OFFX, OFFY, OFFZ).
- Offset drift values can be set with 15bit signed value.

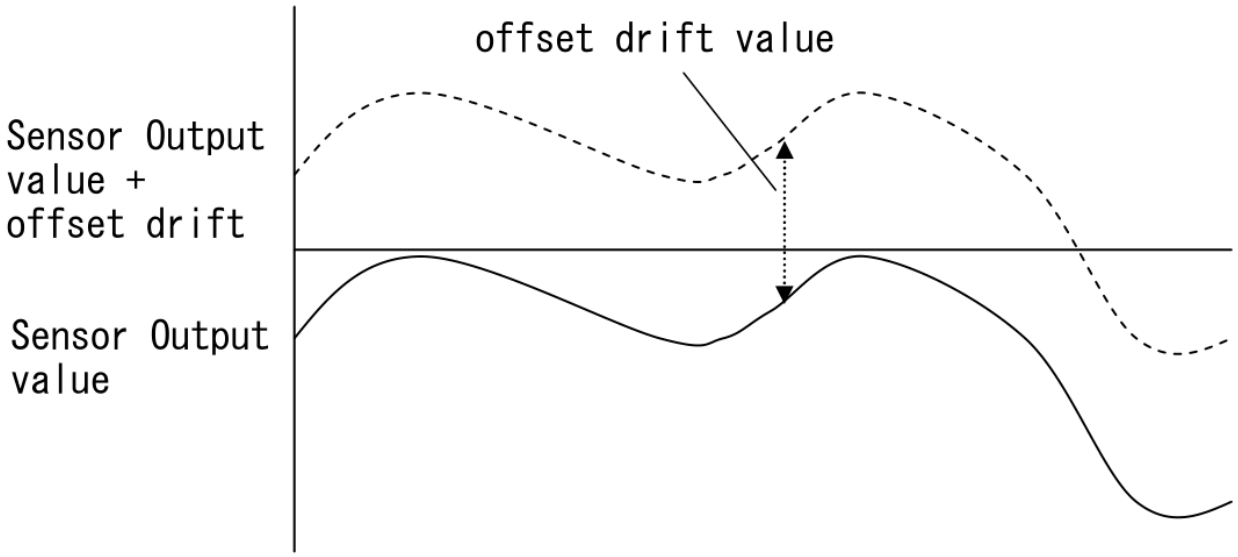


Figure 16 - Magnetometer Offset Drift

6.7 Temperature Measurement and Compensation Function

- The temperature measurement function is executed by setting the register command TCS to "1" while in Force State. After measurement, TCS bit change to "0" and back to what it was before measurement.
- The measurement result is updated in the temperature value register (TEMP).
- Sensor output values are compensated with the temperature value register (TEMP).

7 ACCELEROMETER OPERATION

7.1 Accelerometer General Operation

The acceleration range is factory configured to ±8g. The internal sampling rate is fixed at 1024 samples per second. The resulting sensor readings are provided with 14-bits of resolution.

7.2 Accelerometer Sensor Sampling

Measurement data is stored in the “extended” registers XOUT_EX, YOUT_EX, and ZOUT_EX. The byte with the lower address of the byte pair is the least significant byte while the byte with the next higher address is the most significant byte. The 14-bit measurement is represented as 2’s complement format.14-bit samples occupy bits [13:0], with bits [15:13] occupied by the sign bit. The device sample rate is fixed at 1024 samples/second. The features Tap, Shake, Drop and Orientation detection are available.

Resolution	Acceleration Range	Value per bit (mg/LSB)	Full Scale Negative Reading	Full Scale Positive Reading	Comments
14-bit	±8g	~0.98	0xE000 (-8192)	0x1FFF (+8191)	Signed, 2’s complement number, results in registers XOUT_EX_L, XOUT_EX_H YOUT_EX_L, YOUT_EX_H ZOUT_EX_L, ZOUT_EX_H (Sign-extended. Integer interpretation also shown)

Table 14.Summary of Resolution, Range and Scaling

Based upon the intended application, filtering of the data samples may be desired. The device has several low-pass filter (LPF) options for the raw sample data intended to filter out undesired high frequency components. Related to this LPF setting is the GINT interrupt rate, which can be modified to occur based upon the LPF roll-off frequency, rather than the sample rate (fixed at 1024 samples / second). See Section 7.9Accelerometer GINT Interrupt for more information on this option. The cutoff points for the LPF can be set from 8Hz to 512 Hz. These, and the controls for the GINT rate, are described in Section 10.11Accelerometer OUTCFG: Output Configuration Register.

7.3 Accelerometer Offset and Gain Calibration

Digital offset and gain calibration can be performed on the sensor in order to reduce the effects of post-assembly influences and stresses which may cause the sensor readings to be offset from their factory values. These register controls are described in Sections 10.12 through 10.17.

7.4 Accelerometer Operational States

The device has two states of operation: STANDBY (the default state after power-up) and WAKE.

The STANDBY state offers the lowest power consumption. In this state, the I2C interface is active and all register reads and writes are allowed. There is no event detection, sampling, or acceleration measurement in the STANDBY state. Internal clocking is halted. Complete access to the register set is allowed in this state, but interrupts cannot be serviced. The device defaults to the STANDBY state following power-up. The time to change states from STANDBY to WAKE is less than 10µs.

Registers can be written (and therefore thresholds and other settings can be changed) only when the device is in STANDBY state.

The I2C interface allows write access to all registers only in the STANDBY state. In WAKE state, the only I2C register with write access permitted is the Accelerometer MODE: Mode Register. Full read access is allowed in all states.

State	I2C Bus	Description
STANDBY	Device responds to I2C bus (R/W)	Device is powered; Registers can be accessed via I2C. Lowest power state. No interrupt generation, internal clocking disabled. Default power-on state.
WAKE	Device responds to I2C bus (Read)	Continuous sampling and reading of sense data. All registers except the Accelerometer MODE: Mode Register are read-only.

Table 15.Accelerometer Operational States

7.5 Accelerometer Operational State Flow

Figure 17.Accelerometer Operational State Flow shows the operational state flow for the device. The device defaults to STANDBY following power-on.

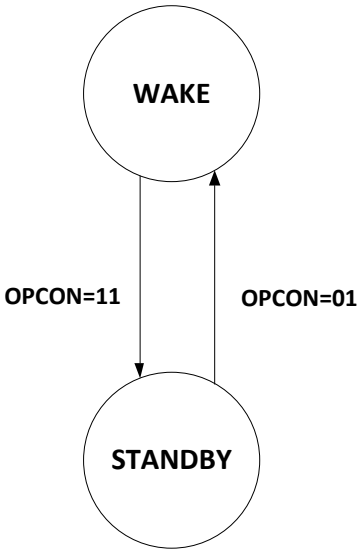


Figure 17.Accelerometer Operational State Flow

The operational state may be forced to a specific state by writing into the OPCON bits, as shown below. Two bits are specified in order to promote software compatibility with other mCube devices. The operational state will stay in the mode specified until changed:

Action	Setting	Effect
Force Wake State	OPCON[1:0] = 01	Switch to and remain in WAKE state Continuous sampling
Force Standby State	OPCON[1:0] = 11	Switch to and remain in STANDBY state Disable sensor and event sampling

Table 16. Forcing Accelerometer Operational States

7.6 Accelerometer Interrupts

The sensor device utilizes output pin INTN to signal to an external processor that an event has been sensed. The processor's interrupt service routine performs certain tasks after receiving this interrupt and reading the associated status bits, perhaps after the product was moved into a certain orientation or had been tapped. The processor sets up the registers such that when a specific event is detected, the processor would receive the interrupt and the interrupt service routine would be executed.

For products that use a polling method of interrupt servicing, the method of reading sensor data is slightly different. Instead of receiving an interrupt when an event occurs, the processor must periodically poll the sensor and read status data. In this case, the INTN pin is not used. For most applications, polling is best done at the sensor sampling rate or faster. Note that at least one I2C STOP condition must be present between samples in order for the sensor to update the sample data registers.

Note: for polling support, the event detection bits (TAPD, SHAKED, DROPD) and associated interrupt enable bits in the Accelerometer TILT: Status Register must still be set up as if interrupts would occur in order for the status registers to be updated with proper data.

Although the INTN is not connected, the registers in the sensor will still contain valid status and so can be used by software to know the orientation of the product or if an event has occurred.

7.7 Enabling and Clearing Interrupts

The Accelerometer INTEN: Interrupt Enable Register determines which events generate interrupts. When an event is detected, it is masked with an interrupt enable bit in this register and the corresponding status bit is set in the Accelerometer TILT: Status Register. Multiple interrupt events might be reported at the same time in the Accelerometer TILT: Status Register, so software must interpret and prioritize the results.

The pin INTN is cleared during the next I2C bus cycle after the device ID has been recognized by the device.

When an interrupt is triggered, the first I2C read access to the device clears INTN pin. The condition (TAPD, SHAKED, DROPD) that generated the interrupt will remain held in the Accelerometer TILT: Status Register until it is read. Note that the orientation bit-fields POLA and BAFR are continuously updated (every sample) in the Accelerometer TILT: Status Register and are not held. Note that multiple interrupts may be active at the same time, and so a software routine reading the Accelerometer TILT: Status Register should account for this.

Any of the following interrupts can be enabled or disabled in the Accelerometer INTEN: Interrupt Enable Register and Accelerometer Drop: Drop Event Control Register.

- Front/Back Interrupt
- Up/Down/Left/Right (portrait / landscape) Interrupt
- Tap Detection Interrupt
- GINT (real-time motion tracking, generate interrupt each sample period)
- Shake on X-axis, Shake on Y-axis, and Shake on Z-axis
- Drop event detection

The Accelerometer INTEN: Interrupt Enable Register contains many of the interrupt enable bits. The drop interrupt enable bit DINT is located in the Accelerometer Drop: Drop Event Control Register.

7.8 Accelerometer Interrupt Support

The following table shows the relationship between motion events and interrupt enable bits for determining when the device will generate an interrupt. No measurements or interrupts are generated in the STANDBY state.

Motion Event	Interrupt Enable Bits
Portrait/Landscape or Front/Back orientation change	FBINT = 1 PLINT = 1
Shake	SHINTX = 1 SHINTY = 1 SHINTZ = 1
Tap	TINT = 1
Drop	DINT = 1
Sample Update	GINT = 1

Table 17.Accelerometer Interrupt Support

7.9 Accelerometer GINT Interrupt

The GINT interrupt can trigger on each sample period (default), or be “filtered” by the bandwidth setting of the LPF. If the Accelerometer OUTCFG: Output Configuration Register IRATE bit is inactive, then the GINT interrupt will trigger each sample period. If the IRATE bit is active, the GINT interrupt rate will be updated based on the low-pass filter setting controlled by bit-field LPF.

7.10 Accelerometer Event Detection

The detection logic monitors and compares sensor outputs against the comparisons selected by the application software. Each type of event can be masked by a separate bit in the Accelerometer INTEN: Interrupt Enable Register. The following table shows how the detection events are evaluated.

Event	X Axis	Y Axis	Z Axis
Up	|Z|< (UD_Z_TH) and |X|> (UD_X_TH) and X < 0 [1]		
Down	|Z|< (UD_Z_TH) and |X|> (UD_X_TH) and X > 0 [1]		
Right		|Z|< (RL_Z_TH) and |Y|> (RL_Y_TH) and Y < 0 [2]	
Left		|Z|< (RL_Z_TH) and |Y|> (RL_Y_TH) and Y > 0 [2]	
Front			Z > FB_Z_TH [3]
Back			Z < -1 * FB_Z_TH [3]
SHAKED [4]	|X| > 1.3g ± SHAKE_TH	|Y| > 1.3g ± SHAKE_TH	|Z| > 1.3g ± SHAKE_TH
DROPD [5]	|X| < 0.5g ± DROP_TH	|Y| < 0.5g ± DROP_TH	|Z| < 0.5g ± DROP_TH
TAPD [6]	|X|> TAP_TH	|Y|> TAP_TH	|Z|> TAP_TH

Table 18.Accelerometer Detection Logic Event Evaluation

[1] Up/Down Z threshold is programmable from 0.425g to 1.172g, up/down X threshold is programmable from |X| to |X| + 0.747g.

[2] Right/left Z threshold is programmable from 0.425g to 1.172g, right/left Y threshold is programmable from |Y| to |Y| + 0.747g.

[3] Front/back Z threshold is programmable from 0.174g to 0.547g.

[4] SHAKED event is triggered when any axis > SHAKE_TH, programmable from 0.925g to 1.1672g.

[5] DROPD event is triggered when condition (a) |X|+|Y|+|Z| < 0.5g + DROP_TH or condition (b) |X|<0.5g ± DROP_TH and |Y| < 0.5g ± DROP_TH and |Z| < 0.5g ± DROP_TH, this is user selectable. The range is from 0.125g to 0.872g.

[6] TAPD event is triggered by |X|> TAP_TH or |Y|>TAP_TH g or |Z|>TAP_TH, where TAP_TH is programmable and any combination of X, Y, and Z may be selected.

7.11 Accelerometer Orientation Detection

The accelerometer in MC7010 allows an application to determine the orientation of the device. The current orientation of the device is reported as Left, Right, Up, Down, Front, and Back for each sampling period. This information generates the Portrait/Landscape status bits in the Accelerometer TILT: Status Register.

7.12 Orientation Hysteresis

Hysteresis can be added to portrait/landscape and front/back detection by modifying the default threshold offset values. See the specific sections below for more information.

7.13 Portrait/Landscape Events

Portrait/landscape detection is a combination of left, right, up, and down events, also partially dependent upon Z sensor readings of the Accelerometer.

The default comparison angle for portrait/landscape is 45 degrees when evaluating differences between LEFT, RIGHT, UP, and DOWN, as long as the magnitude of Z is < 0.8g (default). See Figure 18.

By increasing the threshold values written to the Accelerometer UD_X_TH: Up/Down X Axis Threshold and Accelerometer RL_Y_TH: Right/Left Y Axis Threshold, hysteresis can be introduced to the angle of evaluation. These registers add a small offset to the default X and Y values and introduce additional margin in the portrait/landscape detection logic.

For most applications, the same value should be written to both registers.

When the device orientation is in the hysteresis region, the device will report orientation as “unknown”. When this reading is reported, in order to implement a hysteresis effect for orientation, high-level software should use the last known portrait/landscape information.

In the example shown in Figure 19 the evaluation angle has been decreased to 40 degrees in each threshold, such that there is a 10 degree “deadband” or hysteresis-area between LEFT/RIGHT and DOWN/UP areas. The circle represents the acceleration in the Z axis, which has a default of 0.8g, or about a 33 degree tilt relative to the Z axis.

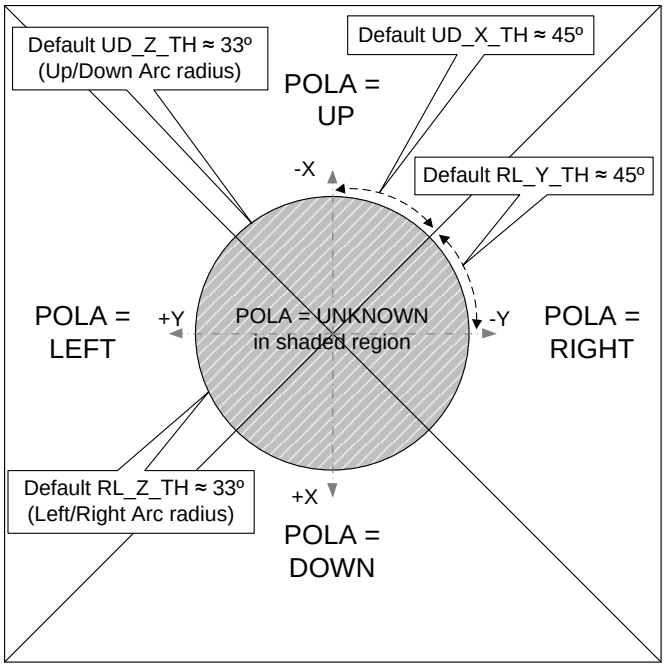


Figure 18. Default Orientation Settings

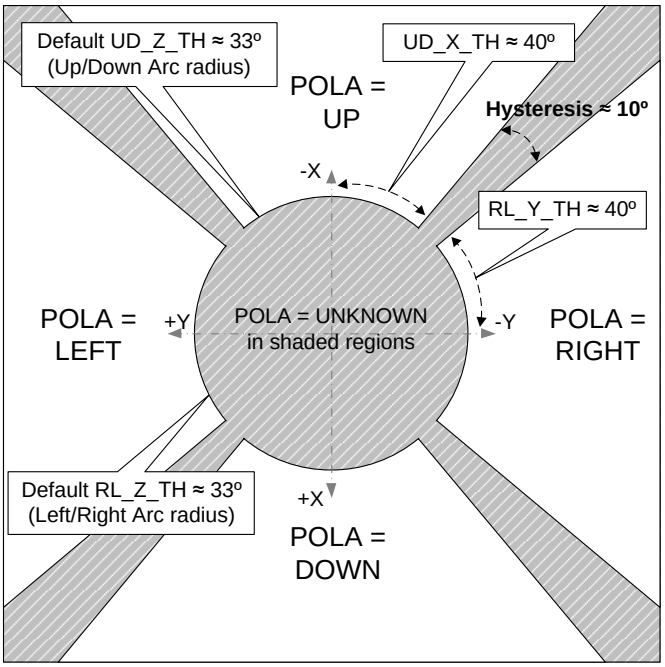


Figure 19. Example Simple Orientation Hysteresis = 10 degrees

The Z threshold for each direction can also be adjusted, as shown in Figure 20. This has the effect of altering the angle relative to the Z axis which causes the orientation state to change.

Figure 21 shows an example of setting the UD_Z_TH and RL_Z_TH registers to different values, as well as setting the UD_X_TH and RL_Y_TH registers to different values. However for most applications the same value should be written to both registers in both cases.

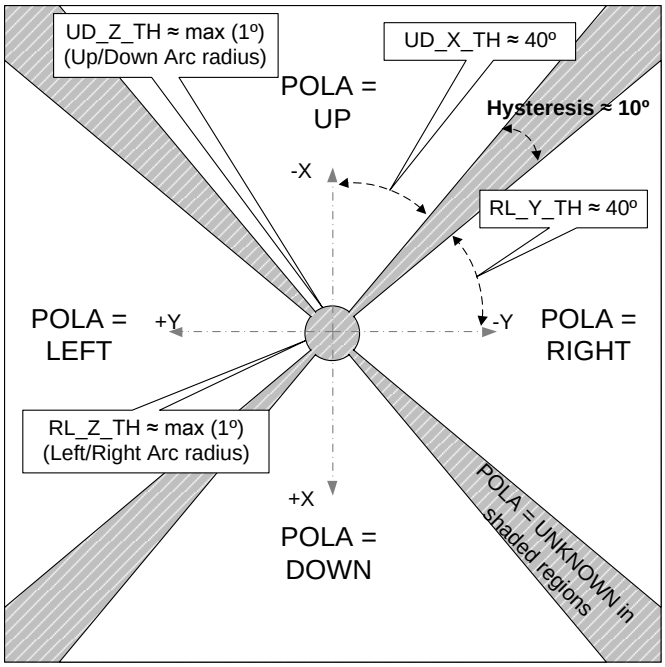


Figure 20. Effect of Changing UD_Z_TH Threshold with Hysteresis = 10 degrees

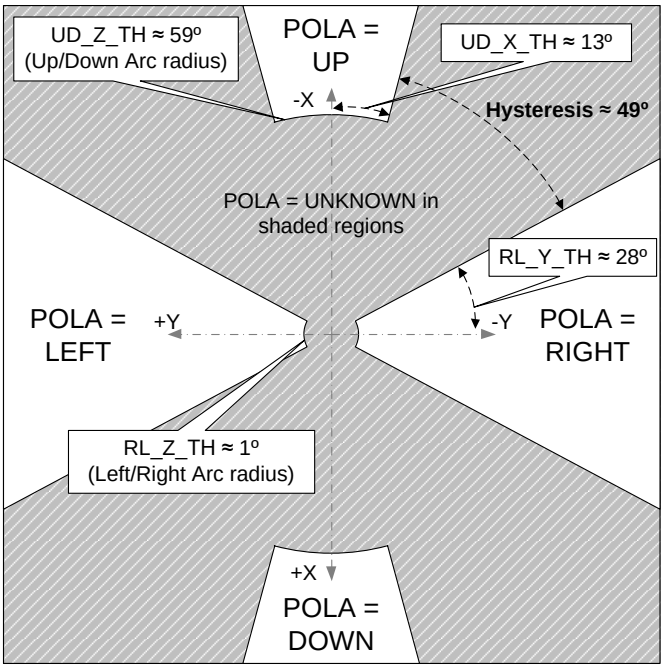


Figure 21. Example of Complex Thresholds for Up/Down X, Right/Left Y, Up/Down Z & Right/Left Z

Table 19 summarizes the portrait/landscape event evaluation criteria. Some example threshold values and the corresponding trip angle and amount of hysteresis are shown in Table 20.

Event	X Axis	Y Axis	Z Axis
Up	|Z|< (UD_Z_TH) and |X|> (UD_X_TH) and X < 0		
Down	|Z|< (UD_Z_TH) and |X|> (UD_X_TH) and X > 0		
Right		|Z|< (RL_Z_TH) and |Y|> (RL_Y_TH) and Y < 0	
Left		|Z|< (RL_Z_TH) and |Y|> (RL_Y_TH) and Y > 0	

Table 19.Accelerometer Portrait/Landscape Event Evaluation Criteria

Registers UD_X_TH or RL_Y_TH Threshold Value	Trip Angle (approx. degrees)	Resulting Hysteresis (approx. degrees)	Corresponding g Value (approximate)
0x00	45	0	0.72
0x10	43	4	0.68
0x20	41	8	0.66
0x30	39	12	0.63
0x40	37	16	0.61
0x50	36	20	0.58
0x60	34	24	0.55
…	…	…	…
0xFF	15	64	0.26

Table 20.Some Approximate X and Y-axis Portrait/Landscape Evaluation Angles and Values

Registers UD_Z_TH or RL_Z_TH Threshold Value	Trip Angle (approx. degrees)	Corresponding g Value (approximate)
0x80	67	0.43
0x90	64	0.47
…	…	…
0xE0	48	0.71
0xF0	45	0.75
0x00	40	0.80
0x10	36	0.85
0x20	32	0.89
…	…	…
0x70	9	1.13
0x7F	3	Max (~1.17)*

Table 21. Some Approximate Z-axis Portrait/Landscape Evaluation Angles and Values

NOTE*: Max values >1.0g are possible, to cover offset variations.

Table 22 shows the orientation event conditions for the portrait/landscape detection hardware.

POLA[2:0]	Left	Right	Down	Up	Description/Comments
000	0	0	0	0	Unknown
001	1	0	0	0	Left/Landscape
010	0	1	0	0	Right/Landscape
101	0	0	1	0	Down/Portrait
110	0	0	0	1	Up/Portrait

Table 22. Portrait/Landscape Accelerometer TILT: Status Register Assignments

7.14 Front/Back Events

The front/back detection compares ZOUT with a low g value, ranging from 0.174g to 0.547g, with the offset from 0.174g specified by the Accelerometer FB_Z_TH: Front/Back Z Axis Threshold Register. This equates to a range of approximately 55 degrees.

The BAFR bit-field is updated in the Accelerometer TILT: Status Register according to the front/back orientation sensed by the device. Additional hysteresis can be added to front/back detection by increasing the front/back Z axis threshold value located in the Accelerometer FB_Z_TH: Front/Back Z Axis Threshold Register.

When the front/back orientation of the device is in the deadband region, BAFR bit-field will report the orientation as “unknown”. The default settings (0x00) equate to a range of approximately 25 degrees where the sensor will report BAFR = FRONT (or BACK). The maximum settings (0xFF) equate to about a 80 degree range. See Figure 22 and Figure 23.

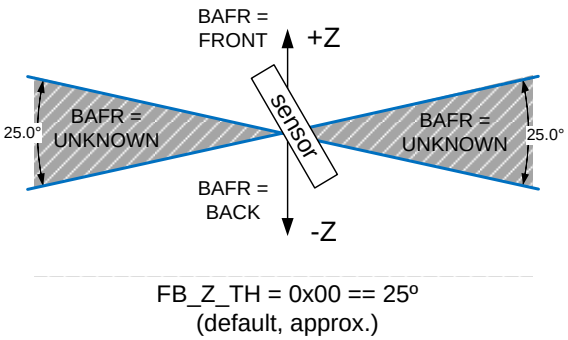


Figure 22. Default Setting of FB_Z_TH for BAFR Readings

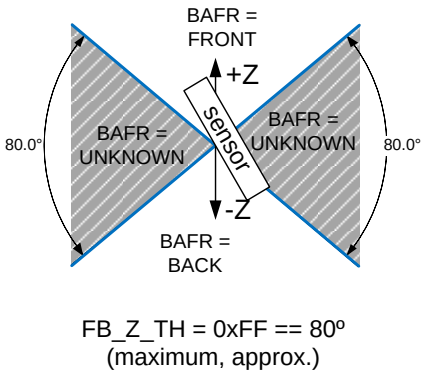


Figure 23.Maximum setting of FB_Z_TH for BAFR Readings

The bit settings for the BAFR bit-field are shown in Table 23. Table 24 shows the front/back orientation evaluation criteria. Some example threshold values and the corresponding trip angles are shown in Table 25. All values are approximate and not tested in production.

BAFR[1:0]	Status
00	Unknown condition of front or back
01	Front: Device is in orientation e. in Figure 3
10	Back: Device is in orientation f. in Figure 3
11	Reserved

Table 23. BAFR Bit Assignments in the Accelerometer TILT: Status Register

Event	X Axis	Y Axis	Z Axis
Front			Z > FB_Z_TH
Back			Z < -1 * FB_Z_TH

Table 24. Front/Back Event Evaluation

Threshold Value	FB_Z_TH Trip Angle (approx. degrees)
0x00	25
0x10	28
0x20	32
0x30	35
0x40	39
0x50	42
0x60	46
0x70	49
…	…
0xFF	80

Table 25. Approximate Front/Back Evaluation Angles and Values

7.15 Shake Detection

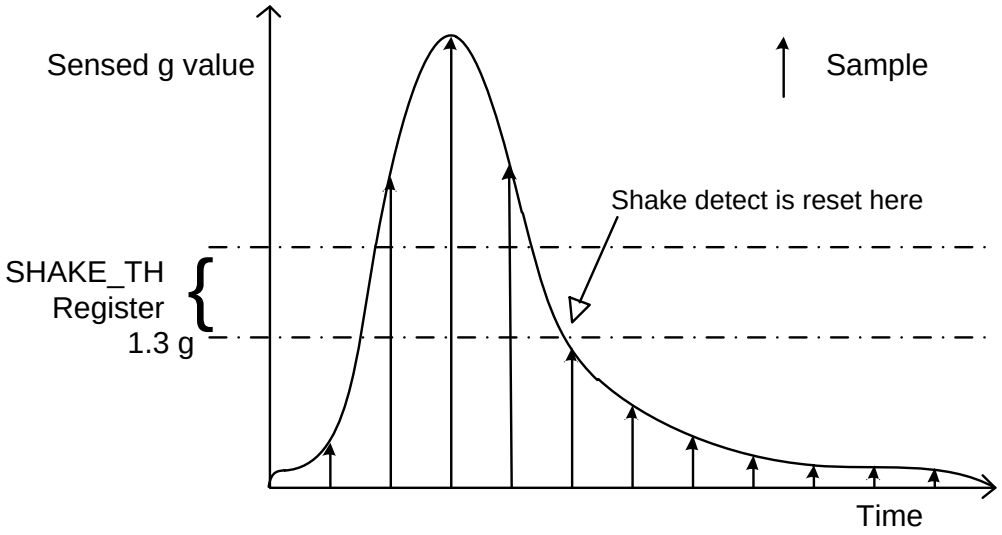
The threshold for detecting a shake event can be set to a range of values around a 1.3g baseline. The shake threshold can range from 0.925g to 1.672g. The value is a signed, 2's complement number. Resolution is approximately 2.9mg/bit.

A shake event will be triggered when high-g values are sensed for a sufficient number of samples. Accelerometer SHDB: Shake Debounce Register can be set to count from 1 to 63 events before setting the SHAKED bit in the Accelerometer TILT: Status Register. Higher values yield longer evaluation periods. See Figure 24 and Figure 25.

Shake detection can be any combination of axes. To enable detection even when not using interrupts, set the corresponding SHINTX, SHINTY, or SHINTZ bit-fields in the Accelerometer INTEN: Interrupt Enable Register.

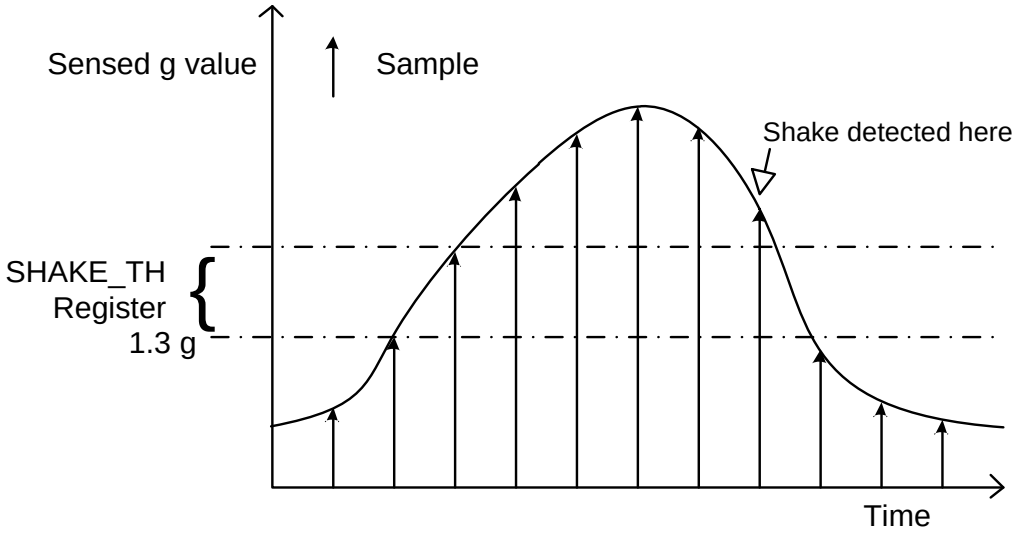
Event	X Axis		Y Axis		Z Axis
Shake	|X| > +1.3g ± Threshold	or	|Y| > +1.3g ± Threshold	or	|Z| > +1.3g± Threshold

Table 26. SHAKE Event Evaluation (Baseline + Offset)



Shake Debounce Register == 4 but the sensed g value is above 1.3g + SHAKE_TH for only 3 samples. Shake event is not detected.

Figure 24.Example Use of Shake Detection Hardware – Shake Not Detected



Shake Debounce Register == 4 and the sensed g value is above 1.3g + SHAKE_TH for 5 samples. Shake event is detected.

Figure 25. Example Use of Shake Detection Hardware – Shake Detected

7.16 Drop Detection

Drop detection is defined as a low-g acceleration applied to all axes. Two modes of drop detection are supported:

Mode A: Drop detection is a summation of all 3 axes:

Drop is detected when:

Sum(S(X) + S(Y) + S(Z)) < 0.5g ± DROP_TH Threshold

else Drop not detected;

Mode B: Drop detection is the logical AND of three comparisons:

Drop is detected when:

S(X) < 0.5g ± DROP_TH Threshold and

S(Y) < 0.5g ± DROP_TH Threshold and

S(Z) < 0.5g ± DROP_TH Threshold

else Drop not detected.

The typical drop threshold value is on the order of < 0.5g for all axes. The drop detection range is from 0.125g to 0.872g. The drop debounce value (bit-field DDB in the Accelerometer Drop: Drop Event Control Register) can filter from 1 to 8 consecutive events before setting the drop interrupt.

Event	**X Axis**		**Y Axis**		**Z Axis**
Drop Mode A	Sum (|X|	+	|Y|	+	|Z|) < 0.5g ± DROP_TH
Drop Mode B	|X| < 0.5g ± DROP_TH	and	|Y| < 0.5g ± DROP_TH	and	|Z| < 0.5g ± DROP_TH

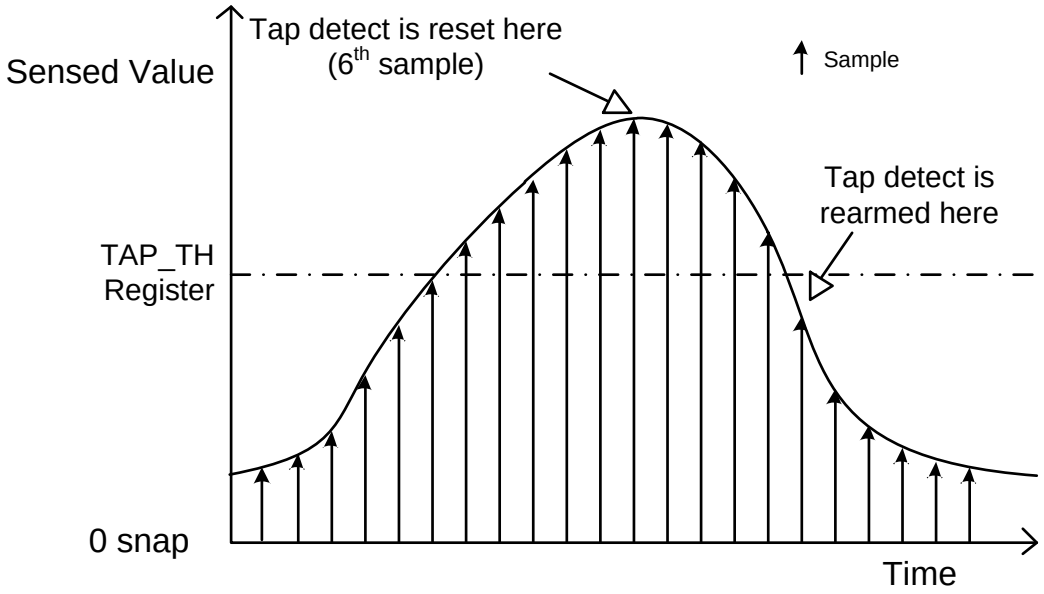
Table 27. Drop Event Evaluation

7.17 Accelerometer Tap Detection

On-chip tap detection hardware allows the device to detect user events such as on-screen button presses. Tap detection can be enabled or disabled on each axis via the Accelerometer TAPEN: Tap Detection Enable Register.

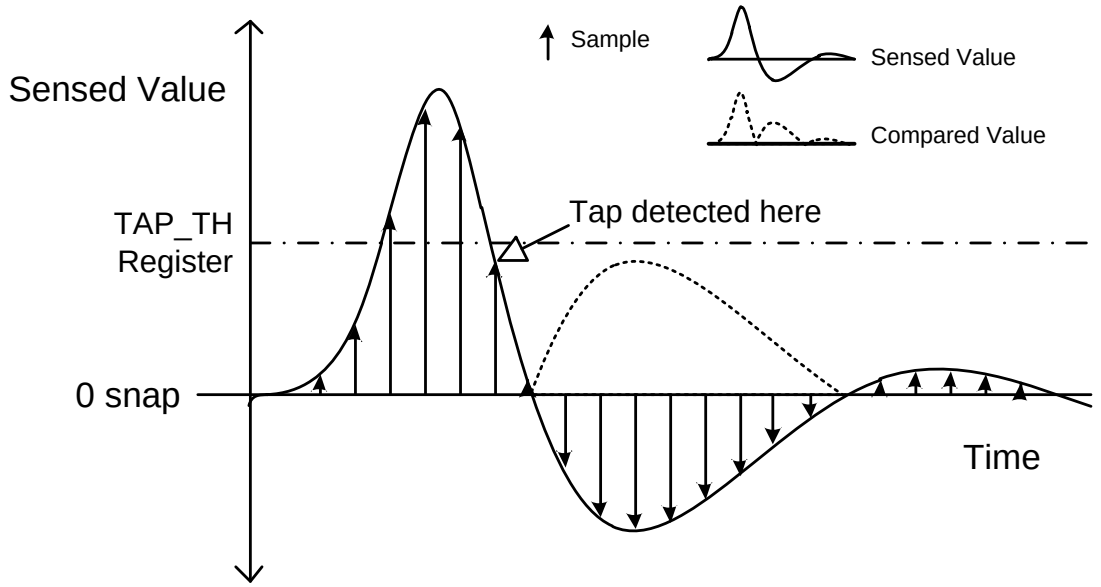
To detect fast, impulse events like a tap, the Accelerometer TAPP: Tap Pulse Register should be written with a tap pulse parameter that sets the maximum number of sample periods that a TAPD event may exceed the threshold before it is ignored by the detection logic. Sensed values that are above the threshold for long periods of time typically do not correspond to tap events.

For example, setting the pulse value to 5 requires that the tap impulse exceed the threshold for at least 1 sample period and up to 5 sample periods. The tap detection hardware is re-armed after the sensed value is below the threshold. See the example in Figure 26 and Figure 27.



Tap Pulse Register == 5 but the sensed value is above the threshold for 10 samples. No tap is detected.

Figure 26. Example Use of Tap Detection Hardware – No Tap Detected



Tap Pulse Register == 5 and the sensed value is above the threshold for 3 samples. Tap is detected.

Figure 27. Example Use of Tap Detection Hardware – Tap Detected

The threshold value, set by writing the Accelerometer TAP_TH: Tap Threshold Register, is an 8-bit unsigned number that species the threshold detection level for all tap events. This value is not an offset, but a magnitude which determines the minimum level for a valid tap event.

Event	X Axis	Y Axis	Z Axis
Tap	|X|> TAP_TH	|Y|> TAP_TH	|Z|> TAP_TH

Table 28. Default Tap Event Evaluation

7.18 Accelerometer Continuous Sampling

The device has the ability to read all sampled readings in a continuous sampling fashion. The device always updates the XOUT_EX, YOUT_EX, and ZOUT_EX registers at 1024 samples/second.

An optional interrupt can be generated each time the sample registers have been updated (GINT interrupt bit in the Accelerometer INTEN: Interrupt Enable Register). See Sections 7.9, 10.4 and 10.11 for GINT operation and options.

8 I2C INTERFACES

The I2C slave interface operates at a maximum speed of 400 kHz. MC7010 has two independent I2C interfaces, a dedicated one for magnetic sensor and one for accelerometer, the SDA (data) are open-drain, bi-directional pins and the SCL (clock) are input pins. SCL and SDA each require an external pull-up resistor, typically 4.7kΩ.

The MC7010 always operates as an I2C slave on both magnetometer and accelerometer I2C interfaces.

An I2C master initiates all communication and data transfers and generates the SCL clock that synchronizes the data transfer. The I2C device default addresses for the accelerometer is 0x4C, for the magnetic sensor is 0x0C.

The I2C interface remains active as long as power is applied to the DVDD and AVDD pins.

In the accelerometer, the device responds to I2C read and write cycles when it is in STANDBY state, but interrupts cannot be serviced or cleared. All registers can be written in the STANDBY state, but in WAKE only, the Accelerometer MODE: Mode Register can be modified. Internally, the registers which are used to store samples are clocked by the sample clock gated by I2C activity. Therefore, in order to allow the device to collect and present samples in the sample registers at least one I2C STOP condition must be present between samples.

The accelerometer requires a Stop bit between I2C transactions.

8.1 I2CSupport

The acceleration sensor supports Standard mode and Fast mode.

The magnetic sensor supports Standard mode, Fast mode , Fast mode Plus and Hi speed mode.

The magnetic sensor can seamlessly change from Fast mode to Hi speed mode using the master code (00001XXX).

The magnetic sensor supports multiple Read and Write mode.

The I2C clock stretch function is not supported.

8.1.1 Accelerometer I2C Address

The I2C device address is 0x4C (8-bit written address 0x98, reading address 0x99).

If an I2C burst read operation reads past register address 0x12 the internal address pointer “wraps” to address 0x03 and the contents of the Accelerometer TILT: Status Register are returned. This allows application software to burst read the contents of the six extended registers and the relevant device state registers in a single I2C cycle.

8.2 Timing

See Section 5.8I2C Timing Characteristics for I2C timing requirements.

8.3 I2CMessage Format

The device uses the following general format for writing to the internal registers. The I2C master generates a START condition, and then supplies the device ID. The 8th bit is the R/W# flag (write cycle = 0). The device pulls SDA low during the 9th clock cycle indicating a positive ACK. This means, from an 8-bit point of view of an external I2C master, writes should be written to address(0x98 for accelerometer) and reads will occur by reading address (0x99 for accelerometer).

The second byte is the 8-bit register address of the device to access, and the last byte is the data to write.

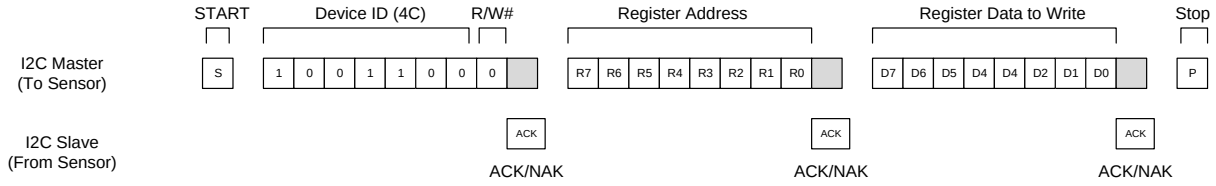


Figure 28.I2C Message Format, Write Cycle, Single Register Write

In a read cycle, the I2C master writes the device ID (R/W#=0) and register address to be read. The master issues a RESTART condition and then writes the device ID with the R/W# flag set to '1'. The device shifts out the contents of the register address.

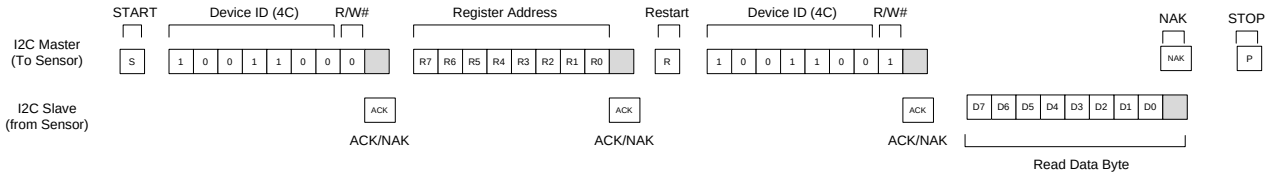


Figure 29.I2C Message Format, Read Cycle, Single Register Read

The I2C master may write or read consecutive register addresses by writing or reading additional bytes after the first access. The device will internally increment the register address.

9 MAGNETOMETER REGISTER INTERFACE

The device has a simple register interface which allows a MCU or I2C master to configure and monitor all aspects of the device. This section lists an overview of user programmable registers. By convention, Bit 0 is the least significant bit (LSB) of a byte register.

Sensor output values are signed integer (2's complement) presentation and little Endian order

The following table summarizes the registers in Magnetometer.

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
00-0B	---	---	---	---	---	---	---	---	---	00
0C	SelfTest response	STB[7:0]								55
0D	More Info version	0	0	0	1	0	0	0	1	11
0E	More Info	0	0	0	1	0	1	0	1	15
0F	Who I am	0	1	0	0	1	0	0	1	49
10	Output X LSB	OUTX[7:0]								00
11	Output X MSB	OUTX[15:8]								00
12	Output Y LSB	OUTY[7:0]								00
13	Output Y MSB	OUTY[15:8]								00
14	Output Z LSB	OUTZ[7:0]								00
15	Output Z MSB	OUTZ[15:8]								00
16-17	---	---	---	---	---	---	---	---	---	00
18	Status	---	DRDY	DOR	---	---	FFU	TRDY	ORDY	00
19	(TBD)	---	---	---	---	FP				00
1A	---	---	---	---	---	---	---	---	---	00
1B	Control1	PC	---	---	ODR[1:0]		---	FS	---	0A
1C	Control2	AVG	FCO	AOR	FF	DEN	DRP	DTS	DOS	04
1D	Control3	SRST	FORCE	---	STC	---	---	TCS	OCL	00
1E	Control4	MMD		---	RS	AS	---	---	---	80
1F	---	---	---	---	---	---	---	---	---	0
20	Offset X LSB	OFFX[7:0]								00
21	Offset X MSB	---	OFFX[14:8]							00
22	Offset Y LSB	OFFY[7:0]								00
23	Offset Y MSB	---	OFFY[14:8]							00
24	Offset Z LSB	OFFZ[7:0]								00
25	Offset Z MSB	---	OFFZ[14:8]							00
26	ITHR_L	ITHR_L								00
27	ITHR_H	---	---	ITHR_H						00
28-2F,30	---	---	---	---	---	---	---	---	---	00
31	Temperature value	TEMP[7:0]								19
32-5F	---	---	---	---	---	---	---	---	---	00

Table 29. Magnetometer Register Summary

9.1 Magnetometer Registers

Self Test Response Register (STB)

Address : 0Ch, Self Test Response (Read Only)

Bit	Name	Description
7:0	STB 7:0	Self test starts by STC bit (CNTL3 register). AAh is stored when CNTL3: bit STC sets to 1. 55h is stored after STB register is read.

Information Registers

Address : 0Dh, More Info version (Read Only)

Bit	Name	Description
7:0	INFO1 7:0	Information Value1 (11h)

Address : 0Eh, More Info (Read Only)

Bit	Name	Description
7:0	INFO2 7:0	Information Value2 (15h)

Address : 0Fh, Who Am I Value (Read Only)

Bit	Name	Description
7:0	WIA 7:0	Identify byte (49h)

Output Data Register (OUTX, OUTY, OUTZ)
- 14bit integer and 1FFFh (8191d) ~ E000h (-8192d)

Address : 10h, X-axis Output Data LSB (Read Only)

Bit	Name	Description
7:0	OUTX 7:0	X-axis Output Data, Signed Integer.

Address : 11h, X-axis Output Data MSB (Read Only)

Bit	Name	Description
7:6	X	Not Used
5:0	OUTX 14:8	X-axis Output Data, Signed Integer.

Address : 12h, Y-axis Output Data LSB (Read Only)

Bit	Name	Description
7:0	OUTY 7:0	Y-axis Output Data, Signed Integer.

Address : 13h, Y-axis Output Data MSB (Read Only)

Bit	Name	Description
7:6	X	Not Used
5:0	OUTY 14:8	Y-axis Output Data, Signed Integer.

Address : 14h, Z-axis Output Data LSB (Read Only)

Bit	Name	Description
7:0	OUTZ 7:0	Z-axis Output Data, Signed Integer.

Address : 15h, Z-axis Output Data MSB (Read Only)

Bit	Name	Description
7:6	X	Not Used
5:0	OUTZ 14:8	Z-axis Output Data, Signed Integer.

Status Register (STAT)

Address : 18h, Status (Read Only)

Bit	Name	Description
7	X	Not Used
6	DRDY	Data Ready Detection 0 = Not Detected, 1 = Detected
5	DOR	Data Overrun Detection 0 = Not Detected, 1 = Detected Note: if Read Output Data Register.
4:3	X	Not Used
2	FFU	Must be use Default setting. 0 = (Default)
1	TRDY	Must be use Default setting. 0 = (Default)
0	ORDY	Must be use Default setting. 0 = (Default)

NOTE: SOFTWARE MUST ALWAYS WRITE '0' TO BITS 0, 1 AND 2.

Control 1 Register (CTRL1)

Address : 1Bh, Control 1 (Write/Read)

Bit	Name	Description
7	PC	Power Mode Control 0 = Stand-by Mode (Default), 1 = Active Mode
6:5	X	Not Used (Read Only)
4:3	ODR 1:0	Output Data Rate Control in Normal State 00 = 0.5 Hz 01 = 10Hz (Default) 10 = 20Hz 11 = 100Hz
2	X	Not Used (Read Only)
1	FS	State Control in Active Mode 0 = Normal State 1 = Force State (Default)
0	X	Not Used (Read Only)

Control 2 Register (CTRL2)

- When a CTRL2 register value was changed during the measurement, The contents of the change are reflected after measurement.

Address : 1Ch, Control 2 (Write/Read)

Bit	Name	Description
7	AVG	Must be use Default setting. 0 = (Default) ※
6	FCO	Must be use Default setting. 0 = (Default) ※
5	AOR	Must be use Default setting. 0 = (Default) ※
4	FF	Must be use Default setting. 0 = (Default) ※
3	—	
2	—	
1	DTS	Must be use Default setting. 0 = (Default) ※
0	DOS	Must be use Default setting. 0 = (Default) ※

※. The change of this bit is prohibited.

Control 3 Register (CTRL3)

- Bit control at the same time is prohibited.
- Priority of this register is MSB.

Address : 1Dh, Control 3 (Write/Read)

Bit	Name	Description
7	SRST	Soft Reset Control Enable 0 = No Action (Default), 1 = Soft Reset Note: return to zero after soft reset.
6	FRC	Start to Measure in Force State 0 = No Action (Default), 1 = Measurement Start Note: return to zero after measurement.
5	X	Not Used (Read Only)
4	STC	Self Test Control Enable 0 = No Action (Default) 1 = Set parameters to Self Test Response (STB) register. Note: return to zero immediately.
3:2	X	Not Used (Read Only)
1	TCS	Start to Measure Temperature in Active Mode 0 = No Action (Default), 1 = Measurement Start
0	OCL	Start to Calibrate Offset in Active Mode 0 = No Action (Default), 1 = Action

Control 4 Register (CTRL4)

- When a CTRL4 register value was changed during the measurement,
  The contents of the change are reflected after measurement.

Address : 1Eh, Control 4 (Write/Read)

Bit	Name	Description
7:6	MMD	Must be use Default setting. 10 = (Default) ※
5	X	Not Used (Read Only)
4	RS	Set Dynamic range of output data. 0 = 14 bit signed value (-8192 to +8191) (Default) 1 = 15 bit signed value (-16384 to +16383)
3	AS	Must be use Default setting. 0 = (Default) ※
2:0	X	Not Used (Read Only)

※. The change of this bit is prohibited.

Offset Drift Value Register (OFFX, OFFY, OFFZ)

- Data is 14bit integer and 1FFFh (8191d) ~ E000h (-8192d)

Address : 20h, 14 bits X-axis Offset Drift Value LSB (Write/Read)

Bit	Name	Description
7:0	OFFX 7:0	X-axis Offset Drift Value, Signed Integer.

Address : 21h, 14 bits X-axis Offset Drift Value MSB (Write/Read)

Bit	Name	Description
7:6	X	Not Used (Read Only)
5:0	OFFX 13:0	X-axis Offset Drift Value, Signed Integer.

Address : 22h, 14 bits Y-axis Offset Drift Value LSB (Write/Read)

Bit	Name	Description
7:0	OFFY 7:0	Y-axis Offset Drift Value, Signed Integer.

Address : 23h, 14 bits Y-axis Offset Drift Value MSB (Write/Read)

Bit	Name	Description
7:6	X	Not Used (Read Only)
5:0	OFFY 13:8	Y-axis Offset Drift Value, Signed Integer.

Address : 24h, 14 bits Z-axis Offset Drift Value LSB (Write/Read)

Bit	Name	Description
7:0	OFFZ 7:0	Z-axis Offset Drift Value, Signed Integer.

Address : 25h, 14 bits Z-axis Offset Drift Value MSB (Write/Read)

Bit	Name	Description
7:6	X	Not Used (Read Only)
5:0	OFFZ 13:8	Z-axis Offset Drift Value, Signed Integer.

Temperature Data Register (TEMP)

- Temperature measurement is performed by setting register command (CNTL3 : bit TCS) when in the active mode
- Result is stored to temperature register (TEMP)
-Sensor output value are compensated with the temperature value stored TEMP register.

Address : 31h, Temperature Data (Read Only)

Bit	Name	Description
7:0	TEMP7:0	Temperature Data, Signed Integer. LSB = 1℃ 1000 0000 = -128℃ 0000 0000 = 0℃ 0111 1111 = 127℃

10 ACCELEROMETER REGISTER INTERFACE

The device has a simple register interface which allows a MCU or I2C master to configure and monitor all aspects of the device. This section lists an overview of user programmable registers. By convention, Bit 0 is the least significant bit (LSB) of a byte register.

Two registers are needed in order to contain each sample, the XOUT_EX, YOUT_EX & ZOUT_EX: X, Y, Z-Axis Extended Accelerometer Registers. The least significant byte is located in the register with a lower address (e.g. XOUT_EX_L), followed by the most significant byte in the next higher address (e.g. XOUT_EX_H).

10.1 Accelerometer Register Summary

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W[5]
0x00-0x02		RESERVED[6]										
0x03	TILT	Tilt Status Register	SHAKED	DROPD	TAPD	POLA [2]	POLA [1]	POLA [0]	BAFR [1]	BAFR [0]	0x00	R
0x04	OPSTAT	Operational State Status Register	OTPA	0	Resv	0	0	0	OPSTAT [1]	OPSTAT [0]	0x03	R
0x05		RESERVED[6]										
0x06	INTEN	Interrupt Enable Register	SHINTX	SHINTY	SHINTZ	GINT	ASINT	TINT	PLINT	FBINT	0x00	W
0x07	MODE	Mode Register	IAH	IPP	Resv[7]	Resv	Resv	0[8]	OPCON [1]	OPCON [0]	0x03	W
0x08		RESERVED[6]										
0x09	TAPEN	Tap Detection Enable Register	ZDA	YDA	XDA	Resv	Resv	Resv	Resv	Resv	0x00	W
0x0A	TAPP	Tap Pulse Register	Resv	Resv	Resv	Resv	TAPP [3]	TAPP [2]	TAPP [1]	TAPP [0]	0x00	W
0x0B	DROP	Drop Event Control Register	DROP_MODE	DINT	Resv	Resv	Resv	DROP_DB[2]	DROP_DB[1]	DROP_DB[0]	0x00	W
0x0C	SHDB	Shake Debounce Register	Resv	Resv	SHDB [5]	SHDB [4]	SHDB [3]	SHDB [2]	SHDB [1]	SHDB [0]	0x00	W
0x0D	XOUT_EX_L	XOUT Extended Register	XOUT_EX[7]	XOUT_EX[6]	XOUT_EX[5]	XOUT_EX[4]	XOUT_EX[3]	XOUT_EX[2]	XOUT_EX[1]	XOUT_EX[0]	0x00	R
0x0E	XOUT_EX_H	XOUT Extended Register	XOUT_EX[15]	XOUT_EX[14]	XOUT_EX[13]	XOUT_EX[12]	XOUT_EX[11]	XOUT_EX[10]	XOUT_EX[9]	XOUT_EX[8]	0x00	R
0x0F	YOUT_EX_L	YOUT Extended Register	YOUT_EX[7]	YOUT_EX[6]	YOUT_EX[5]	YOUT_EX[4]	YOUT_EX[3]	YOUT_EX[2]	YOUT_EX[1]	YOUT_EX[0]	0x00	R
0x10	YOUT_EX_H	YOUT Extended Register	YOUT_EX[15]	YOUT_EX[14]	YOUT_EX[13]	YOUT_EX[12]	YOUT_EX[11]	YOUT_EX[10]	YOUT_EX[9]	YOUT_EX[8]	0x00	R
0x11	ZOUT_EX_L	ZOUT Extended Register	ZOUT_EX[7]	ZOUT_EX[6]	ZOUT_EX[5]	ZOUT_EX[4]	ZOUT_EX[3]	ZOUT_EX[2]	ZOUT_EX[1]	ZOUT_EX[0]	0x00	R
0x12	ZOUT_EX_H	ZOUT Extended Register	ZOUT_EX[15]	ZOUT_EX[14]	ZOUT_EX[13]	ZOUT_EX[12]	ZOUT_EX[11]	ZOUT_EX[10]	ZOUT_EX[9]	ZOUT_EX[8]	0x00	R
0x13-0x1F		RESERVED[6]										
0x20	OUTCFG	Output Configuration Register	IRATE	LPF [2]	LPF [1]	LPF [0]	1[9]	1[9]	1[9]	1[9]	0x0F	W
0x21	XOFFL	X-Offset LSB Register	XOFF[7]	XOFF[6]	XOFF[5]	XOFF[4]	XOFF[3]	XOFF[2]	XOFF[1]	XOFF[0]	Per chip	W
0x22	XOFFH	X-Offset MSB Register	XGAIN[8]	Resv	XOFF [13]	XOFF [12]	XOFF [11]	XOFF [10]	XOFF [9]	XOFF [8]	Per chip	W
0x23	YOFFL	Y-Offset LSB Register	YOFF[7]	YOFF[6]	YOFF[5]	YOFF[4]	YOFF[3]	YOFF[2]	YOFF[1]	YOFF[0]	Per chip	W

[5] 'R' registers are read-only, via external I2C access. 'W' registers are read-write, via external I2C access.
[6] Registers designated as 'RESERVED' should not be accessed by software.
[7] Bits designated as 'Resv' are reserved for future use.
[8] Software must always write a zero '0' to this bit.
[9] Software must always write a one '1' to this bit.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W[5]
0x24	YOFFH	Y-Offset MSB Register	YGAIN[8]	Resv	YOFF [13]	YOFF [12]	YOFF [11]	YOFF [10]	YOFF[9]	YOFF[8]	Per chip	W
0x25	ZOFFL	Z-Offset LSB Register	ZOFF[7]	ZOFF[6]	ZOFF[5]	ZOFF[4]	ZOFF[3]	ZOFF[2]	ZOFF[1]	ZOFF[0]	Per chip	W
0x26	ZOFFH	Z-Offset MSB Register	ZGAIN[8]	Resv	ZOFF [13]	ZOFF [12]	ZOFF [11]	ZOFF [10]	ZOFF[9]	ZOFF[8]	Per chip	W
0x27	XGAIN	X Gain Register	XGAIN[7]	XGAIN[6]	XGAIN[5]	XGAIN[4]	XGAIN[3]	XGAIN[2]	XGAIN[1]	XGAIN[0]	Per chip	W
0x28	YGAIN	Y Gain Register	YGAIN[7]	YGAIN[6]	YGAIN[5]	YGAIN[4]	YGAIN[3]	YGAIN[2]	YGAIN[1]	YGAIN[0]	Per chip	W
0x29	ZGAIN	Z Gain Register	ZGAIN[7]	ZGAIN[6]	ZGAIN[5]	ZGAIN[4]	ZGAIN[3]	ZGAIN[2]	ZGAIN[1]	ZGAIN[0]	Per chip	W
0x2A		RESERVED[6]										
0x2B	SHAKE_TH	Shake Threshold Register	SHAKE_TH[7]	SHAKE_TH[6]	SHAKE_TH[5]	SHAKE_TH[4]	SHAKE_TH[3]	SHAKE_TH[2]	SHAKE_TH[1]	SHAKE_TH[0]	0x00	W
0x2C	UD_Z_TH	Up/Down Z Threshold Register	UD_Z_TH[7]	UD_Z_TH[6]	UD_Z_TH[5]	UD_Z_TH[4]	UD_Z_TH[3]	UD_Z_TH[2]	UD_Z_TH[1]	UD_Z_TH[0]	0x00	W
0x2D	UD_X_TH	Up/Down X Threshold Register	UD_X_TH[7]	UD_X_TH[6]	UD_X_TH[5]	UD_X_TH[4]	UD_X_TH[3]	UD_X_TH[2]	UD_X_TH[1]	UD_X_TH[0]	0x00	W
0x2E	RL_Z_TH	Right/Left Z Threshold Register	RL_Z_TH[7]	RL_Z_TH[6]	RL_Z_TH[5]	RL_Z_TH[4]	RL_Z_TH[3]	RL_Z_TH[2]	RL_Z_TH[1]	RL_Z_TH[0]	0x00	W
0x2F	RL_Y_TH	Right/Left Y Threshold Register	RL_Y_TH[7]	RL_Y_TH[6]	RL_Y_TH[5]	RL_Y_TH[4]	RL_Y_TH[3]	RL_Y_TH[2]	RL_Y_TH[1]	RL_Y_TH[0]	0x00	W
0x30	FB_Z_TH	Front/Back Z Threshold Register	FB_Z_TH[7]	FB_Z_TH[6]	FB_Z_TH[5]	FB_Z_TH[4]	FB_Z_TH[3]	FB_Z_TH[2]	FB_Z_TH[1]	FB_Z_TH[0]	0x00	W
0x31	DROP_TH	Drop Threshold Register	DROP_TH[7]	DROP_TH[6]	DROP_TH[5]	DROP_TH[4]	DROP_TH[3]	DROP_TH[2]	DROP_TH[1]	DROP_TH[0]	0x00	W
0x32	TAP_TH	Tap Threshold Register	TAP_TH[7]	TAP_TH[6]	TAP_TH[5]	TAP_TH[4]	TAP_TH[3]	TAP_TH[2]	TAP_TH[1]	TAP_TH[0]	0x00	W
0x33 to 0x3A		RESERVED[6]										
0x3B	PCODE	Product Code	1	0	0	1	0	0	0	0	0x90	R
0x3C to 0x3F		RESERVED[6]										

Table 30. Accelerometer Register Summary[10]

[10] No registers are updated with new event status or samples while an I2C cycle is in process.

10.2 Accelerometer TILT: Status Register

This register contains bits which are set when a motion event is detected. Each event has a corresponding interrupt enable which can mask any combination of events. The event detection bits (SHAKED, DROPD, TAPD) remain held until the register is read by the I2C interface. Note that the orientation bit-fields POLA and BAFR are continuously updated (every sample) in the Accelerometer TILT: Status Register and are not held. Note that multiple interrupts may be active at the same time, and so a software routine reading the Accelerometer TILT: Status Register should account for this. Refer to Figure 2. Package Axis Reference – Magnetometer & Accelerometer and Figure 3 Package Orientation – Accelerometer.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x03	TILT	Tilt Status Register	SHAKED	DROPD	TAPD	POLA [2]	POLA [1]	POLA [0]	BAFR [1]	BAFR [0]	0x00	R

BAFR[1:0]	Back or Front 00: Unknown condition of front or back 01: Front – Device is in orientation e in Figure 3. Package Orientation. 10: Back – Device is in orientation f in Figure 3. Package Orientation. 11: Reserved
POLA[2:0]	Portrait or Landscape 000: Unknown condition of up, down, left or right 001: Left – Device is in orientation b in Figure 3. Package Orientation. 010: Right – Device is in orientation c in Figure 3. Package Orientation. 011: Reserved 100: Reserved 101: Down – Device is in orientation d in Figure 3. Package Orientation. 110: Up – Device is in orientation a in Figure 3. Package Orientation. 111: Reserved
TAPD	0: Tap event not detected 1: Tap event detected
DROPD	0: Drop event not detected 1: Drop event detected
SHAKED	0: Shake event not detected 1: Shake event detected

Table 31.Accelerometer TILT Status Register Settings

10.3 Accelerometer OPSTAT: Operational State Status Register

The Operational State status register reports which operational state the device is in, either WAKE or STANDBY.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x04	OPSTAT	Operational State Status Register	OTPA	0	Resv	0	0	0	OPSTAT [1]	OPSTAT [0]	0x03	R

OPSTAT[1:0]	**Sampling State Register Status, Wait State Register Status** 00: Reserved 01: Device is in WAKE state 10: Reserved 11: Device is in STANDBY state, no sampling
Resv	Reserved
OTPA	**One-time Programming (OTP) activity status** 0: Internal memory is idle and the device is ready for use 1: Internal memory is active and the device is not yet ready for use

Table 32. Accelerometer Operational State Status Register

10.4 Accelerometer INTEN: Interrupt Enable Register

The interrupt enable register enables or disables interrupts on various motion events. If the corresponding interrupt enable bit is set, a matching event will generate an interrupt transition on the external interrupt pin, INTN. To enable the drop interrupt, set the DINT control bit in the Accelerometer Drop: Drop Event Control Register.

When an interrupt is triggered, the first I2C access to the device will clear the external interrupt pin, but the condition (TAPD, SHAKED, DROPD) that generated the interrupt will remain held in the Accelerometer TILT: Status Register until it is read. Note that the orientation bit-fields POLA and BAFR are continuously updated (every sample) in the Accelerometer TILT: Status Register and are not held.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x06	INTEN	Interrupt Enable Register	SHINTX	SHINTY	SHINTZ	GINT	Resv	TINT	PLINT	FBINT	0x00	W

FBINT	**Front / Back Interrupt** 0: Disable interrupt on front/back position change 1: Enable interrupt on front/back position change
PLINT	**Portrait / Landscape Interrupt** 0: Disable interrupt on up/down/left/right position change 1: Enable interrupt on up/down/left/right position change
TINT	**Tap Interrupt** 0: Disable interrupt on tap detection 1: Enable interrupt on tap detection
Reserved	Reserved
GINT	**Generate Interrupt** 0: Disable automatic interrupt after each measurement 1: Enable automatic interrupt after each measurement is updated in XOUT, YOUT, or ZOUT. The interrupt occurs for each measurement, not value change. See Section 7.9.
SHINTX	**Shake Interrupt, X-axis** 0: Disable X-axis interrupt, SHAKED is not set in Accelerometer TILT: Status Register upon event 1 : Enable X-axis interrupt, SHAKED is set in Accelerometer TILT: Status Register upon event
SHINTY	**Shake Interrupt, Y-axis** 0: Disable Y-axis interrupt, SHAKED bit is not set in Accelerometer TILT: Status Register upon event 1 : Enable Y-axis interrupt, SHAKED bit is set in Accelerometer TILT: Status Register upon event
SHINTZ	**Shake Interrupt, Z-axis** 0: Disable Z-axis interrupt, SHAKED bit is not set in Accelerometer TILT: Status Register upon event 1 : Enable Z-axis interrupt, SHAKED bit is set in Accelerometer TILT: Status Register upon event

Table 33. Accelerometer Interrupt Enable Register Settings

10.5 Accelerometer MODE: Mode Register

The MODE register controls the active operating state of the device. This register can be written from either operational state (STANDBY or WAKE).

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x07	MODE	Mode Register	IAH	IPP	Resv*	Resv*	Resv*	0*	OPCON[1]	OPCON[0]	0x03	W

NOTE*: Software must always write a zero ‘0’ to Bit 2. Bits 3, 4 and 5 are reserved.

OPCON [1:0]	00: Reserved	Set Device Operational State. WAKE or STANDBY
	01: Move to WAKE state and remain there	
	10: Reserved	
	11: Move to STANDBY state and remain there (STANDBY is the default POR state)	
IPP	0: Interrupt pin INTN is open drain (default) and requires an external pull-up to AVDD.	Interrupt Push Pull
	1: Interrupt pin INTN is push-pull. No external pull-up resistor should be installed.	
IAH	0: Interrupt pin INTN is active low	Interrupt Active High
	1: Interrupt pin INTN is active high	

Table 34. Accelerometer Mode Register Functionality

10.6 Accelerometer TAPEN: Tap Detection Enable Register

This register allows individual tap/pulse detection on each axis. Setting XDA, YDA, or ZDA adds the corresponding axis to tap event detection. See also Section 7.17Accelerometer Tap Detection.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x09	TAPEN	Tap Detection Enable Register	ZDA	YDA	XDA	Resv	Resv	Resv	Resv	Resv	0x00	W

XDA	0: Disable Tap detection on X-axis 1: Enable Tap detection on X-axis
YDA	0: Disable Tap detection on Y-axis 1: Enable Tap detection on Y-axis
ZDA	0: Disable Tap detection on Z-axis 1: Enable Tap detection on Z-axis

Table 35. Accelerometer TAPEN Register Settings

10.7 Accelerometer TAPP: Tap Pulse Register

This value sets the number of samples for which a tap pulse must exceed the TAP_TH threshold before it is rejected as not a tap event. If the values detected by the sensor exceed the TAP_TH threshold for longer than the reject count, no tap event is detected and the interrupt is not set. See also Section 7.17Accelerometer Tap Detection.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x0A	TAPP	TAP Pulse Register	Resv	Resv	Resv	Resv	TAPP [3]	TAPP [2]	TAPP [1]	TAPP [0]	0x00	W

TAPP [3:0]	Tap Detection Sample Periods (n)	Description
0x0	1	This tap detection filtering requires the sensed values to exceed the TAP_TH threshold level for n sample periods. When they have, the sensor will set TAPD bit in the Accelerometer TILT: Status Register. In addition, if the TINT tap interrupt is enabled in the Accelerometer INTEN: Interrupt Enable Register then an interrupt will be generated by the device.
0x1	2	
0x2	3	
0x3	4	
…	5 ≤ n ≤ 15	
0xF	16	

Table 36. Accelerometer TAPP Tap Pulse Register Settings

10.8 Accelerometer Drop: Drop Event Control Register

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x0B	DROP	Drop Event Control Register	DROP_MODE	DINT	Resv	Resv	Resv	DROP_DB[2]	DROP_DB[1]	DROP_DB[0]	0x00	W

DROP_DB[2:0]	**Drop Debounce** 000: 1 drop event 001: 2 adjacent drop events 010: 3 adjacent drop events … : 4 ≤ n ≤ 7 adjacent drop events 111: 8 adjacent drop events	Drop event debounce value, the number of drop events detected must reach this count for the final event to be valid.
DINT	**Drop Interrupt** 0: Disable drop event interrupt 1: Enable drop event interrupt	The DROPD bit in the Accelerometer TILT: Status Register will be set upon event occurrence regardless of this bit setting.
DROP_MODE	**Drop Mode** 0: Mode A: Drop detection is a summation of all 3 axes: Drop is detected when: Sum(mag(X) + mag(Y) + mag(Z)) < 0.5g ± DROP_TH Threshold else Drop not detected; 1: Mode B: Drop detection is the logical AND of three comparisons: Drop is detected when: mag(X) < 0.5g ± DROP_TH Threshold and mag(Y) < 0.5g ± DROP_TH Threshold and mag(Z) < 0.5g ± DROP_TH Threshold else Drop not detected.	

Table 37. Accelerometer Drop Event Control Register Settings

10.9 Accelerometer SHDB: Shake Debounce Register

The shake debounce register allows a 1 to 63 event count to be required before a valid shake event is detected or an interrupt is generated. The debounce value applies to all 3-axes.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x0C	SHDB	Shake Debounce Register	Resv	Resv	SHDB [5]	SHDB [4]	SHDB [3]	SHDB [2]	SHDB [1]	SHDB [0]	0x00	W

SHDB[5:0]	Adjacent Shake Events (n)	Description
0x01	1	Shake detection debounce filtering requires n adjacent shake detection events in order to trigger a shake event and set the SHAKED bit in the Accelerometer TILT: Status Register. In addition, if the SHINTX, SHINTY or SHINTZ bits are set in the Accelerometer INTEN: Interrupt Enable Register and that event occurs, then an interrupt will be generated by the device.
0x02	2	
0x03	3	
….	4 ≤ n ≤ 62	
0x3F	63	

Table 38. Accelerometer SH_DB Shake Debounce Register Settings

10.10 XOUT_EX, YOUT_EX & ZOUT_EX: X, Y, Z-Axis Extended Accelerometer Registers

The measurements from sensors for the 3-axes are written to the registers XOUT_EX, YOUT_EX & ZOUT_EX: X, Y, Z-Axis Extended Accelerometer Registers. The most-significant bit of the value is the sign bit, and is sign extended to the higher bits. Note that all 3 axes are sampled and updated simultaneously. If an I2C burst read operation reads past register address 0x12 the internal address pointer “wraps” to address 0x03 and the contents of the Accelerometer TILT: Status Register are returned. This allows application software to burst read the contents of the six extended registers and relevant device state registers in a single I2C read cycle.

Once an I2C start bit has been recognized by the sensor, registers will not be updated until an I2C stop bit has occurred. Therefore, if software desires to read the low and high byte registers ‘atomically’, knowing that the values have not been changed, it should do so by issuing a start bit, reading one register, then reading the other register then issuing a stop bit. Note that all 6 registers may be read in one burst with the same effect.

14-bit samples occupy bits [13:0], with bits [15:13] occupied by the sign bit.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x0D	XOUT_EX_L	XOUT Extended Register	XOUT_EX[7]	XOUT_EX[6]	XOUT_EX[5]	XOUT_EX[4]	XOUT_EX[3]	XOUT_EX[2]	XOUT_EX[1]	XOUT_EX[0]	0x00	R
0x0E	XOUT_EX_H	XOUT Extended Register	XOUT_EX[15]	XOUT_EX[14]	XOUT_EX[13]	XOUT_EX[12]	XOUT_EX[11]	XOUT_EX[10]	XOUT_EX[9]	XOUT_EX[8]	0x00	R
0x0F	YOUT_EX_L	YOUT Extended Register	YOUT_EX[7]	YOUT_EX[6]	YOUT_EX[5]	YOUT_EX[4]	YOUT_EX[3]	YOUT_EX[2]	YOUT_EX[1]	YOUT_EX[0]	0x00	R
0x10	YOUT_EX_H	YOUT Extended Register	YOUT_EX[15]	YOUT_EX[14]	YOUT_EX[13]	YOUT_EX[12]	YOUT_EX[11]	YOUT_EX[10]	YOUT_EX[9]	YOUT_EX[8]	0x00	R
0x11	ZOUT_EX_L	ZOUT Extended Register	ZOUT_EX[7]	ZOUT_EX[6]	ZOUT_EX[5]	ZOUT_EX[4]	ZOUT_EX[3]	ZOUT_EX[2]	ZOUT_EX[1]	ZOUT_EX[0]	0x00	R
0x12	ZOUT_EX_H	ZOUT Extended Register	ZOUT_EX[15]	ZOUT_EX[14]	ZOUT_EX[13]	ZOUT_EX[12]	ZOUT_EX[11]	ZOUT_EX[10]	ZOUT_EX[9]	ZOUT_EX[8]	0x00	R

Table 39. Accelerometer Extended Registers

10.11 Accelerometer OUTCFG: Output Configuration Register

This register can be used to set the resolution of the accelerometer measurements, the maximum g-range and low-pass filter settings for sampling and the bandwidth setting for the GINT interrupt. The lowest 4 bits must be set by software to binary b‘1111.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x20	OUTCFG	Output Configuration Register	IRATE	LPF [2]	LPF [1]	LPF [0]	1*	1*	1*	1*	0x0F	W

NOTE*: Software must always write a ‘1’ to bits 0 to 3.

LPF[2:0]	**Low Pass Filter Bandwidth** 000: Low-pass filter set to 512 Hz bandwidth 001: Low-pass filter set to 256 Hz bandwidth 010: Low-pass filter set to 128 Hz bandwidth 011: Low-pass filter set to 64 Hz bandwidth 100: Low-pass filter set to 32 Hz bandwidth 101: Low-pass filter set to 16 Hz bandwidth 110: Low-pass filter set to 8 Hz bandwidth 111: Reserved
IRATE	**GINT Sample Rate Trigger** 0: GINT interrupt updates at sample acquisition rate 1: GINT interrupt updates at LPF bandwidth setting determined by LPF[2:0] If IRATE=’1’, the GINT interrupt will occur at the same rate as the bandwidth setting of the LPF. This prevents extraneous sample acquisition interrupts at a rate greater than the LPF setting.

Table 40. Accelerometer OUTCFG Resolution and Range Select Register Settings

10.12 Accelerometer X-Axis Offset Registers

This register contains a signed 2's complement 14-bit value applied as an offset adjustment to the output of the sensor values, prior to being sent to the OUT_EX registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x21	XOFFL	X-Offset LSB Register	XOFF [7]	XOFF [6]	XOFF [5]	XOFF [4]	XOFF [3]	XOFF [2]	XOFF [1]	XOFF [0]	Per chip	W
0x22	XOFFH	X-Offset MSB Register	XGAIN [8]	Resv	XOFF [13]	XOFF [12]	XOFF [11]	XOFF [10]	XOFF [9]	XOFF [8]	Per chip	W

Table 41. Accelerometer x-Axis Offset Registers

10.13 Accelerometer Y-Axis Offset Registers

This register contains a signed 2's complement 14-bit value applied as an offset adjustment to the output of the sensor values, prior to being sent to the OUT_EX registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x23	YOFFL	Y-Offset LSB Register	YOFF [7]	YOFF [6]	YOFF [5]	YOFF [4]	YOFF [3]	YOFF [2]	YOFF [1]	YOFF [0]	Per chip	W
0x24	YOFFH	Y-Offset MSB Register	YGAIN [8]	Resv	YOFF [13]	YOFF [12]	YOFF [11]	YOFF [10]	YOFF [9]	YOFF [8]	Per chip	W

Table 42. Accelerometer Y-Axis Offset Registers

10.14 Accelerometer Z-Axis Offset Registers

This register contains a signed 2's complement 14-bit value applied as an offset adjustment to the output of the sensor values, prior to being sent to the OUT_EX registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x25	ZOFFL	Z-Offset LSB Register	ZOFF [7]	ZOFF [6]	ZOFF [5]	ZOFF [4]	ZOFF [3]	ZOFF [2]	ZOFF [1]	ZOFF [0]	Per chip	W
0x26	ZOFFH	Z-Offset MSB Register	ZGAIN [8]	Resv	ZOFF [13]	ZOFF [12]	ZOFF [11]	ZOFF [10]	ZOFF [9]	ZOFF [8]	Per chip	W

Table 43. Accelerometer Z-Axis Offset Registers

10.15 Accelerometer X-Axis Gain Registers

The gain value is an unsigned 9-bit number.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x22	XOFFH	X-Offset MSB Register	XGAIN [8]	Resv	XOFF [13]	XOFF [12]	XOFF [11]	XOFF [10]	XOFF [9]	XOFF [8]	Per chip	W
0x27	XGAIN	X Gain Register	XGAIN [7]	XGAIN [6]	XGAIN [5]	XGAIN [4]	XGAIN [3]	XGAIN [2]	XGAIN [1]	XGAIN [0]	Per chip	W

Table 44. Accelerometer X-Axis Gain Registers

10.16 Accelerometer Y-Axis Gain Registers

The gain value is an unsigned 9-bit number.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x24	YOFFH	Y-Offset MSB Register	YGAIN [8]	Resv	YOFF [13]	YOFF [12]	YOFF [11]	YOFF [10]	YOFF [9]	YOFF [8]	Per chip	W
0x28	YGAIN	Y Gain Register	YGAIN [7]	YGAIN [6]	YGAIN [5]	YGAIN [4]	YGAIN [3]	YGAIN [2]	YGAIN [1]	YGAIN [0]	Per chip	W

Table 45. Accelerometer Y-Axis Gain Registers

10.17 Accelerometer Z-Axis Gain Registers

The gain value is an unsigned 9-bit number.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x26	ZOFFH	Z-Offset MSB Register	ZGAIN [8]	Resv	ZOFF [13]	ZOFF [12]	ZOFF [11]	ZOFF [10]	ZOFF [9]	ZOFF [8]	Per chip	W
0x29	ZGAIN	Z Gain Register	ZGAIN [7]	ZGAIN [6]	ZGAIN [5]	ZGAIN [4]	ZGAIN [3]	ZGAIN [2]	ZGAIN [1]	ZGAIN [0]	Per chip	W

Table 46. Accelerometer Z-Axis Gain Registers

10.18 Accelerometer Shake_Th: Shake Threshold Register

SHAKE_TH has a baseline value of 1.3g plus a threshold, SHAKE_TH. The shake threshold can range from 0.925g to 1.672g. The value is an 8-bit signed 2's complement number. The resolution is approximately 2.9mg/bit. See also Section 7.15Shake Detection.

Shake Event =(mag(X) > 1.3g + SHAKE_TH) or
(mag(Y) > 1.3g + SHAKE_TH) or
(mag(Z) > 1.3g + SHAKE_TH)

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x2B	SHAKE_TH	Shake Threshold Register	Signed 2's complement value								0x00	W

SHAKE_TH[7:0]	Description (~2.9mg/LSB)
0x80	Shake threshold is 0.925g
0x00	Shake threshold is 1.3g
0x7F	Shake threshold is 1.672g

Table 47. Accelerometer SHAKE_TH Threshold Register Settings

10.19 Accelerometer UD_Z_TH: Up/Down Z Axis Threshold Register

The threshold value, UD_Z_TH[7:0] is an 8-bit signed 2's complement number that can range from 0.425g to 1.172g, for determination of the POLA orientation bits. The resolution is approximately 2.9mg/bit. See also Section 7.13Portrait/Landscape.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x2C	UD_Z_TH	Up/Down Z Axis Threshold Register	Signed 2's complement value								0x00	W

UD_Z_TH[7:0]	Description (~2.9mg/LSB)
0x80	Up/down Z axis threshold is 0.425g
0x00	Up/down Z axis threshold is 0.8g
0x7F	Up/down Z axis threshold is 1.172g

Table 48. Accelerometer Up/Down Z-axis Threshold Register Settings

10.20 Accelerometer UD_X_TH: Up/Down X Axis Threshold Register

This 8-bit unsigned value is an offset that is added to the magnitude of the X-axis accelerometer measurement. The range of the offset is 0g to 0.747g; the resolution is approximately 2.9mg/bit. See also Section 7.13Portrait/Landscape.

Increasing this value in conjunction with the Accelerometer RL_Y_TH: Right/Left Y Axis Threshold Register widens the deadband in portrait /landscape detection.

For most applications, the same value should be written to both registers.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x2D	UD_X_TH	Up/Down X Axis Threshold Register	Unsigned value								0x00	W

UD_X_TH[7:0]	Description (~2.9mg/LSB)
0x00	Up/down X threshold offset is 0g
0xFF	Up/down X threshold offset is +0.747g

Table 49. Accelerometer Up/Down X-axis Threshold Register Settings

10.21 Accelerometer RL_Z_TH: Right/Left Z Axis Threshold Register

The threshold value, RL_Z_TH[7:0] is an 8-bit signed 2's complement number that can range from 0.425g to 1.172g, for determination of the POLA orientation bits. The resolution is approximately 2.9mg/bit. See also Section 7.13Portrait/Landscape.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x2E	RL_Z_TH	Right/Left Z Axis Threshold Register	Signed 2's complement value								0x00	W

RL_Z_TH[7:0]	Description (~2.9mg/LSB)
0x80	Right/left Z axis threshold is 0.425g
0x00	Right/left Z axis threshold is 0.8g
0x7F	Right/left Z axis threshold is 1.172g

Table 50. Accelerometer Right/Left Z-axis Threshold Register Settings

10.22 Accelerometer RL_Y_TH: Right/Left Y Axis Threshold Register

This 8-bit unsigned value is an offset this is added to the magnitude of the Y-axis accelerometer measurement. The range of the offset is 0g to 0.747g; the resolution is approximately 2.9mg/bit. See also Section 7.13Portrait/Landscape.

Increasing this value in conjunction with the Accelerometer UD_X_TH: Up/Down X Axis Threshold Register widens the dead-band in portrait /landscape detection.

For most applications, the same value should be written to both registers.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x2F	RL_Y_TH	Right/Left Y Axis Threshold Register	Unsigned value								0x00	W

RL_Y_TH[7:0]	Description (~2.9mg/LSB)
0x00	Right/left Y-axis threshold offset is 0g
0xFF	Right/left Y-axis threshold offset is +0.747g

Table 51. Accelerometer Right/Left Y-axis Threshold Register Settings

10.23 Accelerometer FB_Z_TH: Front/Back Z Axis Threshold Register

The threshold value, FB_Z_TH[7:0] is an 8-bit unsigned number that adds up to + 0.373g to the baseline detection level of 0.174g, in increments of approximately 1.46mg/LSB. Increasing the threshold value increases the hysteresis of the front/back detection level. See also Section7.14Front/Back Events.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x30	FB_Z_TH	Front/Back Z Axis Threshold Register	Unsigned value								0x00	W

FB_Z_TH[7:0]	Description (~1.46mg/LSB)
0x00	Front/back Z threshold is 0.174g
0xFF	Front/back Z threshold is 0.547g

Table 52.Accelerometer Front/Back Z-axis Threshold Register Settings

10.24 Accelerometer DROP_TH: Drop Threshold Register

The threshold value, DROP_TH[7:0] is an 8-bit signed 2's complement number that adjusts the drop-detection baseline detection level of 0.5g. See also Section 7.16Drop Detection.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x31	DROP_TH	Drop Threshold Register	Signed 2's complement value								0x00	W

DROP_TH[7:0]	Description (~2.9mg/LSB)
0x80	Drop threshold is 0.125g
0x00	Drop threshold is 0.5g
0x7F	Drop threshold is 0.872g

Table 53.Accelerometer Drop Threshold Register Settings

10.25 Accelerometer TAP_TH: Tap Threshold Register

The threshold value, TAP_TH[7:0] is an 8-bit unsigned number that species the threshold detection level for all tap events. This value is not an offset, but a magnitude which determines the minimum level for a valid tap event. The detector is implemented as a 2nd-order high pass filter. As such, the units are the 2nd derivative of acceleration, also known as 'snap'. The full range is 0 to 12 snap. The resolution is ~47 milliSnap/bit. See also Section 7.17Accelerometer Tap Detection.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x32	TAP_TH	Tap Threshold Register	Unsigned value								0x00	W

TAP_TH[7:0]	Description (~47 mSnap/LSB)
0x00	Tap threshold is 0 snap
0x80	Tap threshold is 6 snap
0xFF	Tap threshold is 12 snap

Table 54.Accelerometer TAP_TH Tap Threshold Register Settings

10.26 Accelerometer PCODE: Product Code

This register returns a value specific to the part number of this mCube device, noted below.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x3B	PCODE	Product Code	1	0	0	1	0	0	0	0	0x90	R

Table 55. Accelerometer Product Code

11 REVISION HISTORY

Date	Revision	Description
2014-04	APS-048-0022v1.1	First release.
2014-05	APS-048-0022v1.2	Updated iGyro™ interface and specs
2014-10	APS-048-0022v1.3	Added I2C resistors explicitly to Typical Application Circuit. Updated pin descriptions to show recommended connections when not used. Updated noise specification. Added order info.

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