

## Surface Mount Resettable PTCs

### SMD2018 Series

#### Description

The SMD2018 Series PTC provides surface mount over-current protection for applications where space is at a premium and reset table protection is desired.

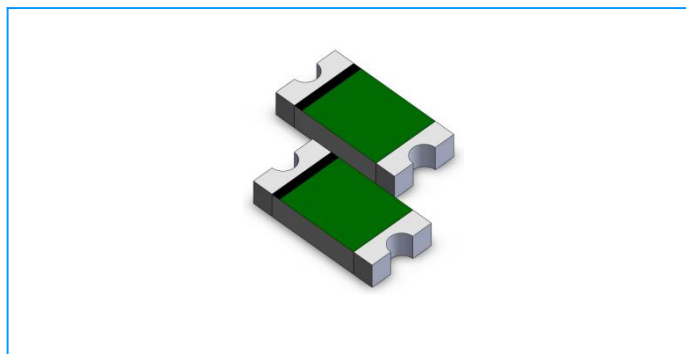
#### Features

- ◆ RoHS compliant, Lead-Free and Halogen-Free
- ◆ Fast time-to-trip
- ◆ Compact design saves board space
- ◆ Agency recognition: UL
- ◆ Low-profile

#### Applicable

Almost anywhere there is a low voltage power supply, up to 30V and a load to be protected, including:

- ◆ Computer mother board, Modem, USB hub
- ◆ PDAs & Charger, Analog & digital line card
- ◆ Digital cameras, Disk drivers, CD-ROMs
- ◆ Power ports
- ◆ General electronics



#### Electrical Parameters

Part Number	I <sub>hold</sub> (A)	I <sub>trip</sub> (A)	V <sub>max</sub> (Vdc)	I <sub>max</sub> (A)	P <sub>dtyp.</sub> (W)	Maximum Time To Trip		Resistance	
						Current (A)	Time (Sec.)	R <sub>min</sub> (Ω)	R <sub>max</sub> (Ω)
SMD2018-030	0.30	0.60	60	100	0.90	1.50	3.00	0.500	2.300
SMD2018-050	0.55	1.20	60	100	1.00	2.50	3.00	0.200	1.000
SMD2018-100	1.10	2.20	15	100	1.10	8.00	0.40	0.060	0.360
SMD2018-150	1.50	3.00	15	100	1.10	8.00	0.80	0.050	0.170
SMD2018-200	2.00	4.00	10	100	1.10	8.00	2.40	0.030	0.100

I<sub>hold</sub> = Hold current: maximum current device will pass without tripping in 25°C still air.

I<sub>trip</sub> = Trip current: minimum current at which the device will trip in 25°C still air.

V<sub>max</sub> = Maximum voltage device can withstand without damage at rated current (I<sub>max</sub>)

I<sub>max</sub> = Maximum fault current device can withstand without damage at rated voltage (V<sub>max</sub>)

P<sub>dtyp.</sub> = Power dissipated from device when in the tripped state at 25°C still air.

R<sub>min</sub> = Minimum resistance of device in initial (un-soldered) state.

R<sub>max</sub> = Maximum resistance of device in initial (un-soldered) state.

R<sub>1max</sub> = Maximum resistance of device at 25°C measured one hour after tripping.

Caution: Operation beyond the specified rating may result in damage and possible arcing and flame.

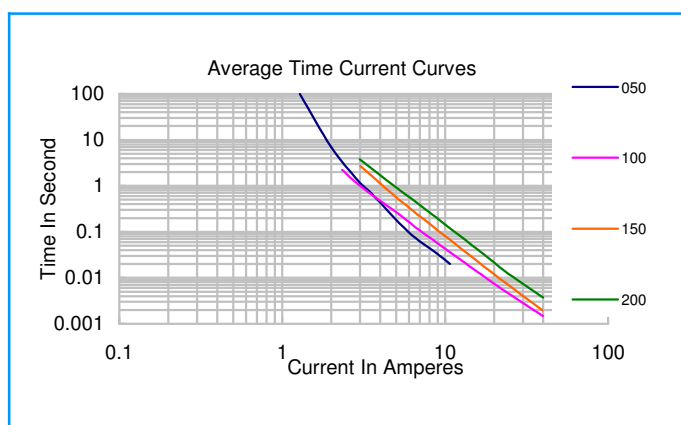
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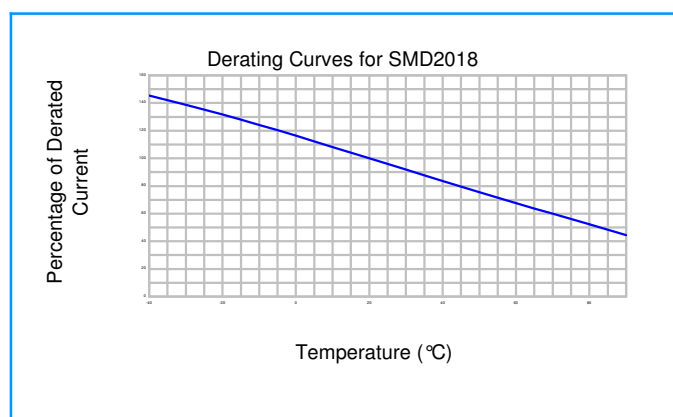
#### Temperature Derating Chart – $I_{hold}$ (A)

Part Number	Ambient Operation Temperature								
	-40°C	-20°C	0°C	25°C	40°C	50°C	60°C	70°C	85°C
	Hold Current (A)								
SMD2018-030	0.48	0.42	0.35	0.30	0.24	0.21	0.17	0.15	0.10
SMD2018-050	0.87	0.77	0.67	0.55	0.46	0.41	0.36	0.31	0.23
SMD2018-100	1.71	1.52	1.32	1.10	0.94	0.84	0.74	0.64	0.50
SMD2018-150	2.38	2.10	1.82	1.50	1.27	1.13	0.99	0.85	0.64
SMD2018-200	2.95	2.65	2.35	2.00	1.74	1.59	1.44	1.29	1.06

#### Average Time Current Curves



#### Temperature Derating Curve



#### Environmental Specifications

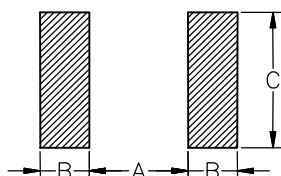
Test	Conditions	Resistance change
Passive aging	+85 °C, 1000 hrs.	±5% typical
Humidity aging	+85 °C, 85% R.H. , 168 hours	±5% typical
Thermal shock	+85 °C to -40 °C, 20 times	±33% typical
Resistance to solvent	MIL-STD-202, Method 215	No change
Vibration	MIL-STD-202, Method 201	No change
Ambient operating conditions :	- 40 °C to 85 °C	
Maximum surface temperature of the device in the tripped state is 125 °C		

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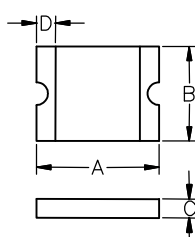
#### Pad Layouts Unit: mm

The dimension in the table below provide the recommended pad layout for each SMD1812 device



Device	A	B	C
	Nominal	Nominal	Nominal
2018Series	3.4	1.5	4.6

#### Dimensions Unit: mm



Part Number	A		B		C		D	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
SMD2018-030	4.72	5.44	4.22	4.93	0.60	1.10	0.30	0.95
SMD2018-050	4.37	4.73	3.07	3.41	0.50	1.00	0.30	0.95
SMD2018-100	4.37	4.73	3.07	3.41	0.50	1.00	0.30	0.95
SMD2018-150	4.37	4.73	3.07	3.41	0.50	1.00	0.30	0.95
SMD2018-200	4.37	4.73	3.07	3.41	0.40	0.90	0.30	0.95

#### Warning



- Use PPTC beyond the maximum ratings or improper use may result in device damage and possible electrical arcing and flame.
- PPTC are intended for protection against occasional over current or over temperature fault conditions and should not be used when repeated fault conditions or prolonged trip events are anticipated.
- Device performance can be impacted negatively if devices are handled in a manner inconsistent with recommended electronic, thermal, and mechanical procedures for electronic components.
- Use PPTC with a large inductance in circuit will generate a circuit voltage ( $L di/dt$ ) above the rated voltage of the PPTC.
- Avoid impact PPTC device its thermal expansion like placed under pressure or installed in limited space.
- Contamination of the PPTC material with certain silicon based oils or some aggressive solvents can adversely impact the performance of the devices. PPTC SMD can be cleaned by standard methods.
- Requests that customers comply with our recommended solder pad layouts and recommended reflow profile. Improper board layouts or reflow profile could negatively impact solderability performance of our devices.