



NGTB20N60L2TF1G

N-Channel IGBT 600V, 20A, $V_{CE(sat)}$;1.45V TO-3PF-3L with Low V_F Switching Diode

ON Semiconductor®

<http://onsemi.com>

Features

- IGBT $V_{CE(sat)}$ =1.45V typ. (I_C =20A, V_{GE} =15V)
- IGBT t_f =67ns typ.
- Diode V_F =1.5V typ. (I_F =20A)
- Diode t_{rr} =70ns typ.
- Adaption of full isolation type package
- Enhancement type
- Maximum junction temperature T_j =175°C

Applications

- Power factor correction of white goods appliance
- General purpose inverter

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, Unless otherwise specified

Parameter	Symbol	Conditions	Ratings	Unit	
Collector to Emitter Voltage	V_{CES}		600	V	
Gate to Emitter Voltage	V_{GES}		± 20	V	
Collector Current (DC)	I_C^{*1}	Limited by T_{jmax}	@ $T_c=25^\circ\text{C} *2$	40	A
			@ $T_c=100^\circ\text{C} *2$	20	A
Collector Current (Pulse)	I_{CP}	Pulse width Limited by T_{jmax}	80	A	
Diode Average Output Current	I_O		20	A	
Allowable Power Dissipation	P_D	$T_c=25^\circ\text{C}$ (Our ideal heat dissipation condition) *2	64	W	

Note : *1 Collector Current is calculated from the following formula.

Continued on next page.

$$I_C(T_c) = \frac{T_{jmax} - T_c}{R_{th(j-c)} \times V_{CE(sat)}(T_{jmax}, I_C(T_c))}$$

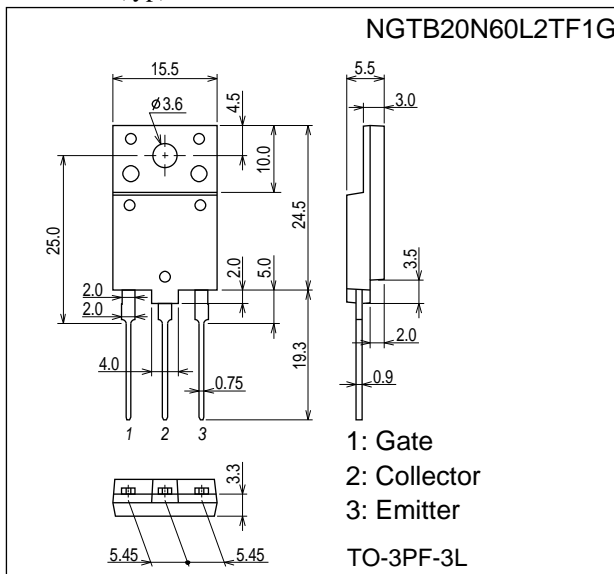
*2 Our condition is radiation from backside.

The method is applying silicone grease to the backside of the device and attaching the device to water-cooled radiator made of aluminium.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

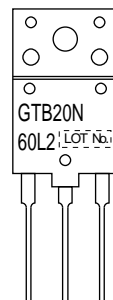
unit : mm (typ) 7538-001



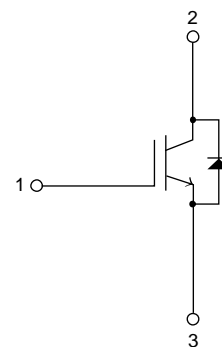
Ordering & Package Information

Device	Package	Shipping	note
NGTB20N60L2TF1G	TO-3PF-3L SC-94	30 pcs. / tube	Pb-Free

Marking



Electrical Connection



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Continued from preceding page.

Parameter	Symbol	Conditions	Ratings	Unit
Junction Temperature	T _j		175	°C
Storage Temperature	T _{stg}		- 55 to +175	°C

Electrical Characteristics at T_a = 25°C, Unless otherwise specified

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector to Emitter Breakdown Voltage	V _{(BR)CES}	I _C =500μA, V _{GE} =0V	600			V
Collector to Emitter Cut off Current	I _{CES}	V _{CE} =600V, V _{GE} =0V T _c =25°C T _c =150°C			10	μA
					1	mA
Gate to Emitter Leakage Current	I _{GES}	V _{GE} =±20V, V _{CE} =0V			±100	nA
Gate to Emitter Threshold Voltage	V _{GE(th)}	V _{CE} =20V, I _C =250μA	4.5		6.5	V
Collector to Emitter Saturation Voltage	V _{CE(sat)}	V _{GE} =15V, I _C =20A T _c =25°C T _c =150°C		1.45	1.65	V
				1.8		V
Diode Forward Voltage	V _F	I _F =20A		1.5		V
Input Capacitance	C _{ies}	V _{CE} =20V, f=1MHz		2000		pF
Output Capacitance	C _{oes}			60		pF
Reverse Transfer Capacitance	C _{res}			50		pF
Turn-ON Delay Time	t _{d(on)}			60		ns
Rise Time	t _r	V _{CC} =300V, I _C =20A R _G =30Ω, L=200μH V _{GE} =0V/15V, V _{clamp} =400V See Fig.1, Fig.2		37		ns
Turn-ON Time	t _{on}			400		ns
Turn-OFF Delay Time	t _{d(off)}			193		ns
Fall Time	t _f			67		ns
Turn-OFF Time	t _{off}			281		ns
Total Gate Charge	Q _g				84	
Gate to Emitter Charge	Q _{ge}	V _{CE} =300V, V _{GE} =15V, I _C =20A		16		nC
Gate to Collector "Miller" Charge	Q _{gc}			37		nC
Diode Reverse Recovery Time	t _{rr}		I _F =10A, di/dt=100A/μs, V _{CC} =50V See Fig.3		70	

Thermal Characteristics at T_a = 25°C, Unless otherwise specified

Parameter	Symbol	Conditions	Ratings	Unit
Thermal Resistance IGBT (junction- case)	R _{th(j-c)} (IGBT)	T _c =25°C (our ideal heat dissipation condition)*2	2.33	°C /W
Thermal Resistance Diode (junction- case)	R _{th(j-c)} (Diode)	T _c =25°C (our ideal heat dissipation condition)*2	2.36	°C /W
Thermal Resistance (junction- atmosphere)	R _{th(j-a)}		47.5	°C /W

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Fig.1 Switching Time Test Circuit

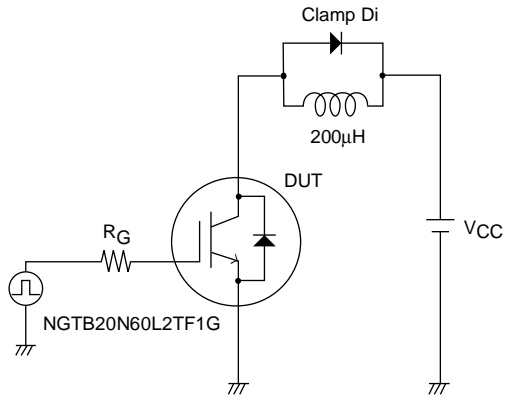


Fig.2 Timing Chart

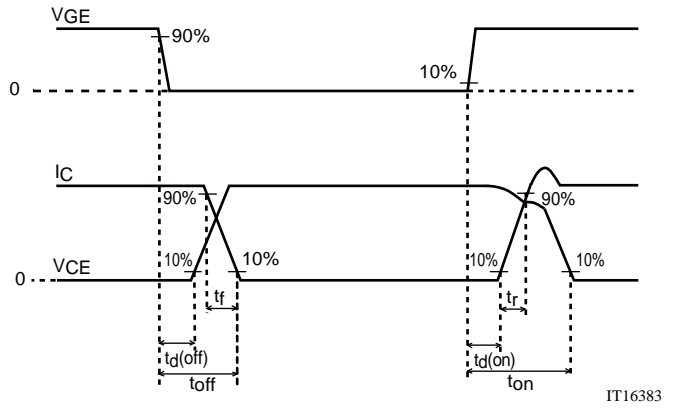
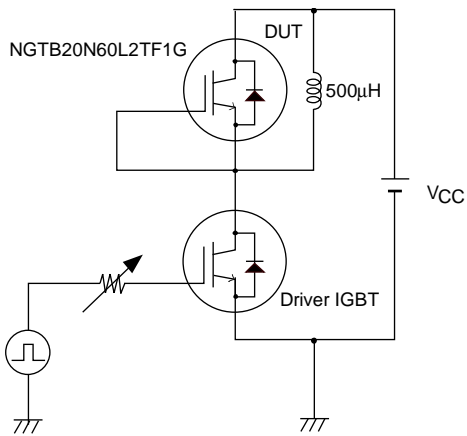
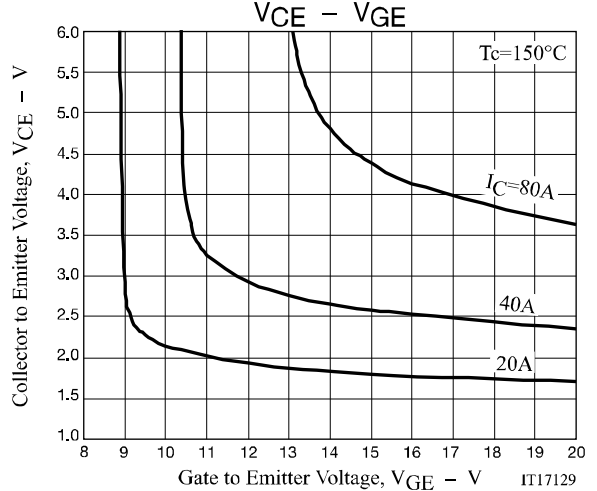
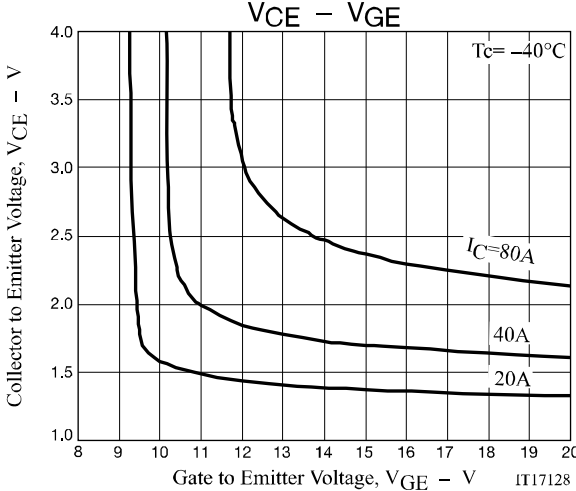
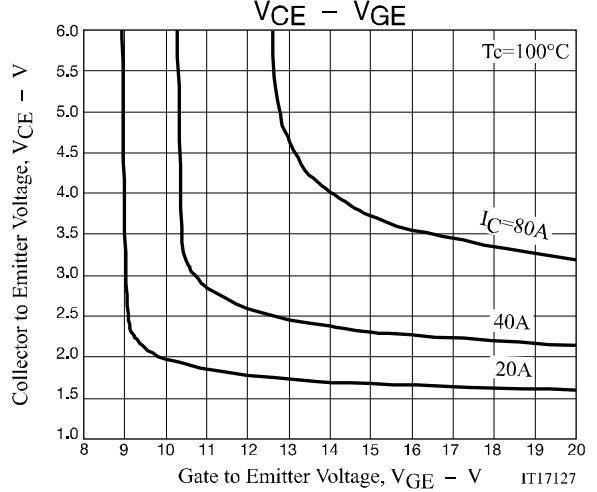
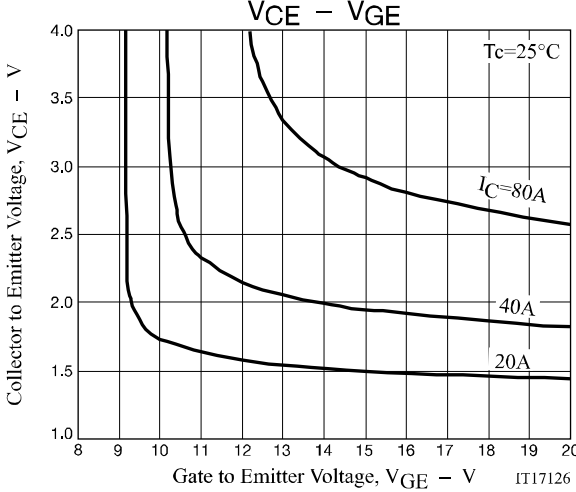
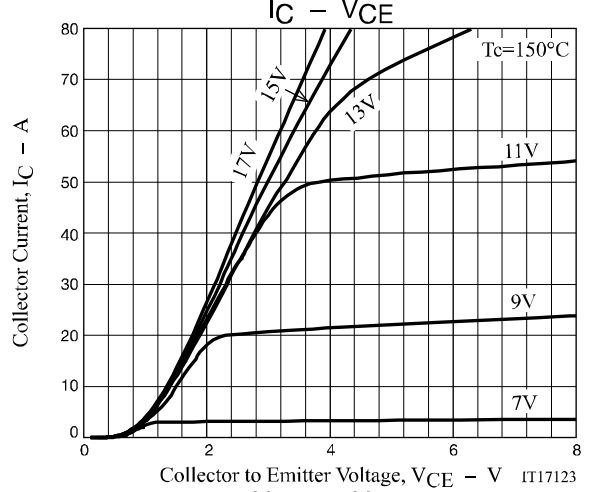
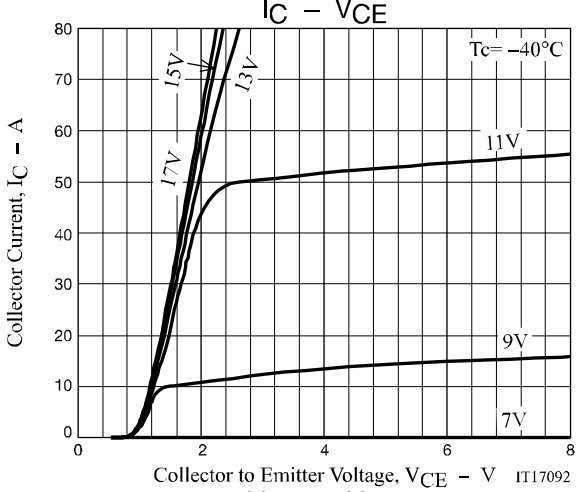
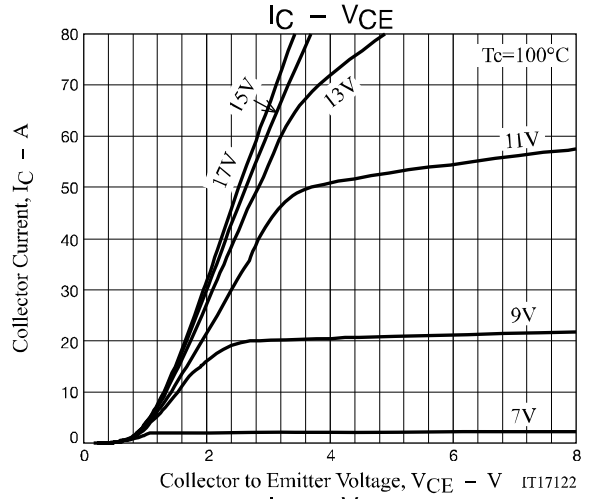
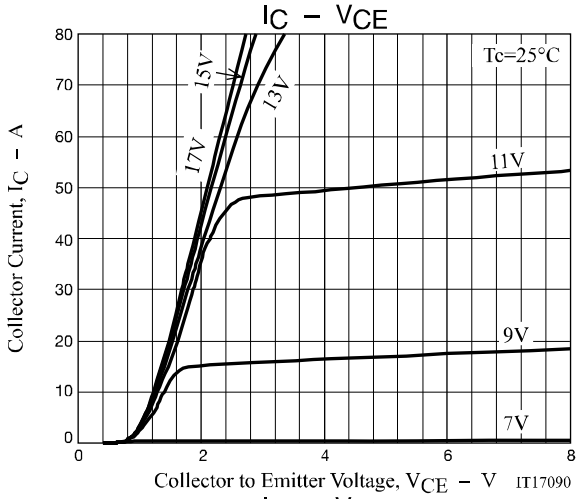


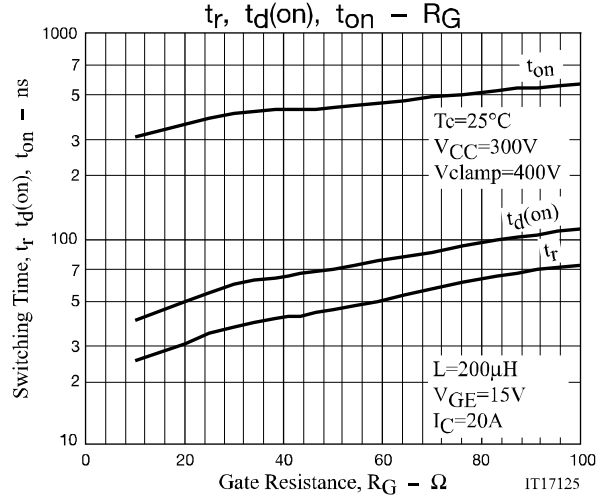
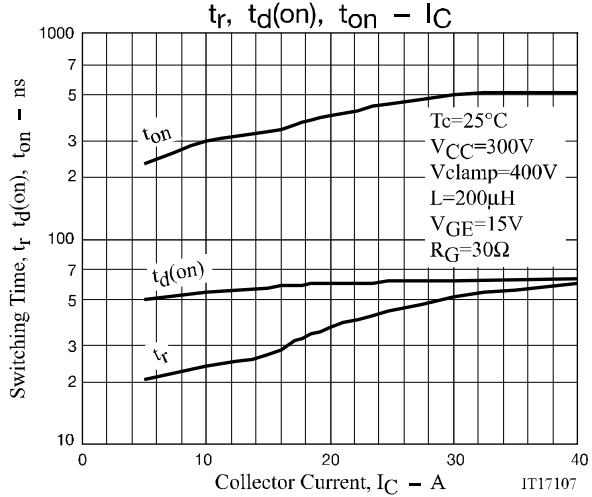
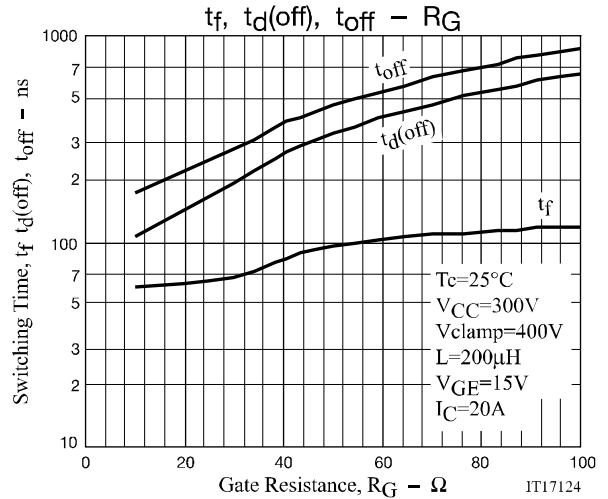
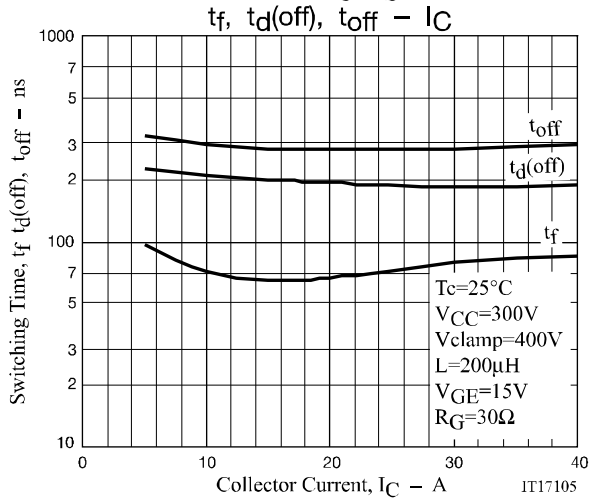
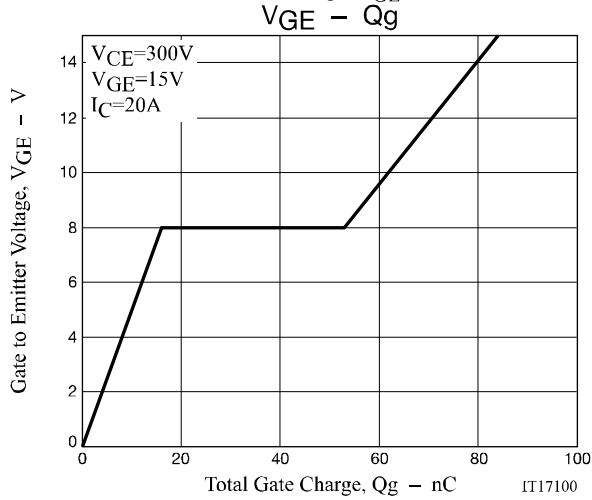
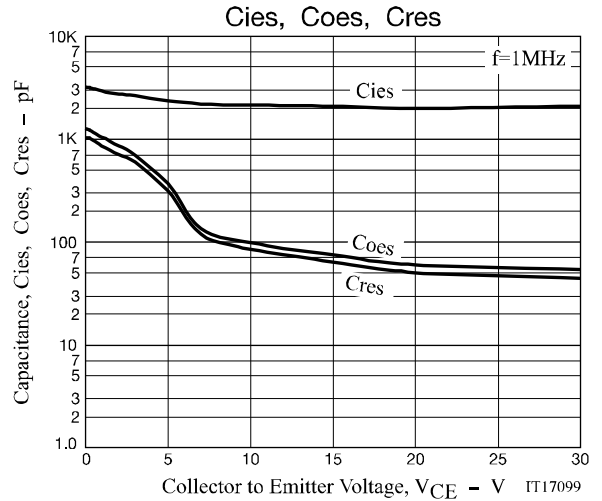
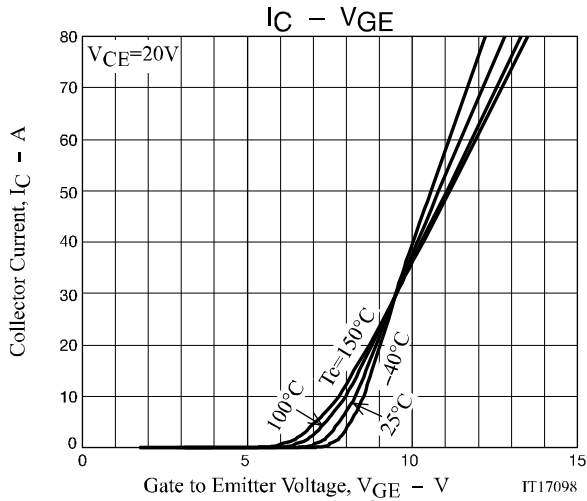
Fig.3 Reverse Recovery Time Test Circuit



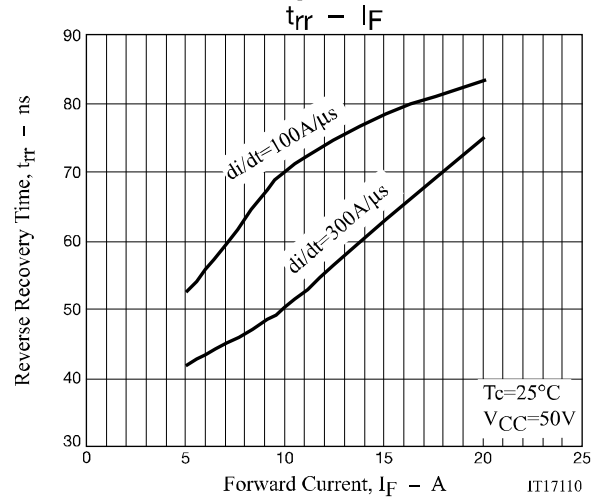
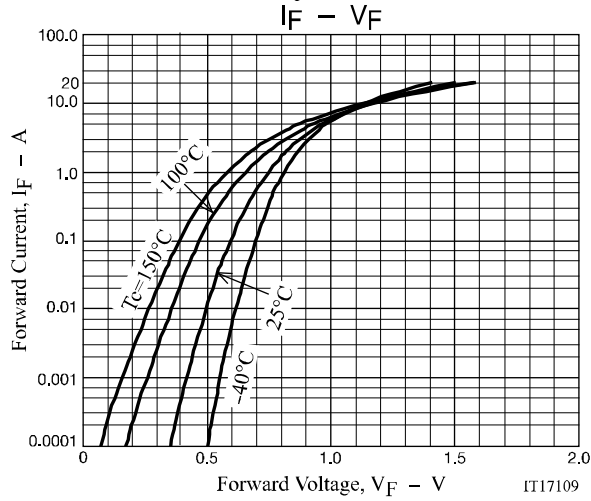
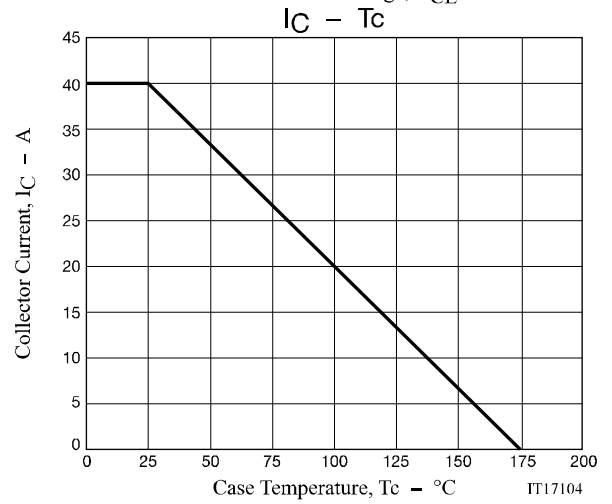
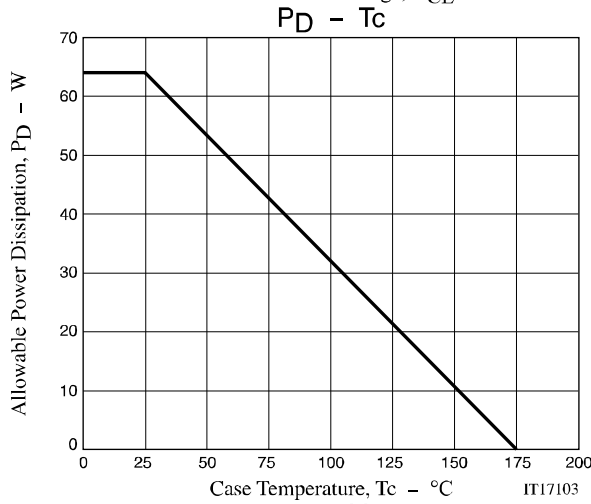
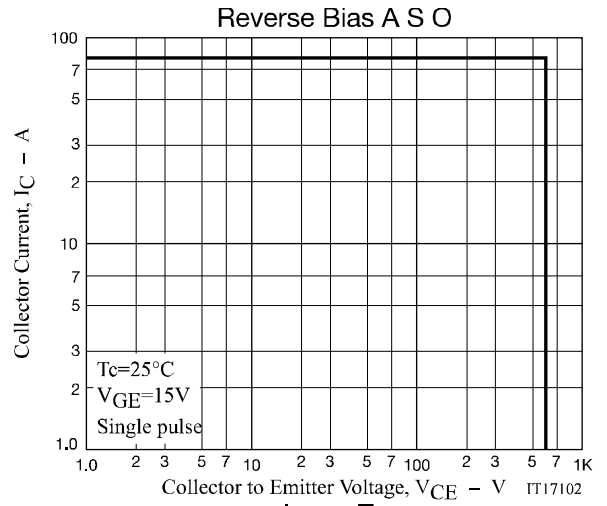
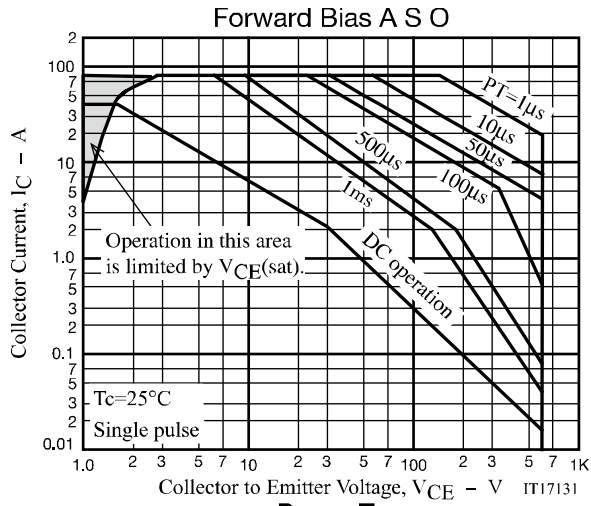
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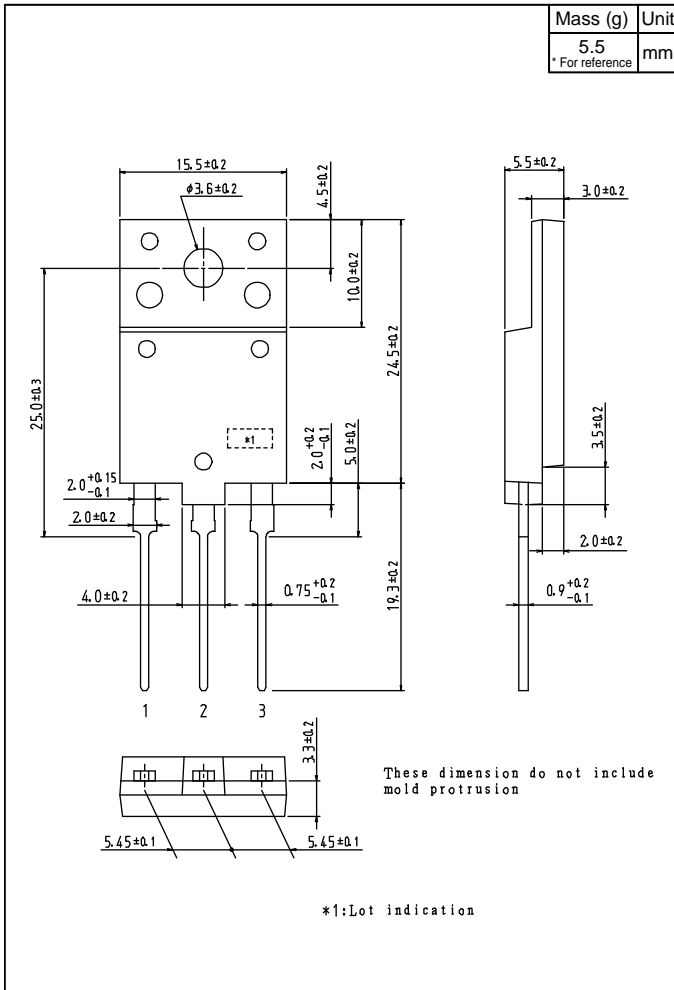
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Outline Drawing

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