MIC24045

I²C Programmable, 4.5V-19V Input, 5A Step-Down Converter

Features

- 4.5V to 19V Input Voltage Range
- 5A (maximum) Output Current
- I²C Programmable Output Voltage:
  - 0.64V to 5.25V in 5 mV, 10 mV, 30 mV and 50 mV steps
- High Efficiency (>95%)
- I²C Programmability of:
  - Soft-Start: 0.16, 0.38, 0.76 and 1.5V/ms ramp rates
  - Switching Frequency: 310 kHz, 400 kHz, 500 kHz, 570 kHz, 660 kHz, 780 kHz, 1 MHz, 1.2 MHz
  - Current Limits for 2A, 3A, 4A and 5A loads
  - Output Voltage Margining: -5%, +5%
  - Start-up delays: 0 ms to 10 ms
- ±1% Output Voltage Accuracy Over Temperature (0.64V to 1.95V)
- Supports Safe Start-Up with Pre-Biased Output
- Extensive Diagnostics through I²C Interface

Applications

- Servers, Data Storage, Routers and Base Stations
- FPGAs, DSP and Low-Voltage ASIC Power

General Description

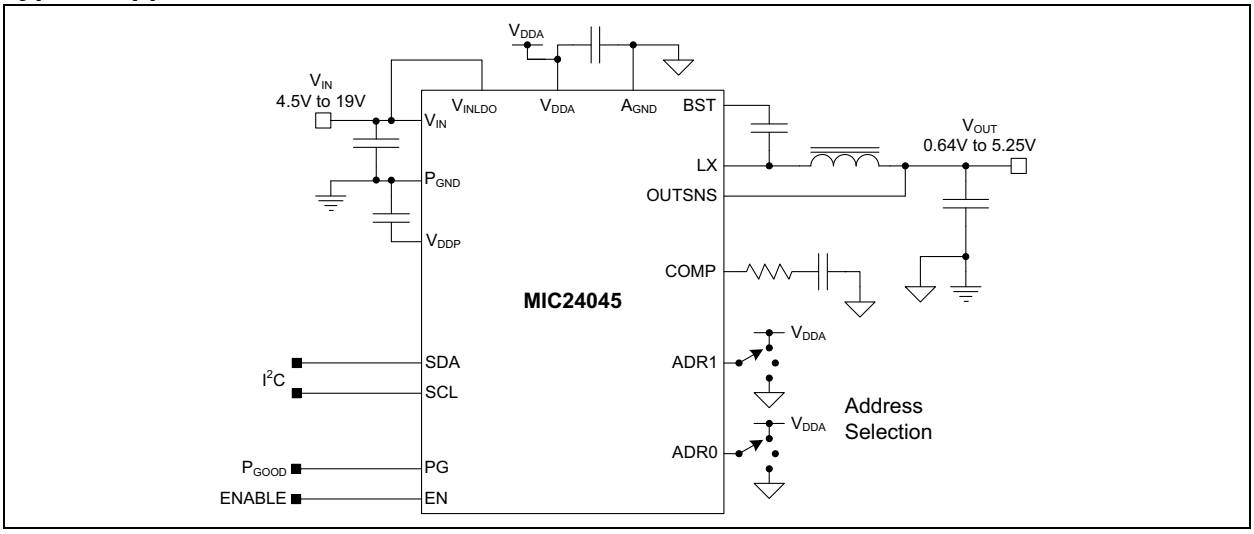
The MIC24045 is an I²C-programmable, high-efficiency, wide input range, 5A synchronous step-down regulator. The MIC24045 is perfectly suited for multiple voltage rail application environments, typically found in computing and telecommunication systems. In the MIC24045 various parameters can be programmed via I²C, such as output voltage, switching frequency, soft-start slope, margining, current limit values and start-up delays. The wide switching frequency adjustment range, valley current-mode control technique, high-performance error amplifier and external compensation allow for the best trade-offs between high efficiency and the smallest possible solution size.

The MIC24045 supports extensive diagnostics and status information through I²C.

The MIC24045 pinout is compatible with the MIC24046 pin-strapping programmable regulator pinout, such that I²C-based implementations can be easily converted into pin-programmable ones.

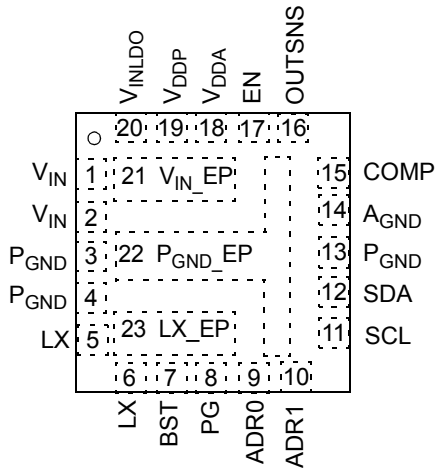
The MIC24045 is available in a thermally-efficient, space-saving 20-pin 3 mm x 3 mm FQFN package, with an operating junction temperature range from -40°C to +125°C.

Typical Application



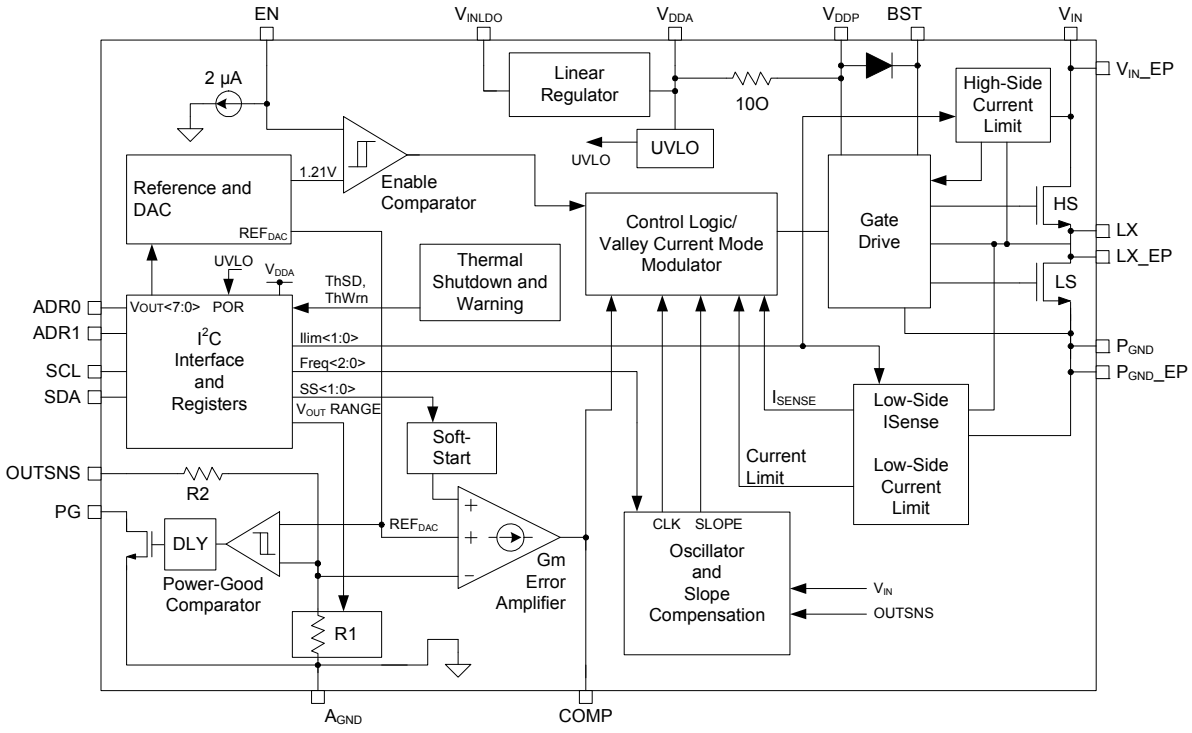
Package Types

MIC24045
3 x 3 FQFN*
(Top View)



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{IN}, V_{INLDO}, V_{LX} to A_{GND} ..... -0.3V to +20V
V_{DDP}, V_{DDA} to A_{GND} ..... -0.3V to +6V
V_{INLDO} to V_{DDA} ..... -0.3V to +20V
V_{DDP} to V_{DDA} ..... -0.3V to +0.3V
V_{ADRx}, V_{SDA}, V_{SCL} to A_{GND} ..... -0.3V to +6V
V_{BST} to V_{LX} ..... -0.3V to +6V
V_{BST} to A_{GND} ..... -0.3V to +26V
V_{EN} to A_{GND} ..... -0.3V to V_{DDA}+0.3V,+6V
V_{PG} to A_{GND} ..... -0.3V to +6V
V_{COMP}, V_{OUTSNS} to A_{GND} ..... -0.3V to V_{DDA}+0.3V,+6V
A_{GND} to P_{GND} ..... -0.3V to +0.3V
Junction Temperature ..... +150°C
Storage Temperature (T_S) ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... 260°C
ESD Rating[1]
HBM 2000V
CDM 2000V

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 k□ in series with 100 pF.

Operating Ratings[1]

Supply Voltage (V_{IN},V_{INLDO}) ..... 4.5V to 19V
Externally Applied Analog and Drivers Supply Voltage (V_{INLDO} = V_{DDA} = V_{DDP}) ..... 4.5V to 5.5V
Enable Voltage (V_{EN}) ..... 0V to V_{DDA}
Power-Good (PG) Pull-up Voltage (V_{PU_PG}) ..... 0V to 5.5V
Output Current 5A
Junction Temperature (T_J) ..... -40°C to +125°C

Note 1: The device is not ensured to function outside the operating range.

ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Specifications: unless otherwise specified, $V_{IN} = V_{INLDO} = 12V$; $C_{VDDA} = 2.2\ \mu F$, $C_{VDDP} = 2.2\ \mu F$, $T_A = +25°C$. **Boldface** values indicate -40°C d T_J d +125°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
V_{IN} Supply						
Input Range	V_{IN}	**4.5**	—	**19**	V	
Disable Current	I_{VINQ}	—	0.2	**2**	µA	EN = 0V
Disable Current	$I_{VINLDOQ}$	—	0.6	**1**	mA	EN = 0V
Operating Current	I_{VINOp}	—	0.3	0.5	mA	EN > 1.28V, ILIM<1:0> = 00, OUTSNS = 1.15 x $V_{OUT(NOM)}$, no switching, $T_A = T_J = +25°C$
Operating Current	$I_{VINLDOOp}$	—	4.5	**7**	mA	EN > 1.28V, OUTSNS = 1.15 x $V_{OUT(NOM)}$, no switching, $T_A = T_J = +25°C$
V_{DDA} 5V Supply						
Operating Voltage	V_{DDA}	**4.8**	5.1	**5.4**	V	I_{VDDA} = 0 mA to 10 mA
Dropout Operation		**3.6**	4.2	—	V	V_{INLDO} = 4.5V, I_{VDDA} = 10 mA
V_{DDA} Undervoltage Lockout						
V_{DDA} UVLO Rising	UVLO_R	**3.1**	3.5	**3.9**	V	V_{DDA} Rising, EN > 1.28V
V_{DDA} UVLO Falling	UVLO_F	**2.87**	3.2	**3.45**	V	V_{DDA} Falling, EN > 1.28V
V_{DDA} UVLO Hysteresis	UVLO_H	—	300	—	mV	
EN Control						
EN Rising Threshold	EN_R	**1.14**	1.21	**1.28**	V	Initiates power-stage operation
EN Falling Threshold	EN_F	—	1.07	—	V	Stops power-stage operation
EN Hysteresis	EN_H	—	135	—	mV	
EN Pull-Down Current	EN_I	1	2	3	µA	$T_A = T_J = +25°C$
Switching Frequency						
Programmable Frequency 0	f_{s0}	**270**	310	**350**	kHz	
Programmable Frequency 1	f_{s1}	**350**	400	**450**	kHz	
Programmable Frequency 2	f_{s2}	**450**	500	**550**	kHz	
Programmable Frequency 3	f_{s3}	**510**	570	**630**	kHz	
Programmable Frequency 4	f_{s4}	**590**	660	**740**	kHz	
Programmable Frequency 5	f_{s5}	**680**	780	**880**	kHz	
Programmable Frequency 6	f_{s6}	**850**	970	**1100**	kHz	
Programmable Frequency 7	f_{s7}	**1050**	1200	**1350**	kHz	
Overcurrent Protection						
HS Current Limit 0	I_{LIM_HS0}	**4.0**	4.7	**6.5**	A	
HS Current Limit 1	I_{LIM_HS1}	**5.4**	6.2	**7.6**	A	
HS Current Limit 2	I_{LIM_HS2}	**7.6**	8.6	**10.6**	A	
HS Current Limit 3	I_{LIM_HS3}	**8.2**	9.4	**12.0**	A	
High Side FET Current-Limit Leading Edge-Blanking Time	LEB	—	108	—	ns	
LS Current Limit 0	I_{LIM_LS0}	**2.0**	3.25	**5.0**	A	
LS Current Limit 1	I_{LIM_LS1}	**3.0**	4.3	**6.0**	A	
LS Current Limit 2	I_{LIM_LS2}	**4.0**	5.6	**7.5**	A	

Note 1: Specification for packaged product only.

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ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Specifications: unless otherwise specified, V_{IN} = V_{INLDO} = 12V; C_{VDDA} = 2.2 µF, C_{VDDP} = 2.2 µF, T_A = +25°C. **Boldface** values indicate -40°C ≤ T_J ≤ +125°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
LS Current Limit 3	I_{LIM_LS3}	**5.0**	6.2	**8.5**	A	
OC Events Count for Hiccup	IN_{HICC_DE}	—	15	—	Clock Cycles	Number of subsequent cycles in current limit before entering hiccup overload protection.
Hiccup Wait Time	t_{HICC_WAIT}	—	13.5V/ SS_SRx	—	ms	Duration of the high-Z state on LX before new soft-start. SS_SRx = SS_SR0, SS_SR1, SS_SR2, SS_SR3
Power Switches						
Low Side FET ON Resistance	R_{LS}	—	16	21	m□	V_{IN} = V_{INLDO} = V_{DDP} = V_{DDA} = 5V, V_{BST}-V_{LX} = 5V, T_A = T_J = +25°C
High Side FET ON Resistance	R_{HS}	—	38	50	m□	V_{IN} = V_{INLDO} = V_{DDP} = V_{DDA} = 5V, V_{BST}-V_{LX} = 5V, T_A = T_J = +25°C
Pulse-Width Modulation (PWM)						
Minimum LX ON Time	$T_{ON(MIN)}$	—	26	—	ns	T_A = T_J = +25°C
Minimum LX OFF time	$T_{OFF(MIN)}$	90	145	190	ns	V_{IN} = V_{INLDO} = V_{DDA} = 5V, V_{OUTSNS} = 3V, 400 kHz setting, V_{OUT} = 3.3V, T_A = T_J = +25°C
Minimum Duty Cycle	D_{MIN}	—	0	—	%	V_{OUTSNS} > 1.1 x $V_{OUT(NOM)}$
Gm Error Amplifier						
Error-Amplifier Transconductance	Gm_{EA}	—	1.4	—	mS	
Error-Amplifier DC Gain	A_{EA}	—	50000	—	V/V	
Error-Amplifier Source Current	I_{SR}	—	400	—	µA	
Error-Amplifier Sink Current	I_{SNK}	—	400	—	µA	
COMP Output Swing High	COMP_H	—	2.5	—	V	
COMP Output Swing Low	COMP_L	—	0.8	—	V	
COMP-to-Inductor Current Transconductance	Gm_{PS}	—	12.5	—	A/V	V_{OUT} = 1.2V, I_{OUT} = 4A
Output Voltage DC Accuracy						
Minimum Programmable Output Voltage	MinOut	—	0.64	—	V	
Maximum Programmable Output Voltage	MaxOut	—	5.25	—	V	
LSB for range 0.640V to 1.280V	LSB1	—	5	—	mV	
LSB for range 1.290V to 1.950V	LSB2	—	10	—	mV	
LSB for range 1.980V to 3.42V	LSB3	—	30	—	mV	
LSB for range 4.75V to 5.25V	LSB4	—	50	—	mV	
Output Voltage Accuracy for Ranges 1 and 2	OutErr12	**-1**	—	**1**	%	4.75V ≤ V_{IN} ≤ 19V, V_{OUT} = 0.64V to 1.95V T_A = T_J = -40°C to +125°C, I_{OUT} = 0A

Note 1: Specification for packaged product only.

ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Specifications: unless otherwise specified, $V_{IN} = V_{INLDO}$ = 12V; C_{VDDA} = 2.2 µF, C_{VDDP} = 2.2 µF, T_A = +25°C. **Boldface** values indicate -40°C ≤ T_J ≤ +125°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Output Voltage Accuracy for Range 3 and 4	OutErr34	**-1.5**	—	**1.5**	%	4.75V ≤ V_{IN} ≤ 19V for V_{OUT} = 1.98V to 3.42V, 6V ≤ V_{IN} ≤ 19V for V_{OUT} = 4.75V to 5.25V, $T_A = T_J$ = -40°C to +125°C, I_{OUT} = 0A
Load Regulation	LoadReg	—	0.2	—	%	I_{OUT} = 0A to 5A, V_{OUT} = 3.3V
Line Regulation	LineReg	—	0.1	—	%	6V < V_{IN} < 19V, I_{OUT} = 2A
Internal Soft-Start						
Reference Soft-Start Slew Rate 0	SS_SR0	—	0.16	—	V/ms	V_{OUT} = 0.64 to 1.28V
Reference Soft-Start Slew Rate 1	SS_SR1	—	0.38		V/ms	V_{OUT} = 0.64 to 1.28V
Reference Soft-Start Slew Rate 2	SS_SR2	—	0.76		V/ms	V_{OUT} = 0.64 to 1.28V
Reference Soft-Start Slew Rate 3	SS_SR3	—	1.5		V/ms	V_{OUT} = 0.64 to 1.28V
Power Good (PG)						
PG Low Voltage	PG_V_{OL}	—	0.18	**0.4**	V	$I_{(PG)}$ = 4 mA
PG Leakage Current	PG_I_{LEAK}	**-1**	0.02	**1**	µA	V_{PG} = 5V
PG Rise Threshold	PG_R	**90**	92.5	**95**	%	V_{OUT} Rising
PG Fall Threshold	PG_F	**87.5**	90	**92.5**	%	V_{OUT} Falling
PG Rise Delay	PG_R_DLY	—	0.45	—	ms	V_{OUT} Rising
PG Fall Delay	PG_F_DLY	—	80	—	µs	V_{OUT} Falling
Thermal Shutdown						
Thermal Shutdown	T_{SHDN}	—	160	—	°C	
Thermal-Shutdown Hysteresis	T_{SHDN_HYST}	—	25	—	°C	
Thermal Warning Threshold	T_{ThWrn}	—	120	—	°C	
Efficiency						
Efficiency	η	—	82.3	—	%	V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 2A, f_S = 400 kHz, L = 1.2 µH, T_A = +25°C
I^2C Interface						
SDA, SCL V_{IH}	V_{IH}	2	—	—	V	V_{DDA} = 5V (levels are 3.3V compatible)
SDA, SCL V_{IL}	V_{IL}	—	—	1	V	V_{DDA} = 5V (levels are 3.3V compatible)
SDA, SCL Input High/Low Current	I_{IH}, I_{IL}	-1	—	1	µA	
SDA Output Low Voltage	V_{OL}	—	—	0.4	V	I_{SDA} = 3 mA

Note 1: Specification for packaged product only.

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TEMPERATURE SPECIFICATIONS

Electrical Specifications: unless otherwise specified, $V_{IN} = V_{INLDO} = 12V$; $C_{VDDA} = 2.2\ \mu F$, $C_{VDDP} = 2.2\ \mu F$, $T_A = +25°C$.
Boldface values indicate -40°C ≤ T_J ≤ +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature	T_J	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 20LD 3x3 FQFN	θ_{JA}	—	29	—	°C/W	

2.0 TYPICAL CHARACTERISTIC CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{IN} = 12V, f_S = 660 kHz, I_{LIM} = I_{LIM_LS3}, L = 2.2 µH, T_A = +25°C.

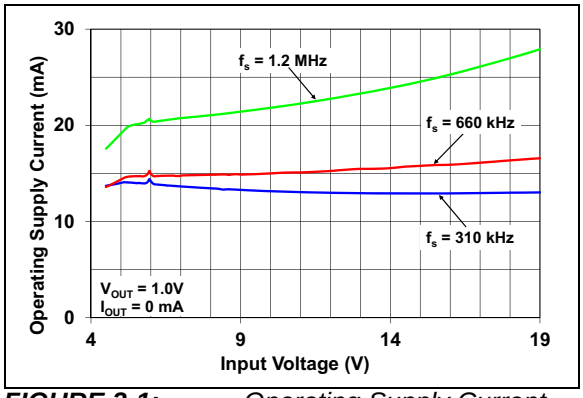

FIGURE 2-1: *Operating Supply Current vs. Input Voltage, Switching.*

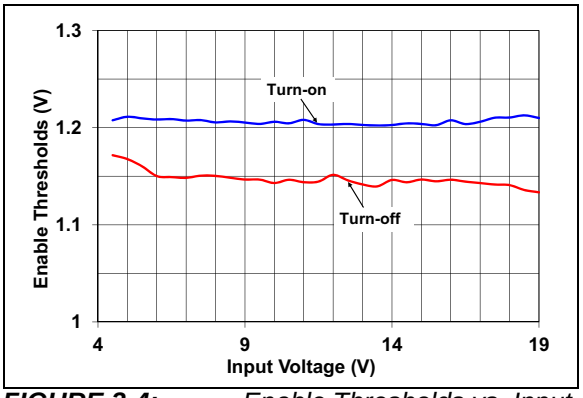

FIGURE 2-4: *Enable Thresholds vs. Input Voltage.*

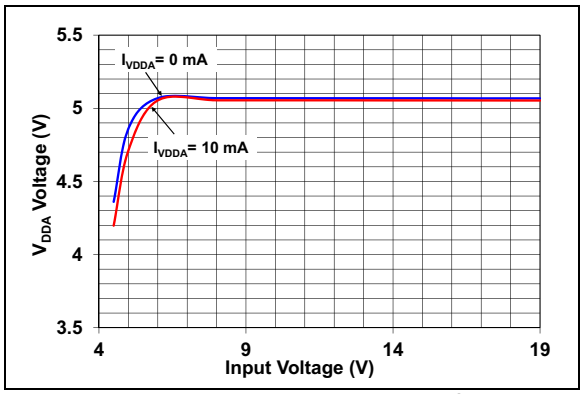

FIGURE 2-2: *V_{DDA} vs. Input Voltage.*

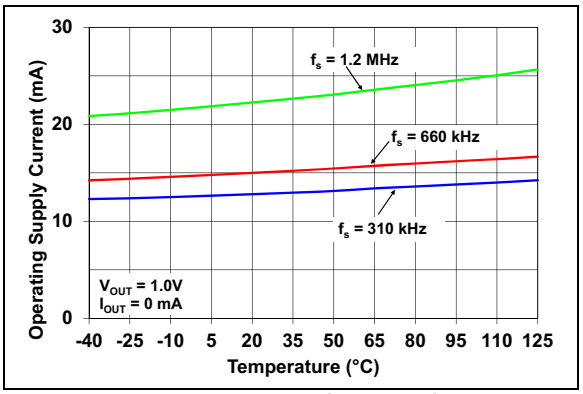

FIGURE 2-5: *Operating Supply Current vs. Temperature, Switching.*

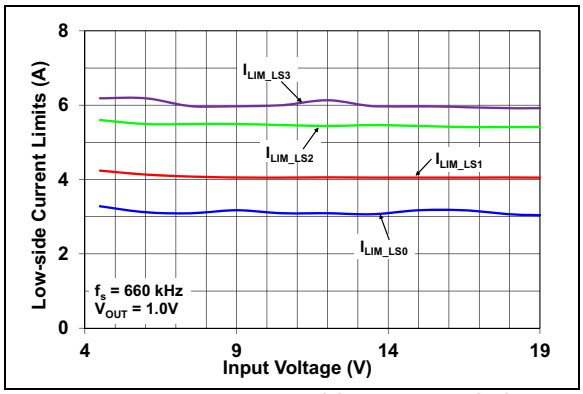

FIGURE 2-3: *Low-Side Current Limits vs. Input Voltage.*

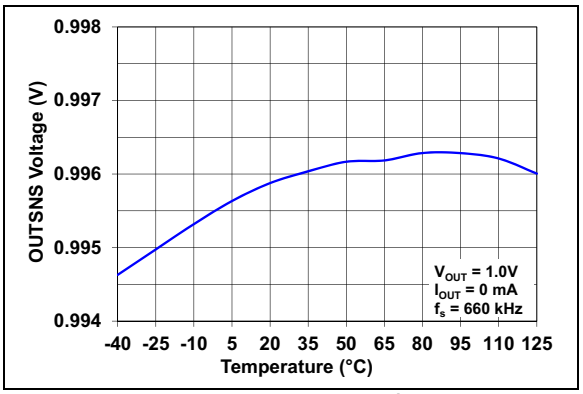

FIGURE 2-6: *OUTSNS Voltage vs. Temperature.*

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Note: Unless otherwise indicated, V_{IN} = 12V, f_S = 660 kHz, I_{LIM} = I_{LIM_LS3}, L = 2.2 µH, T_A = +25°C.

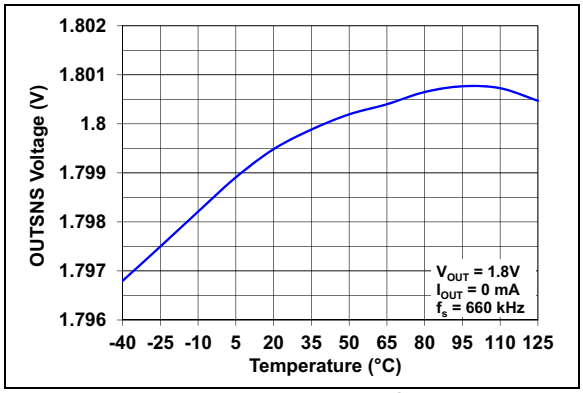

FIGURE 2-7: *OUTSNS Voltage vs. Temperature.*

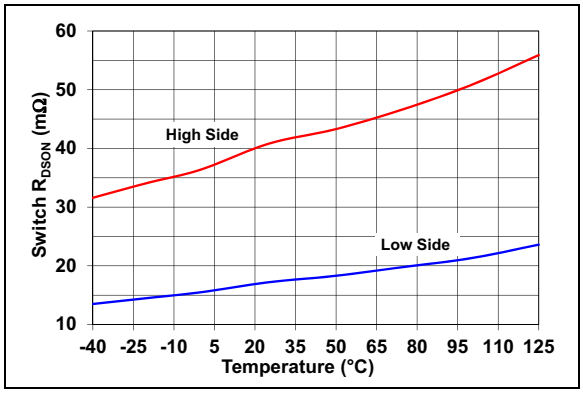

FIGURE 2-10: *$R_{DS(on)}$ vs. Temperature.*

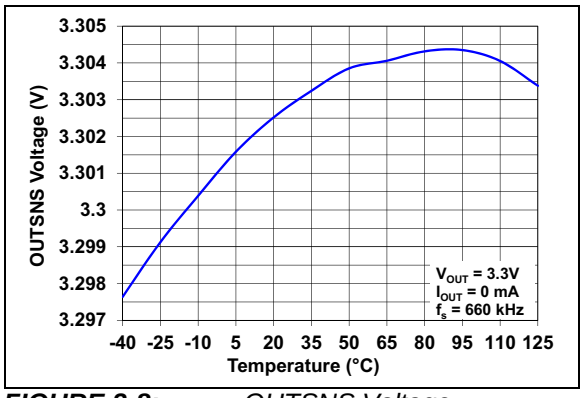

FIGURE 2-8: *OUTSNS Voltage vs.Temperature.*

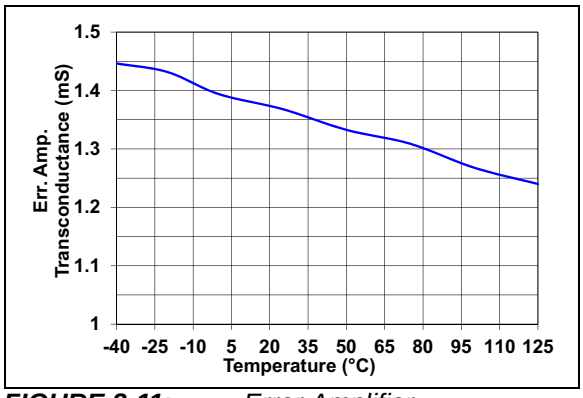

FIGURE 2-11: *Error Amplifier Transconductance vs. Temperature.*

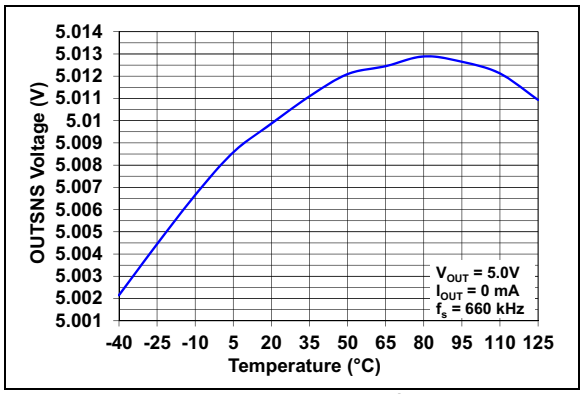

FIGURE 2-9: *OUTSNS Voltage vs.Temperature.*

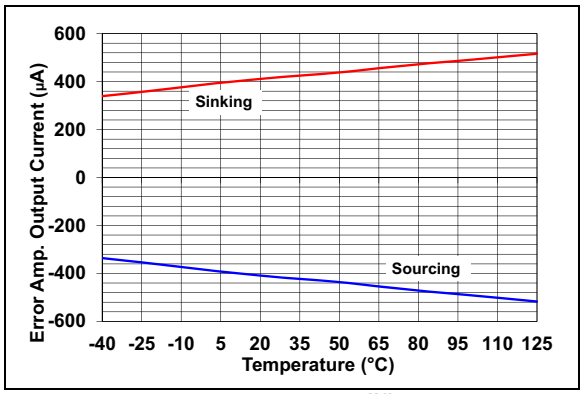

FIGURE 2-12: *Error Amplifier Output Current vs. Temperature.*

Note: Unless otherwise indicated, V_{IN} = 12V, f_S = 660 kHz, I_{LIM} = I_{LIM_LS3}, L = 2.2 µH, T_A = +25°C.

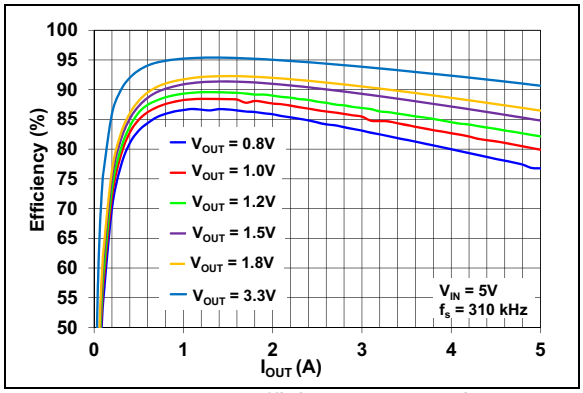

FIGURE 2-13: *Efficiency vs. Load Current.*

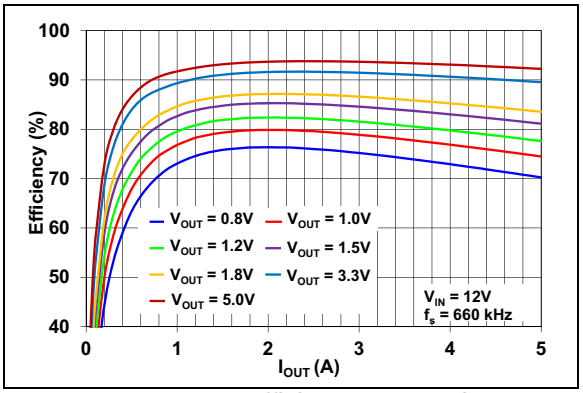

FIGURE 2-16: *Efficiency vs. Load Current.*

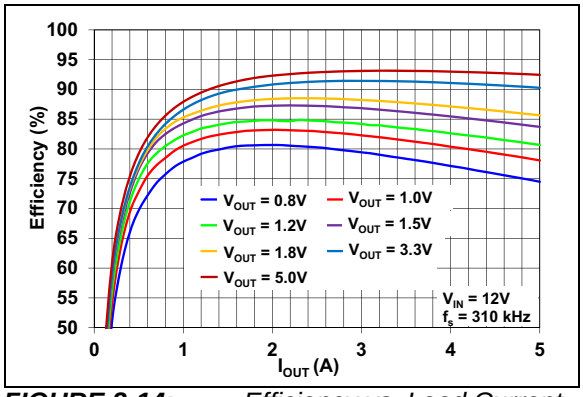

FIGURE 2-14: *Efficiency vs. Load Current.*

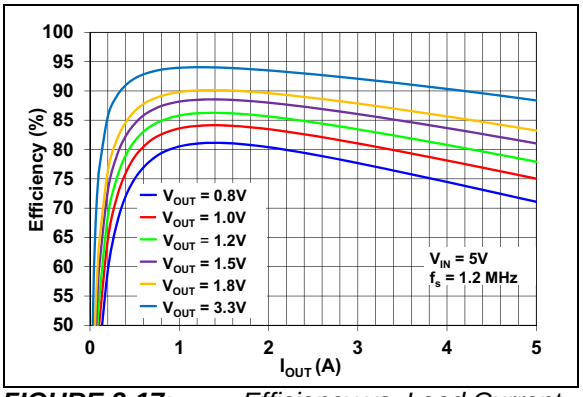

FIGURE 2-17: *Efficiency vs. Load Current.*

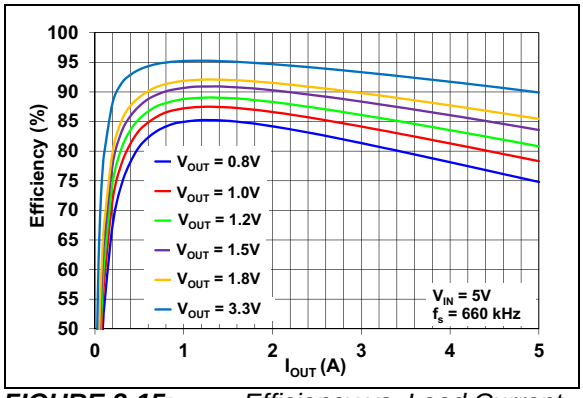

FIGURE 2-15: *Efficiency vs. Load Current.*

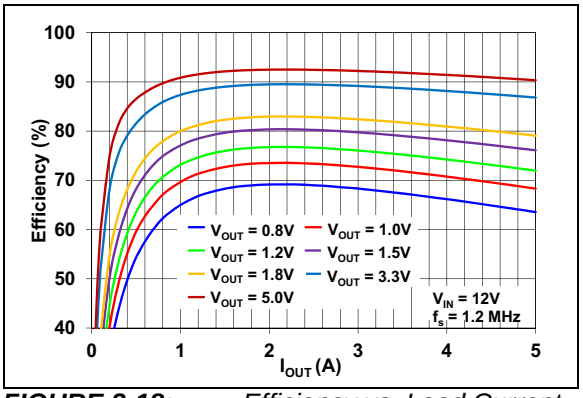

FIGURE 2-18: *Efficiency vs. Load Current.*

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Note: Unless otherwise indicated, V_{IN} = 12V, f_S = 660 kHz, I_{LIM} = I_{LIM_LS3}, L = 2.2 µH, T_A = +25°C.

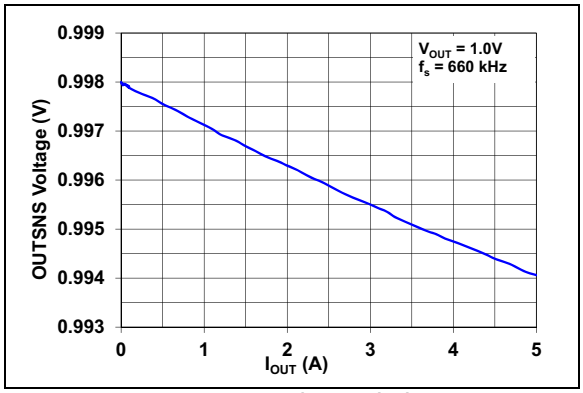

FIGURE 2-19: *Load Regulation: OUTSNS Voltage vs. I_{OUT}.*

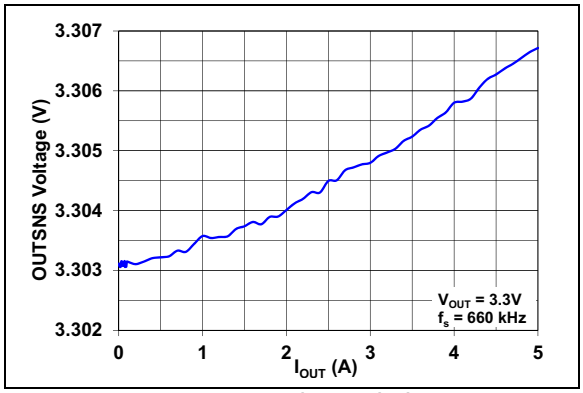

FIGURE 2-21: *Load Regulation: OUTSNS Voltage vs. I_{OUT}.*

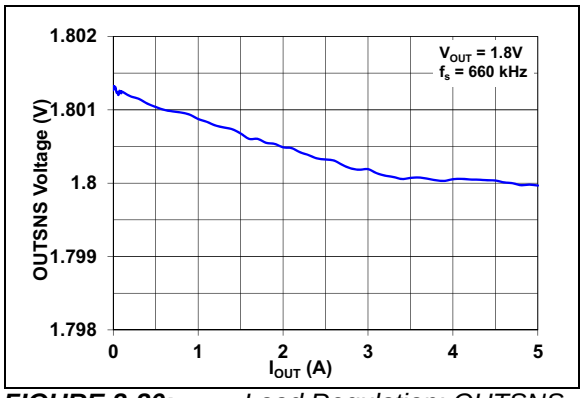

FIGURE 2-20: *Load Regulation: OUTSNS Voltage vs. I_{OUT}.*

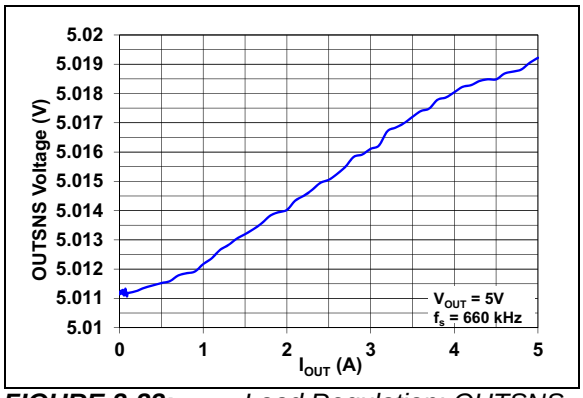

FIGURE 2-22: *Load Regulation: OUTSNS Voltage vs. I_{OUT}.*

Note: Unless otherwise indicated, V_{IN} = 12V, f_S = 660 kHz, I_{LIM} = I_{LIM_LS3}, L = 2.2 µH, T_A = +25°C.

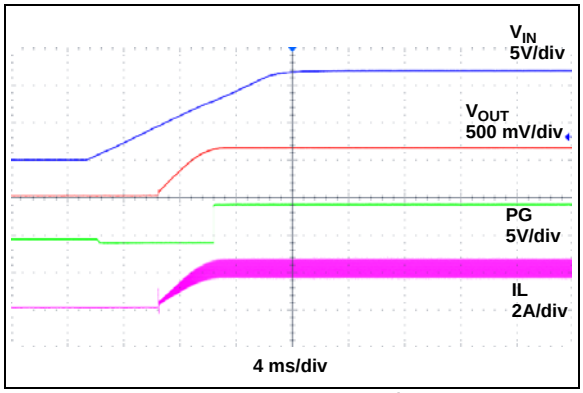

FIGURE 2-23: *V_{IN} Turn-on (EN = V_{DDA}, no I^2C programming, registers default values for 2Z version), R_{LOAD} = 0.3Ω.*

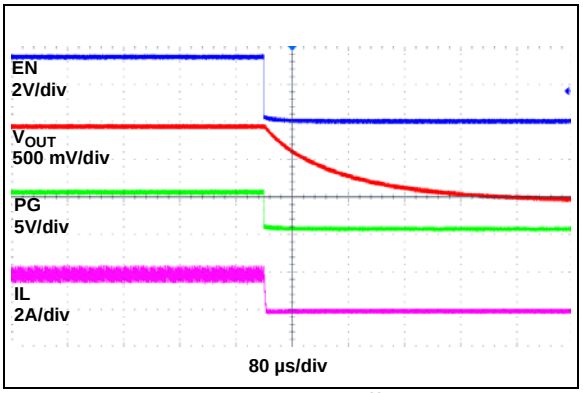

FIGURE 2-26: *EN Turn-off, R_{LOAD} = 0.3Ω.*

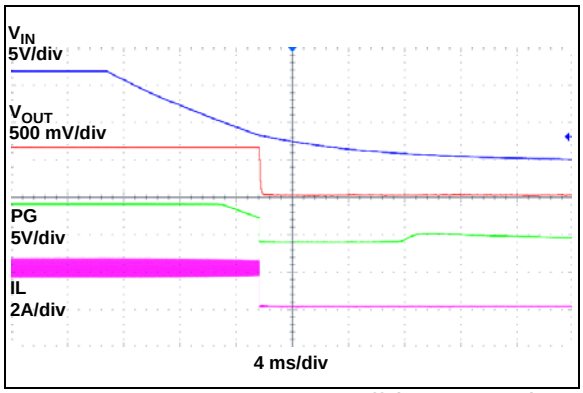

FIGURE 2-24: *V_{IN} Turn-off (EN = V_{DDA}), R_{LOAD} = 0.3Ω.*

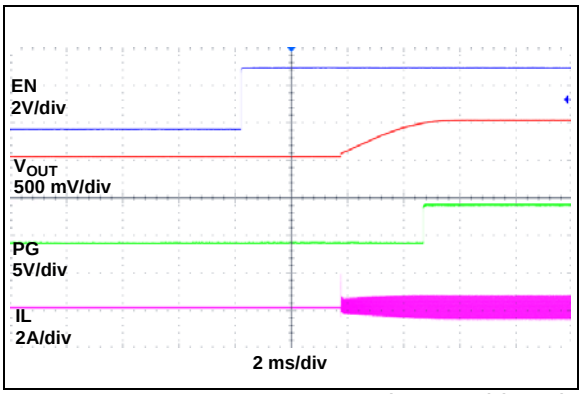

FIGURE 2-27: *EN Turn-on into pre-biased output ($V_{pre\text{-}bias}$ = 0.5V).*

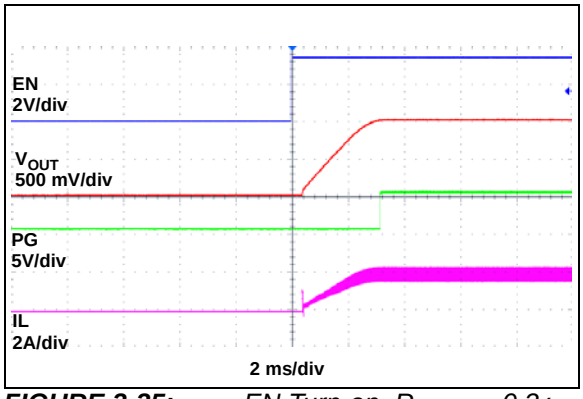

FIGURE 2-25: *EN Turn-on, R_{LOAD} = 0.3Ω.*

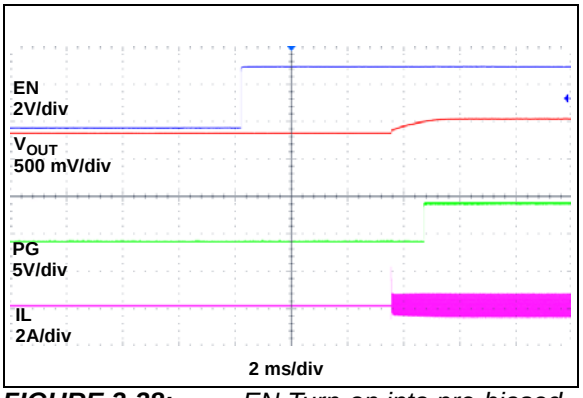

FIGURE 2-28: *EN Turn-on into pre-biased output ($V_{pre\text{-}bias}$ = 0.8V).*

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Note: Unless otherwise indicated, V_{IN} = 12V, f_S = 660 kHz, I_{LIM} = I_{LIM_LS3}, L = 2.2 µH, T_A = +25°C.

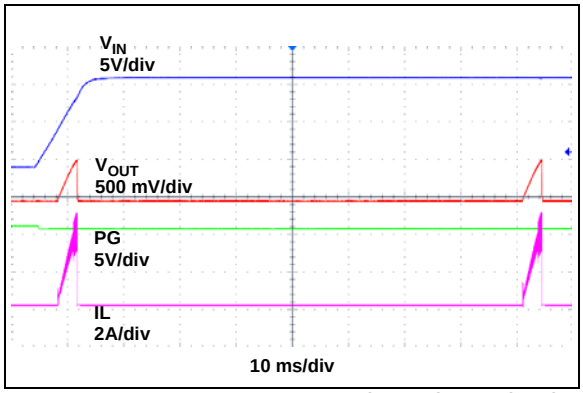

FIGURE 2-29: *Power-up into Short Circuit, (EN = V_{DDA}, no I^2C programming, registers default values for 2Z version).*

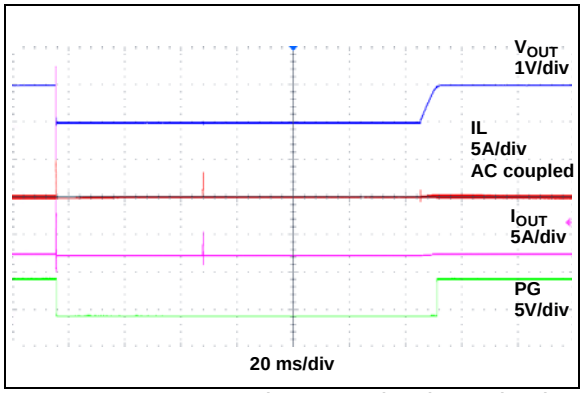

FIGURE 2-32: *Hiccup Mode Short Circuit Current Limit Response.*

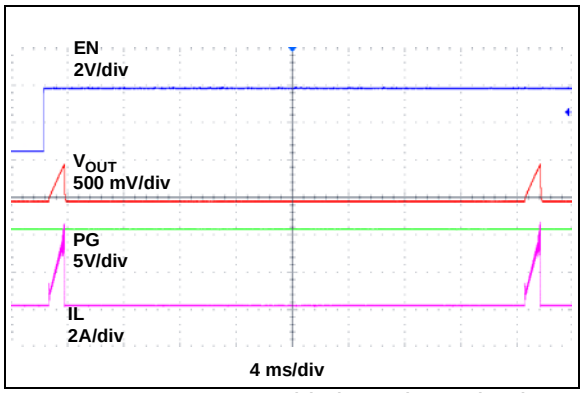

FIGURE 2-30: *Enable into Short Circuit.*

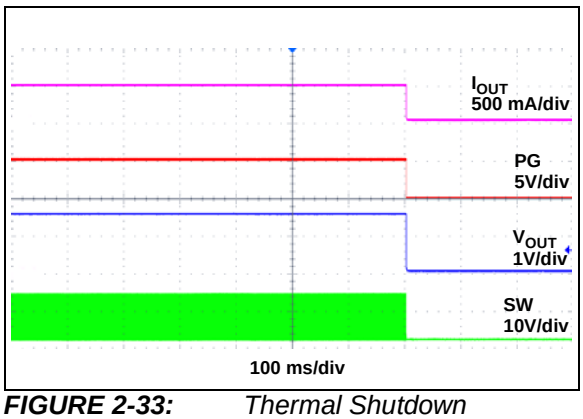

FIGURE 2-33: *Thermal Shutdown Response.*

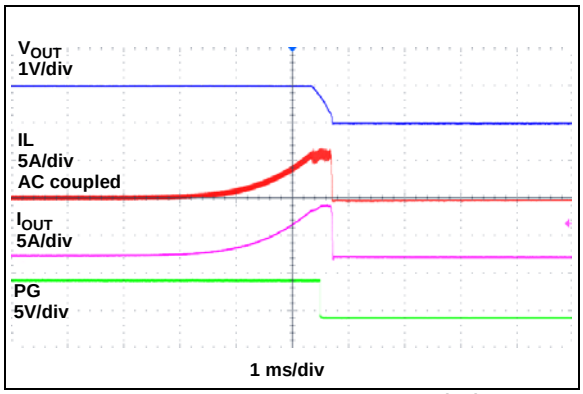

FIGURE 2-31: *Output Current Limit Threshold.*

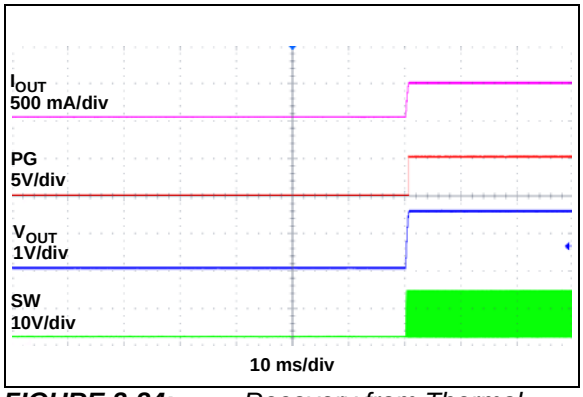

FIGURE 2-34: *Recovery from Thermal Shutdown.*

Note: Unless otherwise indicated, V_{IN} = 12V, f_S = 660 kHz, I_{LIM} = I_{LIM_LS3}, L = 2.2 µH, T_A = +25°C.

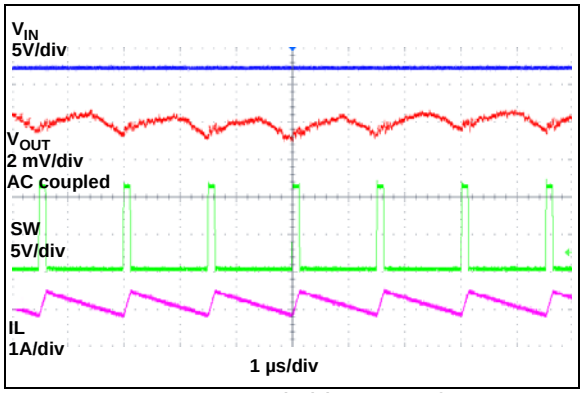

FIGURE 2-35: *Switching Waveforms - f_S = 660 kHz, I_{OUT} = 0A.*

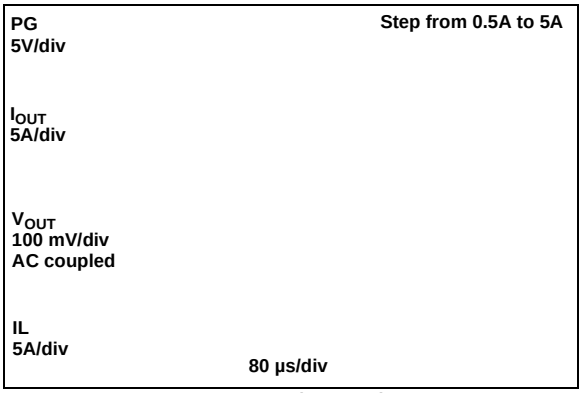

FIGURE 2-38: *Load Transient Response with I_{LIM} = I_{LIM_LS3}.*

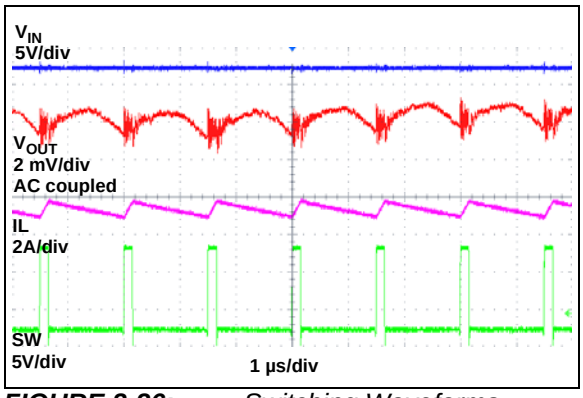

FIGURE 2-36: *Switching Waveforms - f_S = 660 kHz, I_{OUT} = 5A.*

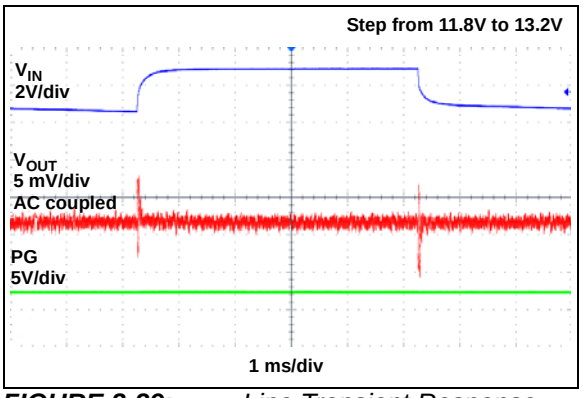

FIGURE 2-39: *Line Transient Response.*

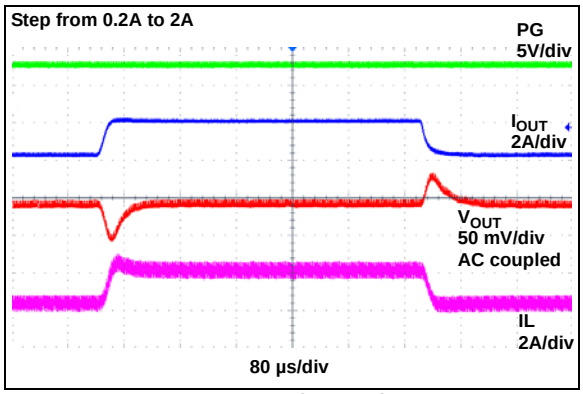

FIGURE 2-37: *Load Transient Response with I_{LIM} = I_{LIM_LS0}.*

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Note: Unless otherwise indicated, V_{IN} = 12V, f_S = 660 kHz, I_{LIM} = I_{LIM_LS3}, L = 2.2 µH, T_A = +25°C.

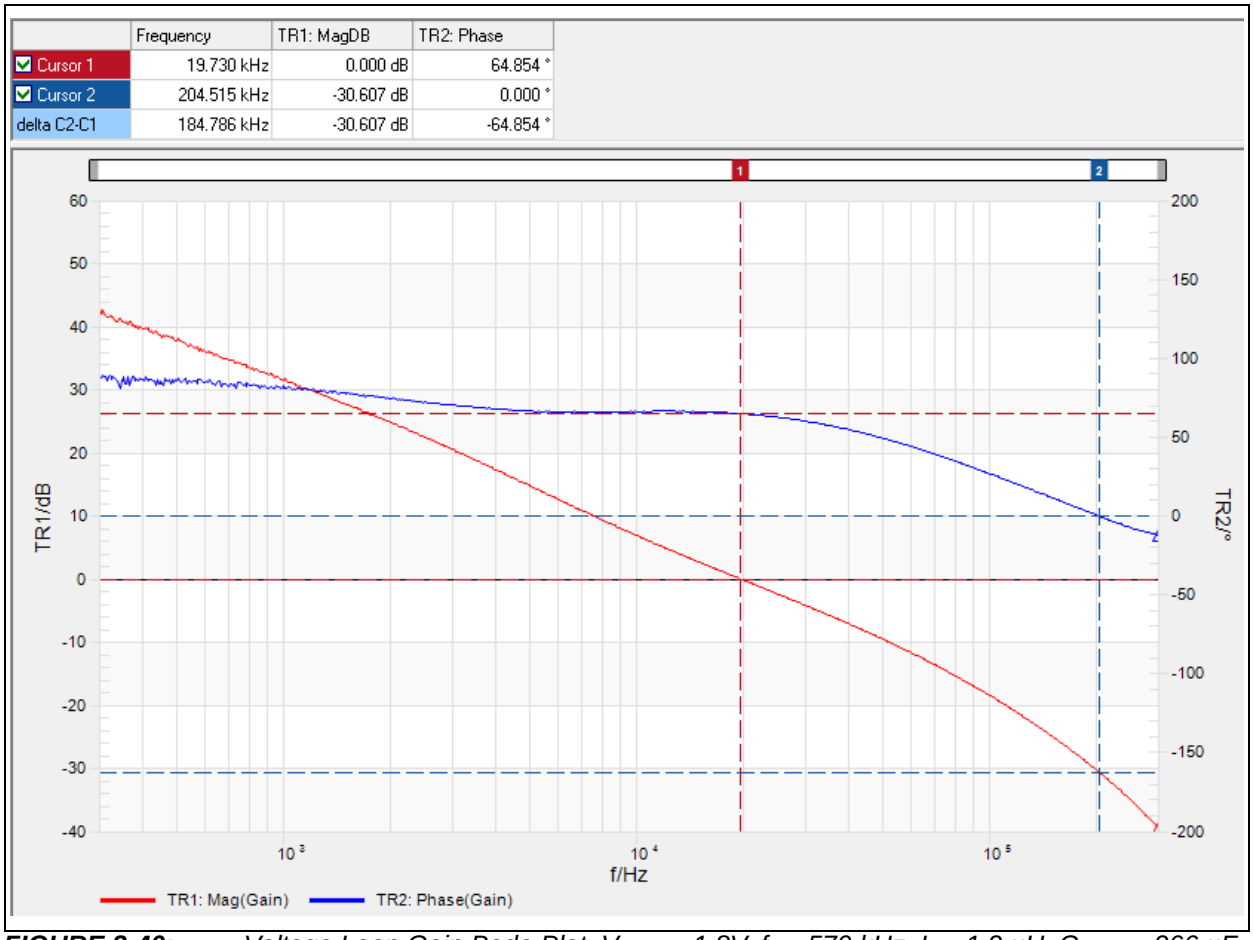

FIGURE 2-40: *Voltage Loop Gain Bode Plot, V_{OUT} = 1.8V, f_s = 570 kHz, L = 1.2 µH, C_{OUT} = 266 µF, R_{C1} = 2.55k: , C_{C1} = 10nF, C_{C2} = 47pF (see Section 7.7, Compensation Design).*

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MIC24045	Symbol	Pin Function
1, 2	V_{IN}	Input Voltage Pin
3, 4, 13	P_{GND}	Power Ground Pin
5, 6	LX	Switch Node Pin
7	BST	Bootstrap Capacitor Pin. A bootstrap capacitor is connected between the BST and LX pins.
8	PG	Power Good Open-Drain Output Pin
9	ADR0	I^2C Address Programming Pin 0
10	ADR1	I^2C Address Programming Pin 1
11	SCL	I^2C Clock Input Pin
12	SDA	I^2C Data Input/Output Pin
14	A_{GND}	Analog Ground Pin
15	COMP	Transconductance Error Amplifier Output Pin. Connect the compensation network from COMP to A_{GND}.
16	OUTSNS	Output Sensing Pin
17	EN	Precision Enable Input Pin
18	V_{DDA}	Internal Regulator Output Pin
19	V_{DDP}	MOSFET Drivers Internal Supply Pin
20	V_{INLDO}	Internal Regulator Input Pin
21	V_{IN}_EP	V_{IN} Exposed Pad. Electrically connected to V_{IN}.
22	P_{GND}_EP	P_{GND} Exposed Pad. Electrically connected to P_{GND}.
23	LX_EP	LX Exposed Pad. Electrically connected to LX.

3.1 Input Voltage Pin (V_{IN})

Input Voltage pin for the Buck converter power stage. These pins are the drain terminal of the internal high-side N-channel MOSFET. A 10 µF minimum ceramic capacitor should be connected from V_{IN} to the P_{GND} pins as close as possible to the device. A combination of multiple ceramic capacitors of different sizes is recommended.

3.2 Power Ground Pin (P_{GND})

Low-side MOSFET source terminal and low-side driver return. Connect the ceramic input capacitors to P_{GND} as close as possible to the device.

3.3 Switch Node Pin (LX)

Drain (low-side MOSFET) and source (high-side MOSFET) connection of the internal power N-channel FETs. The external inductor (switched side) and bootstrap capacitor (bottom terminal) must be connected to these pins.

3.4 Bootstrap Capacitor Pin (BST)

Supply voltage for the driver of the high-side N-channel power MOSFET. Connect the bootstrap capacitor (top terminal) to this pin.

3.5 Power Good Output Pin (PG)

When the output voltage is within 92.5% of the nominal set point, this pin will go from logic low to logic high through an external pull-up resistor. This pin is the drain connection of an internal N-channel FET.

3.6 I^2C Address Programming Pin 0 (ADR0)

Three-state pin (low, high and high-Z) for I^2C address programming. Together with ADR1, ADR0 defines nine logic values corresponding to nine I^2C addresses.

3.7 I^2C Address Programming Pin 1 (ADR1)

Three-state pin (low, high and high-Z) for I^2C address programming. Together with ADR0, ADR1 defines nine logic values corresponding to nine I^2C addresses.

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3.8 I²C Clock Input Pin (SCL)

The SCL pin is the serial interfaces Serial Clock pin.This pin is connected to the Host Controllers SCL pin.

The MIC24045 is a slave device, so its SCL pin accepts only external clock signals.

3.9 I²C Data Input/Output Pin (SDA)

The SDA pin is the serial interface Serial Data pin. This pin is connected to the Host Controllers SDA pin. The SDA pin has an open-drain N-channel driver.

3.10 Analog Ground Pin (A_{GND})

This pin is a quiet ground for the analog circuitry of the internal regulator and a return terminal for the external compensation network.

3.11 Transconductance Error Amplifier Output Pin (COMP)

Connect a compensation network from this pin to A_{GND}.

3.12 Output Sensing Pin (OUTSNS)

Connect this pin directly to the buck converter output voltage. This pin is the top side terminal of the internal feedback divider.

3.13 Precision Enable Input Pin (EN)

The EN pin is compared to a 1.21V typical threshold to determine the turn-on of the device. After reaching the turn-on threshold, the I²C-programmable turn-on delay counter starts. A 2 µA (typical) current source pulls down the EN pin to prevent unwanted power delivery in case of a floating EN input. A 135 mV typical hysteresis prevents chattering when power delivery is started.

3.14 Internal Regulator Output Pin (V_{DDA})

Output of the internal linear regulator and internal supply for analog control. A 1 µF minimum ceramic capacitor should be connected from this pin to A_{GND}; a 2.2 µF typical value is recommended.

3.15 MOSFET Drivers Internal Supply Pin (V_{DDP})

Internal supply rail for the MOSFET drivers, fed by the V_{DDA} pin. An internal resistor (10□) between the V_{DDP} and V_{DDA} pins is provided in the regulator in order to implement an RC filter for switching noise suppression. A 1 µF minimum ceramic capacitor should be connected from this pin to P_{GND}; a 2.2 µF typical value is recommended.

3.16 Internal Regulator Input Pin (V_{INLDO})

This pin is typically connected to the input voltage of the buck converter stage (V_{IN}). If V_{INLDO} and V_{IN} are connected to different voltage rails, individually bypass V_{INLDO} to ground with a 100 nF ceramic capacitor.

3.17 P_{GND} Exposed Pad (P_{GND_EP})

Electrically connected to P_{GND} pins. Connect with thermal vias to the ground plane to ensure adequate heat-sinking. See **Section 9.0 "Packaging Information"**.

3.18 V_{IN} Exposed Pad (V_{IN_EX})

Electrically connected to V_{IN} pins. If an input power distribution plane is available, connect with thermal vias to that plane to improve heat-sinking. See **Section 9.0 "Packaging Information"**.

3.19 LX Exposed Pad (LX_EP)

Electrically connected to LX pins. See **Section 9.0 "Packaging Information"**.

4.0 FUNCTIONAL DESCRIPTION

The MIC24045 is a digitally programmable, 5A valley current-mode controlled regulator featuring an input voltage range from 4.5V to 19V.

Programmability is achieved by means of an I^2C-compatible serial digital interface, which can support Serial Clock (SCL) rates up to 400 kHz (Fast mode).

The MIC24045 requires a minimal amount of external components. Only the inductor, supply decoupling capacitors and compensation network are external. The flexibility in the external compensation design allows the user to optimize their design across the entire range of operating parameters such as input voltage, output voltage, switching frequency and load current.

4.1 Theory of Operation

Valley current-mode control is a fixed-frequency, leading-edge-modulated PWM current-mode control. Differing from Peak Current mode, in valley current-mode the clock marks the turn-off of the high-side switch. Upon this instant, the MIC24045 low-side switch current level is compared against the reference current signal from the error amplifier. When the falling low-side switch current signal drops below the current reference signal, the high-side switch is turned on. As a result, the inductor valley current is regulated to a level dictated by the output of the error amplifier.

As shown in **Section 7.7 "Compensation Design"**, the feedback loop includes an internal programmable reference (REF_{DAC}) and an output voltage sensing attenuator (R2/R1), which removes the need for external feedback components and improves regulation accuracy. Output voltage feedback is achieved by connecting OUTSNS directly to the output. The high-performance transconductance error amplifier drives an external compensation network at the COMP pin. The COMP pin voltage represents the reference current signal. The COMP pin voltage is fed to the valley current-mode modulator, which also adds slope compensation to ensure current-loop stability. Valley current-mode control requires slope compensation at duty cycles less than 50% for current-loop stability. The slope compensation circuit is internal and it is automatically adapted in amplitude depending upon the frequency, output voltage range and voltage differential (V_{IN} - V_{OUTSNS}). The internal low-$R_{DS(ON)}$ power MOSFETs, the associated adaptive gate driver and the internal bootstrap diode complete the power train.

Overcurrent protection and thermal shutdown protect the MIC24045 from faults or abnormal operating conditions.

4.2 Internal LDO, Supply Rails (V_{IN}, V_{INLDO}, V_{DDA}, V_{DDP})

V_{IN} pins represent the power train input. These pins are the drain connection of the internal high-side MOSFET and should be bypassed to P_{GND} with a X5R or X7R 10 µF (minimum) ceramic capacitor, placed as close as possible to the device. A combination of ceramic capacitors of different sizes is recommended.

An internal LDO (biased through V_{INLDO} pin) provides a clean supply (5.1V typical) for the analog circuits and the I^2C interface at pin V_{DDA}. The internal LDO is typically powered from the same power rail feed at V_{IN}; however, V_{INLDO} can also be higher or lower than V_{IN} and can be connected to any other voltage within its recommended limits. V_{INLDO} and V_{DDA} should be locally bypassed (see **Section 3.0 "Pin Description"**). A small series resistor (typically 2□-10□) can be used in combination with the V_{INLDO} bypass capacitor to implement a RC filter for suppression of large high-frequency switching noise.

The internal LDO is always enabled and regulation takes place as soon as enough voltage has established between the V_{INLDO} and V_{DDA} pins. If an external 5V±10% is available, it is possible to bypass the internal LDO by connecting V_{INLDO}, V_{DDA} and V_{DDP} together at the external 5V rail, thus improving overall efficiency.

The MIC24045 does not require a separate supply for the I^2C interface and for the internal logic registers, which are all powered from the V_{DDA} rail. An internal Undervoltage Lock-Out circuit (UVLO) monitors the level of V_{DDA} and resets the interface and the internal registers if the V_{DDA} voltage is below the UVLO threshold.

V_{DDP} is the power supply rail for the gate drivers and bootstrap circuit. This pin is subject to high-current spike with high-frequency content. To prevent these from polluting the analog V_{DDA} supply, a separate capacitor is needed for V_{DDP} pin bypassing. An internal 10□ resistor is provided between pins V_{DDA} and V_{DDP}, allowing a switching noise attenuation RC filter with the minimum amount of external components to be implemented. It is possible, although typically not necessary, to lower the RC time constant by connecting an external resistor between pins V_{DDA} and V_{DDP}.

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4.3 Enable (EN)

The EN pin starts/stops the power delivery to the output. It does not turn off the internal LDO. The EN pin does not act as a Reset signal for the I^2C registers, only the V_{DDA} UVLO circuit does.

Rising threshold is a precise 1.21V±70 mV. A 135 mV typical hysteresis prevents chattering due to switching noise and/or slow edges. A 2 µA typical pull-down current with ±1 µA accuracy prevents unwanted start-ups if the EN pin is momentarily floating. To achieve automatic turn-on as soon as enough voltage is present, connect EN to V_{DDA}.

4.4 Power Good (PG)

PG is an open-drain output. For asserting a logic HIGH level, PG requires an external resistor connected to a pull-up voltage (V_{PU_PG}), which should not exceed 5.5V.

PG is asserted with a typical delay of 0.45 ms when the output voltage (OUTSNS) reaches 92.5% of its target regulation voltage. PG is de-asserted with a typical delay of 80 µs when the output voltage falls below 90% of its target regulation voltage. The PG falling delay acts as a de-glitch timer against very short spikes. The PG output is always immediately de-asserted when the EN pin is below the power delivery enable threshold (EN_R/EN_F). The pull-up resistor should be large enough to limit the PG pin current to below 2 mA. The PG is in a defined state once the V_{DDA} voltage is greater than about 1V, but with reduced current sinking capability.

The PG is also immediately de-asserted (with no delay) whenever an undervoltage condition on V_{DDA} is detected, or in thermal shutdown.

4.5 Inductor (LX) and Bootstrap (BST)

The external inductor is connected to LX. The high-side MOSFET driver circuit is powered between BST and LX by means of an external capacitor (typically 100 nF) that is replenished from rail V_{DDP} during the low-side MOSFET ON-time. The bootstrap diode is internal.

4.6 Output Sensing (OUTSNS) and Compensation (COMP)

OUTSNS should be connected exactly to the desired point-of-load regulation, avoiding parasitic resistive drops. The impedance seen into OUTSNS is high (tens of k□ or more, depending on the selected output voltage value), therefore its loading effect is typically negligible. OUTSNS is also used by the slope compensation generator.

COMP is the connection for the external compensation network. COMP is driven by the output of the transconductance error amplifier. Care must be taken to return the compensation network ground directly to A_{GND}.

4.7 Soft-Start

The MIC24045 features four different I^2C-selectable soft-start slew-rate values (0.16V/ms, 0.38V/ms, 0.76V/ms and 1.5V/ms). See the section **Section 5.0 "Registers Maps and I2C Programmability"** for the value vs. code mapping. The internal reference is ramped up at the selected rate. Note that this is the internal reference soft-start slew rate and that the actual slew rate seen at the output should take into account the internal divider attenuation, as detailed in the **Section 7.0 "Application Information"**.

4.8 Start-Up Delay

The MIC24045 features eight different I^2C-selectable start-up delays (from 0 ms to 10 ms). These represent the added delays from the EN rising edge to the beginning of the power delivery (soft-start). See the section **Section 5.0, Registers Maps and I2C Programmability** for the value vs. code mapping.

4.9 Switching Frequency

The MIC24045 features eight different I^2C-selectable switching frequencies from 310 kHz to 1200 kHz. See **Section 5.0 "Registers Maps and I2C Programmability"** for the value vs. code mapping. Also pay attention to voltage conversion ratio limitations due to minimum T_{ON} and T_{OFF}, as stated in **Section 7.0 "Application Information"**.

4.10 Pre-Biased Output Start-Up

The MIC24045 is designed to achieve safe start-up into a pre-biased output without discharging the output capacitors.

4.11 Thermal Warning and Thermal Shutdown

The MIC24045 has a thermal shutdown protection that prevents operation at excessive temperature. The thermal shutdown threshold is typically set at +160°C with a hysteresis of +25°C.

The MIC24045 features a Thermal Warning flag that is readable through the I^2C interface (register polling is needed). The Thermal Warning flag signals the approaching of thermal shutdown, so that appropriate system-level countermeasures can be undertaken.

Note that a thermal shutdown event will not disable the internal V_{DDA} linear regulator, but only the power stage. In this way, the I^2C interface remains powered and can still be read throughout the duration of the thermal shutdown.

4.12 Overcurrent Protection

The MIC24045 features instantaneous cycle-by-cycle current limit with current sensing both on the low-side and high-side switches. It also offers a Hiccup mode for prolonged overloads or short-circuit conditions.

Low-side cycle-by-cycle protection detects the current level of the inductor current during the low-side MOSFET ON time. The high-side MOSFET turn-on is inhibited as long as the low-side MOSFET current limit is above the low-side current-limit threshold level. The inductor current will continue decaying until the current falls below the threshold, then the high-side MOSFET will be enabled again according to the duty cycle requirement from the PWM modulator.

The mechanism is illustrated in Figure 4-1.

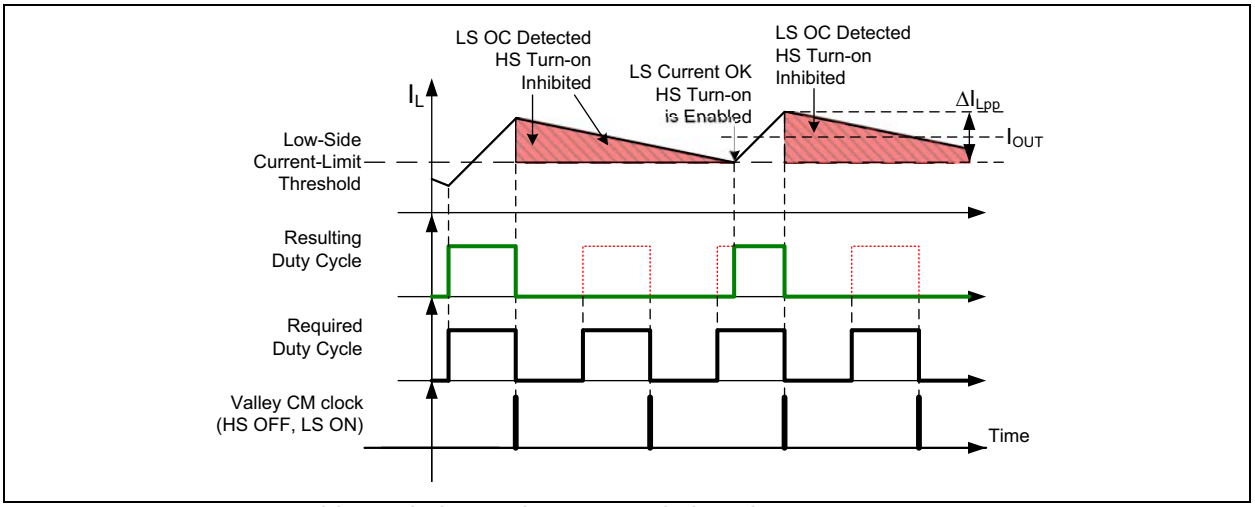

FIGURE 4-1: *Low-Side Cycle-by-Cycle Current-Limit Action.*

The low-side current limit is programmable at four different levels (for 2A, 3A, 4A and 5A loads) in order to optimize inductor size for different application requirements. These levels are listed in **Section 5.0 "Registers Maps and I2C Programmability"**.

Since the low-side current limit acts on the valley current, the DC output current level (I_{OUT}), where the low-side cycle-by-cycle current limit is engaged, will be higher than the current limit value by an amount equal to □IL_{PP}/2, where □IL_{PP} is the peak-to-peak inductor ripple current.

The high-side current limit is approximately 1.4 – 1.5 times greater than the low-side current limit (typical values). The high-side cycle-by-cycle current limit immediately truncates the high-side ON time without waiting for the OFF clocking event.

A leading edge blanking (LEB) timer (108 ns, typical) is provided on the high-side cycle-by-cycle current limit to mask the switching noise and to prevent falsely triggering the protection. High-side cycle-by-cycle current limit action cannot take place before the LEB timer expires.

Hiccup mode protection reduces power dissipation in permanent short-circuit conditions. On each clock cycle, where a low-side cycle-by-cycle current-limit event is detected, a 4-bit up/down counter is incremented. On each clock cycle, without a concurrent low-side current limit event, the counter is decremented or left at zero. The counter cannot wrap-around below `0000` and above `1111`. High-side current limit events do not increment the counter. Only detections from low-side current limit events trigger the counter.

If the counter reaches `1111` (or 15 events), the high and low-side MOSFETs become tri-stated and power delivery to the output is inhibited for a duration which is dependent on the soft-start rate and can be calculated with the following equation:

EQUATION 4-1:

$$Inhibited\ Time = \frac{13.5V}{SS_SRx}$$

Where

SS_SRx = selected soft-start rate (SS_SRx = SS_SR0, SS_SR1, SS_SR2 or SS_SR3). See Electrical Characteristics table.

This digital integration mechanism provides immunity to the momentary overloading of the output. After the wait time, the MIC24045 retries entering operation and initiates a new soft-start sequence.

Note that Hiccup mode short-circuit protection is active at all times, including the soft-start ramp. In case of very large output capacitors, consider slowing down the soft-start slew rate to prevent start-up problems, especially if the load is completely discharging the output capacitor during the hiccup wait time.

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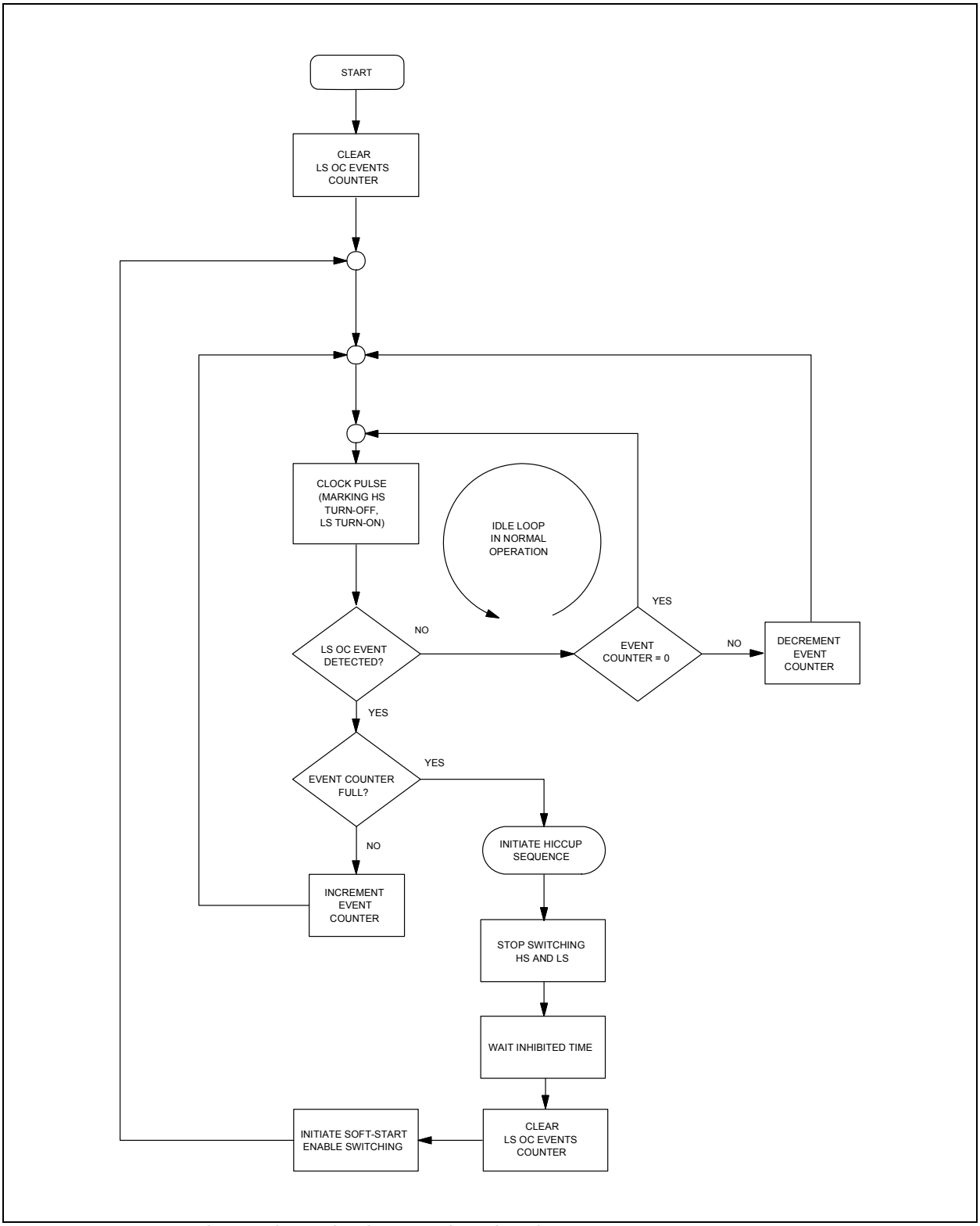

FIGURE 4-2: *Hiccup Short-Circuit Protection Flowchart.*

5.0 REGISTERS MAPS AND I²C PROGRAMMABILITY

The MIC24045 internal registers are summarized in Table 5-1, below.

TABLE 5-1: MIC24045 REGISTER MAP

Register Address	Register Name	Type	B7	B6	B5	B4	B3	B2	B1	B0
0h	Status	RO	OCF	ThSDF	ThWrnF	Reserved	EnS	Reserved	Reserved	PGS
1h	Setting 1	RW	ILIM1	ILIM0	Freq2	Freq1	Freq0	Reserved	Reserved	Reserved
2h	Setting 2	RW	Reserved	SUDly2	SUDly1	SUDly0	Mrg1	Mrg0	SS1	SS0
3h	VOUT	RW	VOUT7	VOUT6	VOUT5	VOUT4	VOUT3	VOUT2	VOUT1	VOUT0
4h	Command	RW	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ClFF

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5.1 STATUS Register

In the read-only STATUS registers, diagnostic information is provided. Bits can be F = latched (Flag) or S = non-latched (Status).

Flag bits are set when the corresponding Fault condition has occurred and do not return-to-zero once the Fault condition has ceased. Flags can only be cleared by writing '1' in Bit 0 of the COMMAND register 4h, or by power cycling. Status bits are set when the corresponding Fault condition has occurred and return to zero automatically once the Fault condition has ceased.

Default bits value at power-up is zero, except for Bit 2 (which will always be read as '1') and Bit 1, which is '1' if no Fault conditions are detected.

REGISTER 5-1: STATUS – STATUS REGISTER (ADDRESS 0h)

R-0	R-0	R-0	R'0'	R-0	R'1'	R-1	R-0
OCF	ThSDF	ThWrnF	Reserved	EnS	Reserved	Reserved	PGS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
RC = Read-then-clear bit			

bit 7 **OCF:** Over-Current Flag bit. OCF is set high whenever an over-current event occurs. Latched.

bit 6 **ThSDF:** Thermal Shut-down Flag bit. ThSDF is set high whenever a Thermal Shutdown occurs. Latched.

bit 5 **ThWrnF:** Thermal Warning Flag bit. ThWrnF is set high whenever a Thermal Warning occurs. Latched.

bit 4 **Reserved:** Flag bit. Always read as zero.

bit 3 **EnS:** Enable Pin Status bit. EnS reflects the logic value present on pin EN. Non-latched.

bit 2 **Reserved:** Status bit. Always read as '1'.

bit 1 **Reserved:** Default status at POR is '1' (no faults detected).

bit 0 **PGS:** Power-Good Status bit. PGS reflects the logic value present on pin PG. Non-latched.

REGISTER 5-2: SETTING 1 – SETTING 1 REGISTER (ADDRESS 1h)

RW-V	RW-V	RW-V	RW-V	RW-V	U-0	U-0	U-0
ILIM1	ILIM0	Freq2	Freq1	Freq0	Reserved	Reserved	Reserved
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
RC = Read-then-clear bit	V = factory-programmed POR value(1)		

Note 1: Default Status settings at power-up can be changed at the factory. Standard selections are described in **Section 6.0 "MIC24045 Default Settings Values at Power-Up"**. Overwriting default settings by I^2C has no permanent effect and values will return to factory default values upon power cycling.

2: Changing Setting 1 Register values while power delivery is enabled is not recommended. To change settings by I^2C, set EN pin low first, then write the new configuration, and finally, set EN pin high again to resume power delivery.

REGISTER 5-2: SETTING 1 – SETTING 1 REGISTER (ADDRESS 1h) (CONTINUED)

bit 7-6 **ILIM<1:0>:** MOSFET Current Limit bit. See the Current Limit selection in table below**:**

ILIM1	ILIM0	TYP Low-Side Current Limit (A)	TYP High-Side Current Limit (A)	Nominal Load Current (A)
0	0	3.25	4.7	2
0	1	4.3	6.2	3
1	0	5.6	8.6	4
1	1	6.2	9.4	5

bit 5-3 **Freq0 (Switching Frequency):** See the Switching Frequency selection in table below:

Freq2	Freq1	Freq0	Frequency (kHz)
0	0	0	310
0	0	1	400
0	1	0	500
0	1	1	570
1	0	0	660
1	0	1	780
1	1	0	970
1	1	1	1200

bit 2-0 **Reserved:** Unimplemented bit. Read as '0'.

Note 1: Default Status settings at power-up can be changed at the factory. Standard selections are described in **Section 6.0 "MIC24045 Default Settings Values at Power-Up"**. Overwriting default settings by I^2C has no permanent effect and values will return to factory default values upon power cycling.

2: Changing Setting 1 Register values while power delivery is enabled is not recommended. To change settings by I^2C, set EN pin low first, then write the new configuration, and finally, set EN pin high again to resume power delivery.

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REGISTER 5-3: SETTING 2 – SETTING 2 REGISTER (ADDRESS 2h)

U-0	RW-V	RW-V	RW-V	RW-0	RW-0	RW-V	RW-V
Reserved	SUDly2	SUDly1	SUDly0	Mrg1	Mrg0	SS1	SS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
RC = Read-then-clear bit	V = factory-programmed POR value(1)		

bit 7 **Reserved:** Unimplemented bit. Read as '0'. Writing to this bit has no effect.

bit 6-4 **SUDly<2:0>:** Start-Up Delay bit. Delay to start power delivery from the rising edge of the EN signal. See the Start-up Delay selection in table below:

SUDly2	SUDly1	SUDly0	Start-Up Delay (ms)
0	0	0	0
0	0	1	0.5
0	1	0	1
0	1	1	2
1	0	0	4
1	0	1	6
1	1	0	8
1	1	1	10

bit 3-2 **Mrg<1:0>:** Voltage Margins bit. These bits can be changed at any time during power delivery. See the Voltage Margining selection in table below:

Mrg1	Mrg0	Change to nominal V_{OUT} Setting (%)
0	0	0%
0	1	-5%
1	0	+5%
1	1	+5%

Default at power-up is <0:0>

bit 1-0 **SS1<1:0>:** Soft-Start Ramp Rate bit. See the Soft-Start Tamp Rates selection in table below:

SS1	SS0	Soft-Start Slope (V/ms)
0	0	0.16
0	1	0.38
1	0	0.76
1	1	1.5

Note 1: For all bits (except Margining bits Mrg<1:0>) the Default Status at power-up can be changed at the factory. Standard selections are described in **Section 6.0 "MIC24045 Default Settings Values at Power-Up"**. Overwriting default settings by I^2C has no permanent effect and values will return to factory default settings upon power cycling. Default power-up status for Mrg<1:0> is <0:0>.

2: With the exception of Margining Bits Mrg<1:0>, changing Setting 2 register values while power delivery is enabled is not recommended. To change settings by I^2C, set EN pin low first, then write the new configuration, and finally, set EN pin high again to resume power delivery.

REGISTER 5-4: VOUT – VOUT REGISTER (ADDRESS 3h)

RW-V	RW-V	RW-V	RW-V	RW-V	RW-V	RW-V	RW-V
VOUT7	VOUT6	VOUT5	VOUT4	VOUT3	VOUT2	VOUT1	VOUT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
RC = Read-then-clear bit	V = factory-programmed POR value(1)		

bit 7-0 **VOUT<7:0>:** VOUT register bits can be changed at any time during power delivery, provided that transitions from one code to another:

- are done step-by-step, by small VOUT increments. The speed of the transition is left to the user and limited by the I^2C writing interface speed.
- code transition shall take place only within the same VOUT Range. Crossing boundaries of resolution ranges may cause VOUT glitches and it is not recommended.

See VOUT selection in table below:

VOUT Range	Step Size	Codes-decimal (hex)
0.640V to 1.280V	5 mV	0 (00h) to 128 (80h)
1.290V to 1.950V	10 mV	129 (81h) to 195 (C3h)
1.980V to 3.420V	30 mV	196 (C4h) to 244 (F4h)
4.750V to 5.250V	50 mV	245 (F5h) to 255 (FFh)

Note 1: Default Status settings at power-up can be changed at the factory. Standard selections are described in **Section 6.0 "MIC24045 Default Settings Values at Power-Up"**. Overwriting default settings by I^2C has no permanent effect and values will return to factory default values upon power cycling.

2: The functionality of the MIC24045 at any output voltage selection is subject to limitations described in **Section 7.0 "Application Information"**.

REGISTER 5-5: COMMAND – COMMAND REGISTER (ADDRESS 4h)

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CIFF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
RC = Read-then-clear bit			

bit 7-1 **Reserved<7:1>:** Writing to these bits has no effect to the device operation.

bit 0 **CIFF:** Clear Fault Flags bit. Writing '1' to bit 0 will clear all Fault Flags. The CIFF bit is self-clearing and it returns to '0' as soon as the Fault Flags have been cleared.

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6.0 MIC24045 DEFAULT SETTINGS VALUES AT POWER-UP

Part number MIC24045-XXYFL also designates different default settings values at power-up, before any I^2C writing operation takes place. These values are programmed at factory.

Different default settings are obtained by burning an OTP memory (fuses). The **XX** code corresponds to a certain combination of output voltage, switching frequency, nominal load current and soft-start ramp rate. Start-up delay and voltage margining always default to 0 ms and 0%. The blank (all zeros) OTP memory option has a special code (**2Z**).

The standard default settings are as shown in Table 6-1. For availability of other default settings, contact the nearest Microchip Sales Office.

TABLE 6-1: STANDARD DEFAULT SETTINGS

Full Part Number	Code	V_{OUT} (V)	Frequency	Load Current	Reference Soft-Start Rate
MIC24045-2ZYFL	**2Z**	0.64	310 kHz	2A	0.16V/ms
MIC24045-DIYFL	**DI**	1.0	780 kHz	5A	0.38V/ms
MIC24045-EIYFL	**EI**	1.2	780 kHz	5A	0.38V/ms
MIC24045-JFYFL	**JF**	3.3	570 kHz	5A	0.38V/ms
MIC24045-KDYFL	**KD**	5.0	570 kHz	3A	0.38V/ms

When power is cycled, the MIC24045 user-programmable registers return to the factory-programmed default settings values, regardless of any prior settings through I^2C bus. Note that the EN pin does NOT act as a Reset signal for the user-programmable registers, only the internal POR (Power-on Reset) based on the V_{DDA} voltage UVLO does (see Functional Block Diagram).

7.0 APPLICATION INFORMATION

7.1 Programming External UVLO

The EN pin can be used to program an automatic turn-on of the MIC24045 when the V_{IN} (or V_{INLDO}) power rails have exceeded a desired threshold. This programmable UVLO function is achieved as described in Figure 7-1.

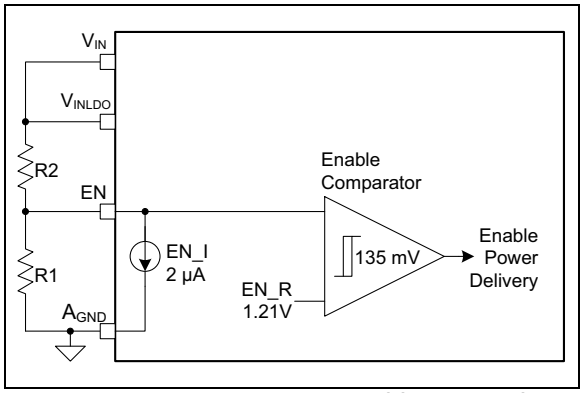

FIGURE 7-1: *Programmable External UVLO Function.*

The programmed V_{IN} UVLO threshold V_{IN_RISE} is given by:

EQUATION 7-1:

$$V_{IN_RISE} = EN_R \times \left(1 + \frac{R2}{R1}\right) + EN_I \times R2$$

where:

EN_R = 1.21V
EN_I = 2 µA
RI, R2 = External resistors

To desensitize the V_{IN} UVLO threshold against variations of the pull-up current EN_I, it is recommended to run the R1-R2 voltage divider at a significantly higher current level than the EN_I current.

The corresponding V_{IN} UVLO hysteresis, V_{IN_HYS}, is calculated as follows:

EQUATION 7-2:

$$V_{IN_HYS} = 135\ \text{mV} \times \left(1 + \frac{R2}{R1}\right)$$

7.2 Output Voltage Sensing

To achieve accurate output voltage regulation, the OUTSNS pin (internal feedback divider top terminal) should be Kelvin-connected as close as possible to the point-of-regulation top terminal. Since both the internal reference and the internal feedback divider's bottom terminal refer to A_{GND}, it is important to minimize voltage drops between the A_{GND} and the point-of-regulation return terminal.

7.3 V_{OUT} On-The-Fly Changes

It is possible to change the output voltage on-the-fly during power delivery by writing a different value to Register 5-4 (Address 3h). Note that V_{OUT} changes are possible only within each V_{OUT} range, as specified in the VOUT selection table in Register 5-4.

The transition from one particular V_{OUT} value to another is under control of the I^2C interface. The number of steps from one code to another and the speed of the transition are left to the end user.

Single Write instructions separated by a Repeated START (Sr) can be used to update Register 5-4 multiple subsequent times, without releasing the I^2C bus. Please refer to section **Section 8.5.2 "Single Write with Repeated Start (Sr)"** for more details.

The minimum t_{SU_STA} specification (set-up time for a repeated START condition), the SCL frequency and the length of the Single Write message (3 bytes) dictate a limitation on the maximum update rate of the VOUT code at Register 5-4.

Ramping down the output voltage at no or light load implies inductor current reversal (i.e., the MIC24045 will be sinking current from the output capacitor). The larger the output capacitor value, the larger the reverse inductor current will be for a given negative V_{OUT} variation.The voltage steps and the ramping step rate should be small enough to maintain a safe level of reverse current magnitude. This is especially important when using large output capacitors.

7.4 Inductor Selection and Slope Compensation

When selecting an inductor, it is important to consider the following factors:

- Inductance
- Rated Current value
- Size requirements
- DC Resistance (DCR)
- Core losses

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The inductance value is critical to the operation of MIC24045. Since the MIC24045 is a valley current-mode regulator, it needs a slope compensation for the stable current loop operation where duty cycles are below 50%. Slope compensation is internally programmed according to the frequency, output voltage and nominal load current selection, assuming there is a minimum inductance value for the given operating condition.

Table 7-1 lists the assumed minimum inductor values recommended for stable current-loop operation. Note that the minimum suggested inductance values should be met when taking into account the inductor tolerance and its change with current level.

TABLE 7-1: MINIMUM RECOMMENDED INDUCTANCE VALUES

Nominal I_{OUT}	V_{OUT}	Minimum Inductance L_{MIN} (µH)							
3A-4A-5A	0.64V-1.28V	1.27	0.97	0.78	0.68	0.58	0.49	0.39	0.29
3A-4A-5A	1.29V-1.95V	1.96	1.51	1.21	1.06	0.91	0.76	0.61	0.45
3A-4A-5A	1.98V-3.42V	3.14	2.42	1.94	1.70	1.46	1.21	0.97	0.73
3A-4A-5A	4.57V-5.25V	3.69	2.36	2.27	1.99	1.70	1.42	1.14	0.85
2A	0.64V-1.28V	2.52	1.94	1.55	1.36	1.16	0.97	0.78	0.58
2A	1.29V-1.95V	4.07	3.13	2.50	2.18	1.87	1.56	1.25	0.94
2A	1.98V-3.42V	6.53	5.03	4.01	3.52	3.02	2.52	2.01	1.51
2A	4.57V-5.25V	9.14	6.99	5.60	4.91	4.18	3.49	2.80	2.10
		310	**400**	**500**	**570**	**660**	**780**	**970**	**1200**

The slope compensation is also internally adapted to the input-output voltage differential.

In practical implementations of valley current-mode control, slope compensation is also added to any duty cycle larger than 50% as part of improving current loop stability and noise immunity for all input and output voltage ranges. Consequently, the MIC24045 adds internal slope compensation signal up to 80% duty cycle. Above this, no slope compensation is added. For this reason, the PWM modulator gain exhibits an abrupt change when the duty cycle exceeds 80%, possibly leading to some increase in jitter and noise susceptibility. If operation around and above 80% duty cycle is considered, a more conservative design of the compensation loop might help in reducing jitter and noise sensitivity.

Inductor current ratings are generally stated as permissible DC current and saturation current. Permissible DC current can be rated for a +20°C to +40°C temperature rise. Saturation current can be rated for a 10% to 30% loss in inductance. Ensure that the nominal current of the application is well within the permissible DC current ratings of the inductor, depending on the allowed temperature rise. Note that the inductor permissible DC current rating typically does not include inductor core losses. These are very important contributors of total inductor core loss and temperature increase in high-frequency DC/DC converters because core losses increase rapidly with the excitation frequency.

When saturation current is specified, make sure that there are enough design margins so the peak current does not cause the inductor to enter deep saturation.

Pay attention to the inductor saturation characteristic in current limit. The inductor should not heavily saturate, even in current limit operation. If there is heavy saturation, the current may instantaneously run away and reach potentially destructive levels. Typically, ferrite-core inductors exhibit an abrupt saturation characteristic, while powdered-iron or composite inductors have a soft-saturation characteristic. Peak current can be calculated with Equation 7-3.

EQUATION 7-3:

$$I_{L,PEAK} = \left[I_{OUT} + V_{OUT} \cdot \frac{1 - \frac{V_{OUT}}{V_{IN}}}{2 \cdot f_S \cdot L} \right]$$

As shown in Equation 7-3, the peak inductor current decreases with the switching frequency and the inductance. At a given I_{OUT} load current, the lower the switching frequency or inductance, the higher the peak current. As input voltage increases, the peak current also increases.

7.5 Output Capacitor Selection

Two main requirements determine the size and characteristics of the output capacitor C_{OUT}:

- Steady-state ripple
- Maximum voltage deviation during load transient

For steady-state ripple calculation, both the ESR and the capacitive ripple contribute to the total ripple amplitude.

From the switching frequency, input voltage, output voltage setting, and load current, the peak-to-peak inductor current ripple and the peak inductor current can be calculated as:

EQUATION 7-4:

$$\Delta I_{L_PP} = V_{OUT} \frac{1 - V_{OUT} / V_{IN}}{f_S \times L}$$

EQUATION 7-5:

$$I_{L,PEAK} = I_{OUT} + \frac{\Delta I_{L_PP}}{2}$$

The capacitive ripple $\Delta V_{R,C}$ and the ESR ripple $\Delta V_{R,ESR}$ are given by:

EQUATION 7-6:

$$\Delta V_{R,C} = \frac{\Delta I_{L_PP}}{8 \times f_S \times C_{OUT}}$$

EQUATION 7-7:

$$\Delta V_{R,ESR} = ESR \times \Delta I_{L_PP}$$

The total peak-to-peak output ripple is then conservatively estimated as:

EQUATION 7-8:

$$\Delta V_R \approx \Delta V_{R,C} + \Delta V_{R,ESR}$$

The output capacitor value and the ESR should be chosen so that ΔV_R is within specifications. Capacitor tolerance should be considered for worst-case calculations. In the case of ceramic output capacitors, factor into account the decrease of effective capacitance versus applied DC bias.

The worst-case load transient for output capacitor calculation is an instantaneous 100% to 0% load release when the inductor current is at its peak value. In this case, all the energy stored in the inductor is absorbed by the output capacitor while the converter stops switching and keeps the low-side FET ON.

The peak output voltage overshoot (ΔV_{OUT}) happens when the inductor current has decayed to zero. This can be calculated with Equation 7-9:

EQUATION 7-9:

$$\Delta V_{OUT} = \sqrt{V_{OUT}^2 + \frac{L}{C_{OUT}} I_{L,PEAK}^2} - V_{OUT}$$

Equation 7-10 calculates the minimum output capacitance value ($C_{OUT(MIN)}$) needed to limit the output overshoot below ΔV_{OUT}.

EQUATION 7-10:

$$C_{OUT(MIN)} = \frac{L \times I_{L,PEAK}^2}{\Delta V_{OUT} \times \left(\Delta V_{OUT} + V_{OUT}\right)^2 - V_{OUT}^2}$$

The result from the minimum output capacitance value for load transient is the most stringent requirement found for capacitor value in most applications. Low equivalent series resistance (ESR) ceramic output capacitors, with X5R or X7R temperature characteristics, are recommended.

For low-output voltage applications with demanding load transient requirements, using a combination of polarized and ceramic output capacitors may be most convenient for smallest solution size.

7.6 Input Capacitor Selection

Two main requirements determine the size and characteristics of the input capacitor:

- Steady-state ripple
- RMS current

The buck converter input current is a pulse train with very fast rising and falling times so low-ESR ceramic capacitors are recommended for input filtering, because of their good high-frequency characteristics.

For ideal input filtering (assuming a DC input current feeding the filtered buck power stage) and by neglecting the capacitor ESR contribution to the input ripple (typically possible for ceramic input capacitors), the minimum capacitance value $C_{IN(MIN)}$ needed for a given input peak-to-peak ripple voltage $\Delta V_{r,IN}$ can be estimated as shown in Equation 7-11:

EQUATION 7-11:

$$C_{IN(MIN)} = \frac{I_{OUT} \times D \times (1 - D)}{\Delta V_{r,IN} \times f_S}$$

where:

D = the duty cycle at the given operating point

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The RMS current $I_{IN,RMS}$ of the input capacitor is estimated as in Equation 7-12:

EQUATION 7-12:

$$I_{IN,\,RMS} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)}$$

Note that, for a given output current I_{OUT}, the worst-case values are obtained at D = 0.5.

Multiple input capacitors can be used to reduce input ripple amplitude and/or individual capacitor RMS current.

7.7 Compensation Design

As a simple first-order approximation, the valley current-mode controlled buck power stage can be modeled as a voltage-controlled current-source feeding the output capacitor and the load. The inductor current state-variable is removed and the power-stage transfer function from COMP to the inductor current is modeled as a transconductance (Gm_{PS}). The simplified model of the control loop is shown in Figure 7-2. The power-stage transconductance Gm_{PS} shows some dependence on current levels and it is also somewhat affected by process variations, therefore some design margin is recommended against the typical value Gm_{PS} = 12.5A/V (see **Electrical Characteristics**).

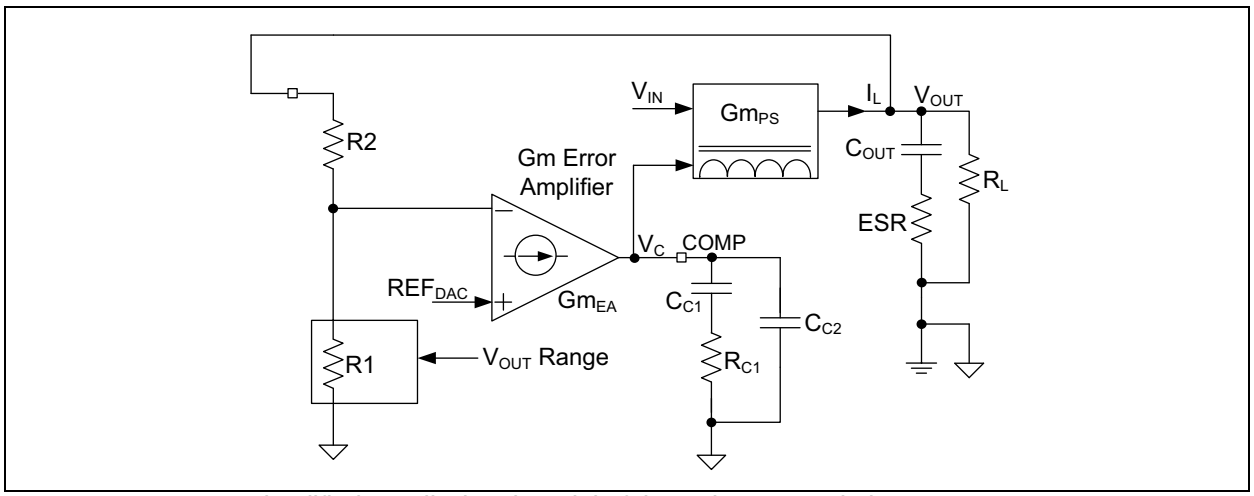

FIGURE 7-2: *Simplified Small-Signal Model of the Voltage Regulation Loop.*

This simplified approach disregards all issues related to the inner current loop, like its stability and bandwidth. This approximation is good enough for most operating scenarios, where the voltage-loop bandwidth is not pushed to aggressively high frequencies.

Based on the model shown in Figure 7-2, the control-to-output transfer function is:

EQUATION 7-13:

$$G_{CO\,S} = \frac{V_{OUT\,S}}{V_{C\,S}} = Gm_{PS} \cdot R_L \cdot \frac{1 + \frac{s}{2\pi \cdot f_z}}{1 + \frac{s}{2\pi \cdot f_p}}$$

where:

f_Z, f_P = The frequencies associated with the output capacitor ESR zero and with the load pole, respectively:

$$f_Z = \frac{1}{2\pi \cdot C_{OUT} \cdot ESR}$$

$$f_P = \frac{1}{2\pi \cdot C_{OUT} \cdot (ESR + R_L)}$$

The MIC24045 uses a transconductance (Gm_{EA} = 1.4 mA/V) error amplifier. Frequency compensation is implemented with a Type-II network (R_{C1}, C_{C1} and C_{C2}) connected from COMP to A_{GND}. The compensator transfer function consists of an integrator for zero DC voltage regulation error, a zero to boost the phase margin of the overall loop gain around the crossover frequency and an additional pole that can be used to cancel the output capacitor ESR zero, or to further attenuate switching frequency ripple. In both cases, the additional pole makes the regulation loop less susceptible to switching frequency noise. The additional pole is created by capacitor C_{C2}. Equation 7-14 details the compensator transfer function $H_{C(S)}$ (from OUTSNS to COMP).

EQUATION 7-14:

$$H_{C\,S} = -\frac{R1}{R1 + R2} \cdot Gm_{EA} \cdot \frac{1}{S \cdot (C_{C1} + C_{C2})} \cdot \frac{1 + S \cdot R_{C1} \cdot C_{C1}}{1 + S \cdot R_{C1} \cdot \frac{C_{C1} \cdot C_{C2}}{C_{C1} + C_{C2}}}$$

For polarized output capacitor, compensator pole placement at the ESR zero frequency is achieved, as shown in Equation 7-20 below:

EQUATION 7-20:

$$C_{C2} = \frac{1}{\frac{R_{C1}}{C_{OUT} \cdot ESR} - \frac{1}{C_{C1}}}$$

For ceramic output capacitor, compensator pole placement at $N \times f_{XO}$ ($N \geq 5$, $N \times f_{XO} < f_S$) is achieved, as detailed in Equation 7-21:

EQUATION 7-21:

$$C_{C2} = \frac{1}{2\pi \cdot R_{C1} \cdot N \cdot f_{XO}} - \frac{1}{C_{C1}}$$

7.8 Output Voltage Soft-Start Rate

The MIC24045 features internal, I^2C programmable soft-start, such that the output voltage can be smoothly increased to the target regulation voltage. The soft-start rate given in the Electrical Characteristics refers to the error amplifier reference, and therefore the effective soft-start rate value seen at the output of the module has to be scaled according to the internal feedback divider attenuation values listed in Table 7-2. To calculate the effective output voltage soft-start slew rate SS_SR_{OUT}, based on the particular output voltage setting and the reference soft-start slew rate SS_SRx (x = 0, 1, 2, 3 depending on selection), use the following formula:

EQUATION 7-22:

$$SS_SR_{OUT} = A \cdot SS_SRx$$

where:

A = amplification (see Table 7-2 for A values.)

7.9 Minimum T_{ON} and Minimum T_{OFF} Limitations

The valley current-mode control method utilized in the MIC24045 allows very small minimum controllable ON time (around 26 ns), so that it is possible to convert from 19V down to very low voltages at high frequency. Note that the high-side current limit circuit may not be able to detect an overcurrent event if the ON time is below the high side switch current limit leading edge blanking time (LEB, see Electrical Characteristics).

Conversely, some minimum OFF time is needed for valley current-mode modulator operation. This $T_{OFF(MIN)}$ specification (see Electrical Characteristics) may dictate a limit on the maximum attainable output voltage for a given V_{IN} voltage. The maximum attainable output voltage (at no load) is calculated as follows:

EQUATION 7-23:

$$V_{OUT,max} = V_{IN} \cdot \left(1 - f_S \cdot T_{OFF(MIN)}\right)$$

It is advisable to use a safe headroom margin against the calculated value of $V_{OUT,max}$ for DC load and good dynamic performance.

8.0 I²C INTERFACE DESCRIPTION

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are: a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy. MIC24045 is a slave-only device (i.e., it cannot generate a SCL signal and does not have SCL clock stretching capability). Every data transfer to and from the MIC24045 must be initiated by a master device which drives the SCL line.

The MIC24045 is a Fast mode device, supporting data transfers at up to 400 Kbit/s.

The MIC24045 device assumes that the I²C logic levels on the bus are generated by a device operating from a nominal supply voltage of 3.3V (with +/-10% tolerance). Therefore, V_{IH} and V_{IL} are not related to the V_{DDA} value of the MIC24045. The SDA and SCL lines must not be pulled up to the V_{DDA} voltage of the MIC24045, but to the I²C master interface supply voltage (3.3V nominal).

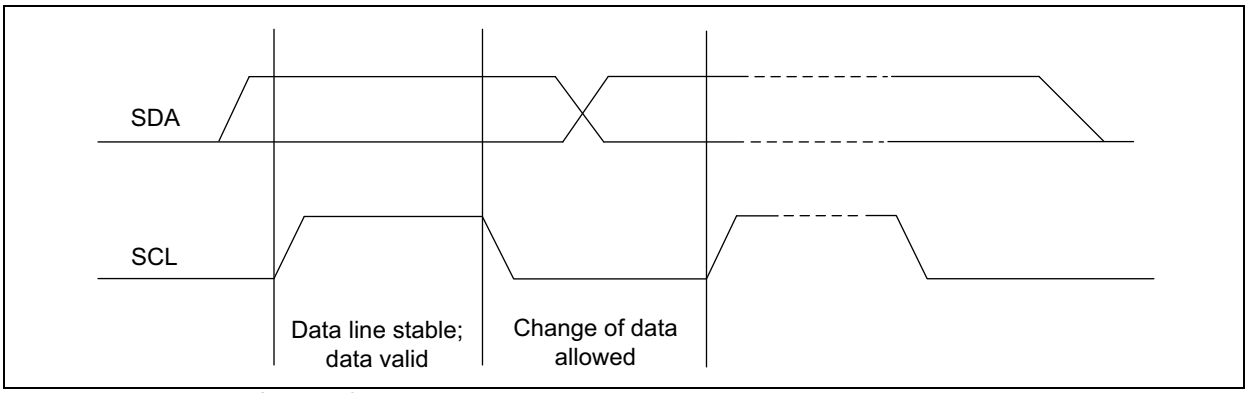

FIGURE 8-1: *Bit Transfer.*

8.1 Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

8.2 START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START (S) or repeated START (Sr) condition. A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition. The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition.

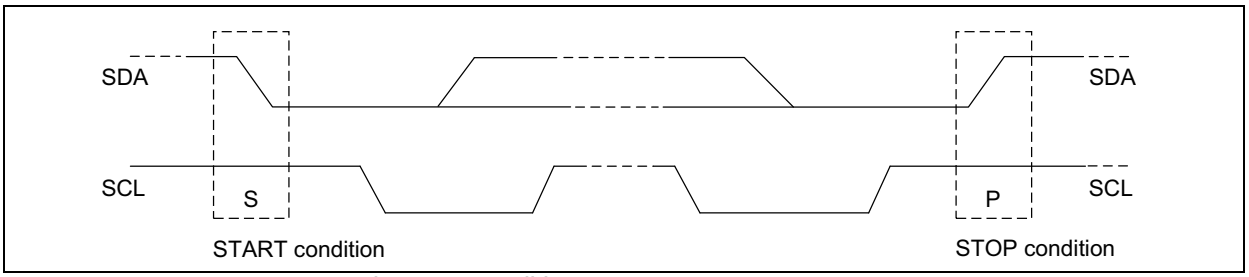

FIGURE 8-2: *START and STOP Conditions.*

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8.3 Device Address

The MIC24045 device uses a 7-bit address, which is set in hardware, using three-state pins ADR0 and ADR1 (HIGH, LOW, or high-Z). These two three-state pins allow for nine different addresses, as described in Table 8-1 below.

TABLE 8-1: MIC24045 I²C ADDRESS SETTING

ADR1	ADR0	I²C Address
0	0	101 0000
0	1	101 0001
1	0	101 0010
1	1	101 0011
0	high-Z	101 0100
high-Z	0	101 0101
1	high-Z	101 0110
high-Z	1	101 0111
high-Z	high-Z	101 1000

8.4 Acknowledge

The number of data bytes transferred between the START and the STOP conditions, from transmitter to receiver, is not limited. Each byte of eight bits is followed by one Acknowledge bit. The Acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge-related clock pulse. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse; setup and hold times must be taken into account.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte.

Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter, except on the last received byte. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave transmitter. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

8.5 Bus transactions

8.5.1 SINGLE WRITE

The first seven bits of the first byte make up the slave address. The eighth bit is the LSB (Least Significant bit). It determines the direction of the message (R/W). A ‘zero’ in the least significant position of the first byte means that the master will write information to a selected slave. A ‘1’ in this position means that the master will read information from the slave. When an address is sent, each device in a system compares the first seven bits after the START condition with its address. If they match, the device considers itself addressed by the master as a slave-receiver or slave-transmitter, depending on the R/W bit.

Command byte is a data byte which selects a register on the device. The Least Significant six bits of the command byte determine the address of the register that needs to be written.

The data to port is the 8-bit data that needs to be written to the selected register. This is followed by the acknowledge from the slave and then the STOP condition.

The Write command is as follows and it is illustrated in the timing diagram below:

1. Send START sequence
2. Send 7-bit slave address
3. Send the R/W bit - 0 to indicate a write operation
4. Wait for acknowledge from the slave
5. Send the command byte – address that needs to be written
6. Wait for acknowledge from the slave
7. Receive the 8-bit data from the master and write it to the slave register indicated in step 5 starting from MSB
8. Acknowledge from the slave
9. Send STOP sequence

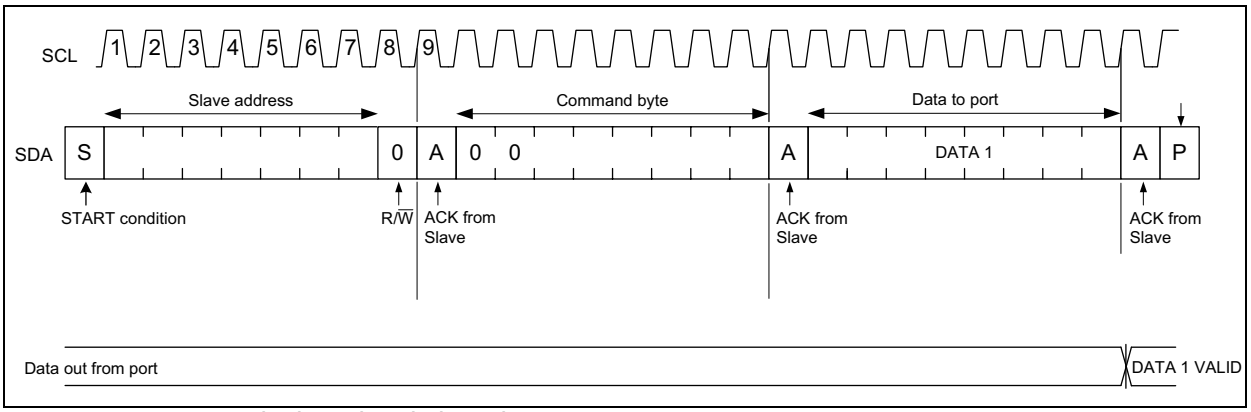

FIGURE 8-3: *Single Write Timing Diagram.*

Note:	Writing to a non-existing register location will generate a reject action (NACK) by the MIC24045 after the command byte.

8.5.2 SINGLE WRITE WITH REPEATED START (Sr)

In multi-master I^2C systems, this bus transaction is the recommended method to execute V_{OUT} on-the-fly changes in multiple steps.

The sequence is the same as for the previous Single Write transaction, except that at the end the master issues a Repeated START (Sr) instead of a STOP (P), and another (or more) Single Write operation takes place until the master releases the bus with a STOP. This way the master does not release the bus after the first Single Write and can accomplish the V_{OUT} on-the-fly change in multiple steps, without interference from other master devices.

The Single Write with Repeated Start (Sr) command is as follows and it is illustrated in the timing diagram of Figure 8-4 below:

1. Send START sequence
2. Send 7-bit slave address
3. Send the R/W bit - 0 to indicate a write operation
4. Wait for acknowledge from the slave
5. Send the command byte – address that needs to be written
6. Wait for acknowledge from the slave
7. Receive the 8-bit data – DATA 1 from the master and write it to the slave register indicated in step 5, starting from MSB
8. Acknowledge from the slave – The register is updated with DATA 1
9. Send START sequence
10. Send 7-bit slave address
11. Send the R/W bit - 0 to indicate a write operation
12. Wait for acknowledge from the slave
13. Send the command byte – address that needs to be written
14. Wait for acknowledge from the slave
15. Receive the 8-bit data – DATA 2 from the master and write it to the slave register indicated in step 13, starting from MSB
16. Acknowledge from the slave – The register is updated with DATA 2

These steps (steps 9 through 16) can continue as many times as needed to write to the same register (or another valid writable register as indicated in steps 5 and 13) without sending a STOP sequence. The master will conclude the data transfer on the last write operation by generating a STOP condition.

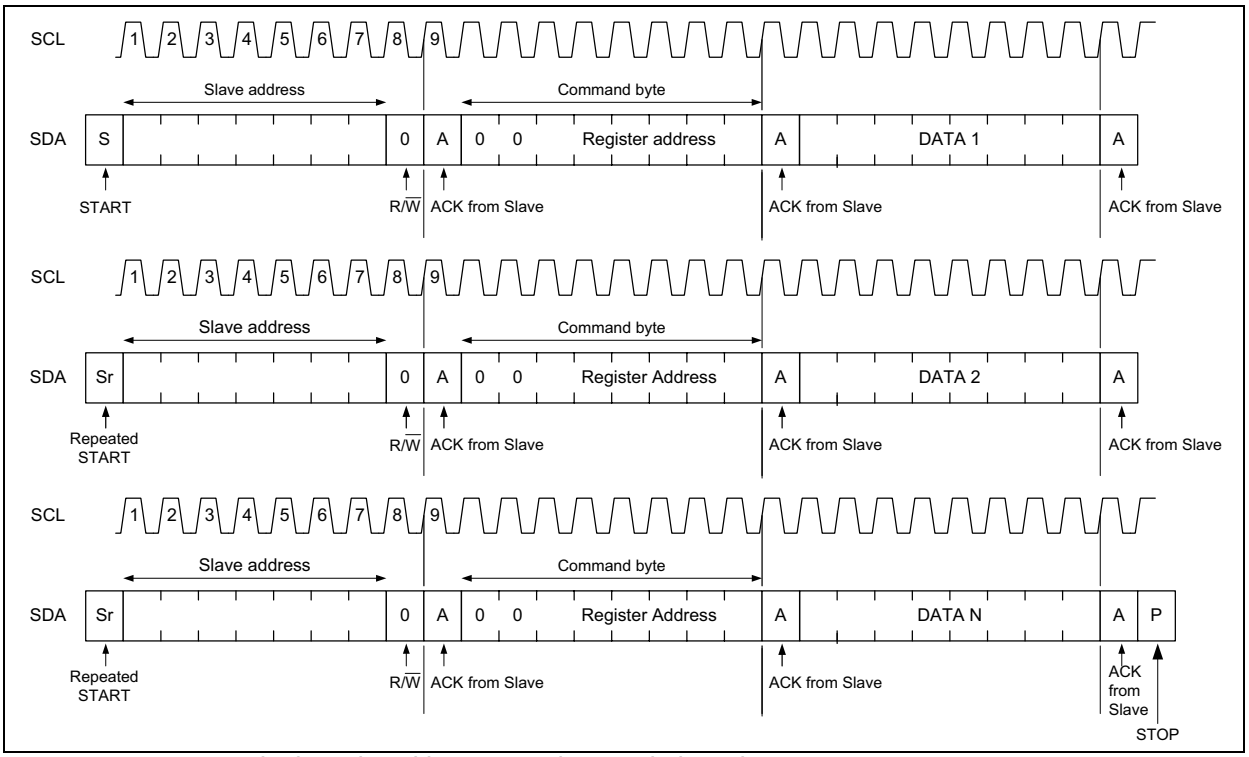

FIGURE 8-4: *Single Write with Repeated Start Timing Diagram.*

Note:	Writing to a non-existing register location will generate a reject action (NACK) by the MIC24045 after the command byte.

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8.5.3 SINGLE READ

This reads a single byte from a device, from a designated register. The register is specified through the command byte.

The Read command is as follows and it is illustrated in the timing diagram of Figure 8-5 below.

1. Send START sequence
2. Send 7-bit slave address
3. Send the R/W bit - 0 to indicate a write operation
4. Wait for acknowledge from the slave
5. Send the register address that needs to be read
6. Wait for acknowledge from the slave
7. Send START sequence again (Repeated START condition)
8. Send the 7-bit slave address
9. Send R/W bit - 1 to indicate a read operation
10. Wait for acknowledge from the slave
11. Receive the 8-bit data from the slave starting from MSB
12. Acknowledge from the master. On the received byte, the master receiver issues a NACK in place of ACK to signal the end of the data transfer.
13. Send STOP sequence

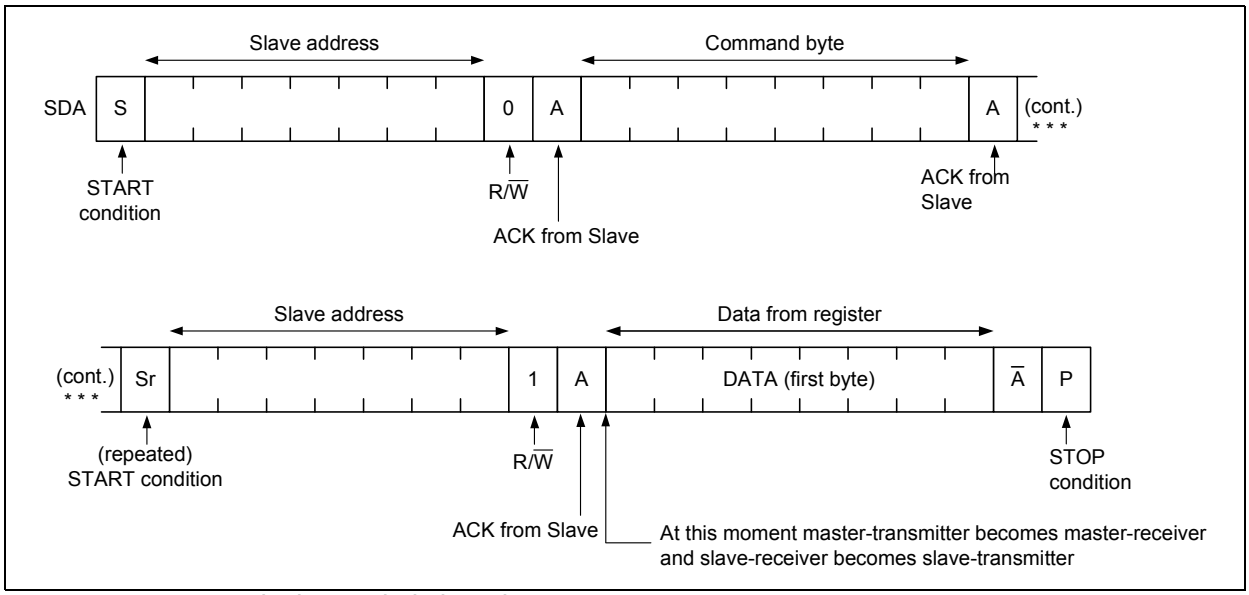

FIGURE 8-5: *Single Read Timing Diagram.*

Note: Attempts to read from a non-existing register location will generate a reject action (NACK) by the MIC24045 after the command byte.

8.5.4 BLOCK READ (AUTO INCREMENT MODE)

This command reads a block of bytes, starting from a designated register that is specified through the command byte. Bit<6> of the command byte indicates the Auto-Increment mode. If this bit is set, the address gets incremented by one automatically and the registers are read in order, starting from the address provided by the command byte.

The Block/Auto-Increment Read command is as follows and it is illustrated in the timing diagram of Figure 8-6.

1. Send START sequence
2. Send 7-bit slave address
3. Send the R/W bit - 0 to indicate a write operation
4. Wait for acknowledge from the slave
5. Send the command byte – address that needs to be read with Bit<6> set high to indicate the Auto-Increment Read mode.
6. Wait for acknowledge from the slave
7. Send START sequence again
8. Send the 7-bit slave address
9. Send R/W bit - 1 to indicate a read operation
10. Wait for acknowledge from the slave
11. Receive the 8-bit data from the slave register indicated in step 5, starting from MSB
12. Acknowledge from the master receiver. On the last byte, master receiver issues a NACK in place of ACK to signal the end of the data transfer.
13. Repeat steps 11 and 12 until last byte
14. STOP sequence is sent

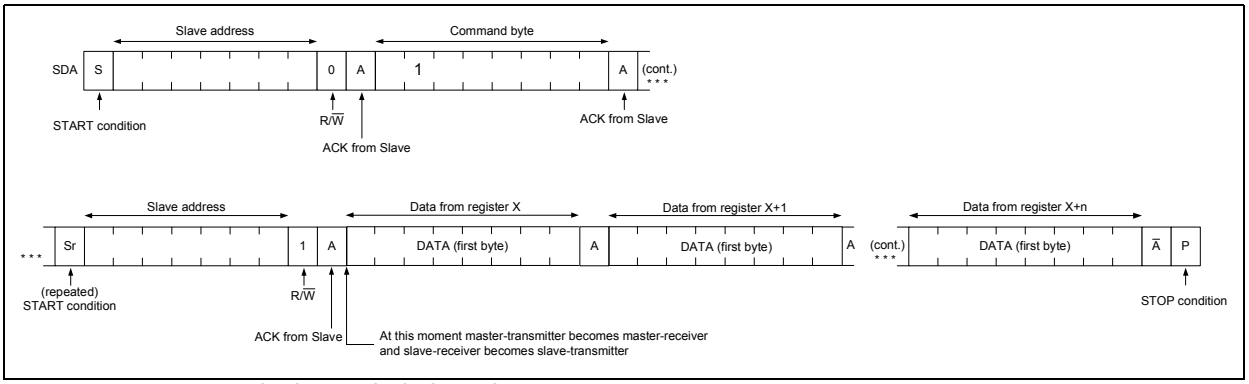

FIGURE 8-6: *Block Read Timing Diagram.*

Note:	If the master is using a non-existing register location in the command byte, a reject (NACK) will be generated by the MIC24045.

In Block Read Auto-Increment mode, the master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

If the master keeps reading beyond the valid user-accessible register locations, the content of internal test registers will be streamed out until location 15 (Fh) is reached. After that, the read operation wraps-around and restarts from register location 0h and so on, until the master stops reading.

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8.5.5 BLOCK WRITE (AUTO-INCREMENT MODE)

This command writes data to the designated register and to all the following registers that are specified through the command byte. Bit<6> of the command byte indicates the Auto-Increment mode. If this bit is set, the address gets incremented by one automatically and the registers are written in order, starting from the address provided by the command byte.

The Block/Auto-Increment Write command is as follows and it is illustrated in the timing diagram of Figure 8-7 below.

1. Send START sequence
2. Send 7-bit slave address
3. Send the R/W bit - 0 to indicate a write operation
4. Wait for acknowledge from the slave
5. Send the command byte – address that needs to be written with Bit<6> set high to indicate the Auto-Increment Write mode.
6. Wait for acknowledge from the slave.
7. Receive the 8-bit data from the master and write it to the slave register indicated in step 5, starting from MSB.
8. Acknowledge from the slave
9. Repeat steps 7 and 8 until the entire data is sent
10. Send STOP sequence

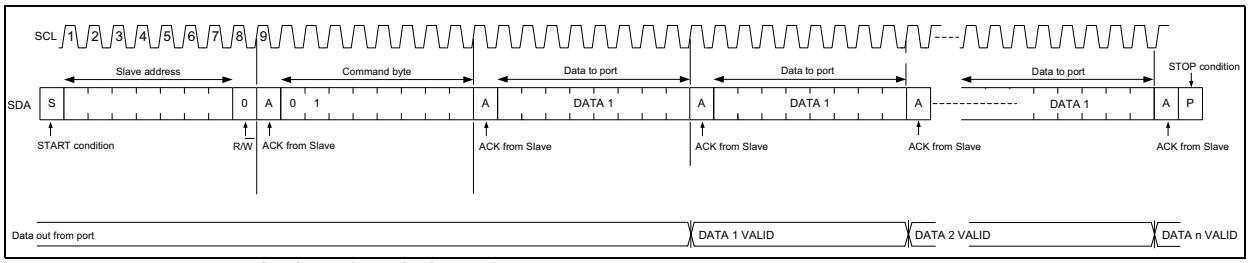


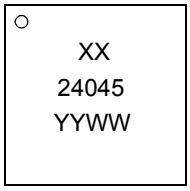
FIGURE 8-7: *Block Write Timing Diagram.*

Note:	If the master is using a non-existing register location, a reject (NACK) will be generated.

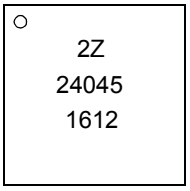
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

20-Pin FQFN (3 x 3 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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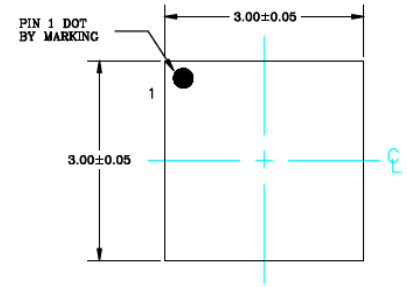
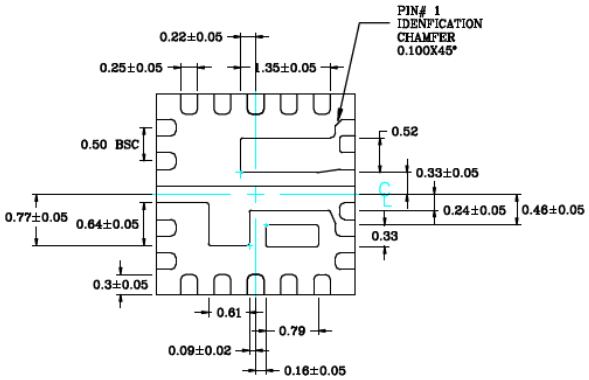
TITLE

20 LEAD FQFN 3x3mm PACKAGE (Flip Chip) OUTLINE & RECOMMENDED LAND PATTERN

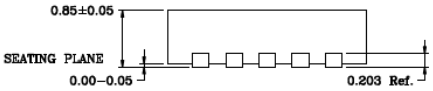
DRAWING #	FQFN33-20LD-PL-1	UNIT	MM
Lead Frame	Cu	Lead Finish	Matte Tin



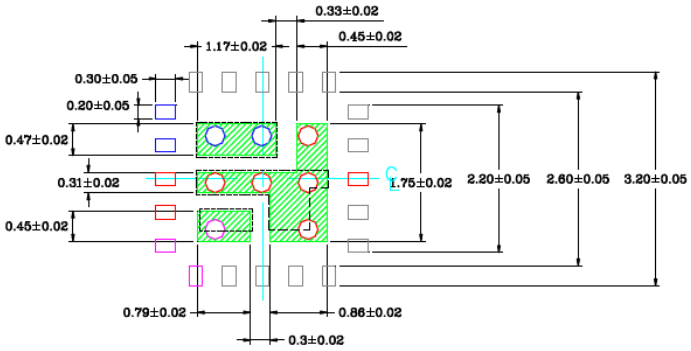
TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



SIDE VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN
NOTE: 4, 5, 6, 7

NOTE:

1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 (TOP) IS LASER MARKED.
4. RED CIRCLES IN LAND PATTERN REPRESENTS THERMAL VIA AND SHOULD BE CONNECTED TO GROUND FOR MAXIMUM PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) ARE RECOMMENDED SOLDER STENCIL OPENNING ON EXPOSED PAD AREA.
6. BLUE COLOR AND PURPLE COLOR PADS REPRESENT DIFFERENT POTENTIALS. DO NOT CONNECT TO GROUND.
7. VIA SIZE is 0.30mm DIAMETER and 0.70mm PITCH.

NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (May 2016)

- Original release of this document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-XX	X	XX
Device	Default settings	Lead Finish	Package Code

Device:	MIC24045: I^2C-programmable, high-efficiency, wide input range, 5A synchronous step-down regulator		
	XX	=	device code for default settings (see Table 6-1)
Lead Finish	Y	=	Pb-Free with Industrial Temperature Grade
Package	FL	=	Flip-chip QFN, 0.85 mm thickness

Examples:

a) MIC24045-2ZYFL: 2Z default settings option, Pb-Free, 20-pin 3 x 3 mm FQFN Package.

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