

Silicon PNP Power Transistors

2SB506

DESCRIPTION

- With TO-3 package
- Wide area of safe operation

APPLICATIONS

- Low frequency power amplification
- Power switching application

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

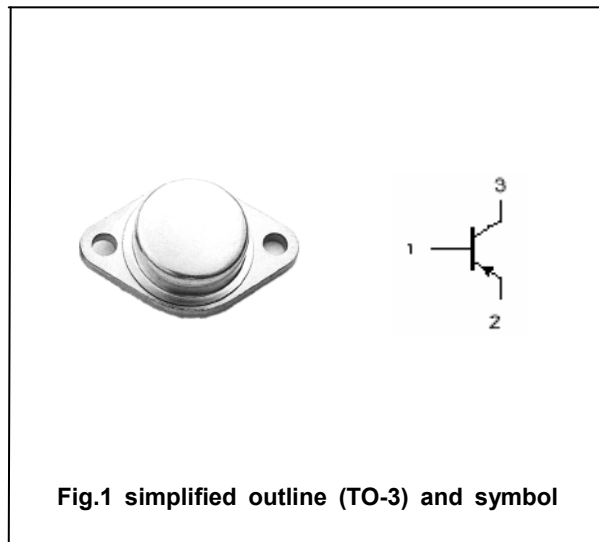


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings($T_a = \square$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-150	V
V_{CEO}	Collector-emitter voltage	Open base	-100	V
V_{EBO}	Emitter-base voltage	Open collector	-7	V
I_C	Collector current		-5	A
P_C	Collector power dissipation	$T_C = 25 \square$	60	W
T_j	Junction temperature		100	\square
T_{stg}	Storage temperature		-55~100	\square

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CHARACTERISTICS

T_j=25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-10mA; I _B =0	-100			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =-1mA; I _C =0	-7			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-5A; I _B =-0.5A			-1.0	V
V _{BEsat}	Base-emitter saturation voltage	I _C =-5A; I _B =-0.5A			-1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =-100V; I _E =0			-0.1	mA
I _{EBO}	Emitter cut-off current	V _{EB} =-7V; I _C =0			-0.1	mA
h _{FE}	DC current gain	I _C =-1A; V _{CE} =-5V	35		200	
f _T	Transition frequency	I _C =-0.3A; V _{CE} =-10V		20		MHz

PACKAGE OUTLINE

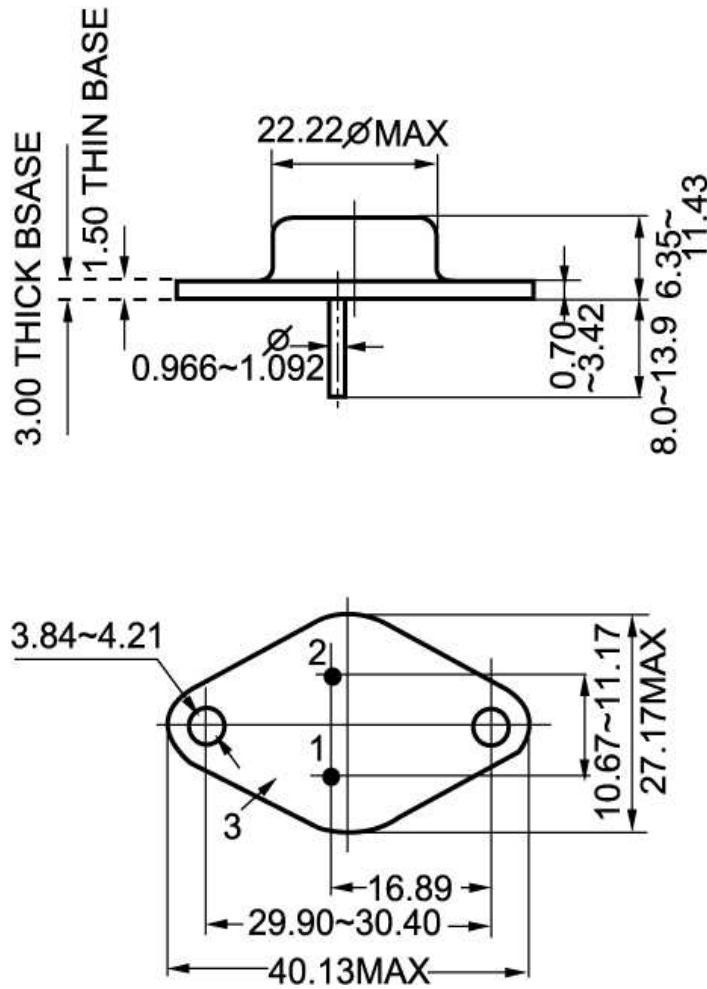


Fig.2 outline dimensions (unindicated tolerance:±0.1mm)