

# 1-Mbit (64 K × 16) Static RAM

## Features

- Temperature ranges
  - Automotive-E: -40 °C to 125 °C
- Pin and function compatible with CY7C10212CV33
- High speed
  - $t_{AA} = 12$  ns (Automotive-E)
- CMOS for optimum speed and power
- Low active power: 325 mW (max)
- Automatic power down when deselected
- Independent control of upper and lower bits
- Available in Pb-free 48-ball FBGA package

## Functional Description

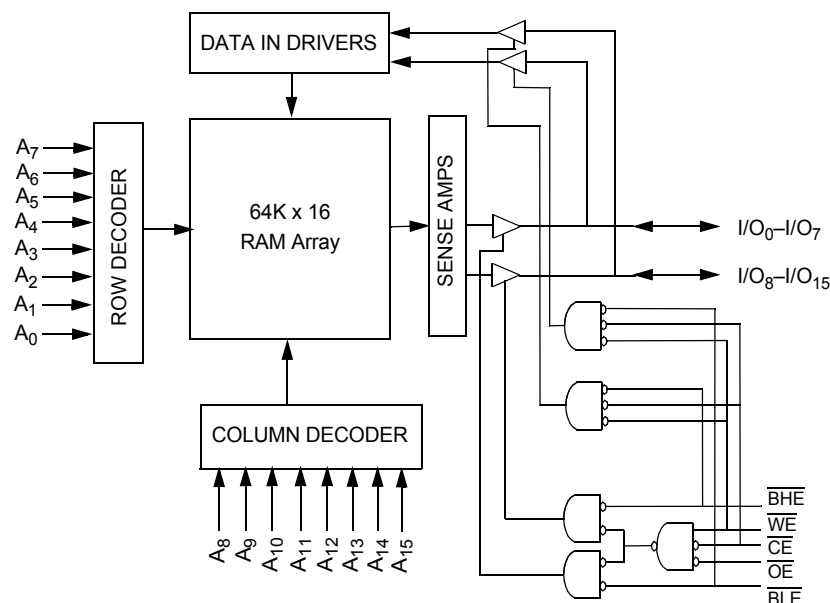
The CY7C10212CV33 is a high performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O<sub>8</sub> to I/O<sub>15</sub>. For more information, see the Truth Table on page 9 for a complete description of Read and Write modes.

The input and output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation ( $\overline{CE}$  LOW and WE LOW).

## Logic Block Diagram



## Contents

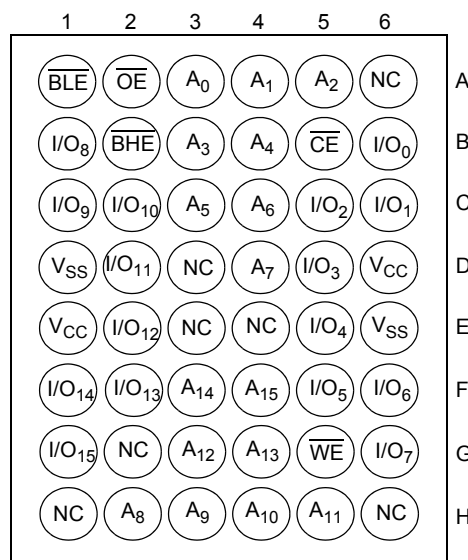
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### Selection Guide

| Description                  | -12 | Unit |
|------------------------------|-----|------|
| Maximum Access Time          | 12  | ns   |
| Maximum Operating Current    | 90  | mA   |
| Maximum CMOS Standby Current | 10  | mA   |

### Pin Configuration

Figure 1. 48-ball FBGA pinout <sup>[1]</sup>



**Note**

1. NC pins are not connected on the die.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

|   |                                   |
|---|-----------------------------------|
| Storage Temperature .....                                   | -65 °C to +150 °C                 |
| Ambient Temperature with Power Applied .....                | -55 °C to +125 °C                 |
| Supply Voltage on V <sub>CC</sub> Relative to GND [2] ..... | -0.3 V to +4.6 V                  |
| DC Voltage Applied to Outputs in High Z State [2] .....     | -0.3 V to V <sub>CC</sub> + 0.3 V |

|   |                                   |
|---|-----------------------------------|
| DC Input Voltage [2] .....                                | -0.3 V to V <sub>CC</sub> + 0.3 V |
| Current into Outputs (LOW) .....                          | 20 mA                             |
| Static Discharge Voltage (MIL-STD-883, Method 3015) ..... | > 2001 V                          |
| Latch Up Current .....                                    | > 200 mA                          |

## Operating Range

| Range        | Ambient Temperature (T <sub>A</sub> ) | V <sub>CC</sub> |
|--------------|---------------------------------------|-----------------|
| Automotive-E | -40 °C to +125 °C                     | 3.3 V ± 10%     |

## Electrical Characteristics

Over the Operating Range

| Parameter        | Description                                   | Test Conditions   | -12  |                       | Unit |
|------------------|---|---|------|-----------------------|------|
|                  |   |   | Min  | Max                   |      |
| V <sub>OH</sub>  | Output HIGH Voltage                           | V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA  | 2.4  | -                     | V    |
| V <sub>OL</sub>  | Output LOW Voltage                            | V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA   | -    | 0.4                   | V    |
| V <sub>IH</sub>  | Input HIGH Voltage                            |   | 2.0  | V <sub>CC</sub> + 0.3 | V    |
| V <sub>IL</sub>  | Input LOW Voltage [2]                         |   | -0.3 | 0.8                   | V    |
| I <sub>IX</sub>  | Input Leakage Current                         | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>  | -12  | +12                   | μA   |
| I/O <sub>Z</sub> | Output Leakage Current                        | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output disabled  | -12  | +12                   | μA   |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current      | V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>  | -    | 90                    | mA   |
| I <sub>SB1</sub> | Automatic CE Power Down Current — TTL Inputs  | Max V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> | -    | 20                    | mA   |
| I <sub>SB2</sub> | Automatic CE Power Down Current — CMOS Inputs | Max V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3$ V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3 V, or V <sub>IN</sub> ≤ 0.3 V, f = 0           | -    | 10                    | mA   |

### Note

2. V<sub>IL(min)</sub> = -2.0 V and V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.5 V for pulse durations of less than 20 ns.

### Capacitance

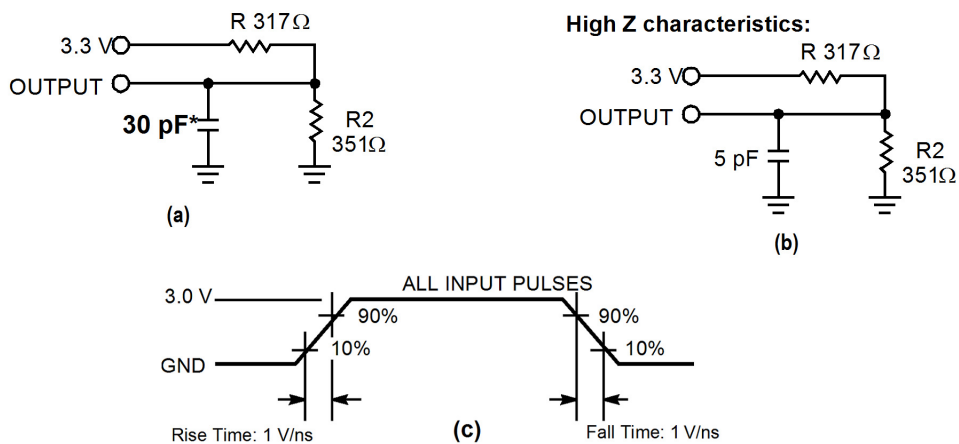
| Parameter <sup>[3]</sup> | Description        | Test Conditions  | Max | Unit |
|--------------------------|--------------------|--|-----|------|
| C <sub>IN</sub>          | Input Capacitance  | T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 3.3 V | 8   | pF   |
| C <sub>OUT</sub>         | Output Capacitance |  | 8   | pF   |

### Thermal Resistance

| Parameter <sup>[3]</sup> | Description                              | Test Conditions   | 48-ball FBGA | Unit |
|--------------------------|--|---|--------------|------|
| Θ <sub>JA</sub>          | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51 | 95.32        | °C/W |
| Θ <sub>JC</sub>          | Thermal resistance (junction to case)    |   | 10.68        | °C/W |

### AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms <sup>[4]</sup>



**Notes**

- 3. Tested initially and after any design or process changes that may affect these parameters.
- 4. Speed is tested using the Thevenin load shown in Figure 2 (a). High Z characteristics are tested using the test load shown in Figure 2 (b).

## Switching Characteristics

Over the Operating Range

| Parameter <sup>[5]</sup>          | Description                                      | -12 |     | Unit    |
|-----------------------------------|--|-----|-----|---------|
|                                   |  | Min | Max |         |
| <b>Read Cycle</b>                 |  |     |     |         |
| $t_{power}^{[6]}$                 | $V_{CC}$ (Typical) to the First Access           | 100 | –   | $\mu$ s |
| $t_{RC}$                          | Read Cycle Time                                  | 12  | –   | ns      |
| $t_{AA}$                          | Address to Data Valid                            | –   | 12  | ns      |
| $t_{OHA}$                         | Data Hold from Address Change                    | 3   | –   | ns      |
| $t_{ACE}$                         | $\overline{CE}$ LOW to Data Valid                | –   | 12  | ns      |
| $t_{DOE}$                         | $\overline{OE}$ LOW to Data Valid                | –   | 6   | ns      |
| $t_{LZOE}$                        | $\overline{OE}$ LOW to Low Z <sup>[7]</sup>      | 0   | –   | ns      |
| $t_{HZOE}$                        | $\overline{OE}$ HIGH to High Z <sup>[7, 8]</sup> | –   | 6   | ns      |
| $t_{LZCE}$                        | $\overline{CE}$ LOW to Low Z <sup>[7]</sup>      | 3   | –   | ns      |
| $t_{HZCE}$                        | $\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup> | –   | 6   | ns      |
| $t_{PU}^{[9]}$                    | $\overline{CE}$ LOW to Power Up                  | 0   | –   | ns      |
| $t_{PD}^{[9]}$                    | $\overline{CE}$ HIGH to Power Down               | –   | 12  | ns      |
| $t_{DBE}$                         | Byte Enable to Data Valid                        | –   | 6   | ns      |
| $t_{LZBE}$                        | Byte Enable to Low Z                             | 0   | –   | ns      |
| $t_{HZBE}$                        | Byte Disable to High Z                           | –   | 6   | ns      |
| <b>Write Cycle<sup>[10]</sup></b> |  |     |     |         |
| $t_{WC}$                          | Write Cycle Time                                 | 12  | –   | ns      |
| $t_{SCE}$                         | $\overline{CE}$ LOW to Write End                 | 9   | –   | ns      |
| $t_{AW}$                          | Address Setup to Write End                       | 9   | –   | ns      |
| $t_{HA}$                          | Address Hold from Write End                      | 0   | –   | ns      |
| $t_{SA}$                          | Address Setup to Write Start                     | 0   | –   | ns      |
| $t_{PWE}$                         | $\overline{WE}$ Pulse Width                      | 8   | –   | ns      |
| $t_{SD}$                          | Data Setup to Write End                          | 6   | –   | ns      |
| $t_{HD}$                          | Data Hold from Write End                         | 0   | –   | ns      |
| $t_{LZWE}$                        | $\overline{WE}$ HIGH to Low Z <sup>[7]</sup>     | 3   | –   | ns      |
| $t_{HZWE}$                        | $\overline{WE}$ LOW to High Z <sup>[7, 8]</sup>  | –   | 6   | ns      |
| $t_{BW}$                          | Byte Enable to End of Write                      | 8   | –   | ns      |

### Notes

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
6.  $t_{POWER}$  gives the minimum amount of time that the power supply is at typical  $V_{CC}$  values until the first memory access is performed.
7. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
8.  $t_{HZOE}$ ,  $t_{HZBE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of [Figure 2 on page 5](#). Transition is measured  $\pm 500$  mV from steady state voltage.
9. This parameter is guaranteed by design and is not tested.
10. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW, and  $\overline{BHE}/\overline{BLE}$  LOW.  $\overline{CE}$ ,  $\overline{WE}$ , and  $\overline{BHE}/\overline{BLE}$  is LOW to initiate a write. The transition of these signals terminate the write. The input data setup and hold timing is referenced to the leading edge of the signal that terminates the write.

### Switching Waveforms

Figure 3. Read Cycle No. 1 (Address Transition Controlled) [11, 12]

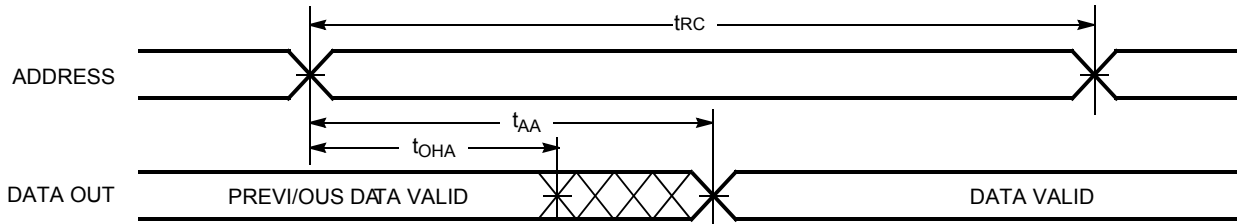
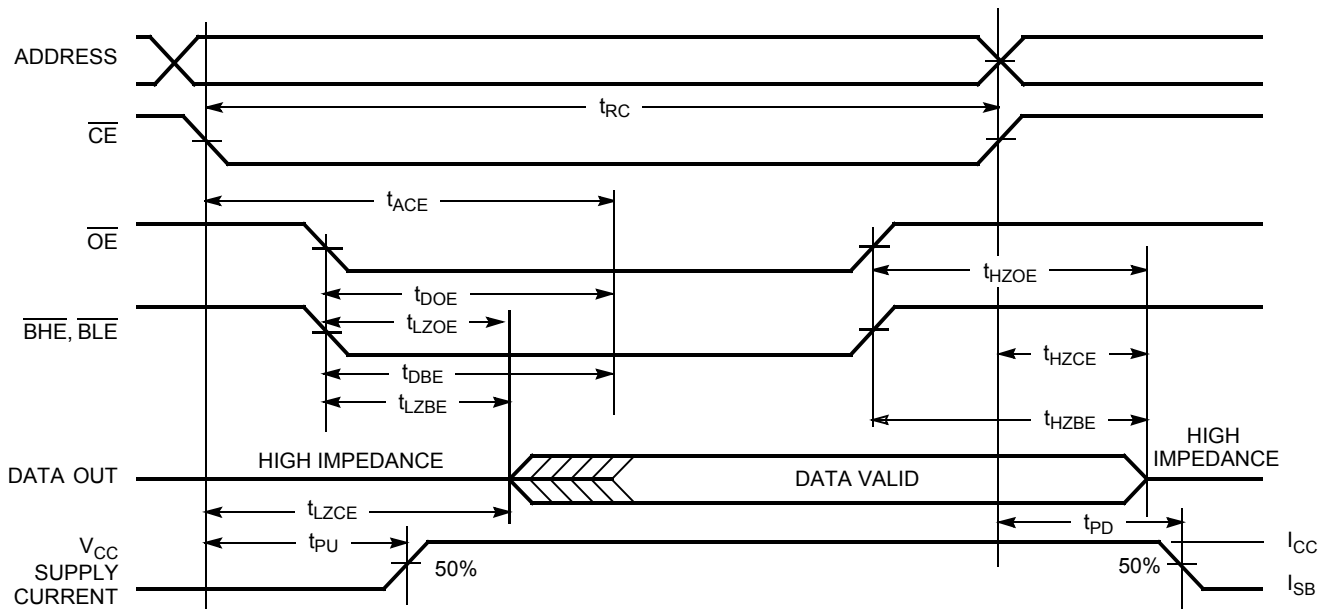


Figure 4. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [12, 13]



**Notes**

- 11. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$ , and/or  $\overline{BLE}$  =  $V_{IL}$ .
- 12.  $\overline{WE}$  is HIGH for read cycle.
- 13. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [14, 15]

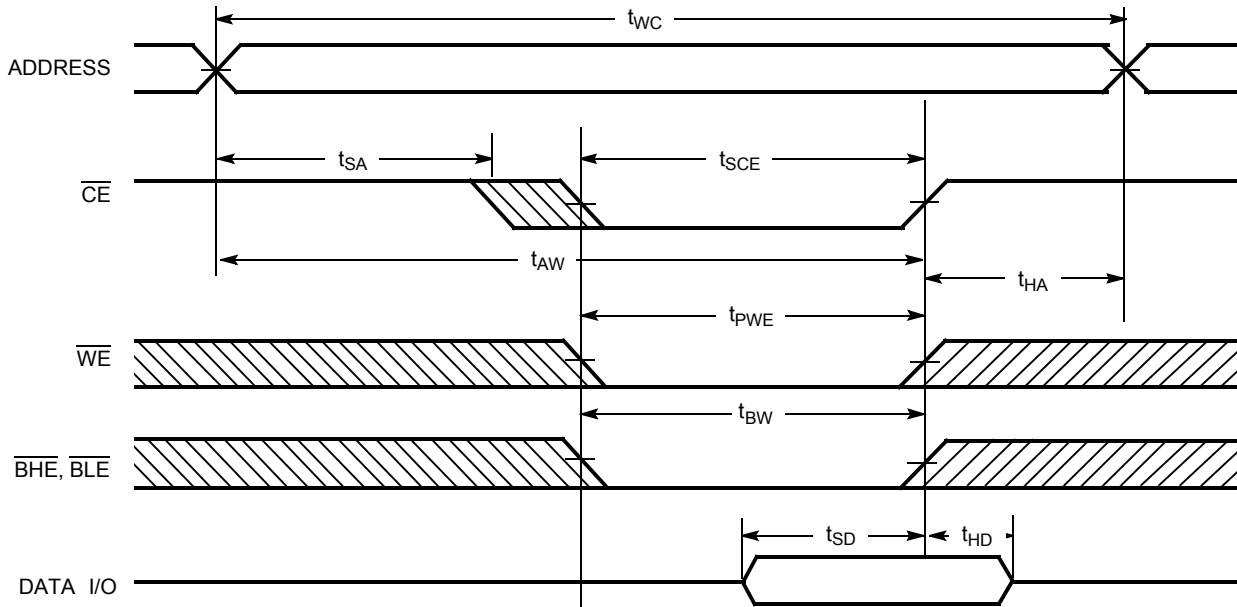
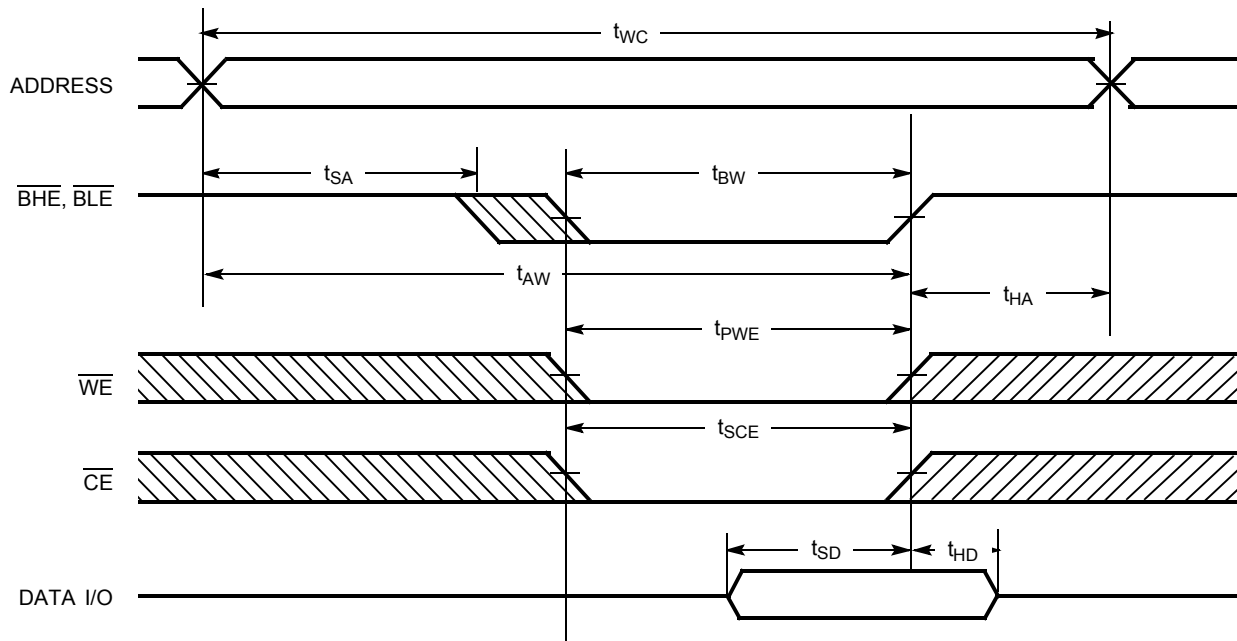


Figure 6. Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)



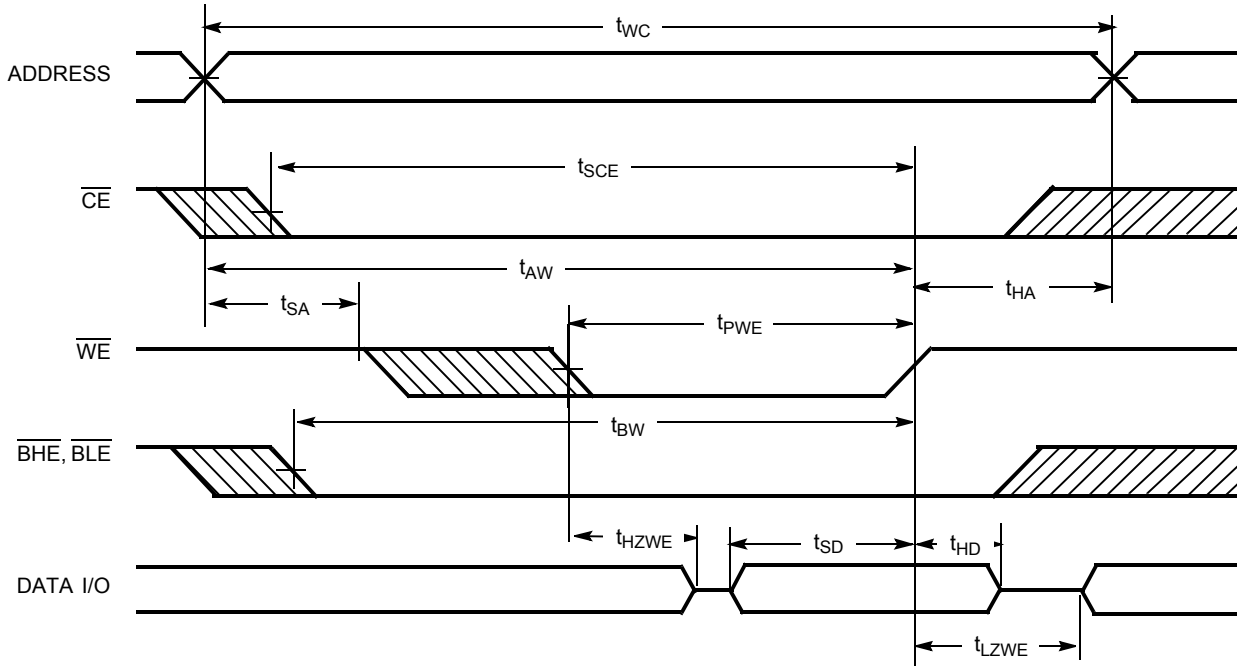
Notes

- 14. Data I/O is high impedance if  $\overline{\text{OE}}$ ,  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .
- 15. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high impedance state.



Switching Waveforms (continued)

Figure 7. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled, LOW)



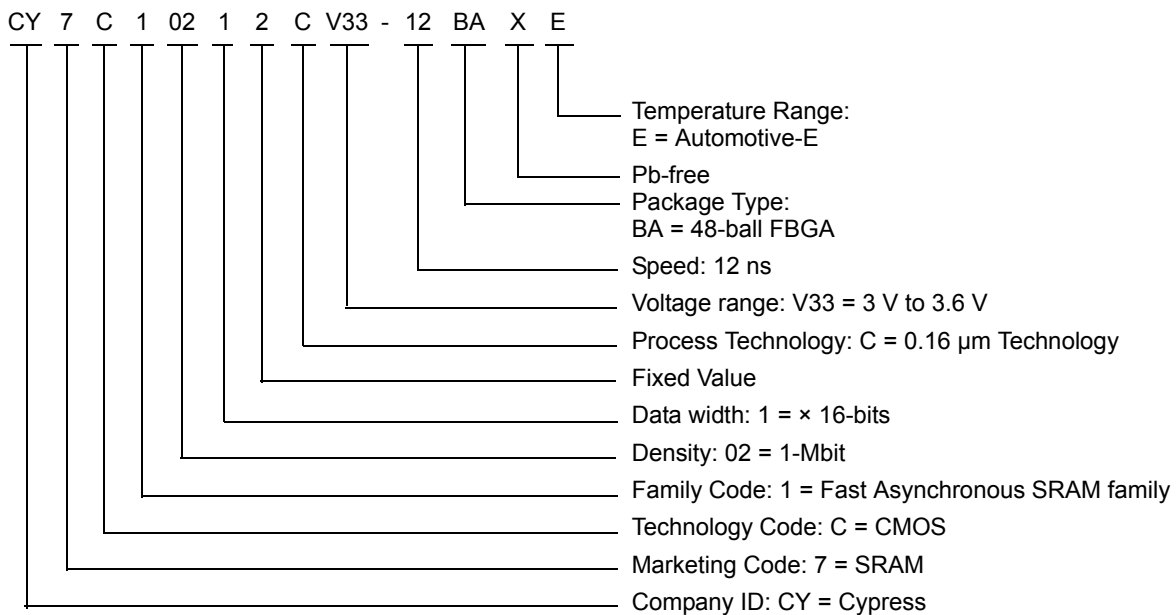
Truth Table

| $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | $\overline{\text{BLE}}$ | $\overline{\text{BHE}}$ | I/O <sub>0</sub> – I/O <sub>7</sub> | I/O <sub>8</sub> – I/O <sub>15</sub> | Mode                       | Power                       |
|------------------------|------------------------|------------------------|-------------------------|-------------------------|-------------------------------------|--------------------------------------|----------------------------|-----------------------------|
| H                      | X                      | X                      | X                       | X                       | High Z                              | High Z                               | Power Down                 | Standby ( $I_{\text{SB}}$ ) |
| L                      | L                      | H                      | L                       | L                       | Data Out                            | Data Out                             | Read – All Bits            | Active ( $I_{\text{CC}}$ )  |
|                        |                        |                        | L                       | H                       | Data Out                            | High Z                               | Read – Lower Bits Only     | Active ( $I_{\text{CC}}$ )  |
|                        |                        |                        | H                       | L                       | High Z                              | Data Out                             | Read – Upper Bits Only     | Active ( $I_{\text{CC}}$ )  |
| L                      | X                      | L                      | L                       | L                       | Data In                             | Data In                              | Write – All Bits           | Active ( $I_{\text{CC}}$ )  |
|                        |                        |                        | L                       | H                       | Data In                             | High Z                               | Write – Lower Bits Only    | Active ( $I_{\text{CC}}$ )  |
|                        |                        |                        | H                       | L                       | High Z                              | Data In                              | Write – Upper Bits Only    | Active ( $I_{\text{CC}}$ )  |
| L                      | H                      | H                      | X                       | X                       | High Z                              | High Z                               | Selected, Outputs Disabled | Active ( $I_{\text{CC}}$ )  |
| L                      | X                      | X                      | H                       | H                       | High Z                              | High Z                               | Selected, Outputs Disabled | Active ( $I_{\text{CC}}$ )  |

### Ordering Information

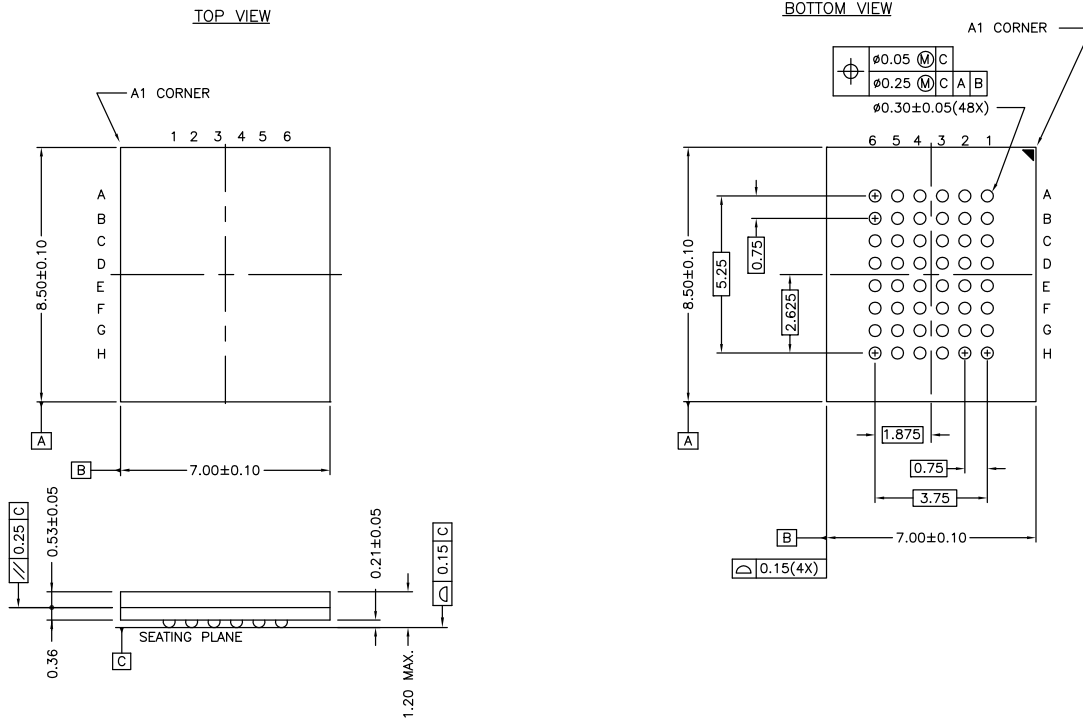
| Speed (ns) | Ordering Code        | Package Diagram | Package Type           | Operating Range |
|------------|----------------------|-----------------|------------------------|-----------------|
| 12         | CY7C10212CV33-12BAXE | 51-85106        | 48-ball FBGA (Pb-free) | Automotive-E    |

### Ordering Code Definitions



Package Diagrams

Figure 8. 48-ball FBGA (7 × 8.5 × 1.2 mm) BA48A Package Outline, 51-85106



51-85106 \*G

**Acronyms**

| Acronym         | Description                             |
|-----------------|---|
| BGA             | Ball Grid Array                         |
| $\overline{CE}$ | Chip Enable                             |
| CMOS            | Complementary Metal Oxide Semiconductor |
| FBGA            | Fine-Pitch Ball Grid Array              |
| I/O             | Input/Output                            |
| $\overline{OE}$ | Output Enable                           |
| SRAM            | Static Random Access Memory             |
| TQFP            | Thin Quad Flat Pack                     |
| TTL             | Transistor-Transistor Logic             |
| $\overline{WE}$ | Write Enable                            |

**Document Conventions**

**Units of Measure**

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| μA     | microampere     |
| μs     | microsecond     |
| mA     | milliampere     |
| mm     | millimeter      |
| mW     | milliwatt       |
| MHz    | megahertz       |
| ns     | nanosecond      |
| %      | percent         |
| pF     | picofarad       |
| V      | volt            |
| W      | watt            |

## Document History Page

| Document Title: CY7C10212CV33, 1-Mbit (64 K × 16) Static RAM<br>Document Number: 001-82303 |         |                 |                 |   |
|--|---------|-----------------|-----------------|---|
| Rev.   | ECN No. | Submission Date | Orig. of Change | Description of Change                                 |
| **   | 3723052 | 10/29/2012      | TAVA            | New data sheet.                                       |
| *A   | 4178071 | 10/30/2013      | VINI            | Updated in new template.<br>Completing Sunset Review. |

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