

## Silicon Carbide Junction Transistor/Schottky Diode Co-Pack

$V_{DS}$	=	1200 V
$R_{DS(ON)}$	=	20 mΩ
$I_D$ (@ 25°C)	=	80 A
$I_D$ (@ 115°C)	=	50 A
$h_{FE}$ (@ 25°C)	=	100

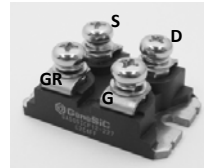
### Features

- 175 °C Maximum Operating Temperature
- Gate Oxide Free SiC Switch
- Optional Gate Return Pin
- Exceptional Safe Operating Area
- Integrated SiC Schottky Rectifier
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Coefficient of  $R_{DS,ON}$
- Suitable for Connecting an Anti-parallel Diode

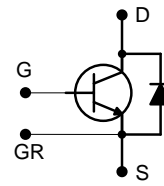
### Advantages

- Compatible with Si MOSFET/IGBT Gate Drive ICs
- > 20 μs Short-Circuit Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth
- Reduced cooling requirements
- Reduced system size

### Package



**Isolated Baseplate SOT-227**



Pin D - Drain  
Pin S - Source  
Pin GR - Gate Return  
Pin G - Gate

Please note: The Source and Gate Return pins are not exchangeable. Their exchange might lead to malfunction.

### Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

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### Section I: Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit	Notes
<b>SiC Junction Transistor</b>					
Drain – Source Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$	1200	V	
Continuous Drain Current	$I_D$	$T_C = 25^\circ\text{C}$	80	A	Fig. 17
Continuous Drain Current	$I_D$	$T_C = 115^\circ\text{C}$	50	A	Fig. 17
Continuous Gate Current	$I_G$		3.5	A	
Continuous Gate Return Current	$I_{GR}$		3.5	A	
Turn-Off Safe Operating Area	RBSOA	$T_{VJ} = 175^\circ\text{C}$ , Clamped Inductive Load	$I_{D,max} = 50$ @ $V_{DS} \leq V_{DSmax}$	A	Fig. 19
Short Circuit Safe Operating Area	SCSOA	$T_{VJ} = 175^\circ\text{C}$ , $I_G = 1\text{ A}$ , $V_{DS} = 800\text{ V}$ , Non Repetitive	>20	μs	
Reverse Gate – Source Voltage	$V_{SG}$		30	V	
Reverse Drain – Source Voltage	$V_{SD}$		25	V	
Power Dissipation	$P_{tot}$	$T_C = 25^\circ\text{C} / 115^\circ\text{C}$ , $t_p > 100\text{ ms}$	265 / 106	W	Fig. 16
Operating and storage temperature	$T_{stg}$		-55 to 175	°C	

Parameter	Symbol	Conditions	Value	Unit	Notes
<b>Free-Wheeling SiC Diode</b>					
Repetitive peak reverse voltage	$V_{RRM}$		1200	V	
Continuous forward current	$I_F$	$T_C \leq 115^\circ\text{C}$	50	A	
RMS forward current	$I_{F(RMS)}$	$T_C \leq 115^\circ\text{C}$	87	A	
Surge non-repetitive forward current, Half Sine Wave	$I_{FSM}$	$T_C = 25^\circ\text{C}, t_p = 10\text{ ms}$	350	A	
		$T_C = 115^\circ\text{C}, t_p = 10\text{ ms}$	313	A	
Non-repetitive peak forward current	$I_{F,max}$	$T_C = 25^\circ\text{C}, t_p = 10\ \mu\text{s}$	1625	A	
$I^2t$ value	$\int I^2 dt$	$T_C = 25^\circ\text{C}, t_p = 10\text{ ms}$	450	$\text{A}^2\text{s}$	
		$T_C = 115^\circ\text{C}, t_p = 10\text{ ms}$	300	$\text{A}^2\text{s}$	

**Thermal Characteristics**

Thermal resistance, junction - case	$R_{thJC}$	SiC Junction Transistor	0.57	$^\circ\text{C/W}$	Fig. 20
Thermal resistance, junction - case	$R_{thJC}$	SiC Diode	0.53	$^\circ\text{C/W}$	Fig. 21

**Section II: Static Electrical Characteristics**

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		
<b>A: On State</b>							
Drain – Source On Resistance	$R_{DS(ON)}$	$I_D = 50\text{ A}, T_J = 25^\circ\text{C}$		20		m $\Omega$	Fig. 5
		$I_D = 50\text{ A}, T_J = 150^\circ\text{C}$		36			
		$I_D = 50\text{ A}, T_J = 175^\circ\text{C}$		42			
Gate – Source Saturation Voltage	$V_{GS,SAT}$	$I_D = 50\text{ A}, I_D/I_G = 40, T_J = 25^\circ\text{C}$		3.42		V	Fig. 7
		$I_D = 50\text{ A}, I_D/I_G = 30, T_J = 175^\circ\text{C}$		3.23			
DC Current Gain	$h_{FE}$	$V_{DS} = 8\text{ V}, I_D = 50\text{ A}, T_J = 25^\circ\text{C}$		100		–	Fig. 4
		$V_{DS} = 8\text{ V}, I_D = 50\text{ A}, T_J = 125^\circ\text{C}$		65			
		$V_{DS} = 8\text{ V}, I_D = 50\text{ A}, T_J = 175^\circ\text{C}$		58			
FWD forward voltage	$V_F$	$I_F = 50\text{ A}, T_J = 25^\circ\text{C}$		1.4	1.8	V	
		$I_F = 50\text{ A}, T_J = 175^\circ\text{C}$		2.1	3.0		
<b>B: Off State</b>							
Drain Leakage Current	$I_{DSS}$	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$		100		$\mu\text{A}$	Fig. 8
		$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 150^\circ\text{C}$		200			
		$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 175^\circ\text{C}$		500			
Gate Leakage Current	$I_{SG}$	$V_{SG} = 20\text{ V}, T_J = 25^\circ\text{C}$		20		nA	

**Section III: Dynamic Electrical Characteristics**

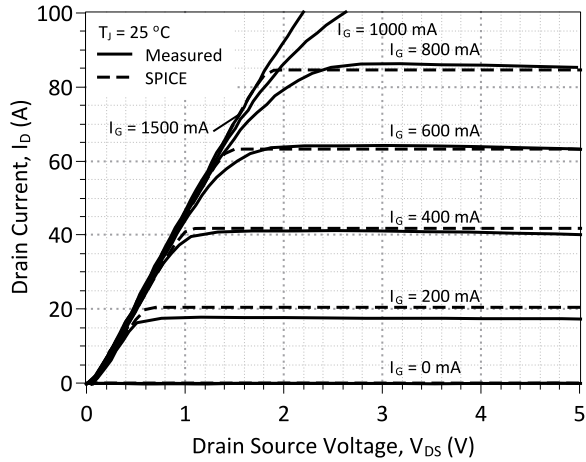
Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		
<b>A: Capacitance and Gate Charge</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V}, f = 1\text{ MHz}$		7770		pF	Fig. 9
Reverse Transfer/Output Capacitance	$C_{rss}/C_{oss}$	$V_{DS} = 1\text{ V}, f = 1\text{ MHz}$		3370		pF	Fig. 9
		$V_{DS} = 400\text{ V}, f = 1\text{ MHz}$		335			
		$V_{DS} = 800\text{ V}, f = 1\text{ MHz}$		250			
Total Output Capacitance Charge	$Q_{oss}$	$V_R = 400\text{ V}$		230		nC	
		$V_R = 800\text{ V}$		345			
Output Capacitance Stored Energy	$E_{OSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V}, f = 1\text{ MHz}$		100		$\mu\text{J}$	Fig. 10
Effective Output Capacitance, time related	$C_{oss,tr}$	$I_D = \text{constant}, V_{GS} = 0\text{ V}, V_{DS} = 0\dots 800\text{ V}$		430		pF	
Effective Output Capacitance, energy related	$C_{oss,er}$	$V_{GS} = 0\text{ V}, V_{DS} = 0\dots 800\text{ V}$		315		pF	
Gate-Source Charge	$Q_{GS}$	$V_{GS} = -5\dots 3\text{ V}$		65		nC	
Gate-Drain Charge	$Q_{GD}$	$V_{GS} = 0\text{ V}, V_{DS} = 0\dots 800\text{ V}$		345		nC	
Gate Charge - Total	$Q_G$			410		nC	

Parameter	Symbol	Conditions	Value			Unit	Notes	
			Min.	Typical	Max.			
<b>B: SJT Switching<sup>1</sup></b>								
Internal Gate Resistance – ON	$R_{G(INT-ON)}$	$V_{GS} > 2.5 \text{ V}, V_{DS} = 0 \text{ V}, T_J = 175 \text{ }^\circ\text{C}$		50		m $\Omega$		
Turn On Delay Time	$t_{d(on)}$	$T_J = 25 \text{ }^\circ\text{C}, V_{DS} = 800 \text{ V}, I_D = 50 \text{ A},$ Resistive Load Refer to Section V for additional driving information.		10		ns		
Fall Time, $V_{DS}$	$t_f$			35		ns	Fig. 11, 13	
Turn Off Delay Time	$t_{d(off)}$			35		ns		
Rise Time, $V_{DS}$	$t_r$			20		ns	Fig. 12, 14	
Turn On Delay Time	$t_{d(on)}$			10		ns		
Fall Time, $V_{DS}$	$t_f$	$T_J = 175 \text{ }^\circ\text{C}, V_{DS} = 800 \text{ V}, I_D = 50 \text{ A},$ Resistive Load		35		ns	Fig. 11	
Turn Off Delay Time	$t_{d(off)}$			65		ns		
Rise Time, $V_{DS}$	$t_r$			15		ns	Fig. 12	
Turn-On Energy Per Pulse	$E_{on}$		$T_J = 25 \text{ }^\circ\text{C}, V_{DS} = 800 \text{ V}, I_D = 50 \text{ A},$ Inductive Load Refer to Section V.		1450		$\mu\text{J}$	Fig. 11, 13
Turn-Off Energy Per Pulse	$E_{off}$				400		$\mu\text{J}$	Fig. 12, 14
Total Switching Energy	$E_{tot}$			1850		$\mu\text{J}$		
Turn-On Energy Per Pulse	$E_{on}$	$T_J = 175 \text{ }^\circ\text{C}, V_{DS} = 800 \text{ V}, I_D = 50 \text{ A},$ Inductive Load			1410		$\mu\text{J}$	Fig. 11
Turn-Off Energy Per Pulse	$E_{off}$				400		$\mu\text{J}$	Fig. 12
Total Switching Energy	$E_{tot}$			1810		$\mu\text{J}$		

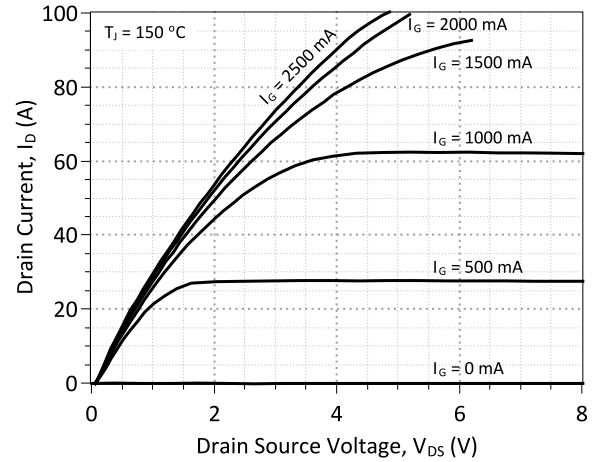
<sup>1</sup> – All times are relative to the Drain-Source Voltage  $V_{DS}$

**Section IV: Figures**

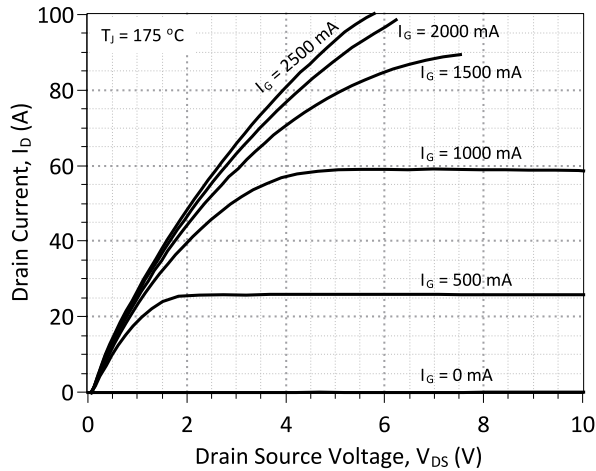
**A: Static Characteristics**



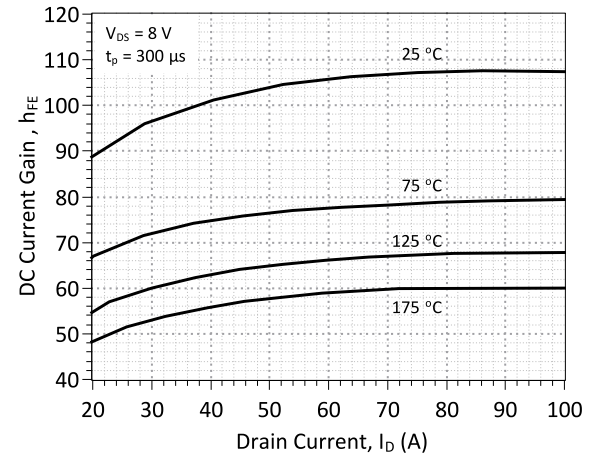
**Figure 1: Typical Output Characteristics at 25 °C**



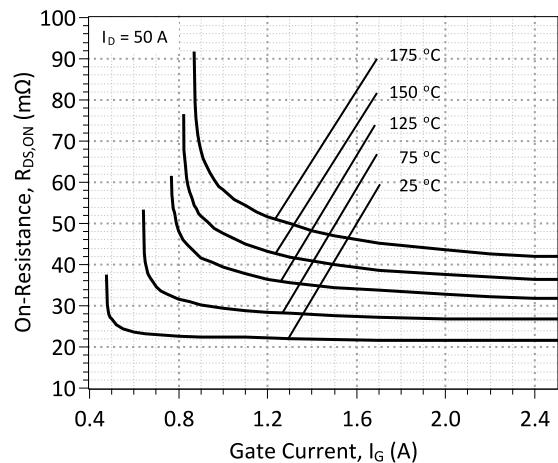
**Figure 2: Typical Output Characteristics at 150 °C**



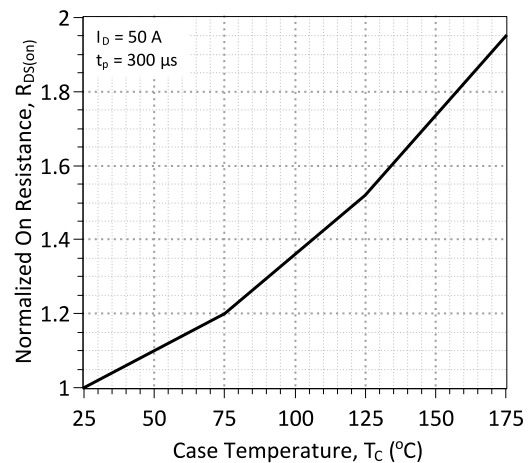
**Figure 3: Typical Output Characteristics at 175 °C**



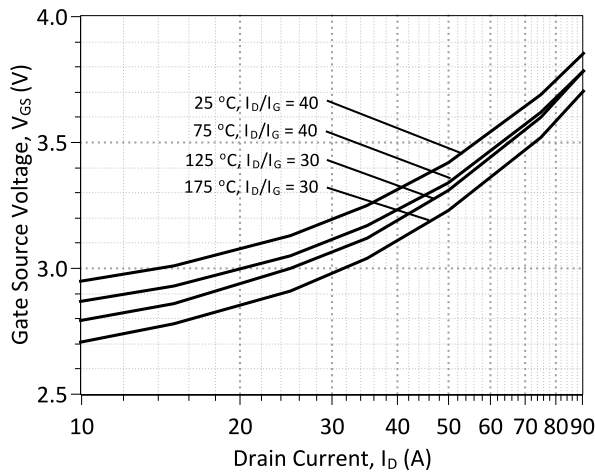
**Figure 4: DC Current Gain vs. Drain Current**



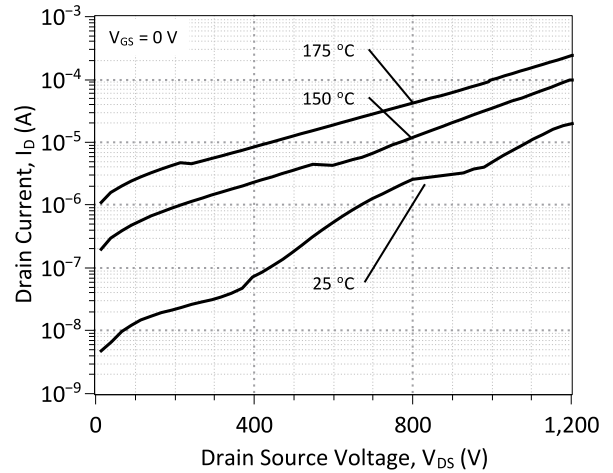
**Figure 5: On-Resistance vs. Gate Current**



**Figure 6: Normalized On-Resistance vs. Temperature**

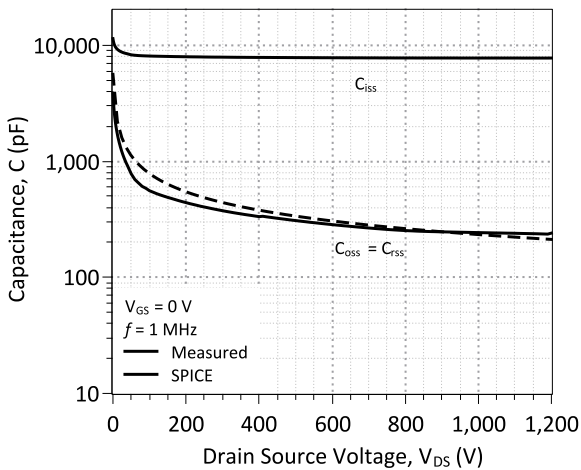


**Figure 7: Typical Gate – Source Saturation Voltage**

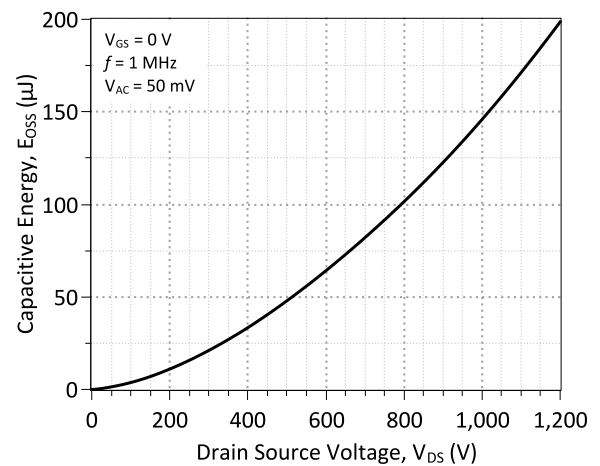


**Figure 8: Typical Blocking Characteristics**

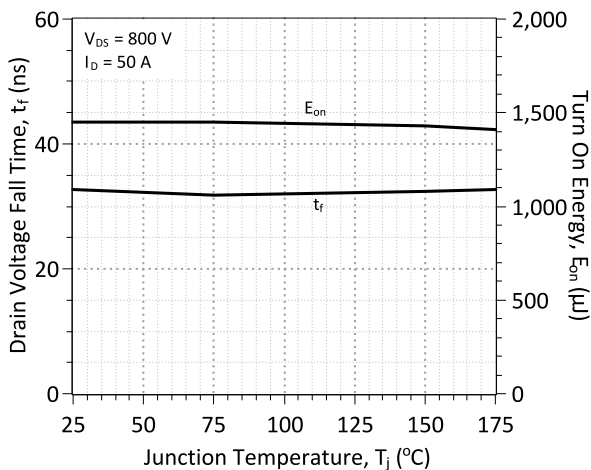
**B: Dynamic Characteristics**



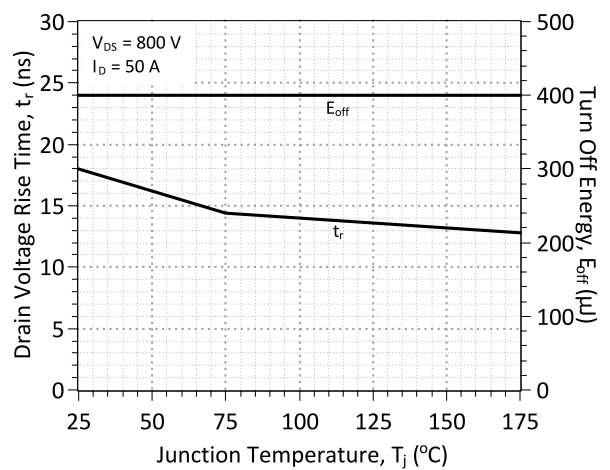
**Figure 9: Input, Output, and Reverse Transfer Capacitance**



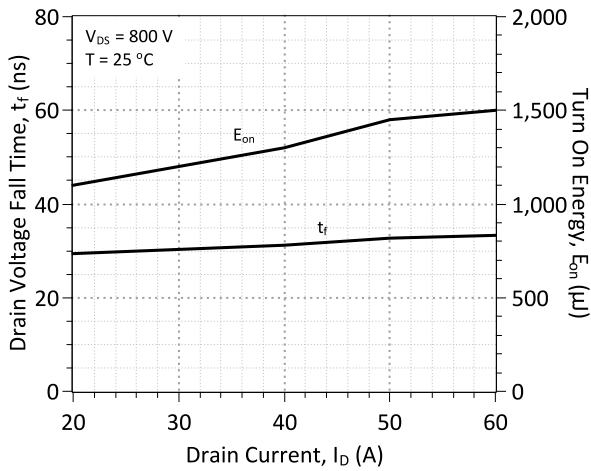
**Figure 10: Energy Stored in Output Capacitance**



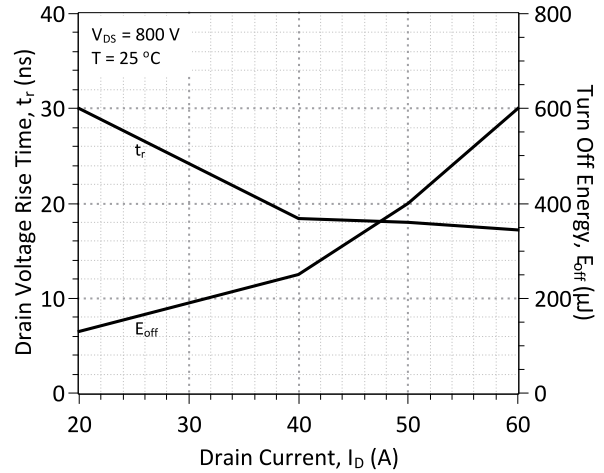
**Figure 11: Typical Switching Times and Turn On Energy Losses vs. Temperature**



**Figure 12: Typical Switching Times and Turn Off Energy Losses vs. Temperature**

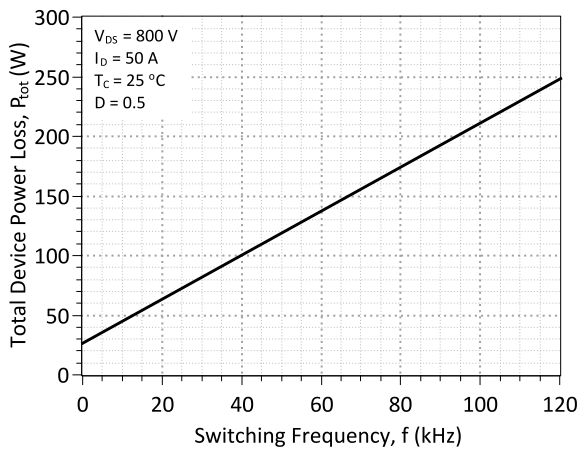


**Figure 13: Typical Switching Times and Turn On Energy Losses vs. Drain Current**

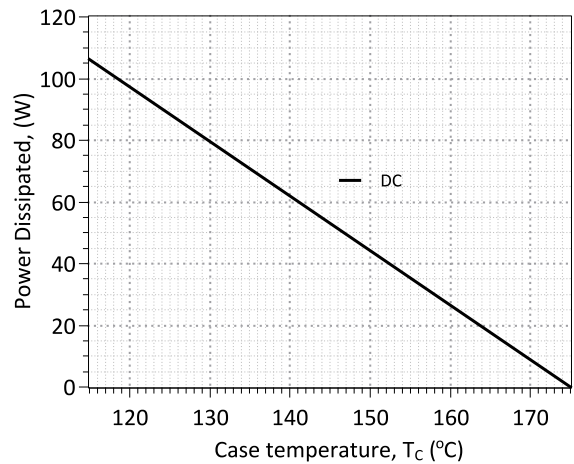


**Figure 14: Typical Switching Times and Turn Off Energy Losses vs. Drain Current**

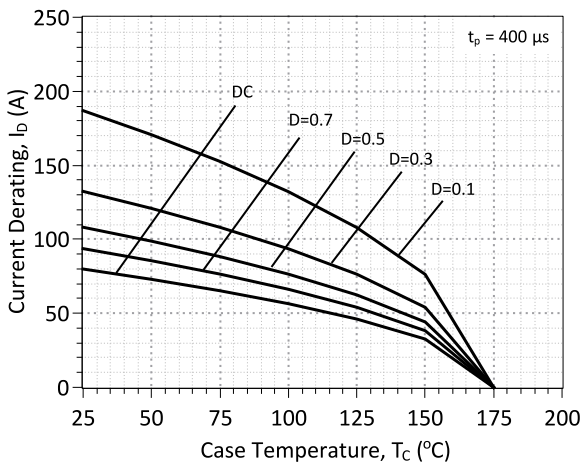
**C: Current and Power Derating**



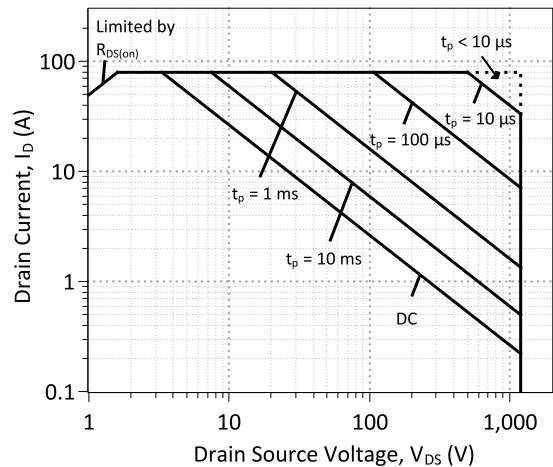
**Figure 15: Typical Hard Switched Device Power Loss vs. Switching Frequency<sup>2</sup>**



**Figure 16: Power Derating Curve**

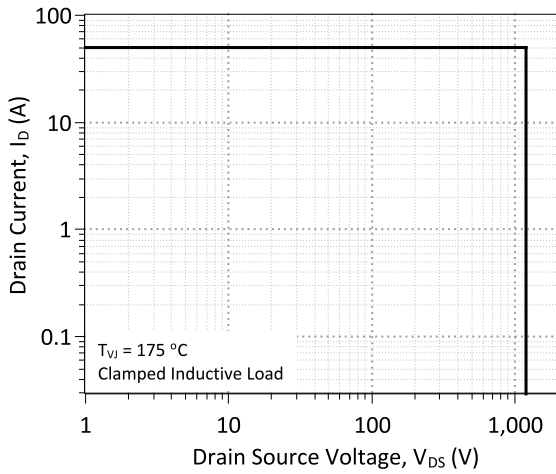


**Figure 17: Drain Current Derating vs. Temperature**

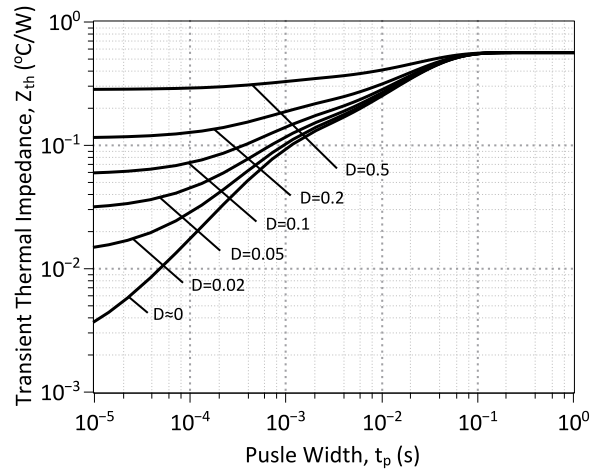


**Figure 18: Forward Bias Safe Operating Area at  $T_c = 25$  °C**

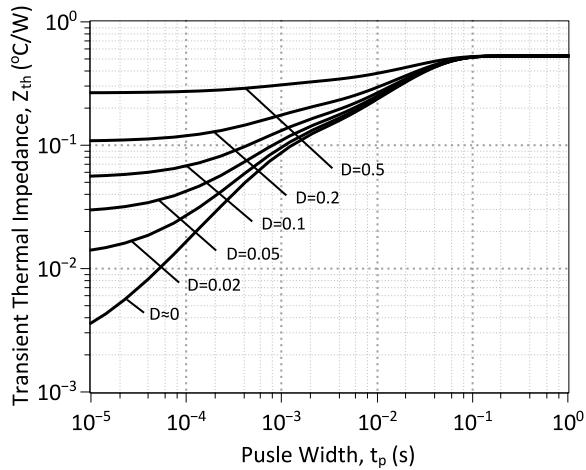
<sup>2</sup> – Representative values based on device conduction and switching loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.



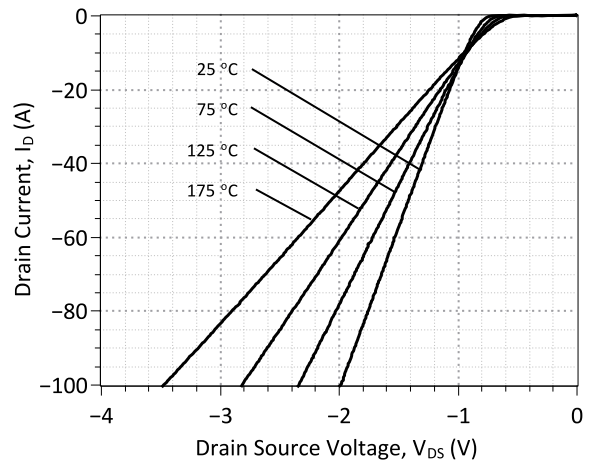
**Figure 19: Turn-Off Safe Operating Area**



**Figure 20: SJT Transient Thermal Impedance**



**Figure 21: FWD Transient Thermal Impedance**



**Figure 22: Typical FWD Forward Characteristics**

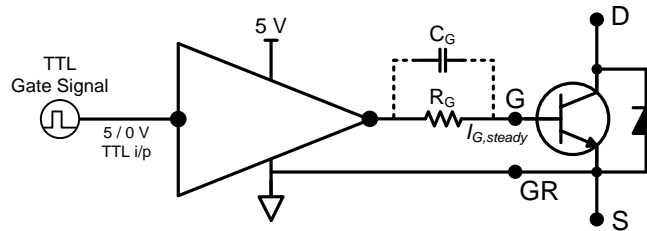
**Section V: Driving the GA50SICP12-227**

Drive Topology	Gate Drive Power Consumption	Switching Frequency	Application Emphasis	Availability
TTL Logic	High	Low	Wide Temperature Range	Coming Soon
Constant Current	Medium	Medium	Wide Temperature Range	Coming Soon
High Speed – Boost Capacitor	Medium	High	Fast Switching	Production
High Speed – Boost Inductor	Low	High	Ultra Fast Switching	Coming Soon
Proportional	Lowest	High	Wide Drain Current Range	Coming Soon
Pulsed Power	Medium	N/A	Pulse Power	Coming Soon

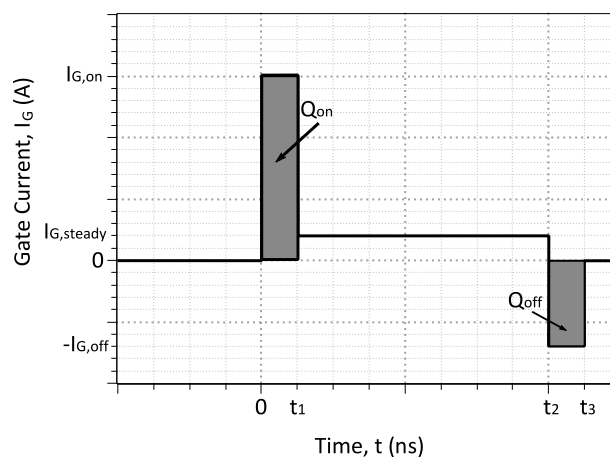
**A: Static TTL Logic Driving**

The GA50SICP12-227 may be driven with direct (5 V) TTL logic and current amplification. The amplified current level of the supply must meet or exceed the steady state gate current ( $I_{G,steady}$ ) required to operate the GA50SICP12-227. Minimum  $I_{G,steady}$  is dependent on the anticipated drain current  $I_D$  through the SJT and the DC current gain  $h_{FE}$ , it may be calculated from the following equation. An accurate value of the  $h_{FE}$  may be read from Figure 4. An optional resistor  $R_G$  may be used in series with the gate pin to trim  $I_{G,steady}$ , also an optional capacitor  $C_G$  may be added in parallel with  $R_G$  to facilitate faster SJT switching if desired, further details on these options are given in the following section.

$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$


**Figure 23: TTL Gate Drive Schematic**
**B: High Speed Driving**

The SJT is a current controlled transistor which requires a positive gate current for turn-on and to remain in on-state. An idealized gate current waveform for ultra-fast switching of the SJT while maintaining low gate drive losses is shown in Figure 24, it features a positive current peak during turn-on, a negative current peak during turn-off, and continuous gate current during on-state.


**Figure 24: An idealized gate current waveform for fast switching of an SJT.**

An SJT is rapidly switched from its blocking state to on-state when the necessary gate charge,  $Q_G$ , for turn-on is supplied by a burst of high gate current,  $I_{G,on}$ , until the SJT gate-source capacitance,  $C_{GS}$ , and gate-drain capacitance,  $C_{GD}$ , are fully charged.

$$Q_{on} = I_{G,on} * t_1$$

$$Q_{on} \geq Q_{gs} + Q_{gd}$$



Ideally,  $I_{G, on}$  should terminate when the drain voltage falls to its on-state value in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the  $I_{G, on}$  pulse is affected by the parasitic inductances,  $L_{par}$  in the device package and drive circuit. A voltage developed across the parasitic inductance in the source path,  $L_s$ , can de-bias the gate-source junction, when high drain currents begin to flow through the device. The voltage applied to the gate pin should be maintained high enough, above the  $V_{GS, sat}$  (see Figure 7) level to counter these effects.

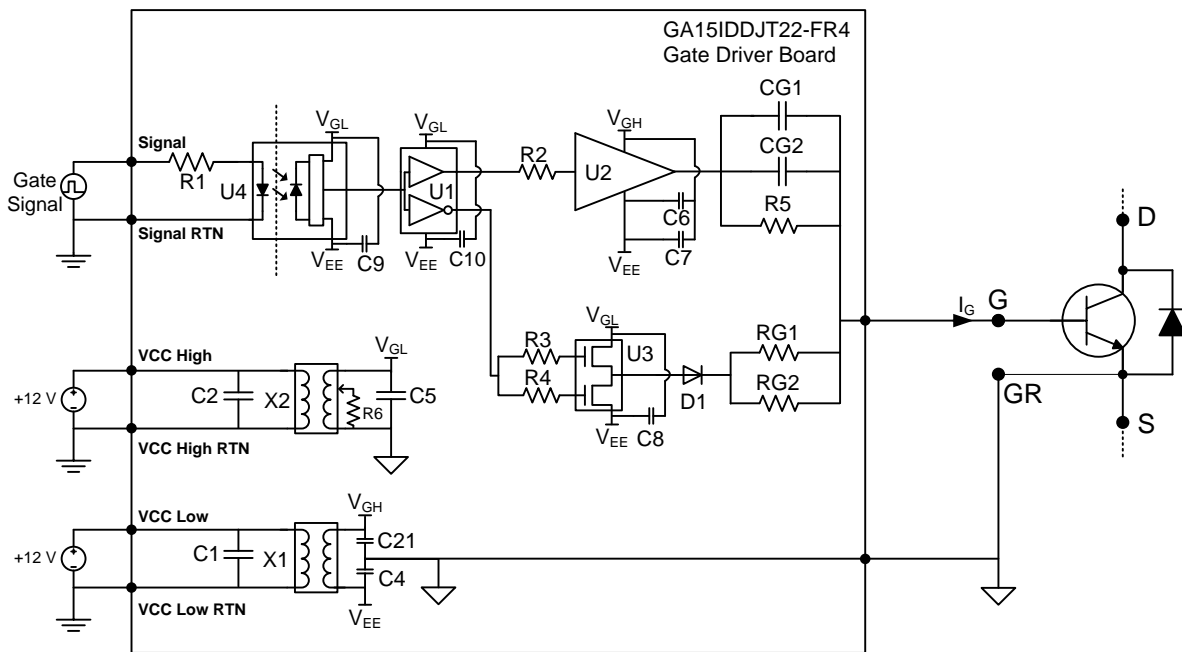
A high negative peak current,  $-I_{G, off}$  is recommended at the start of the turn-off transition, in order to rapidly sweep out the injected carriers from the gate, and achieve rapid turn-off. Turn off can be achieved with  $V_{GS} = 0$  V, however a negative gate voltage  $V_{GS}$  may be used in order to speed up the turn-off transition.

### Gate Return Pin

The optional gate return (GR) pin allows for a reduction of source path inductive and resistive coupling in the gate driver connection to the GA50SICP12-227. Drain currents through the source pin during transient and steady state operation induce an undesirable source voltage in all power transistors due to unavoidable source pin inductance and resistance. This voltage can negatively affect gate driving performance, however the gate return pin allows for decoupling from these source current path effects which results in faster switching and higher efficiency gate driving.

#### B:1: High Speed, Low Loss Drive with Boost Capacitor, GA15IDDJT22-FR4

The GA50SICP12-227 may be driven using a High Speed, Low Loss Drive with Boost Capacitor topology in which multiple voltage levels, a gate resistor, and a gate capacitor are used to provide fast switching current peaks at turn-on and turn-off and a continuous gate current while in on-state. An evaluation gate drive board (GA15IDDJT22-FR4) utilizing this topology is commercially available low-side driving, its datasheet provides additional details.



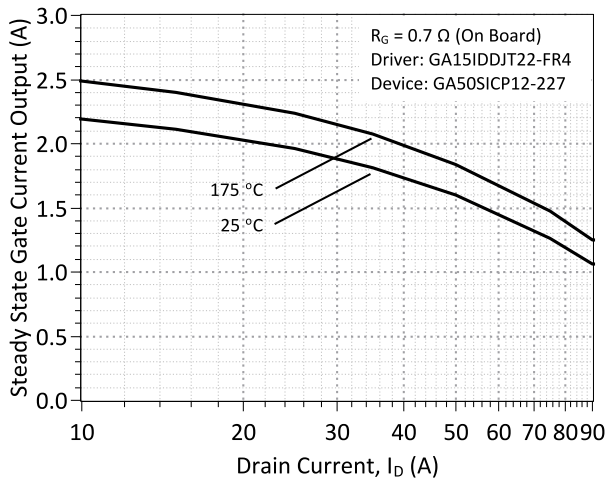
**Figure 25: Topology of the GA15IDDJT22-FR4 Two Voltage Source gate driver.**

The GA15IDDJT22-FR4 evaluation board comes equipped with two on board gate drive resistors (RG1, RG2) pre-installed for an effective gate resistance<sup>3</sup> of  $R_G = 0.7 \Omega$ . It may be necessary for the user to reduce RG1 and/or RG2 under high drain current conditions for safe operation of the GA50SICP12-227. The steady state current supplied to the gate pin of the GA50SICP12-227 with on-board  $R_G = 0.7 \Omega$ , is shown in Figure 26. The maximum allowable safe value of  $R_G$  for the user's required drain current can be read from Figure 27.

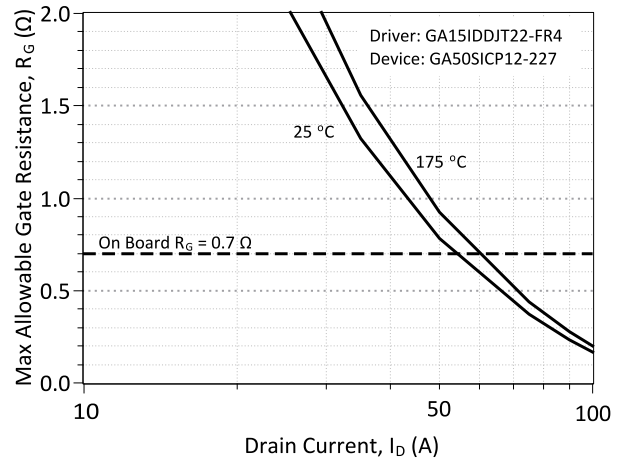
**For the GA50SICP12-227,  $R_G$  must be reduced or shorted for  $I_D \geq \sim 60$  A for safe operation with the GA15IDDJT22-FR4.**

For operation at  $I_D \geq \sim 60$  A,  $R_G$  may be calculated from the following equation, which contains the DC current gain  $h_{FE}$  and the gate-source saturation voltage  $V_{GS, sat}$  (Figure 7).

$$R_{G, max} = \frac{(4.7V - V_{GS, sat}) * h_{FE}(T, I_D)}{I_D * 1.5} - 0.1\Omega$$



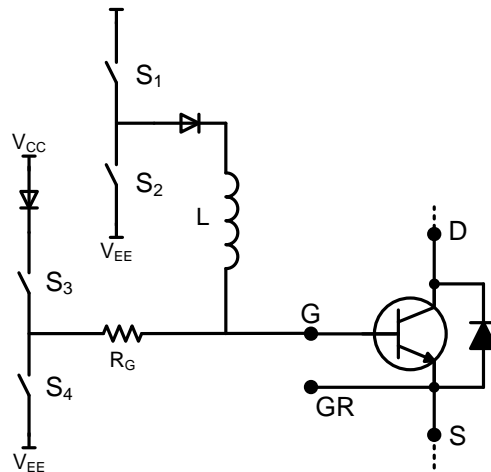
**Figure 26: Typical steady state gate current supplied by the GA15IDDJT22-FR4 board for the GA50SICP12-227 with the on board resistance of 0.7 Ω**



**Figure 27: Maximum gate resistance for safe operation of the GA50SICP12-227 at different drain currents using the GA15IDDJT22-FR4 board.**

**B:2: High Speed, Low Loss Drive with Boost Inductor**

A High Speed, Low-Loss Driver with Boost Inductor is also capable of driving the GA50SICP12-227 at high-speed. It utilizes a gate drive inductor instead of a capacitor to provide the high-current gate current pulses  $I_{G,on}$  and  $I_{G,off}$ . During operation, inductor L is charged to a specified  $I_{G,on}$  current value then made to discharge  $I_L$  into the SJT gate pin using logic control of  $S_1$ ,  $S_2$ ,  $S_3$ , and  $S_4$ , as shown in Figure 28. After turn on, while the device remains on the necessary steady state gate current  $I_{G,steady}$  is supplied from source  $V_{CC}$  through  $R_G$ . Please refer to the article “A current-source concept for fast and efficient driving of silicon carbide transistors” by Dr. Jacek Rąbkowski for additional information on this driving topology.<sup>4</sup>



**Figure 28: Simplified Inductive Pulsed Drive Topology**

<sup>3</sup> –  $R_G = (1/RG1 + 1/RG2)^{-1}$ . Driver is pre-installed with  $RG1 = 2.2 \Omega$ ,  $RG2 = 1.0 \Omega$

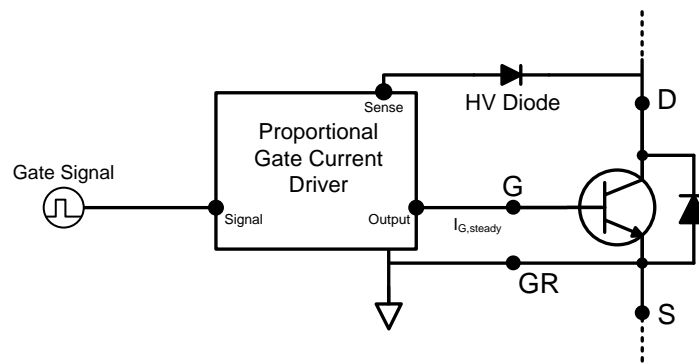
<sup>4</sup> – Archives of Electrical Engineering. Volume 62, Issue 2, Pages 333–343, ISSN (Print) 0004-0746, DOI: 10.2478/ae-2013-0026, June 2013

**C: Proportional Gate Current Driving**

For applications in which the GA50SICP12-227 will operate over a wide range of drain current conditions, it may be beneficial to drive the device using a proportional gate drive topology to optimize gate drive power consumption. A proportional gate driver relies on instantaneous drain current  $I_D$  feedback to vary the steady state gate current  $I_{G,steady}$  supplied to the GA100SICP2-227

**C:1: Voltage Controlled Proportional Driver**

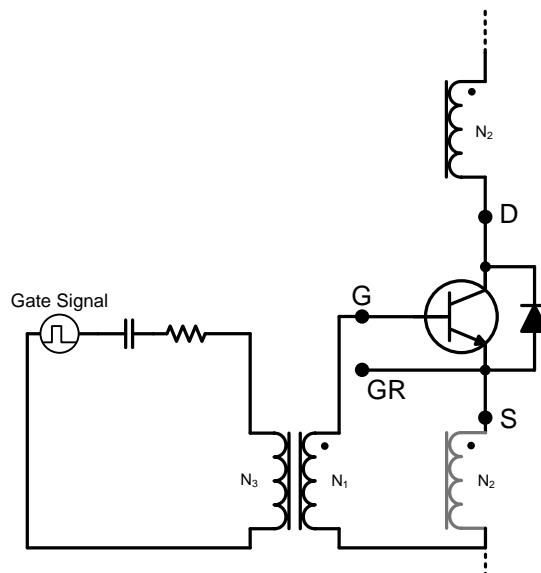
The voltage controlled proportional driver relies on a gate drive IC to detect the GA50SICP12-227 drain-source voltage  $V_{DS}$  during on-state to sense  $I_D$ . The gate drive IC will then increase or decrease  $I_{G,steady}$  in response to  $I_D$ . This allows  $I_{G,steady}$ , and thus the gate drive power consumption, to be reduced while  $I_D$  is relatively low or for  $I_{G,steady}$  to increase when is  $I_D$  higher. A high voltage diode connected between the drain and sense protects the IC from high-voltage when the driver and GA50SICP12-227 are in off-state. A simplified version of this topology is shown in Figure 29, additional information will be available in the future at <http://www.genesicsemi.com/commercial-sic/sic-junction-transistors/>



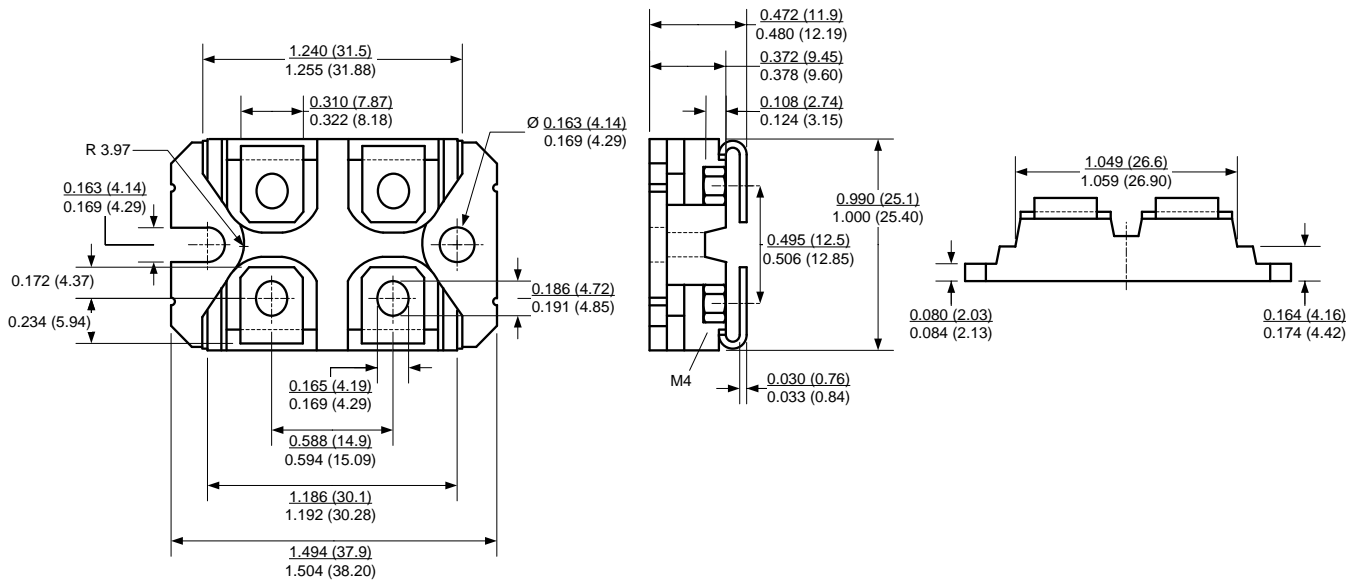
**Figure 29: Simplified Voltage Controlled Proportional Driver**

**C:2: Current Controlled Proportional Driver**

The current controlled proportional driver relies on a low-loss transformer in the drain or source path to provide feedback  $I_D$  of the GA50SICP12-227 during on-state to supply  $I_{G,steady}$  into the device gate.  $I_{G,steady}$  will then increase or decrease in response to  $I_D$  at a fixed forced current gain which is set by the turns ratio of the transformer,  $h_{force} = I_D / I_G = N_2 / N_1$ . GA50SICP12-227 is initially turned-on using a gate current pulse supplied into an RC drive circuit to allow  $I_D$  current to begin flowing. This topology allows  $I_{G,steady}$ , and thus the gate drive power consumption, to be reduced while  $I_D$  is relatively low or for  $I_{G,steady}$  to increase when is  $I_D$  higher. A simplified version of this topology is shown in Figure 30, additional information will be available in the future at <http://www.genesicsemi.com/commercial-sic/sic-junction-transistors/>.



**Figure 30: Simplified Current Controlled Proportional Driver**

**Section VI: Package Dimensions**
**SOT-227**
**PACKAGE OUTLINE**

**NOTE**

1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

**Revision History**

Date	Revision	Comments	Supersedes
2015/12/07	1	Updated Electrical Characteristics	
2015/03/26	0	Initial release	

Published by  
 GeneSiC Semiconductor, Inc.  
 43670 Trade Center Place Suite 155  
 Dulles, VA 20166

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**Section VII: SPICE Model Parameters**

This is a secure document. Please copy this code from the SPICE model PDF file on our website ([http://www.genesicsemi.com/images/products\\_sic/igbt\\_copack/GA50SICP12-227\\_SPICE.pdf](http://www.genesicsemi.com/images/products_sic/igbt_copack/GA50SICP12-227_SPICE.pdf)) into LTSPICE (version 4) software for simulation of the GA50SICP12-227.

```

*      MODEL OF GeneSiC Semiconductor Inc.
*      $Revision:      2.0      $
*      $Date:      07-DEC-2015      $
*
*      GeneSiC Semiconductor Inc.
*      43670 Trade Center Place Ste. 155
*      Dulles, VA 20166
*
*      COPYRIGHT (C) 2015 GeneSiC Semiconductor Inc.
*      ALL RIGHTS RESERVED
*
*      These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
*      OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
*      TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
*      PARTICULAR PURPOSE."
*      Models accurate up to 2 times rated drain current.
*
*      Start of GA50SICP12-227 SPICE Model
*
.SUBCKT GA50SIPC12 DRAIN GATE SOURCE
Q1 DRAIN GATE SOURCE GA50SIPC12_Q
D1 SOURCE DRAIN GA50SIPC12_D1
D2 SOURCE DRAIN GA50SIPC12_D2
*
.model GA50SIPC12_Q NPN
+ IS      9.833E-48      ISE      1.073E-26      EG      3.23
+ BF      110      BR      0.55      IKF      9000
+ NF      1      NE      2      RB      0.95
+ RE      0.005      RC      0.014      CJC      2.120E-9
+ VJC      2.8346      MJC      0.4846      CJE      6.026E-09
+ VJE      3.1791      MJE      0.5295      XTI      3
+ XTB      -1.5      TRC1      9.0E-03      MFG      GeneSiC_Semi
+ IRB      0.005      RBM      0.073
.MODEL GA50SIPC12_D1 D
+ IS      1.99E-16      RS      0.015652965      N      1
+ IKF      1000      EG      1.2      XTI      3
+ TRS1      0.0042      TRS2      1.3E-05      CJO      3.86E-09
+ VJ      1.362328465      M      0.48198551      FC      0.5
+ TT      1.00E-10      IAVE      50
.MODEL GA50SIPC12_D2 D
+ IS      1.54E-19      RS      0.1      N      3.941
+ EG      3.23      TRS1      -0.004      IKF      19
+ XTI      0      FC      0.5      TT      0
.ENDS
*      End of GA50SICP12-227 SPICE Model

```