PD-94168C

International
IOR Rectifier

RADIATION HARDENED POWER MOSFET SURFACE MOUNT (SMD-2)

IRHNA597260
200V, P-CHANNEL
R5 TECHNOLOGY

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D
IRHNA597260	100K Rads (Si)	0.102Ω	-33.5A
IRHNA593260	300K Rads (Si)	0.102Ω	-33.5A

SMD-2

International Rectifier's R5™ technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm^2)). The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:

- Single Event Effect (SEE) Hardened
- Ultra Low $R_{DS(on)}$
- Low Total Gate Charge
- Proton Tolerant
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Ceramic Package
- Light Weight

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
I_D @ V_{GS} = -12V, T_C = 25°C	Continuous Drain Current	-33.5	A
I_D @ V_{GS} = -12V, T_C = 100°C	Continuous Drain Current	-21	
I_{DM}	Pulsed Drain Current ①	-134	
P_D @ T_C = 25°C	Max. Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	303	mJ
I_{AR}	Avalanche Current ①	-33.5	A
E_{AR}	Repetitive Avalanche Energy ①	25	mJ
dv/dt	Peak Diode Recovery dv/dt ③	10	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150	°C
	Pckg. Mounting Surface Temp.	300 (for 5s)	
	Weight	3.3 (Typical)	g

For footnotes refer to the last page

01/16/08

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-200	—	—	V	V_{GS} = 0V, I_D = -1.0mA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.25	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.102	Ω	V_{GS} = -12V, I_D = -21A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -1.0mA
g_{fs}	Forward Transconductance	23	—	—	S	V_{DS} > -15V, I_D = -21A
I_{DSS}	Drain-to-Source Leakage Current	—	—	-10	µA	V_{DS} = -160V, V_{GS} = 0V
		—	—	-25		V_{DS} = -160V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V_{GS} = -20V
	Gate-to-Source Reverse Leakage	—	—	100		V_{GS} = 20V
Q_g	Total Gate Charge	—	—	180	nC	V_{GS} = -12V, I_D = -33.5A
Q_{gs}	Gate-to-Source Charge	—	—	75		V_{DS} = -100V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	50		
$t_{d(on)}$	Turn-On Delay Time	—	—	50	ns	V_{DD} = -100V, I_D = -33.5A
t_r	Rise Time	—	—	100		V_{GS} = -12V, R_G = 2.35 Ω
$t_{d(off)}$	Turn-Off Delay Time	—	—	190		
t_f	Fall Time	—	—	175		
$L_S + L_D$	Total Inductance	—	4.0	—	nH	Measured from center of drain pad to center of source pad
C_{iss}	Input Capacitanc	—	7170	—	pF	V_{GS} = 0V, V_{DS} = -25V
C_{oss}	Output Capacitance	—	920	—		f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	—	86	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-33.5	A	
I_{SM}	Pulse Source Current (Body Diode))	—	—	-134		
V_{SD}	Diode Forward Voltage	—	—	-5.0	V	T_j = 25°C, I_S = -33.5A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	450	ns	T_j = 25°C, I_F = -33.5A, di/dt ≤ -100A/µs
Q_{RR}	Reverse Recovery Charge	—	—	5.5	µC	V_{DD} ≤ -50V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	0.5	°C/W	
$R_{thJ-PCB}$	Junction-to-PC board	—	1.6	—		soldered to a 2” square copper-clad board

Note: Corresponding Spice and Saber models are available on International Rectifier Website.

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ④⑤

	Parameter	100K Rads(Si)[1]		300K Rads(Si)[2]		Units	Test Conditions
		Min	Max	Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-200	—	-200	—	V	V_{GS} = 0V, I_D = -1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	-4.0	-2.0	-5.0		V_{GS} = V_{DS}, I_D = -1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	-100	—	-100	nA	V_{GS} = -20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	100	—	100		V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	—	-10	—	-10	µA	V_{DS} = -160V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.103	—	0.103	Ω	V_{GS} = -12V, I_D = -21A
V_{SD}	Diode Forward Voltage ④	—	-5.0	—	-5.0	V	V_{GS} = 0V, I_S = -33.5A

1. Part number IRHNA597260
2. Part number IRHNA593260

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET (MeV/(mg/cm²))	Energy (MeV)	Range (µm)	VDS (V)				
				@VGS=0V	@VGS=5V	@VGS=10V	@VGS=15V	@VGS=20V
Br	37.3	285	36.8	- 200	- 200	- 200	- 200	-75
I	59.9	345	32.7	- 200	- 200	- 200	- 50	—
Au	82.3	357	28.5	- 200	- 200	- 200	- 35	—

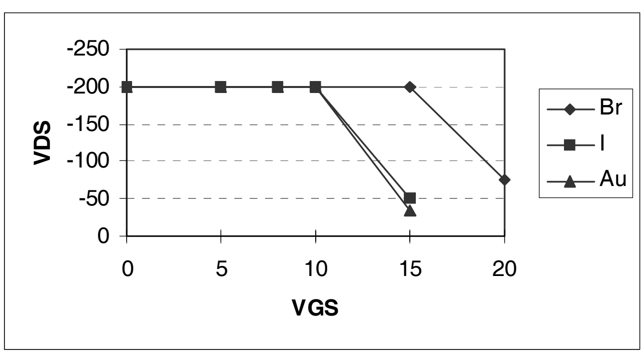


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

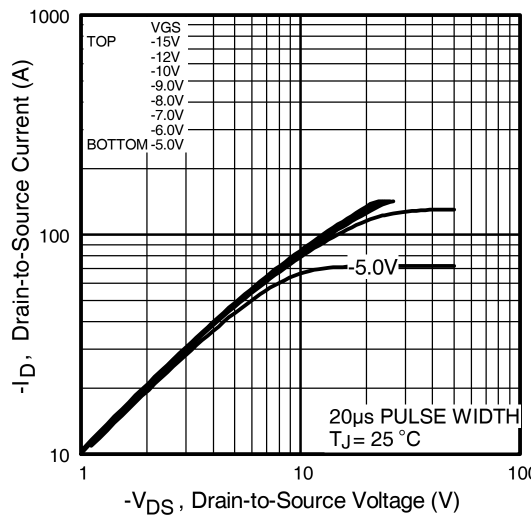


Fig 1. Typical Output Characteristics

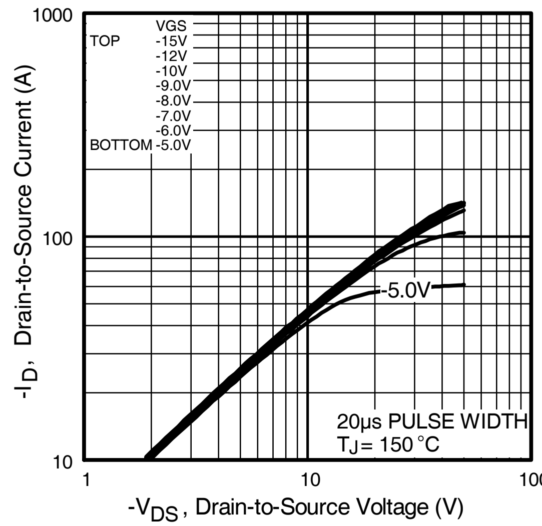


Fig 2. Typical Output Characteristics

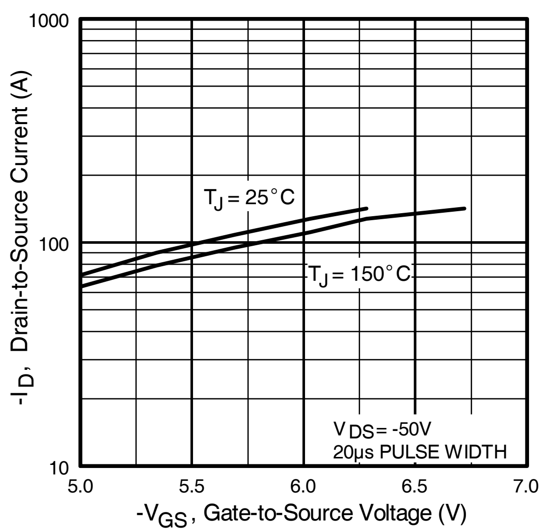


Fig 3. Typical Transfer Characteristics

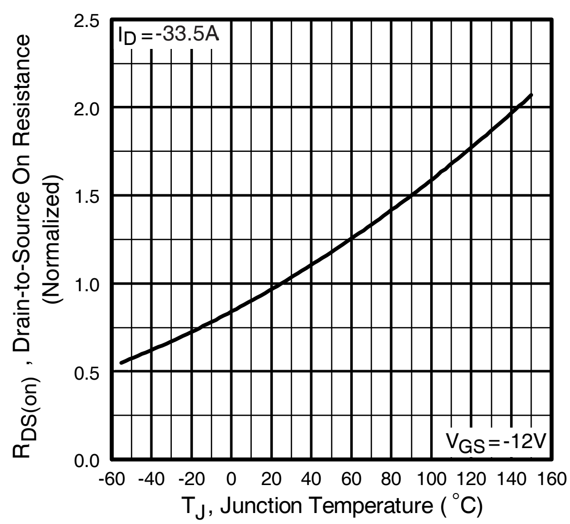


Fig 4. Normalized On-Resistance Vs. Temperature

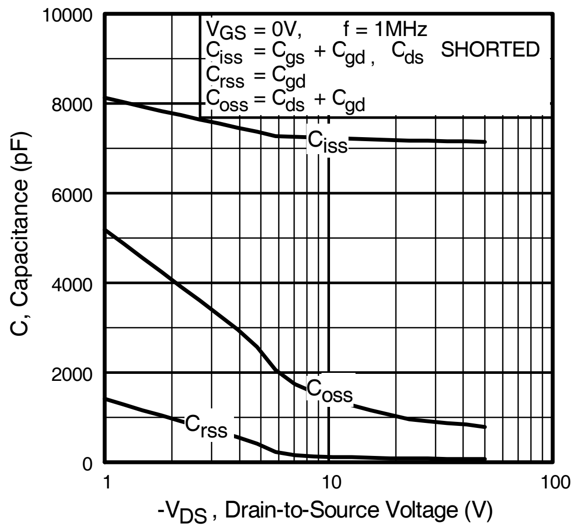


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

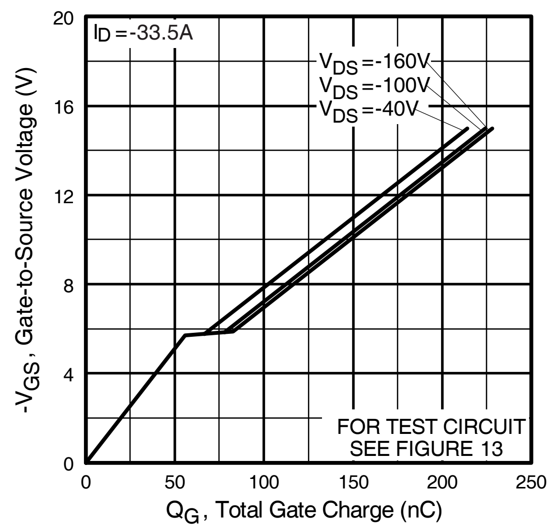


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

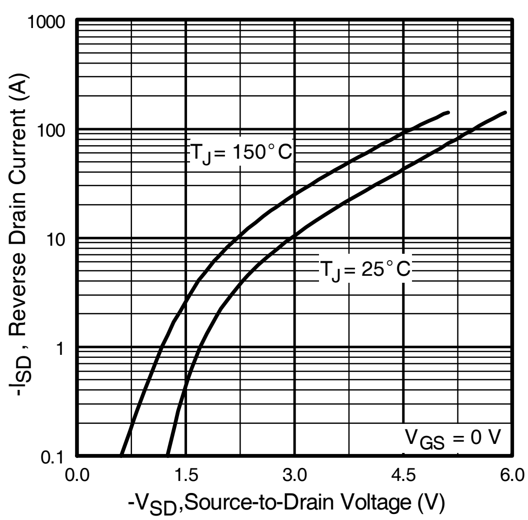


Fig 7. Typical Source-Drain Diode Forward Voltage

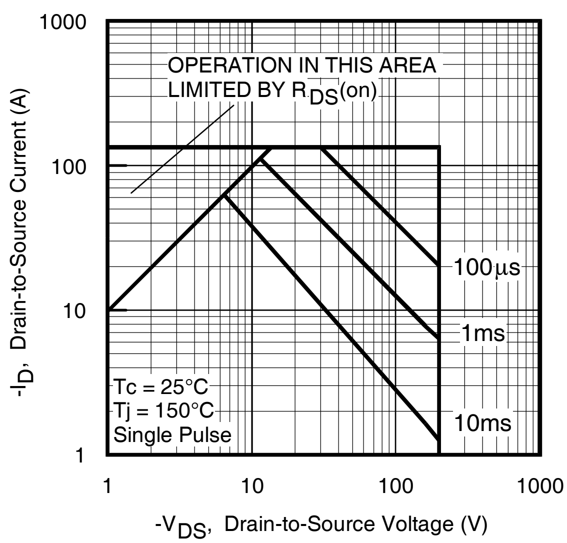


Fig 8. Maximum Safe Operating Area

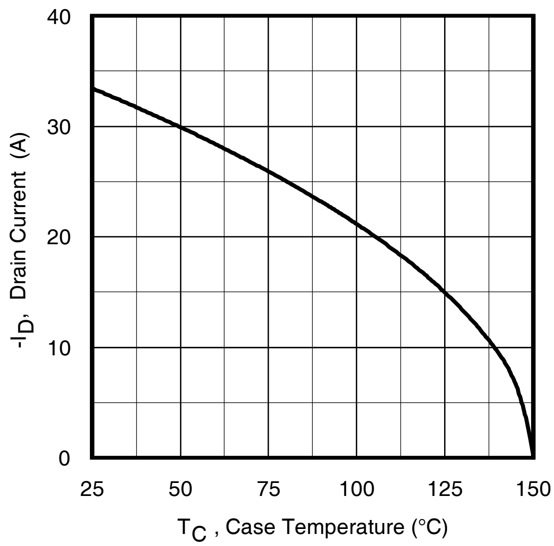


Fig 9. Maximum Drain Current Vs. Case Temperature

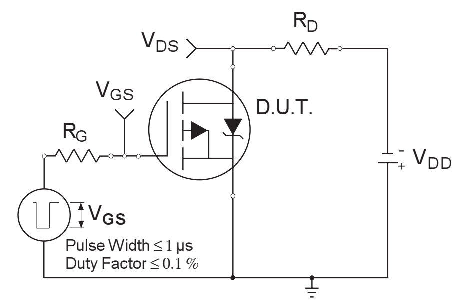


Fig 10a. Switching Time Test Circuit

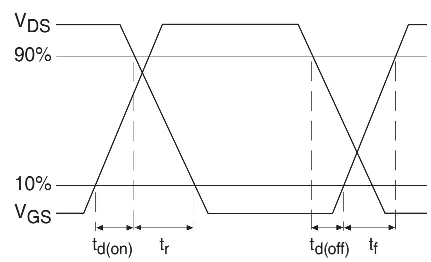


Fig 10b. Switching Time Waveforms

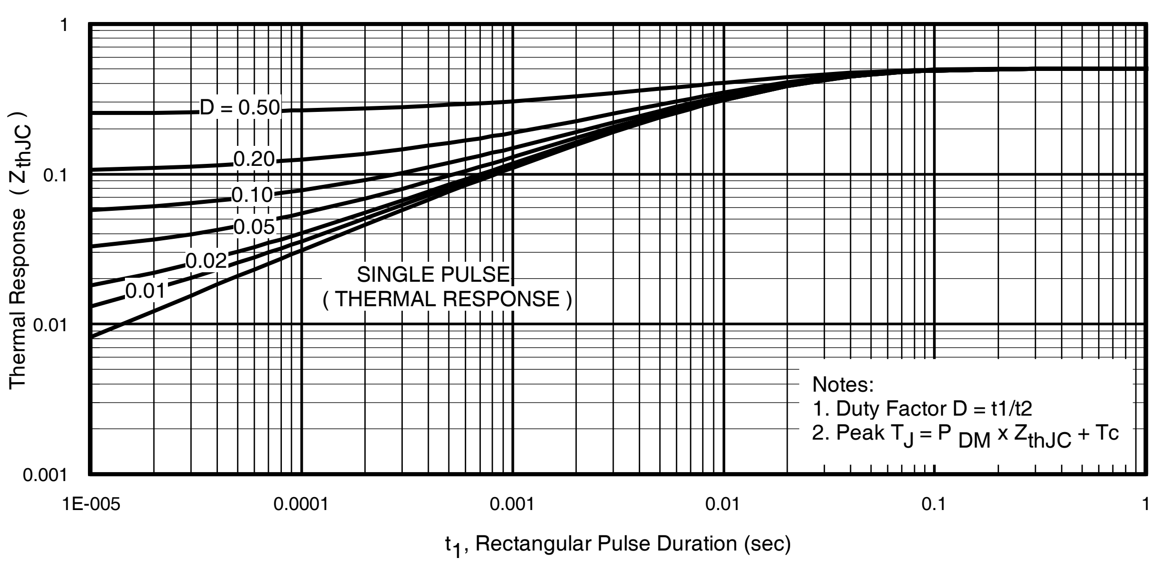


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

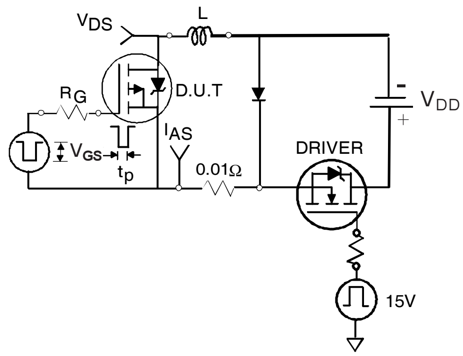


Fig 12a. Unclamped Inductive Test Circuit

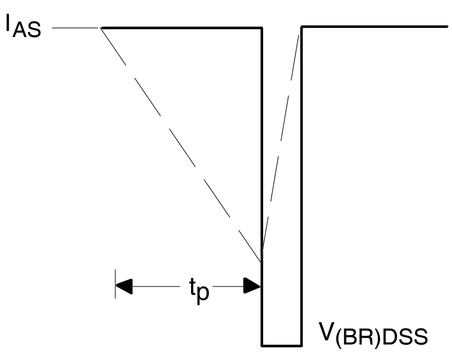


Fig 12b. Unclamped Inductive Waveforms

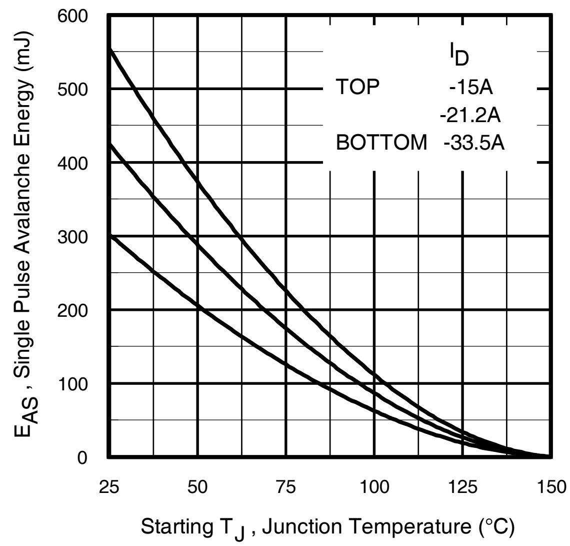


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

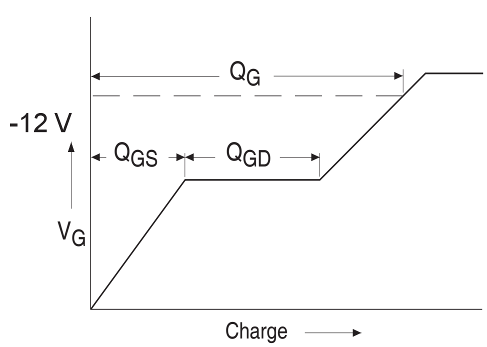


Fig 13a. Basic Gate Charge Waveform

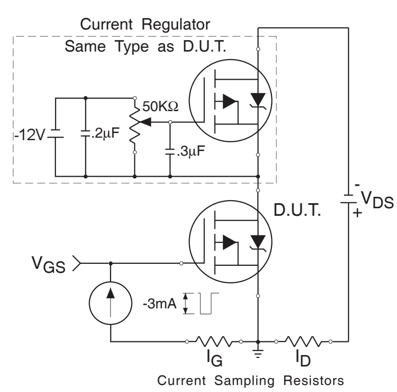
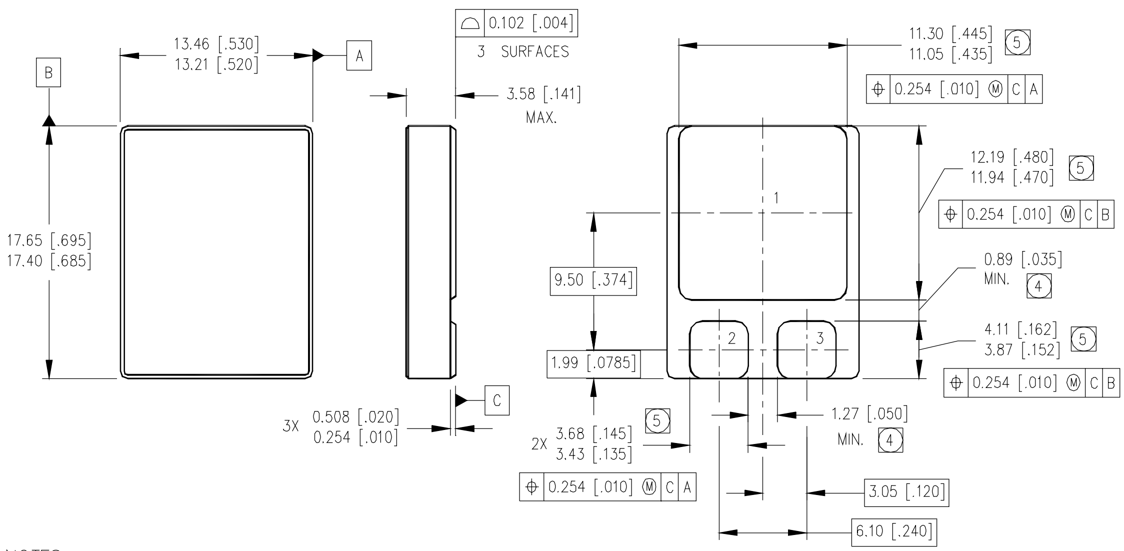


Fig 13b. Gate Charge Test Circuit

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.
② V_{DD} = -50V, starting T_J = 25°C, L= 0.54mH Peak I_L = -33.5A, V_{GS} = -12V
③ I_{SD} ≤ -33.5A, di/dt ≤ - 450A/µs, V_{DD} ≤ - 200V, T_J ≤ 150°C
④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%
⑤ **Total Dose Irradiation with V_{GS} Bias.** -12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.
⑥ **Total Dose Irradiation with V_{DS} Bias.** -160 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — SMD-2



NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. DIMENSION INCLUDES METALLIZATION FLASH.
5. DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

PAD ASSIGNMENTS

1 = DRAIN
2 = GATE
3 = SOURCE

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR LEOMINSTER : 205 Crawford St., Leominster, Massachusetts 01453, USA Tel: (978) 534-5776
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.
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