AMD64 Processor VRM Controller

PRELIMINARY DATA SHEET

DESCRIPTION

The LX1677 is a highly integrated VRM power supply controller IC featuring two PWM switching regulator stages.

The two constant frequency voltage-mode PWM phases are configured as a single biphase high current output core supply.

In biphase operation, the high current (>35A) output is generated by a LoadSHARE™† technique that balances the currents in the two phases. Power loss and noise, due to the ESR of the input capacitors, are minimized by operating the PWMs 180° out of phase.

A synchronized Transient Correction Loop† provides exceptional control of the output droop and overshoot during very high di/dt load changes, the circuit can be configured for droop only, overshoot only or both.

This architecture also minimizes capacitor requirements while maximizing regulator response.

A true differential input amplifier is used for remote voltage sensing at the processor core.

A VID code generator provides an internal reference that will set the output voltage. This VID code can be changed during operation and the reference will slew the output voltage to its new setting at a preset rate. During VID changes on the fly the Power Good indication will stay valid.

The current through the lower phase 1 MOSFET will be sampled using its $R_{DS(ON)}$ for current limit and shut down.

For further protection, an over voltage circuit will trip at a specified setting and clamp the output by turning off the upper MOSFETs and turning on the lower MOSFETs.

The upper MOSFET drivers use a bootstrap capacitor to provide the upper drive voltage over the input voltage range of 6 to 24 volts.

IMPORTANT: For the most current data, consult *MICROSEMI*'s we bsite: http://www.microsemi.com

† Patent numbers US6292378,US6285571,US6356063, US6605931

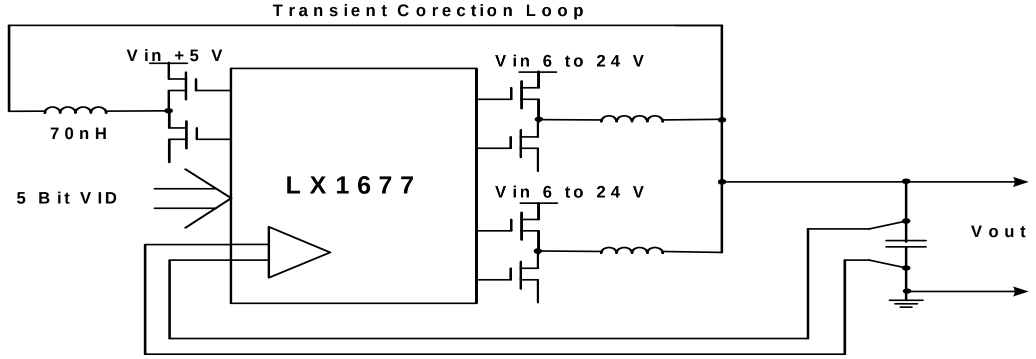
KEY FEATURES

- High Current Biphase Operation
- Outputs As Low As 0.800V
- † Biphase LoadSHARE™
- † Transient Correction Loop Reduces Required Capacitance
- Differential Amplifier For Remote Voltage Sensing
- Integrated High Current MOSFET Drivers
- 200KHz to 1MHz Frequency Operation
- Programmable Slew Rate Control For Start-Up Sequence and VID change
- VID Changes On The Fly
- Power Good Indicator
- Short Circuit Protection
- Output Over Voltage and Under Voltage Protection
- No current-sense resistors

APPLICATIONS

- AMD Athlon 64™ and AMD Opteron™ Processors
- Processor Core Voltage Supply
- Voltage Regulator Modules

PRODUCT HIGHLIGHT



PACKAGE ORDER INFO

T_J (°C)	PW Plastic TSSOP 38-Pin	LQ Plastic MLPQ 38-Pin
0 to 70	LX1677-CPW	LX1677-CLQ

Note: Available in Tape & Reel.
Append the letter "T" to the part number.
(i.e. LX1677-CLQT)

Rev 0.4, 2003-03-03

Microsemi
Integrated Products Division
11861 Western Avenue, Garden Grove, CA. 92841, 714-898-8121, Fax: 714-893-2570

ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage (VCCL, VCC)..-0.3V to 6.0V
Battery Input Voltage (VIN)..-0.3V to 36V
Current Limit Sense (ILIM1, ILIM3)..-0.3V to 36V
Topside Driver Supply Input Voltage (VC1, VC2, VC3)........ -0.3 to VS*x* + 6.0V
Topside Driver Return Input Voltage (VS1, VS2)...............................-5V to 36V
Differential Sense Input Voltage (FB+, FB-)..................................-0.3V to 6.0V
VID0 – VID4, Input Voltage..-0.3V to 6V
High Side Driver Peak (<500ns) Current (HO1/2, I-MAX)..........................±1A
Low Side Driver Peak (<500ns) Sink Current (LO1/2, I-MIN)...................±1.5A
Operating Junction Temperature.. 150°C
Storage Temperature Range..-65°C to 150°C
Lead Temperature (Soldering 10 seconds).. 300°C

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.
x denotes respective pin designator 1, 2, or 3

THERMAL DATA

LQ Plastic MLPQ 38-Pin

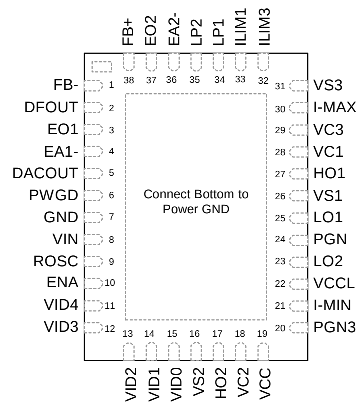
THERMAL RESISTANCE-JUNCTION TO CASE, θ_{JC}	8°C/W
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	35°C/W

PW Plastic TSSOP 38-Pin

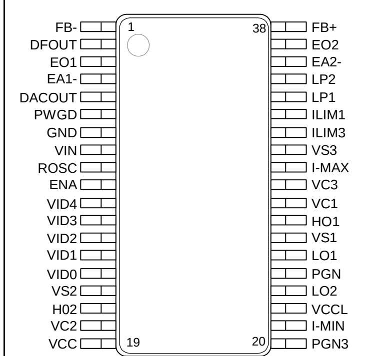
THERMAL RESISTANCE-JUNCTION TO CASE, θ_{JC}	12.2°C/W
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	38°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

PACKAGE PIN OUT



LQ PACKAGE
(Top View)



PW PACKAGE
(Top View)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	LX1677			Units
		Min	Typ	Max	
IC Input Supply Voltage	VCC	4.5		5.5	V
Battery Input Voltage	VIN	5.7		25.2	V
Biphase Topside Driver Return Voltage	VS1, VS2	0		25.2	V
Transient Correction Phase Driver Return Voltage	VS3	0		5.5	V

FUNCTIONAL PIN DESCRIPTION

Name	Description
FB+	Differential Amplifier Positive Input – Feedback from output
FB-	Differential Amplifier Negative Input – Feedback from output
DFOUT	Differential Amplifier Output
EA1-	Phase 1 Error Amplifier Negative Input
EO1	Phase 1 Error Amplifier Output
GND	Analog Ground
ROSC	A resister to ground sets PWM frequency
ENA	Enable Input – Logic Low disables all converter phases
DACOUT	DAC Output voltage – 50uA bi-directional current source
VID4	Digital Input for VID code – Has an internal pull-up resister
VID3	Digital Input for VID code – Has an internal pull-up resister
VID2	Digital Input for VID code – Has an internal pull-up resister
VID1	Digital Input for VID code – Has an internal pull-up resister
VID0	Digital Input for VID code – Has an internal pull-up resister
PWGD	Power Good Output Pin – Open drain output pin for power good indication. High = Power Good
VCC	IC Supply Voltage. Nominal +5V
VC3	Supply for transient correction phase upper MOSFET driver, bootstrap voltage
PGN3	Power ground pin for Transient Correction Loop driver
I-MIN	Output Driver for lower Transient Correction Loop MOSFET
VS3	Low side of upper driver for Transient Correction Loop – MOSFET Driver power return
I-MAX	Output Driver for upper Transient Correction Loop MOSFET
ILIM3	Transient Correction Loop current sense – A resister sets an upper limit for over current detection and shut down.
LP1	Phase 2 differential amplifier positive input, filtered feedback from phase 1 output
EA2-	Negative Input of phase 2 integrating amplifier
EO2	Output of phase 2 integrating amplifier
LP2	Phase 2 differential amplifier negative input, filtered feedback from phase 2 output
VIN	Battery Voltage Input.
LO2	Driver Output for phase 2 lower MOSFET
VS2	Low side of upper gate driver for phase 2.
HO2	Driver Output for phase 2 upper MOSFET
VC2	Supply for phase 2 upper MOSFET driver, bootstrap voltage
PGN	Power ground pin for current sensing of lower MOSFET $R_{DS(ON)}$ for phase 1.
LO1	Driver Output for phase 1 lower MOSFET
ILIM1	Over-Current Limit Set – A resister sets an upper limit for over current detection and shut down.
VS1	Low side of upper gate driver for phase #1.
HO1	Driver Output for phase 1 upper MOSFET
VC1	Supply for phase 1 upper MOSFET driver, bootstrap voltage
VCCL	Voltage bus for the lower MOSFET drivers. Nominal +5V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature 0°C ≤ T_A ≤ 70°C except where otherwise noted and the following test conditions: VCC = 5V, VCCL = 5V, VIN = 12V, Switching Frequency = 500KHz.

Parameter	Symbol	Test Conditions	LX1677 Min	LX1677 Typ	LX1677 Max	Units
REGULATOR						
IC Supply Current	$I_{Q(VCC)}$	ENA = VCC, FB+ = FB-	1	5	9	mA
		ENA = GND			1	µA
Low Side Driver Operating Current	$I_{Q(VCCL)}$	ENA = VCC, FB+ = FB-		0.5	1	mA
High Side Driver Operating Current	$I_{Q(VCx)}$	ENA = VCC, FB+ = FB-		2	4	mA
ERROR AMPLIFIER: PHASE 1						
Input Offset Voltage	V_{OS}	Common Mode Voltage (V_{CM}) = 1.4V	-6		6	mV
Input Bias Current	I_{EA1}		-100		100	nA
DC Open Loop Gain			60	70		dB
Input Common Mode Range	V_{ICM}	CMRR > 50dB	0.8		2.5	V
Output Voltage Swing	$V_{EO1(MAX)}$	I_{EA1} = 2mA		4.0		V
	$V_{EO1(MIN)}$	I_{EA1} = -20uA		0.15	0.5	
Unity Gain Bandwidth	UGBW			20		MHz
DIFFERENTIAL AMPLIFIER						
Input Offset Voltage	V_{OS}	V_{CM}=1.4V	-6		6	mV
Gain	A_{DA}		0.99	1	1.01	V/V
Common Mode Rejection Ratio	$CMRR_{DA}$	0.8V < V_{CM} < 2.5V		65		dB
Input Resistance	R_{IN}	Measured at FB+ Input		30		KΩ
Input Common Mode Range	V_{CM}		0		3	V
Source / Sink Current		V_{DFOUT} = 0V		5		mA
Output Voltage Swing	$V_{DFOUT(MAX)}$	I_{DFOUT} = 2mA		4.0		V
	$V_{DFOUT\ (MIN)}$	I_{EA1} = -20uA		0.2		
Unity Gain Bandwidth	UGBW			10		MHz
Slew Rate	SR			5		V/µs
OSCILLATOR						
Maximum Clock Frequency	f_{MAX}	R_{PWM}=10kΩ	0.9	1	1.1	MHz
Minimum Clock Frequency	f_{MIN}	R_{PWM}=50kΩ	150	200	220	KHz
Frequency Stability				4		%
PWM OUTPUT						
Maximum Duty Cycle	DC_{MAX}	During Transient Correction Switching			100	%
		Transient Correction Not Switching	40		50	
Minimum Pulse Width	$t_{PWM(MIN)}$	3000pF Load		60		nS
Dead Time		3000pF Load at 50% of VCCL	50	80	200	nS
Ramp Amplitude	V_{RAMP}	VIN = 6V		0.70		V
		VIN = 12		1.40		
		VIN = 24 V		2.80		
PHASE 2 INTEGRATING AMPLIFIER						
Input Offset Voltage	V_{OS}	V_{CM}=1.4V	-6		6	mV
DC Open Loop Gain				70		dB
Output Voltage Swing	$V_{EO2(MAX)}$	I_{EA2} = 2mA		4.0		V
	$V_{EO2(MIN)}$	I_{EA2} = -20uA		0.15	0.5	
Unity Gain Bandwidth	UGBW			20		MHz

Microsemi
Integrated Products Division
11861 Western Avenue, Garden Grove, CA. 92841, 714-898-8121, Fax: 714-893-2570

Microsemi
INTEGRATED PRODUCTS

ELECTRICAL CHARACTERISTICS (CONT)

Unless otherwise specified, the following specifications apply over the operating ambient temperature 0°C ≤ T_A ≤ 70°C except where otherwise noted and the following test conditions: VCC = 5V, VCCL = 5V, VIN = 12V, Switching Frequency = 500KHz.

Parameter	Symbol	Test Conditions	LX1677 Min	LX1677 Typ	LX1677 Max	Units
PHASE 2 DIFFERENTIAL AMPLIFIER						
Input Offset Voltage	V_{OS}	LP1=LP2	-6		6	mV
Gain	A_{DA}		0.98	1	1.02	V/V
Common Mode Rejection Ratio	$CMRR_{DA}$	Common Mode Voltage = 0 to 2 V		60		dB
Input Resistance	R_B			180		KΩ
Unity Gain Bandwidth	UGBW			4		MHz
TRANSIENT CONTROL LOOP						
Voltage Droop Sense Propagation Delay : FB+ and FB- to I-MAX				50		nS
Voltage Overshoot Sense Propagation Delay : FB+ and FB- to I-MIN				50		nS
Voltage Droop Sense Threshold		V_{DFOUT} Rising 3000pF Load		40		mV
Voltage Overshoot Sense Threshold		V_{DFOUT} Falling 3000pF Load		40		mV
OUTPUT DRIVERS						
Driver ▪ Rise Time ▪ Fall Time	t_{RISE} t_{FALL}	CL = 3000pF, VC*x* - VS*x* = 5V		50 50		nS
High Side Driver Voltage: [V_{HOx} - V_{VSx}] ▪ Drive High ▪ Drive Low		V_{HOx} = 20mA, VC*x* - VS*x* = 5.0 V V_{HOx} = -20mA, VC*x* - VS*x* = 5.0 V	4.8	4.9 0.1	 0.2	V
Low Side Driver Voltage: [V_{LOx} – V_{PGN}] ▪ Drive High ▪ Drive Low		V_{LOx} = 20mA, VCCL - VPGN = 5.0 V V_{LOx} = -20mA, VCCL - VPGN = 5.0 V	4.8	4.9 0.1	 0.2	V
High Side Driver Current	I_{HOx}	VC*x* - VS*x* = 5.0 V, Load = 3300pf at <500nSec		1		A
Lower MOSFET Driver Current	I_{LOx}	VCCL - PGN = 5.0 V, Load = 3300pf at <500nSec		1.5		A
PHASE 1 OVER CURRENT PROTECTION						
Current Sense Bias Current	I_{ILIM1}		44	50	60	µA
Current Sense Delay	$t_{CSD(ILIM1)}$		200	400	500	nS
TRANSIENT CORRECTION LOOP OVER CURRENT PROTECTION						
Current Sense Bias Current	I_{ILIM3}		40	50	60	µA
Current Sense Delay	$t_{CSD(ILIM3)}$		200	400	500	nS
ENABLE INPUT / VOLTAGE IDENTIFICATION (VID)						
Logic Low Threshold				1.5		V
Hysteresis				0.3		V
Pullup Resistance				100		KΩ
POWER GOOD						
Low Output Voltage	V_{PWGD}	I_{PWGD} = -3mA		0.5		V

ELECTRICAL CHARACTERISTICS (CONT)

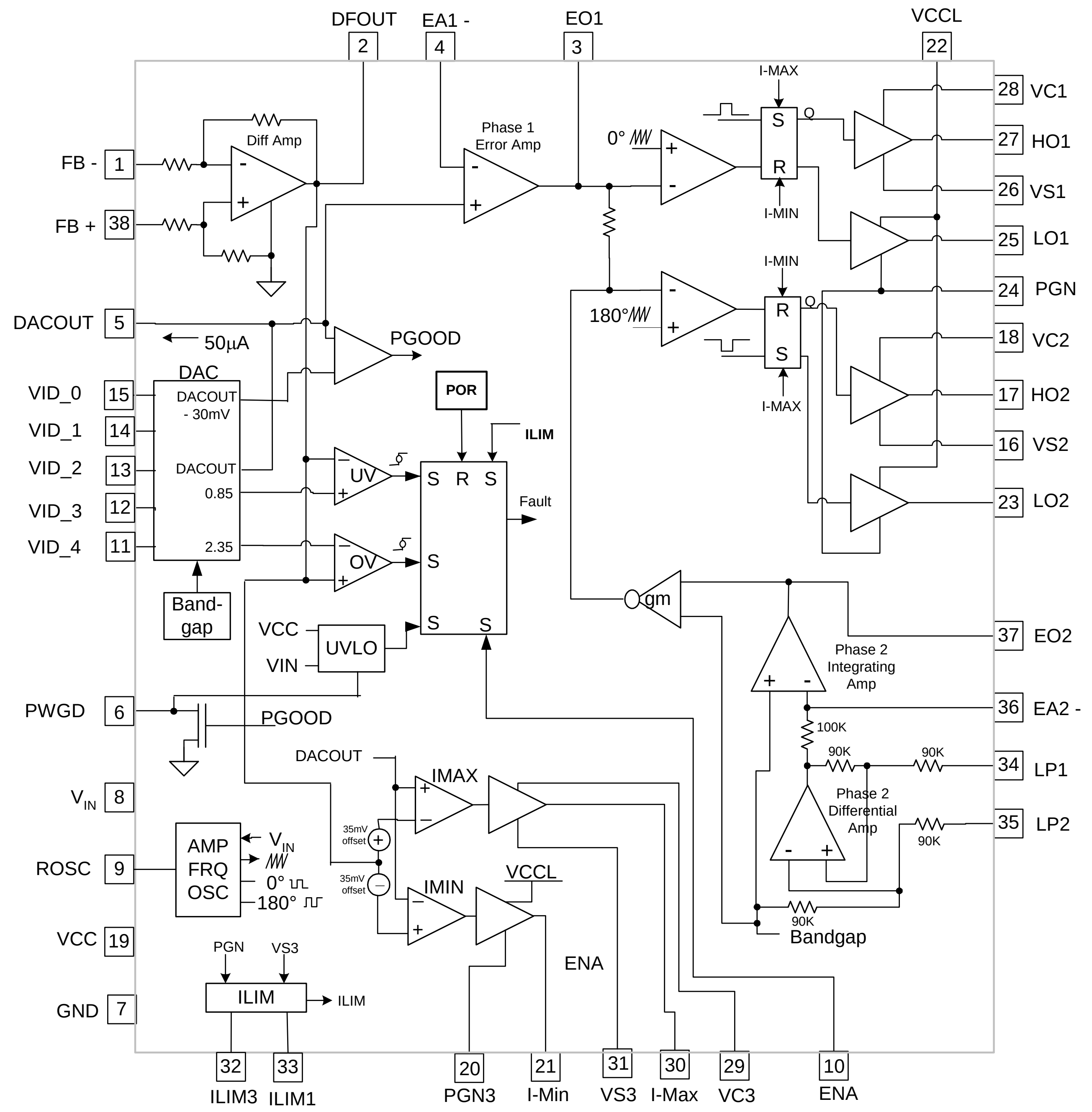
Unless otherwise specified, the following specifications apply over the operating ambient temperature 0°C ≤ T_A ≤ 70°C except where otherwise noted and the following test conditions: VCC = 5V, VCCL = 5V, VIN = 12V, Switching Frequency = 500KHz.

Parameter	Symbol	Test Conditions	LX1677 Min	LX1677 Typ	LX1677 Max	Units
UVLO						
VCC						
▪ Threshold		VCC Rising		4.2		V
▪ Hysteresis				0.3		V
VIN						
▪ Threshold		VIN Rising		5.5		V
▪ Hysteresis				0.3		V
OVER VOLTAGE PROTECTION						
Over Voltage Threshold	-			1.85		V
UNDER VOLTAGE PROTECTION						
Under Voltage Threshold				0.725		V
DAC						
Initial DACOUT Accuracy		$1 \le V_{DACOUT} \le 1.4$			1	%
		$0.925 \le V_{DACOUT} < 1$ $1.4 < V_{DACOUT} \le 2$			2	%
High Side Driver Current	I_{HOx}	VC*x* - VS*x* = 5.0 V, Load = 3300pf at <500nSec		1		A
Lower MOSFET Driver Current	I_{LOx}	VCCL - PGN = 5.0 V, Load = 3300pf at <500nSec		1.5		A
VID Logic High Threshold			0.5	1.3	2	V
VID Hysteresis				0.3		V

VOLTAGE IDENTIFICATION (VID) CODE

VID[4:0]	V_{OUT} (V)	VID[4:0]	V_{OUT} (V)
00000	1.550	10000	1.150
00001	1.525	10001	1.125
00010	1.500	10010	1.100
00011	1.475	10011	1.075
00100	1.450	10100	1.050
00101	1.425	10101	1.025
00110	1.400	10110	1.000
00111	1.375	10111	0.975
01000	1.350	11000	0.950
01001	1.325	11001	0.925
01010	1.300	11010	0.900
01011	1.275	11011	0.875
01100	1.250	11100	0.850
01101	1.225	11101	0.825
01110	1.200	11110	0.800
01111	1.175	11111	Shutdown

SIMPLIFIED BLOCK DIAGRAM



APPLICATION CIRCUITS

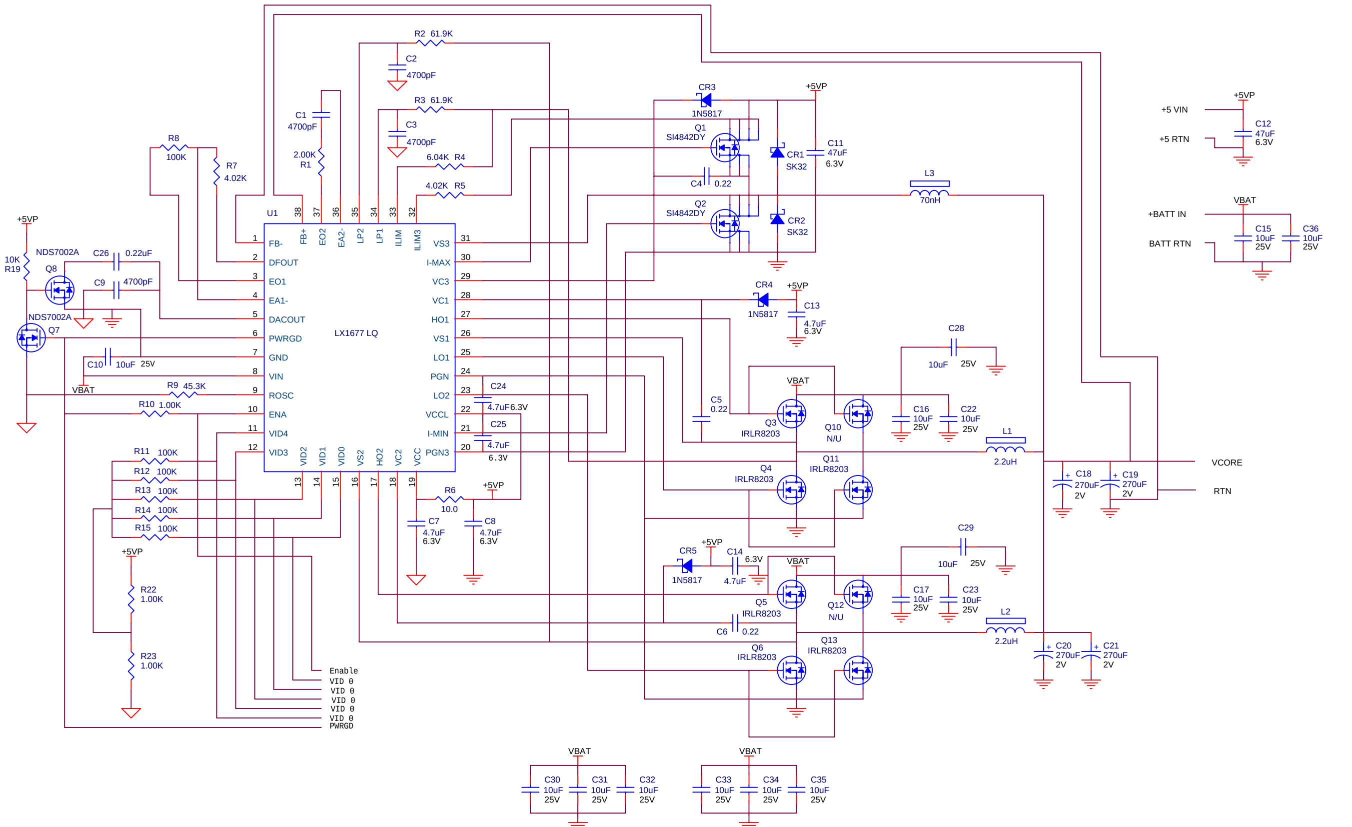


Figure 2 – Typical VRM Application

THEORY OF OPERATION

GENERAL DESCRIPTION

The LX1677 is a voltage-mode pulse-width modulation controller integrated circuit. The PWM frequency is programmable from 200kHz to 1MHz. The device has external compensation, for more flexibility of the loop response. The LX1677 also makes use of a true differential input amplifier for remote voltage sensing at the actual processor core. This is a very important feature now that the core voltages are in the 1 to 2 volt range. The reference for the biphase PWM output is a 5 bit VID code DAC. The VID code DAC can generate a reference voltage of 0.925 to 2.000 volts. The output of the DAC is a bi-directional current source and is connected to the DACOUT pin. Connecting a capacitor from this pin to ground will generate a linear ramp, which will determine the rate of change of the output voltage. The rate of change can be set so that the current required to charge the total output capacitance is below the maximum current limit trip point. This will allow VID changes on the fly without tripping the over current sensor.

POWER UP AND INITIALIZATION

At power up, the LX1677 monitors the supply voltage to VCC and Vin, Before both supplies reach their under-voltage lock-out (UVLO) thresholds, a power on reset condition will prevent soft-start from beginning, the oscillator is disabled and all MOSFETs are kept off.

SOFT-START

Once the supplies are above the UVLO threshold and the Enable pin is brought high, the soft-start capacitor begins to be charged up by the reference DAC through the DACOUT pin. The capacitor voltage at the DACOUT pin rises as a linear ramp. The DACOUT pin is connected to the error amplifier's non-inverting input which controls the output voltage. The output voltage will follow the DACOUT pin voltage.

Phase 3 (hysteretic phase) is disabled during soft-start.

OVER-CURRENT PROTECTION

There are two separate current limit circuits in the LX1677. One looks at the phase 1 lower MOSFET drain current and the second looks at the phase 3 upper MOSFET drain current. Both circuits have a 400 nS delay before a current limit command is issued to the current limit latch, once set the current limit latch will hold all three phases off until it is reset.

The Over-Current Protection is disabled during positive VID changes.

To reset the current limit latch either the enable command (ENA) must be cycled low then back high or the input power must cycle off and then back on.

OVER-CURRENT PROTECTION (PHASE 1)

The phase 1 current limit uses the RDS(ON) of the lower MOSFET, together with a resistor (RSET) to set the actual current limit point. The current limit comparator senses the current 400 nS after the lower MOSFET is switched on. A current source supplies a current (ISET), of 50µA which flows into RSET and determines the current limit trip point. The value of RSET is selected to set the current limit for the application.

Phase 1 RSET is calculated by:

$$R_{SET} = \frac{ILimit \bullet R_{DS(ON)}}{50\mu A}$$

The current limit comparator will trip when the drop across RSET equals the drop across the lower MOSFET RDS(ON)., at this time the comparator outputs a signal to set the I limit latch and removes the enable command. The Over-Current sensing is done on phase 1 only because phase 2 current is always being forced to equal the phase 1 current, therefore the current trip point is set at half of the desired current limit. For an output current limit setting of 30 amps, the current trip point for phase 1 is set at 15 amps.

When the phase 1 over current latch is set all three phases are disabled, all MOSFETs are turned off.

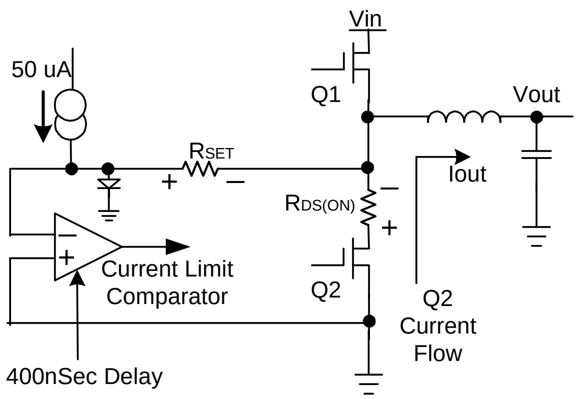


Figure 3 – Phase 1 Current Limit

The delay before current limit is activated will result in current pulses exceeding the calculated values during the delay period if a short circuit is applied during that time.

Microsemi
Integrated Products Division
11861 Western Avenue, Garden Grove, CA. 92841, 714-898-8121, Fax: 714-893-2570

THEORY OF OPERATION (CONTINUED)

OVER-CURRENT PROTECTION (PHASE 3)

The hysteretic phase has its own current limit protection because with it's very fast response time with a 100 nH inductor the upper MOSFET cannot be allowed to stay on during an output short circuit condition. The phase 3 over-current sensing uses the RDS(ON) of the upper MOSFET with a resistor RSET to determine the over current limit point. A current source draws 50uA through RSET which determines the required drop across the MOSFET RDS(ON) to initiate a current limit condition.

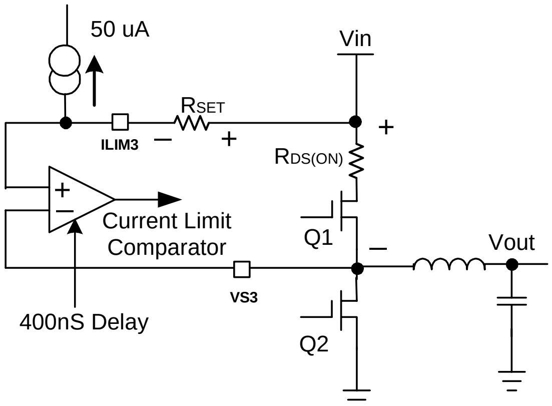


Figure 4 – Phase 3 Current Limit

Phase 3 RSET is calculated by:

$$\text{Rset} = \frac{\text{ILimit} \bullet \text{RDSon}}{50\text{uA}}$$

OVER VOLTAGE PROTECTION

An over voltage protection circuit monitors the output voltage and will latch all three phases off if an over voltage condition (greater than 2.35 V) is detected. Both MOSFETs for phase 3 will be held off and the lower MOSFETs for phase 1 and 2 will be held on to discharge the output capacitor till the output voltage drops below .85 volt, at .85 volts all MOSFETs will be turned off.

FAULT LOGIC

There are a number of possible states that will cause a fault condition that will disable the output MOSFET drivers. A fault condition will be caused by the following:

- Enable (ENA) pin being pulled low
- Over-current condition on either phase 1 or phase 3
- Over Voltage output $\geq$ 1.85V
- Under Voltage output $\leq$ 0.725V

In all cases except Over Voltage all MOSFET drivers will be latched off. For an Over Voltage fault the lower MOSFETs for phase 1 and 2 will be held on to discharge the bulk capacitance on the output till a lower limit of 0.725 volts is reached then all MOSFETS will be turned off.

To reset a fault it necessary to cycle the ENA pin low then back high or remove and reapply the input voltage VIN.

The Under Voltage monitor is not enabled until the output voltage has ramped up to the level commanded by the DACOUT pin and the PWGD output in high.

PWM FREQUENCY

An external resistor sets the PWM frequency from the ROSC pin to ground.

The equation for ROSC is:

$$\text{ROSC} = \frac{1}{(\text{K} \bullet \text{f}) + 100\text{e}-9}$$

where ROSC is in Ω, f is in Hz, K=105e-12

THEORY OF OPERATION (CONTINUED)

THEORY OF OPERATION FOR A BI-PHASE, LOADSHARE™ CONFIGURATION

The basic principle used in LoadSHARE™ in a multiple phase buck converter topology is that if multiple, identical, inductors have the same identical voltage impressed across their leads, they must then have the same identical current passing through them. The current that we would like to balance between inductors is mainly the DC component along with as much as possible the transient current. All inductors in a multiphase buck converter topology have their output side tied together at the output filter capacitors. Therefore this side of all the inductors has the same identical voltage.

If the input side of the inductors can be forced to have the same equivalent DC potential on this lead, then they will have the same DC current flowing. To achieve this requirement, phase 1 will be the control phase that sets the output operating voltage, under normal PWM operation. To force the current of phase 2 to be equal to the current of phase 1; a second feedback loop is used. Phase 2 has a low pass filter connected from the input side of each inductor. This side of the inductors has a square wave signal that is proportional to its duty cycle. The output of each LPF is a DC (+ some AC) signal that is proportional to the magnitude and duty cycle of its respective inductor signal.

The second feedback loop will use the output of the phase 1 LPF as a reference signal for an error amplifier that will compare this reference to the output of the phase 2 LPF. This error signal will be amplified and used to control the PWM circuit of phase 2. Therefore, the duty cycle of phase 2 will be set so that the equivalent voltage potential will be forced across the phase 2 inductor as compared to the phase 1 inductor. This will force the current in the phase 2 inductor to follow and equal the phase 1 inductor current.

With the LoadSHARE™ topology it is possible to imbalance the phases so that one phase will supply more current than the other under unique situations. The LX1677 will normally be used with the same supply voltages on phase 1 and 2 PWM inputs and will have equal currents in both phases.

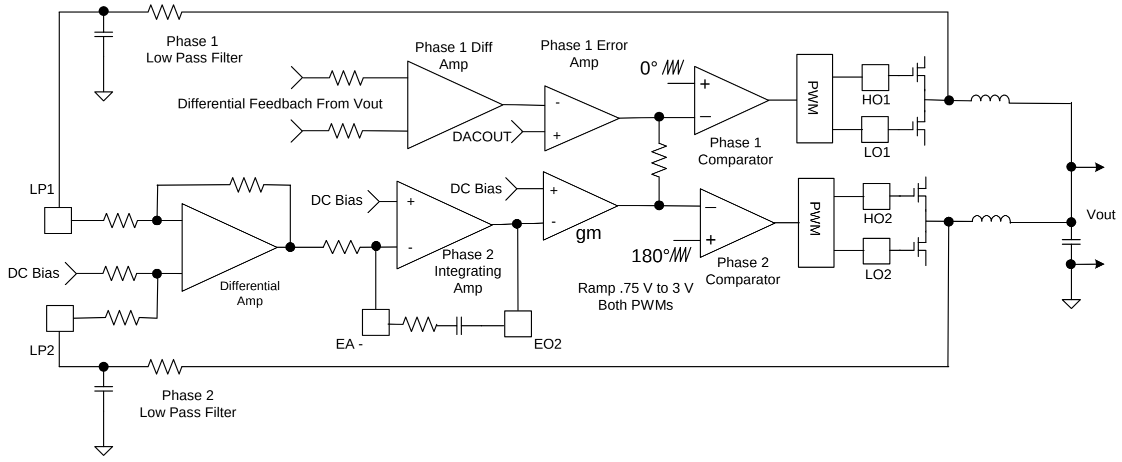


Figure 5 – LoadSHARE Control Loop

THEORY OF OPERATION (CONTINUED)

LOOP GAIN AUTOMATIC COMPENSATION

The PWM ramp shown in Figure 5 is automatically adjusted to keep its amplitude a fixed percentage of Vin over the range of 6 to 24 V input.

This maintains a constant loop gain that is set by the feedback networks around the error amplifiers independent of PWM input voltage.

TRANSIENT CORRECTION LOOP

Phase 3 is a Transient Correction Loop that can sum a large amount of current into the output node when required by an out of range condition. The differential feedback summing amplifier is connected directly to the output terminals and has sufficient bandwidth to follow any fast changes in output voltage. The feedback error voltage is compared to the commanded reference voltage (DACOUT) by two high speed comparators, I-Max and I-Min. The other inputs of these comparators are offset from the DACOUT as shown in Fig 6. If the error in output voltage exceeds the offset in either direction the appropriate MOSFET will be turned on to force current into or out of the output node to correct the voltage error. The very low value inductor (100nH) allows large amounts of current to be forced into or out of the output node very quickly.

When the Transient Correction Loop is switching it forces the appropriate upper or lower MOSFETs in phases 1 and 2 to stay on (100% or 0% duty cycle) until the error is corrected.

The two drivers for the Transient Correction Loop have outputs (I-Max) and (I-Min) that may be used to drive a half bridge to correct for both low and high output voltage conditions. This permits pulling the output low if an overshoot occurs due to a rapid reduction in load current. With a conventional Buck regulator rapid changes in the negative direction are not possible due to the low voltage available as a forcing function.

The two outputs (I-MAX and I-MIN) are completely independent. A single MOSFET and diode can be used to correct for voltage droop only or voltage overshoot only when driven by the appropriate output. If the I-MAX driver is not used the VC3 and VS3 pins must be connected to +5 volts.

Under normal operation the Transient Correction phase is only active for a very brief time during high di/dt loads on the output.

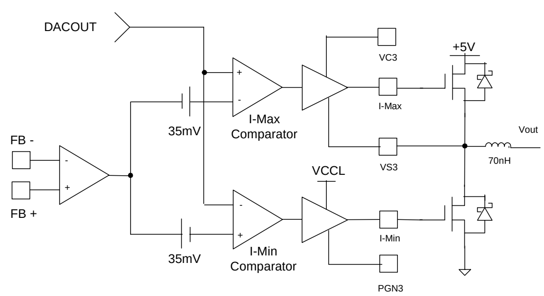


Figure 6 – Phase 3 Transient Correction Loop

APPLICATION NOTE

OUTPUT INDUCTOR

The output inductor should be selected to meet the requirements of the output voltage ripple in steady-state operation and the inductor current slew-rate during transient. The peak-to-peak output voltage ripple is:

$$V_{RIPPLE} = ESR \times I_{RIPPLE}$$

where

$$\Delta I = \frac{V_{IN} - V_{OUT}}{L} \times \frac{D}{f\,s}$$

ΔI is the inductor ripple current, L is the output inductor value and ESR is the Effective Series Resistance of the output capacitor.

ΔI should typically be in the range of 20% to 40% of the maximum output current. Higher inductance results in lower output voltage ripple, allowing slightly higher ESR to satisfy the transient specification. Higher inductance also slows the inductor current slew rate in response to the load-current step change, ΔI, resulting in more output-capacitor voltage droop. When using electrolytic capacitors, the capacitor voltage droop is usually negligible, due to the large capacitance

The inductor-current rise and fall times are:

$$T_{RISE} = L \times \frac{\Delta I}{\left(V_{IN} - V_{OUT}\right)}$$

and

$$T_{FALL} = L \times \frac{\Delta I}{V_{OUT}}$$

.

The inductance value can be calculated by:

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \times \frac{D}{f\,s}$$

OUTPUT CAPACITOR

The output capacitor is sized to meet ripple and transient performance specifications. Effective Series Resistance (ESR) is a critical parameter. When a step load current occurs, the output voltage will have a step that equals the product of the ESR and the current step, ΔI. In an advanced microprocessor power supply, the output capacitor is usually selected from ESR instead of capacitance or RMS current capability. A capacitor that satisfies the ESR requirements usually has a larger capacitance and current capability than strictly needed

The allowed ESR can be found by:

$$ESR \times \left(I_{RIPPLE} + \Delta I\right) < V_{EX}$$

Where IRIPPLE is the inductor ripple current, ΔI is the maximum load current step change, and VEX is the allowed output voltage excursion in the transient.

Electrolytic capacitors can be used for the output capacitor, but are less stable with age than tantalum capacitors. As they age, their ESR degrades, reducing the system performance and increasing the risk of failure. It is recommended that multiple parallel capacitors be used, so that, as ESR increase with age, overall performance will still meet the processor's requirements.

There is frequently strong pressure to use the least expensive components possible, however, this could lead to degraded long-term reliability, especially in the case of filter capacitors. Microsemi's demonstration boards use the CDE Polymer AL-EL (ESRE) filter capacitors, which are aluminum electrolytic, and have demonstrated reliability. The OS-CON series from Sanyo generally provides the very best performance in terms of long term ESR stability and general reliability, but at a substantial cost penalty. The CDE Polymer AL-EL (ESRE) filter series provides excellent ESR performance at a reasonable cost. Beware of off-brand, very low-cost filter capacitors, which have been shown to degrade in both ESR and general electrolytic characteristics over time.

INPUT CAPACITOR

The input capacitor and the input inductor, if used, are to filter the pulsating current generated by the buck converter to reduce interference to other circuits connected to the same 5V rail. In addition, the input capacitor provides local de-coupling the buck converter. The capacitor should be rated to handle the RMS current requirements. The RMS current is:

$$I_{RMS} = I_L \sqrt{d(0.5 - d)} \quad \text{for } d \le 0.5$$

Where I_L is the inductor current and d is the duty cycle. The maximum RMS value of $0.25I_L$ will occur when d = 25% or 75%.

Microsemi
Integrated Products Division
11861 Western Avenue, Garden Grove, CA. 92841, 714-898-8121, Fax: 714-893-2570

APPLICATION NOTE (CONTINUED)

SOFT-START CAPACITOR

An external soft-start capacitor is connected to the DACOUT pin and will be charged, or discharged, at a linear rate by the internal 50uA bi-directional current source after the UVLO circuit has been satisfied. Whenever the VID code is changed during normal operation the soft-start capacitor will determine the rate of change at the output.

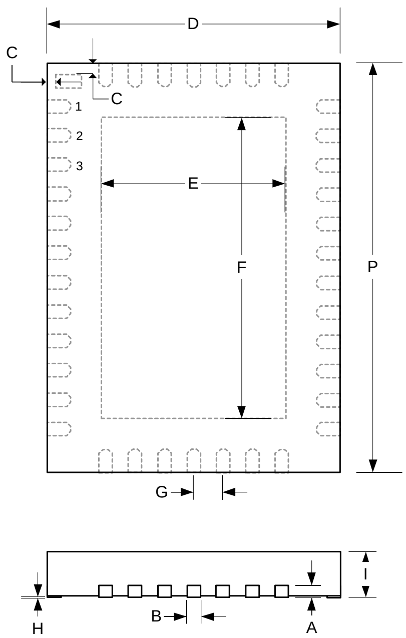
PROGRAMMING THE OUTPUT VOLTAGE

Output voltage is determined by the internal 5 bit DAC. The DAC inputs are the Voltage Identification (VID) 0-4 lines, the VID table lists the available output voltages for the corresponding VID codes.

There are no external resistor dividers to program output voltage and only the steps listed are available.

PACKAGE DIMENSIONS

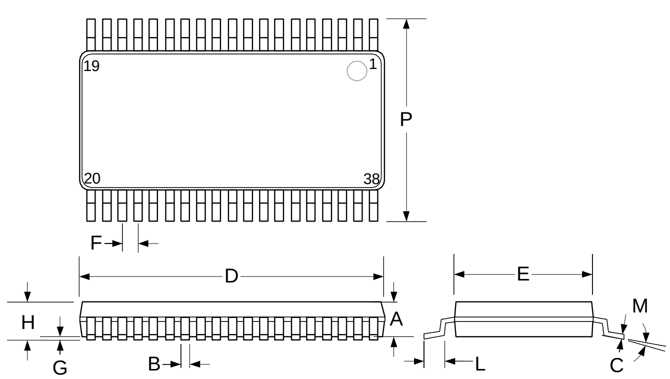
LQ 38-Pin Micro Leadframe Package (MLPQ)



Dim	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	0.20 REF		0.0078 REF	
B	.18	.30	0.007	0.011
C	.18	.18	0.007	.007
D	5.00 BSC		.196 BSC	
E	3.00	3.25	0.118	0.127
F	5.00	5.25	.196	.206
G	0.50 BSC		0.019 BSC	
H	0	0.05	0	0.019
I	0.70	0.80	0.027	0.031

Note: Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

PW 38-Pin Thin Small Shrink Outline (TSSOP)



Dim	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	0.85	0.95	0.033	0.037
B	0.19	0.25	0.19	0.009
C	0.09	0.20	0.003	0.008
D	9.60	9.80	0.378	0.390
E	4.30	4.50	0.169	0.176
F	0.50 BSC		0.0196 BSC	
G	0.05	0.15	0.002	0.005
H	–	1.10	–	0.043
L	0.50	0.75	0.020	0.030
M	0°	8°	0°	8°
P	6.25	6.50	0.246	0.256
*LC	–	0.10	–	0.004

NOTES