BelaSigna R281

Always-Listening, Voice Trigger Solution

Introduction

BelaSigna® R281 is an ultra−low−power voice trigger solution for a wide range of consumer electronic devices. In a typical application BelaSigna R281 is "always listening" and will detect a single, user−trained trigger phrase, asserting a wake−up signal when this trigger phrase is detected.

"Always−listening" key phrase detection with an average power consumption of less than 300 μW (not including the power consumption of the microphone) preserves Standby battery life.

BelaSigna R281 is an ultra−miniature solution that is available in both a 5 mm x 5 mm QFN32 package (488AM) and a 2.42 mm x 2.74 mm WLCSP package (available soon). It can be designed onto a single layer PCB with 4 mil routing and with a minimal amount of external components.

An external, I^2C host controller is required to configure the device for operation.

Key Features

Proven Ultra−Low−Power Digital Signal Processing (DSP) Technology

- Audio DSP Technology Originally Developed for Hearing Aids Offers the Required Computational Power at Extremely Low Current Consumption
- < 300 μW Average Current Consumption (not including microphone)

Mixed−Signal System−on−Chip (SoC)

- Audio−grade, Analog Input with Onboard Pre−amplifier
- Built−in, Regulated Voltages Including Onboard Microphone Bias (1 V or 2 V) for Power Efficient Operation
- Supports Analog or Digital Microphone Input

Interfaces and Peripherals

- I^2C−based Device Configuration and Control
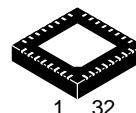- GPIO Wake Signal
- Internal Oscillator

Applications

- Mobile Phones
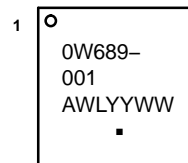- Tablets
- Portable Electronic Devices
- Wearables
- Toys

ON Semiconductor®

MARKING DIAGRAM

QFN32
CASE 488AM

```
          1
       0W689−
       001
       AWLYYWW
          ▪
```

0W689−001 = Specific Device Code
A   = Assembly Location
WL   = Wafer Lot
YY   = Year
WW   = Work Week
▪   = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

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Figures and Data

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Input Voltage on any Digital Pin		−0.3	3.8	V
Input Voltage on any Analog Pin		−0.3	3.8	V
Input Voltage on any Supply Pin		−0.3	3.8	V
Current on any Digital Pin			± 5	mA
Current on any Analog Pin			± 10	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max		Units
Power Supply Applied to VBAT	VBAT	1.75	1.8	QFN	3.63	V
				WLCSP	1.98	
Power Supply Applied to VDDO	VDDO	1.75	1.8	3.63		V
Internal Oscillator Clock Frequency		1	2.56	20		MHz
Ambient Operating Temperature Range	Ta	−40		85		°C

Table 3. ESD AND LATCH−UP CHARACTERISTICS

Parameter	Conditions	Max	Units
ESD – Human Body Model	JEDEC JS − 001 − 2010, all pins	2000	V
ESD – Charged Device Model	JESD22 − C101 − E, all pins	750	V
ESD – Machine Model	JESE22 − A115 − C, all pins	250	V
Latch − Up	JEDEC STD − 78, all pins	± 100	mA

Electrical Performance Specifications

Typical Values

Unless otherwise noted, Typ values specify the typical values based on design and characterization data under normal operating conditions. Normal operating conditions include a supply voltage (VBAT) of 1.8 V and an operating temperature of 25°C. For specific blocks, the details of the normal operation conditions are described in their respective sections.

Minimum and Maximum Values

Unless otherwise noted, Min and Max values specify the designed range or measurement range and are guaranteed by design and/or characterization.

Min and Max values specified may be based on factory production test limits, design, or characterization data.

Normal Operating Conditions

Unless otherwise noted, normal operating conditions indicate an ambient temperature Ta = 25°C and a supply voltage VBAT = 1.8 V. VDDD and VDDA are calibrated to their preset factory calibration settings and correspond to their respective Typ values. VDDO is powered externally at 1.8 V. No external loads are applied to digital I/O or analog pins.

Table 4. SYSTEM DC ELECTRICAL CHARACTERISTICS

Typical operating conditions (Ta = 25°C, VBAT=VDDO=1.8 V, VDDD=1.4 V) unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Average Run Mode Current	IDD	VBAT=VDDA=1.8 V, charge pump disabled Assumes a ratio of speech present versus quiet environment of 20/80		170		μA

Table 5. DIGITAL I/O PINS (I2C, WAKE_UP, DMIC) DC ELECTRICAL CHARACTERISTICS

Typical operating conditions (Ta = 25°C, VDDO = 1.8 V, Pull – up/Pull – down Enabled) unless otherwise noted

Parameter	Symbol	Conditions		Min	Typ	Max	Units
VDDO Supply Voltage Range	VDDO			1.25	1.8	3.63	V
Output Low Level	V_{ol}	I_{ol} = 4 mA			0	0.2 x VDDO	V
Output High Level	V_{oh}	I_{ol} = –4 mA		0.8 x VDDO	VDDO		V
Input Low Level	V_{il}				0	0.2 x VDDO	V
Input High Level	V_{ih}			0.8 x VDDO	VDDO		V
Pull–Up Resistance	R_{pu}	Non–I2C	VDDO = 1.8 V	80	122	160	kΩ
			VDDO = 3.3 V	30	48	60	
		I2C (strong/weak)	VDDO = 1.8 V	0.8 / 8	1 / 10	1.2 / 12	
			VDDO = 3.3 V	0.8 / 8	1 / 10	1.2 / 12	
Pull–Down Resistance	R_{pd}	VDDO = 1.8 V		120	168	210	kΩ
		VDDO = 3.3 V		30	60	80	
Pin Capacitance	C_{pd}				5		pF
Maximum Output Current	I_{ol}, I_{oh}					± 4	mA
Input Leakage Current	I_l					± 1	μA

Table 6. VDDA REGULATOR DC & AC ELECTRICAL CHARACTERISTICS

Typical operating conditions (Ta = 25°C), unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage	VDDA	CL = 1 μF	1.8	1.98	2.0	V
Load Current					4	mA
Load Regulation				5		mV/mA
Line Regulation				20		mV/V
PSRR		@ 1 kHz unloaded	20			dB

Table 7. VREG REGULATOR DC & AC ELECTRICAL CHARACTERISTICS

Typical operating conditions (Ta = 25°C), unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage	VREG	CL = 1 μF	0.95	1.0	1.05	V
Load Current					2	mA
Load Regulation					20	mV/mA
Line Regulation					5	mV/V
PSRR		@ 1 kHz unloaded	40			dB

Table 8. VDDD REGULATOR DC & AC ELECTRICAL CHARACTERISTICS

Typical operating conditions (Ta = 25°C), unless otherwise noted

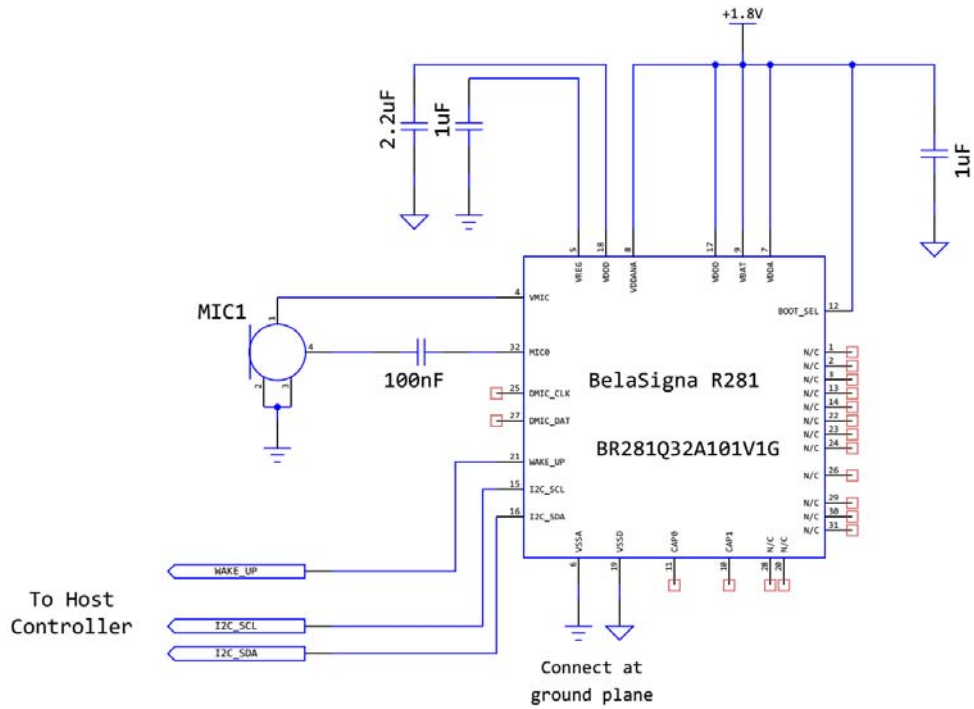| Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage	VDDD	CL = 1 μF	1.2	1.4	1.7	V
Load Current					15	mA
Load Regulation					10	mV/mA
Line Regulation					20	mV/V
PSRR		@ 1 kHz unloaded	20			dB

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System Diagrams

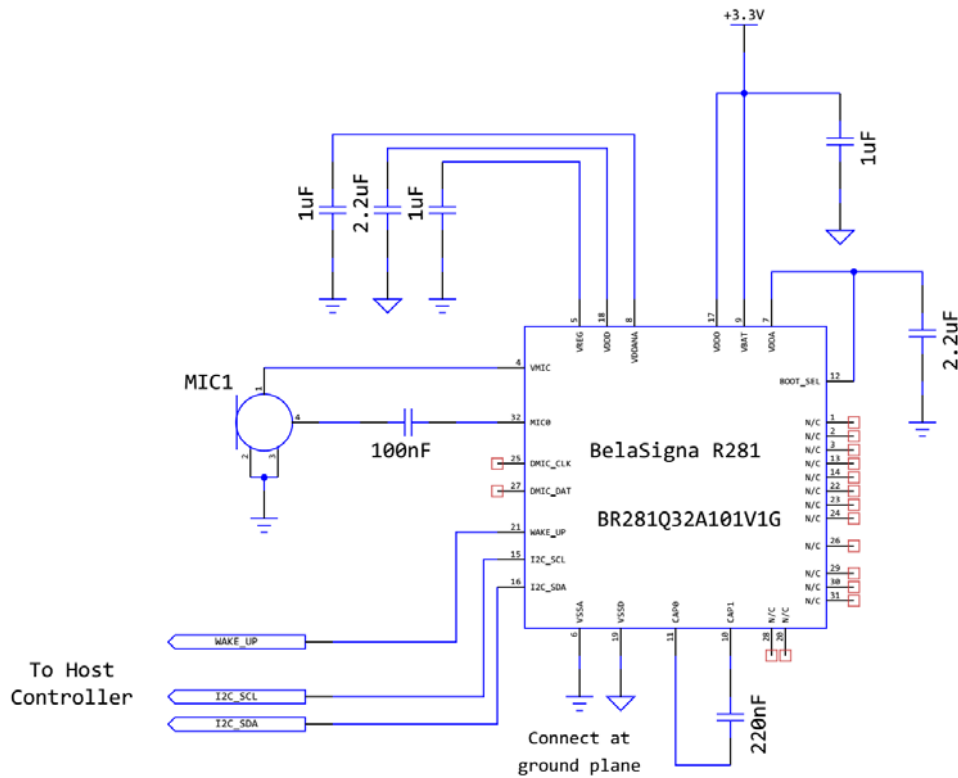**Figure 1. BelaSigna R281 System Diagram (Analog Microphone, VBAT = 1.8 V)**

Figure 2. BelaSigna R281 System Diagram (Analog Microphone, VBAT = 3.3 V)
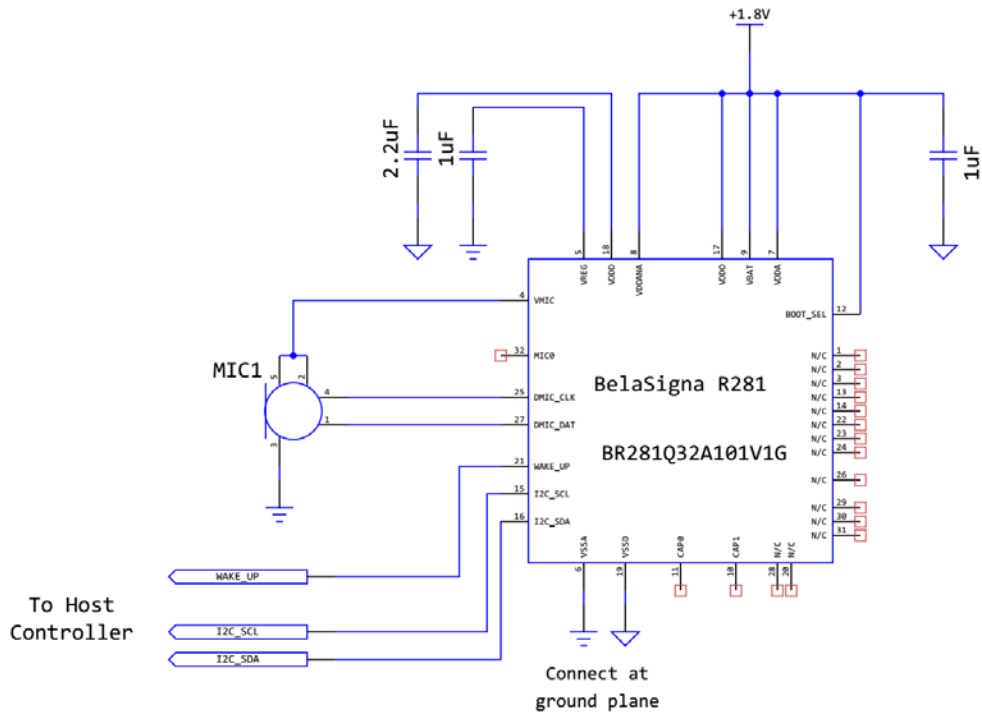
Figure 3. BelaSigna R281 System Diagram (Digital Microphone, VBAT = 1.8 V)

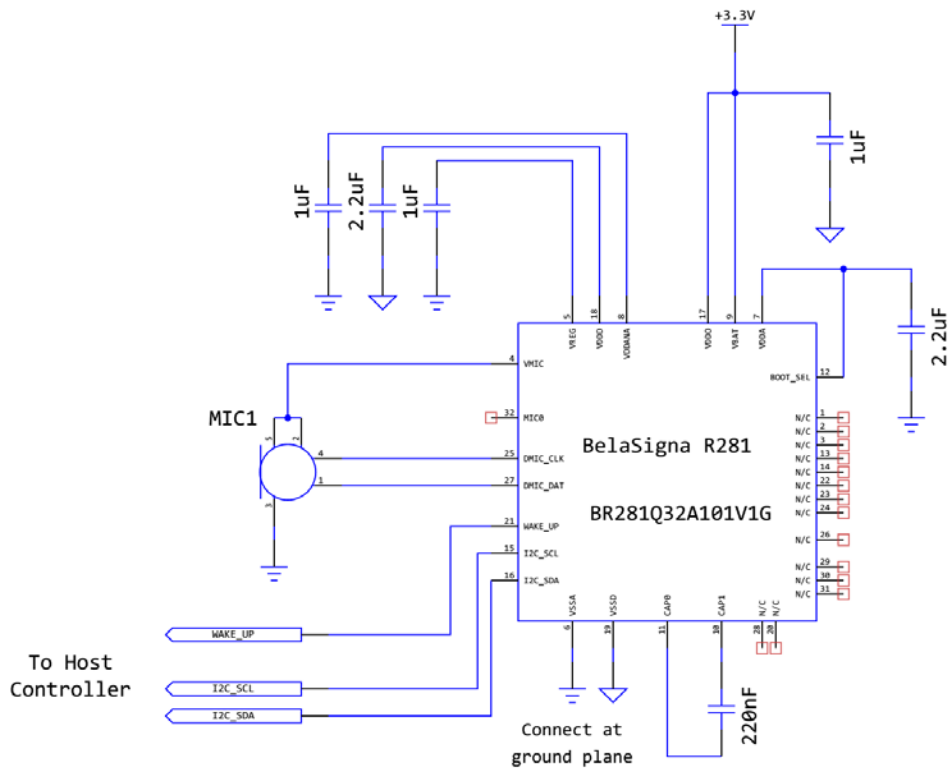**Figure 4. BelaSigna R281 System Diagram (Digital Microphone, VBAT = 3.3 V)**

Description of Operation

Efficient implementation of the trigger phrase recognition algorithm is accomplished through the use of three processing units running concurrently. In addition to the main DSP core performing system configuration and signal processing, an input/output processor continuously collects frames of input speech signals which are analyzed by a highly optimized frequency domain co−processor.

There are two main modes of operation: Recognition Mode and Training Mode.

Recognition Mode

When in Recognition Mode, the entire system remains in an extremely low−power, "always−on" state continuously listening for speech. When speech is detected, the algorithm proceeds to extract features from the collected audio data, comparing these features to a known set of data computed during the training process. If the features appear to be similar enough to the trained feature data, a match is indicated on the WAKE_UP pin.

Once the feature extraction and comparison is complete, the system returns to its original low−power state, once again waiting until speech is detected.

Training Mode

Before BelaSigna R281 can be placed into Recognition Mode, it must be trained. Training involves recording and analyzing three utterances of a *trigger phrase*. A trigger phrase can be any collection of words or sounds, in any language, up to a maximum length of approximately 1.5 seconds.

When speaking a given phrase, a human will naturally say the same phrase subtly different each time. Having multiple instances of the same phrase, each slightly different, helps to make the matching algorithm more robust.

Training must be performed in a quiet environment, or the trigger phrase match results in Recognition Mode will be unpredictable. BelaSigna R281 is placed into Training Mode by issuing an appropriate SetMode command via I^{2}C. The algorithm stores relevant feature data from the three separate utterances of the trigger phrase, also known as *training templates*.

Once training is complete, the training templates can be read from memory and stored offline. This template data can then be loaded into memory in the event of a power cycle and the device can be placed directly into Recognition Mode, thus avoiding the need to re−train the device. This same procedure can be used to recognize multiple trigger phrases, provided they have each been individually trained and stored offline. Only one trigger phrase can be active at any one time.

Refer to AND9267/D for more information on the different modes, as well as a description of the I^{2}C host control protocol.

Initial Power−On State

When BelaSigna R281 is powered on, the device will perform a brief initialization procedure and then wait for a connection to be made from an external host via I^{2}C. At this point, the host controller must connect to BelaSigna R281 and load its memory with the algorithm binary image, as well as the training template data. Once this has been completed, the device can be put into Recognition Mode. If no training template data is available (e.g. the training procedure has never been performed), then BelaSigna R281 must be placed into Training Mode and the training procedure performed before entering Recognition Mode.

Whenever power is removed from the device, the contents of memory are lost and must be re−loaded.

For more information refer to AND9267/D.

System Performance

Recognition Rate

Performance has been measured in various noise conditions and is shown in Figure 5. Tests were performed in a sound isolation booth with a series of pre–recorded trigger and non–trigger phrases playing continuously, mixed

with varying levels of noise. Recognition rate is 100% in a quiet environment (no noise playing). The system was trained in a quiet environment. In all cases, the false trigger rate (the number of times the system triggered on a non–trigger phrase) was 0%.
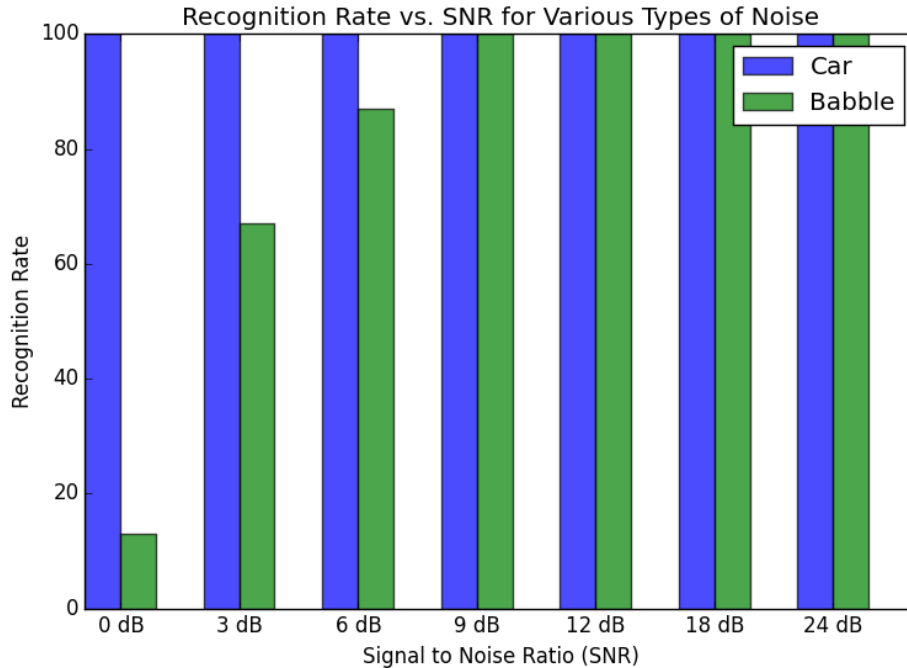

Figure 5. Recognition Rate Versus SNR

Current Consumption

Average current consumption was also measured with the device operating in a pure noise environment with no speech present. The results are presented in Table 9.

Table 9. AVERAGE CURRENT CONSUMPTION

Condition	Average Current Consumption (uA), VBAT = 1.8 V
Quiet Environment	160
Babble Noise	170

*Not including microphone current consumption

Single User Operation

Because BelaSigna R281 performs recognition based on a training procedure performed by a specific individual, recognition of the trigger phrase is effectively "single–user". Only the person who trained the system (or an individual with an extremely similar voice print) will be able to reliably trigger the device.

Digital Interfaces

Wake Up Pin

The Wake Up pin is a digital output (referenced to VDDO) which is used to indicate that the trigger phrase was detected. It is intended to be connected to a digital input of an external

host, and its behavior (active high versus active low and duration) is configurable via I^2C.

For more information refer to AND9267/D.

Boot Select Pin

This pin is reserved for future purpose and must be connected to VDDA.

Inter−IC Communication (I^2C) Interface

The I^2C interface is an industry–standard interface that can be used for high–speed transmission of data between BelaSigna R281 and an external device. The interface operates at speeds up to 100 Kbit/sec, and always operates in slave mode at an address of 0x62.

Digital Microphone (DMIC) Interface

The digital microphone interface provides a means of interfacing a digital microphone to the system instead of an analog microphone. When the device is configured to use a digital microphone input instead of an analog microphone input (the default), an appropriate clock is output on the DMIC_CLK pin and device accepts PDM signals from a digital microphone on the DMIC_DAT input pin. A separate algorithm binary image is available supporting a digital microphone input.

Figure 6 shows the timing of the DMIC interface. For more information refer to AND9267/D.
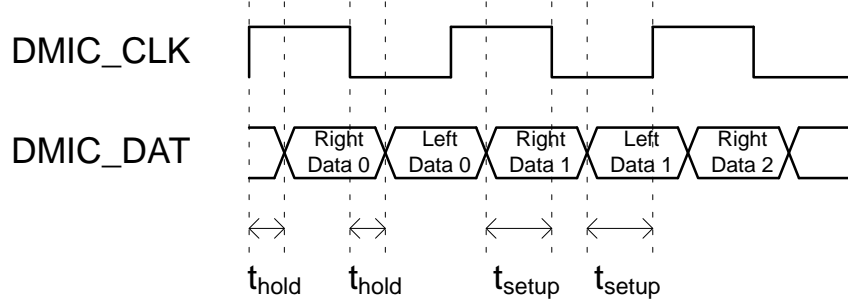
Figure 6. DMIC Timing Diagram

Mechanical Information and Circuit Design Guidelines

BelaSigna R281 is available in two packages:
1. A 5 x 5 mm QFN32 package
2. A 2.42 x 2.74 mm ultra−miniature wafer−level chip scale package (WLCSP)

Table 10. PIN DESCRIPTION

QFN32 Pin #	WLCSP Ball Index	Name	Description	Pad Type	Pull
9	A1	VBAT	Main power supply	P	
6	F2	VSSA	Analog ground	P	
8	N/A	VDDANA	Analog supply voltage (output), capacitor to VSSA, or connected to VBAT (max. 1.98 V)	A	
5	E1	VREG	Analog supply voltage (output), capacitor to VSSA	A	
11	B2	CAP0	Charge pump capacitor to CAP1	A	
10	D2	CAP1	Charge pump capacitor to CAP0	A	
7	C1	VDDA	Analog supply voltage (output), capacitor to VSSA, or connected to VBAT (max. 1.98 V)	P	
4	H2	VMIC	Analog microphone supply output	A	
1	I1	N/A	No connection	NC	
32	K1	MIC0	Analog microphone input	AI	
31	M1	N/A	No connection	NC	
30	L2	N/A	No connection	NC	
29	M3	N/A	No connection	NC	
3	K3	N/A	No connection	NC	
2	J2	N/A	No connection	NC	
14	A3	N/A	No connection	NC	
13	C3	N/A	No connection	NC	
12	E3	BOOT_SEL	Boot selection (always connect to VDDA)	AI	
17	A5	VDDO	Digital I/O supply, capacitor to VSSD, typically connected to VBAT	P	
18	E5	VDDD	Digital supply, capacitor to VSSD	P	
19	C5	VSSD	Digital core and I/O ground, connect to VSSA on PCB	P	
28	I3	N/A	No connection	NC	
21	K5	WAKE_UP	Wake up signal (output)	DIO	
22	I5	N/A	No connection	NC	
23	H4	N/A	No connection	NC	
24	F4	N/A	No connection	NC	
26	J4	N/A	No connection	NC	
27	L4	DMIC_DAT	Digital microphone data input (optional)	DIO	
15	B4	I2C_SCL	I^{2}C clock	DIO	PU
16	D4	I2C_SDA	I^{2}C data	DIO	PU (Note 1)
25	M5	DMIC_CLK	Digital microphone clock (optional)	DIO	PU (Note 2)
20	G3	N/A	No connection	NC	

1. The value of the I^{2}C pull−ups is 10 K
2. Pull−up is disabled when the DMIC interface is enabled.

Legend:

Type: A = analog; D = digital; I = input; O = output; P = power; NC = not connected
Pull: PU = pull up; PD = pull down
All digital pads have a Schmitt trigger input

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Reflow Information

The reflow profile depends on the equipment that is used for the re−flow and the assembly that is being re−flowed. Information from JEDEC Standard 22−A113D and J−STD−020D.01 can be used as a guideline.

Electrostatic Discharge (ESD) Device

CAUTION: ESD sensitive device. Permanent damage may occur on devices subjected to high−energy electrostatic discharges. Proper ESD precautions in handling, packaging and testing are recommended to avoid performance degradation or loss of functionality.

Ordering Information

To order BelaSigna R281, please contact your account manager and ask for part number BR281Q32A101V1G.

Chip Identification

Chip identification information can be retrieved using the GetChipID I^{2}C command. The key identifier components and values are as follows for the different package options:

Refer to AND9267/D for more details regarding supported I^{2}C commands.

Company or Product Inquiries

For more information about ON Semiconductor Sales products or services visit our website at http://onsemi.com.

ORDERING INFORMATION

Part Number	Package Option	Chip ID
BR281Q32A101V1G	QFN32	0x5000

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PACKAGE DIMENSIONS

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

TOP VIEW

DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS

DETAIL B
ALTERNATE
CONSTRUCTION

SIDE VIEW

BOTTOM VIEW
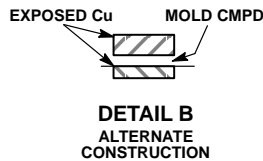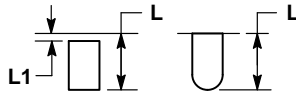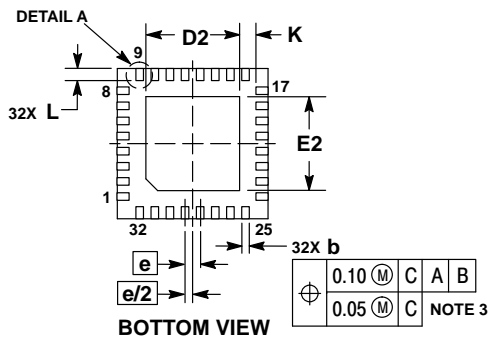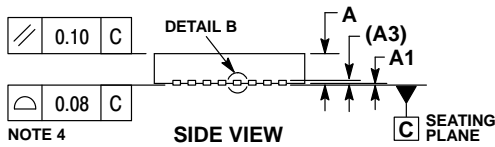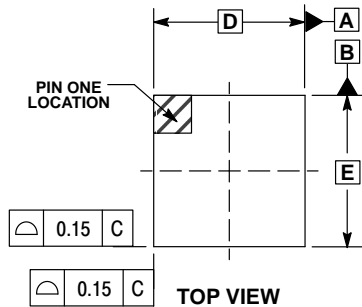
NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	–––	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	–––
L	0.30	0.50
L1	–––	0.15

RECOMMENDED SOLDERING FOOTPRINT*
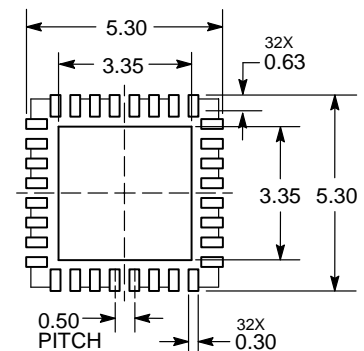
DIMENSION: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PUBLICATION ORDERING INFORMATION

R281/D