P-Channel Logic Level Enhancement Mode Power MOSFET

MTDA0P10FP

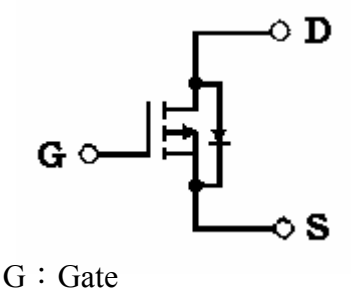
BV_{DSS}	-100V
I_D	-22A
$R_{DSON(MAX)}$	120mΩ

Features

- Low Gate Charge
- Simple Drive Requirement
- Pb-free lead plating package

Equivalent Circuit

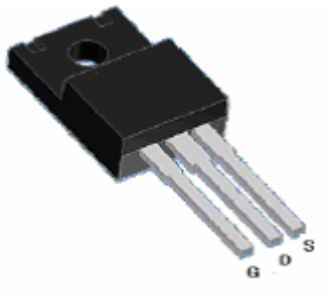
MTDA0P10FP



G：Gate
D：Drain
S：Source

Outline

TO-220FP



Absolute Maximum Ratings (Tc=25°C, unless otherwise noted)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	±20	
Continuous Drain Current @ Tc=25°C	I_D	-22	A
Continuous Drain Current @ Tc=100°C	I_D	-15	
Pulsed Drain Current *1	I_{DM}	-75	
Avalanche Current	I_{AS}	-15	
Avalanche Energy @ L=0.1mH, I_D=-15A, R_G=25Ω	E_{AS}	22.5	mJ
Repetitive Avalanche Energy @ L=0.05mH *2	E_{AR}	11.25	
Total Power Dissipation @Tc=25℃	Pd	62	W
Total Power Dissipation @Tc=100℃		31	
Operating Junction and Storage Temperature Range	Tj, Tstg	-55~+175	°C

Note : *1. Pulse width limited by maximum junction temperature
*2. Duty cycle ≤ 1%

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j-c}$	2.42	°C/W
Thermal Resistance, Junction-to-ambient, max	$R_{th,j-a}$	62.5	°C/W

Characteristics (Tc=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	-100	-	-	V	V_{GS}=0, I_D=-250μA
$V_{GS(th)}$	-1.5	-2.5	-4.0	V	V_{DS} =V_{GS}, I_D=-250μA
I_{GSS}	-	-	±100	nA	V_{GS}=±20, V_{DS}=0
I_{DSS}	-	-	-1	μA	V_{DS} =-80V, V_{GS} =0
	-	-	-25		V_{DS} =-70V, V_{GS} =0, T_J=125°C
$I_{D(ON)}$ *1	-22	-	-	A	V_{DS} =-5V, V_{GS} =-10V
$R_{DS(ON)}$ *1	-	105	120	mΩ	V_{GS} =-10V, I_D=-11A
G_{FS} *1	-	8	-	S	V_{DS} =-5V, I_D=-11A
Dynamic					
Qg *1, 2	-	58	-	nC	I_D=-11A, V_{DS}=-80V, V_{GS}=-10V
Qgs *1, 2	-	13.8	-		
Qgd *1, 2	-	10.5	-		
$t_{d(ON)}$ *1, 2	-	15	-	ns	V_{DS}=-10V, I_D=-1A, V_{GS}=-10V, R_G=6Ω
tr *1, 2	-	67	-		
$t_{d(OFF)}$ *1, 2	-	50	-		
t_f *1, 2	-	50	-		
Ciss	-	7760	-	pF	V_{GS}=0V, V_{DS}=-25V, f=1MHz
Coss	-	1683	-		
Crss	-	1643	-		
Rg	-	4.5	-	Ω	V_{GS}=15mV, V_{DS}=0, f=1MHz
Source-Drain Diode					
I_S *1	-	-	-22	A	
I_{SM} *3	-	-	-75		
V_{SD} *1	-	-	-1.3	V	I_F=I_S, V_{GS}=0V
trr	-	150	-	ns	I_F=-5A, dI_F/dt=100A/μs
Qrr	-	830	-	nC	

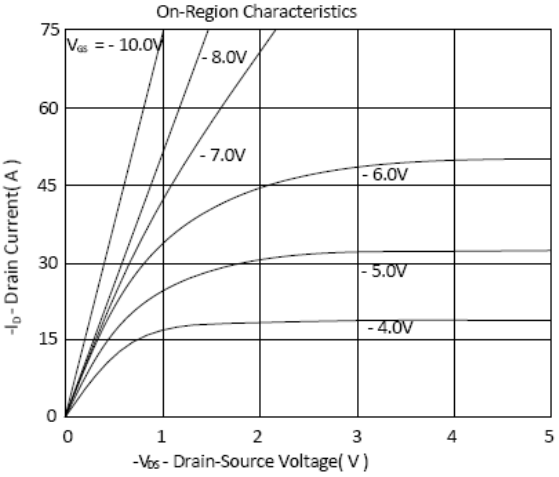
Note : *1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
*2.Independent of operating temperature
*3.Pulse width limited by maximum junction temperature.

Ordering Information

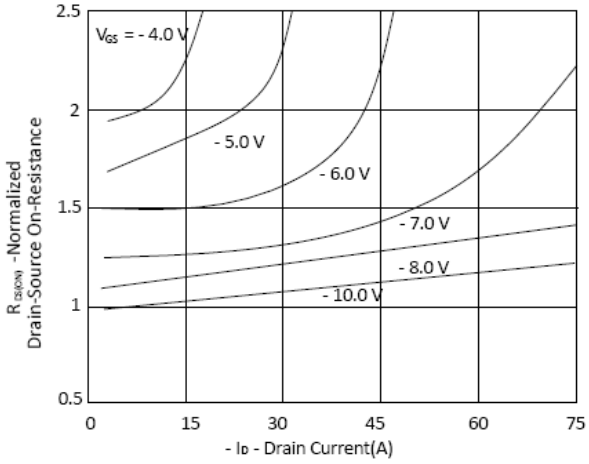
Device	Package	Shipping
MTDA0P10FP	TO-220FP (Pb-free lead plating package)	50 pcs / tube, 20 tubes/box, 4 boxes/carton

Typical Characteristics

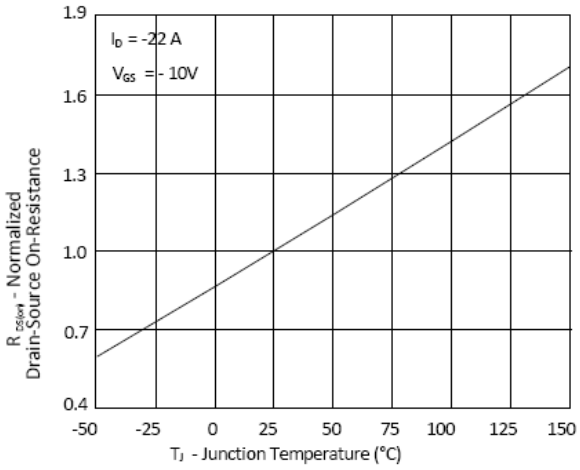
On-Region Characteristics



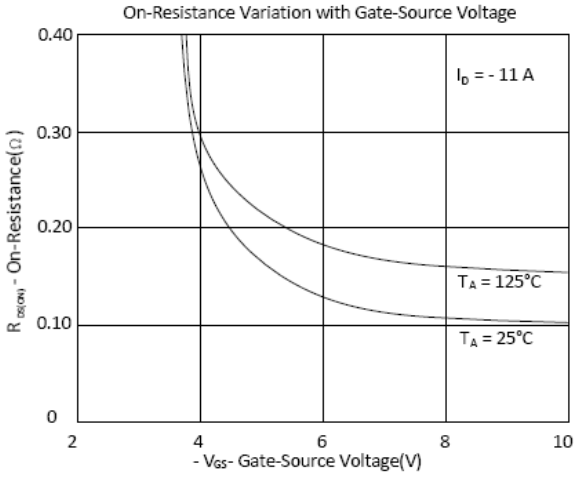
On-Resistance Variation with Drain Current and Gate Voltage



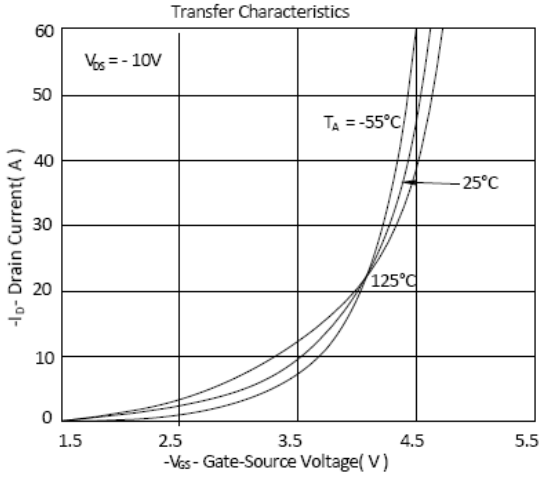
On-Resistance Variation with Temperature



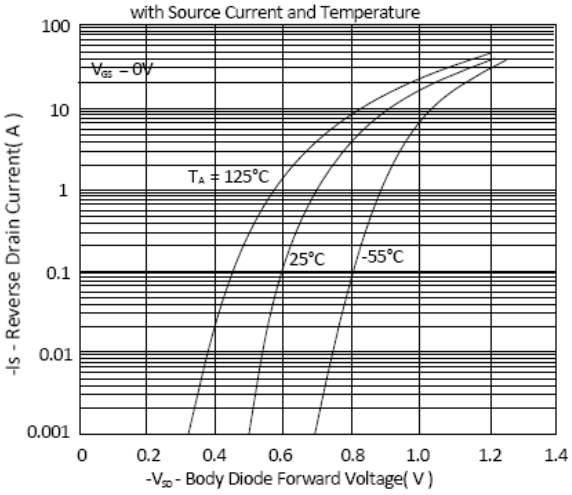
On-Resistance Variation with Gate-Source Voltage



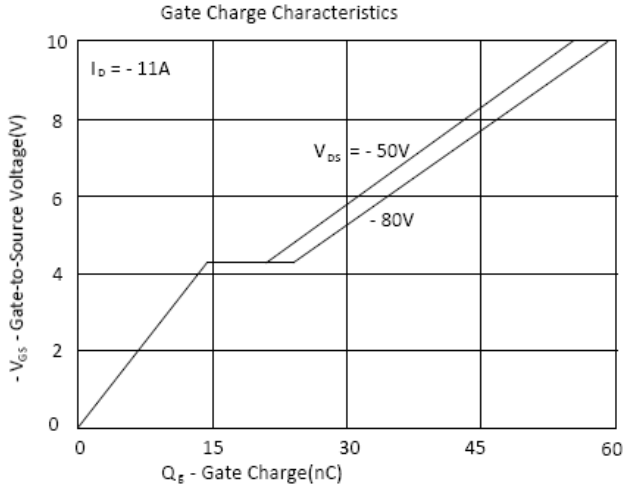
Transfer Characteristics

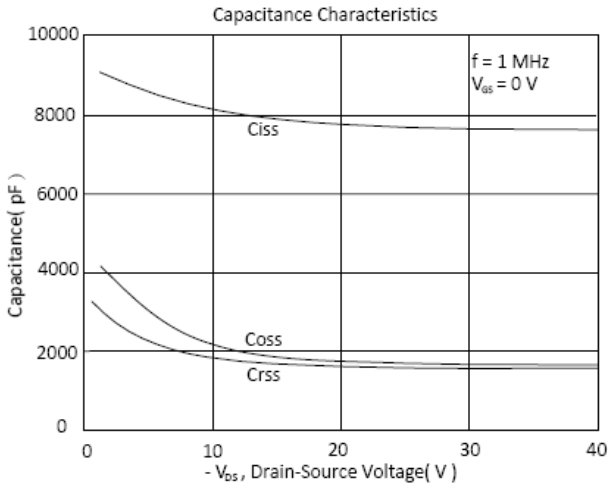


Body Diode Forward Voltage Variation
with Source Current and Temperature



Typical Characteristics(Cont.)

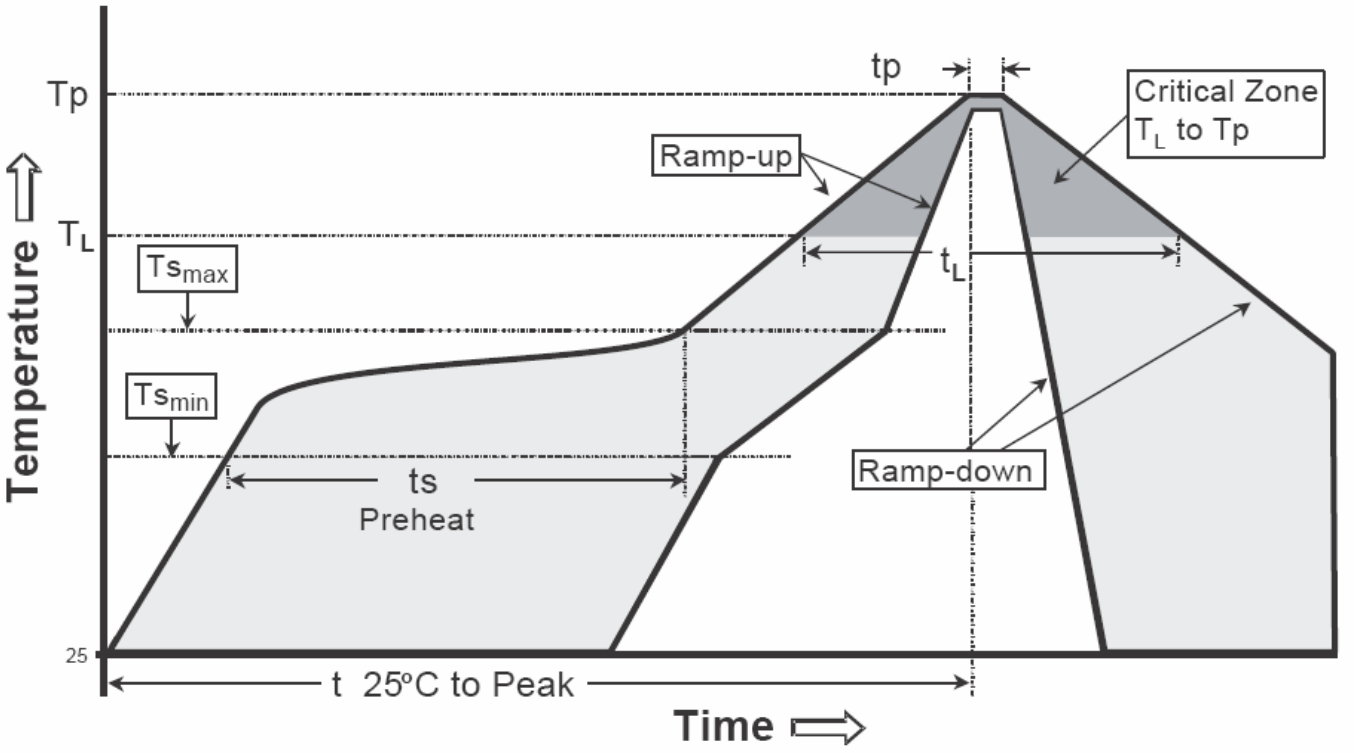




Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

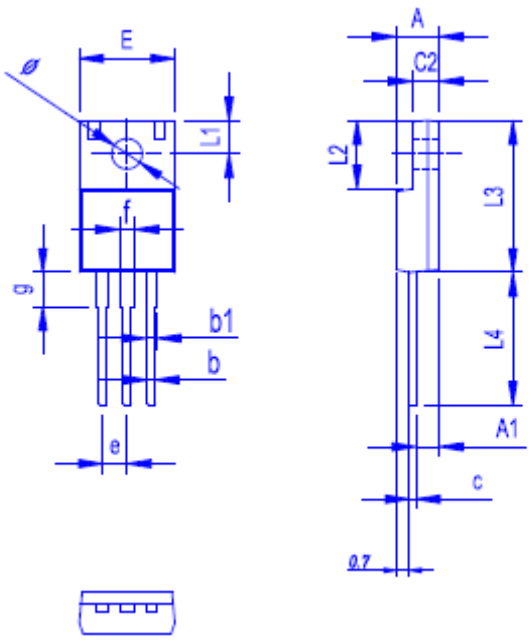
Recommended temperature profile for IR reflow



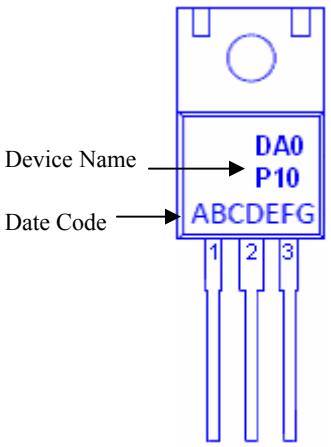
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(T_S min) −Temperature Max(T_S max) −Time($t_{s\ min}$ to $t_{s\ max}$)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (T_L) − Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-220FP Dimension



Marking:



Style: Pin 1.Gate 2.Drain 3.Source

3-Lead TO-220FP Plastic Package
CYStek Package Code: FP

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1654	0.1890	4.20	4.80	L2	0.2717	0.2953	6.90	7.50
A1	0.0768	0.1122	1.95	2.85	L3	0.6181	0.6417	15.70	16.30
b	0.0256	0.0413	0.65	1.05	L4	0.5315	0.5709	13.50	14.50
b1	0.0354	0.0591	0.90	1.50	Φ	0.1181	0.1339	3.00	3.40
c	0.0217	0.0315	0.55	0.80	e	0.0925	0.1083	2.35	2.75
c2	0.0984	0.1220	2.50	3.10	f	0.0512	0.0748	1.30	1.90
E	0.3819	0.4055	9.70	10.30	g	0.1339	0.1496	3.40	3.80
L1	0.1260	0.1496	3.20	3.80					

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead : Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.