65536-BIT DYNAMIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION

The MMN 4164 is a MOS dynamic random access memory circuit organized as 65536 words by 1 bit. The use of dynamic circuitry throughout, including the 512 sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or internal and external operating margins.
Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between dynamic RAM generations.
Multiplexed address inputs permits the MMN4164 to be packaged in a standard 16-pin DIP with only 15 pins required for basic functionality.
The output of the MMN4164 can be held valid indefinitely by holding $\overline{CAS}$ active low. This is quite useful since a refresh cycle can be performed while holding data valid from a previou cycle.

FEATURES

- single +5 V (+/−10%) supply operation
- on chip substrate bias generator for optimum performance
- low power 300 mW active max
  28 mW standby max
- 150 ns access time, 270 ns cycle time (MMN 4164.1)
- 200 ns access time, 330 ns cycle time (MMN 4164.2, .3)
- 250 ns access time, 410 ns cycle time (MMN 4164.4)
- indefinite Dout hold using CAS/control
- common I/O capability using "early write"
- Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- all inputs TTL compatible, low capacitance, and protected against static charge
- 128 refresh cycles (2 mS)

ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage relative to V_{SS}	−0.5 V to +7.0 V
V_I, V_O	Voltage on anyI/O terminal	−2.0 V to +7.0 V
T_A	Operating temperature	0 C to +70 C
T_s	Storage temperature (plastic)	−55 C to +125 C
Ts	Storage temperature (ceramic)	−65 C to +150 C
P_{tot}	Total power dissipation	1 W

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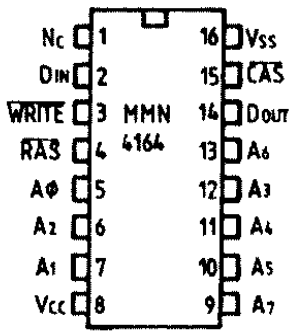
CONNECTION DIAGRAM



PIN FUNCTIONS

A0...A7	Address inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read Write Input
Vcc	Power (+5 V)
Vss	Ground

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to 70°C)

	PARAMETER	MMN 4164.2			MMN 4164.1,.3,.4			UNIT	NOTES
		MIN	TYP	MAX	MIN	TYP	MAX		
V_{CC}	Supply voltage	4,5	5,0	5,5	4,75	5,0	5,25	V	1
V_{iH}	Input high (logic 1) voltage	2,4	—	5,5	2,4	—	5,25	V	1
V_{iL}	Input low (logic 0) voltage*)	−0,3	—	0,8	−0,3	—	0,8	V	1

*) Input low voltage may reach −2V for a time period shorter than 40 ns.

DC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5,0 V ±5% or 10% depending on type specified above)

	PARAMETER	CONDITIONS	VALUE		UNIT	NOTES
			MIN	MAX		
I_{CC0}	Operating current ($\overline{RAS}$ – $\overline{CAS}$ cycle)	$t_{RLRL} = t_{RLRL}$min T = 25°C	—	55	mA	2
I_{CCr}	Standby current	$\overline{RAS} = V_{ih}$ DO = High Z	—	5	mA	2
I_{li}	Input leakage	V_i = 0...Vcc	−10	10	µA	
I_{lo}	Output leakage	Vo = 0...Vcc DO = High Z $\overline{RAS}$ $\overline{CAS}$ = V_{ih}	−10	10	µA	
V_{oH}	Output high (logic 1) voltage	I_O = −4 mA	2,4	—	V	
V_{oL}	Output low (logic 0) voltage	I_O = 4 mA	—	0,4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(NOTES 3, 4, 5, 15)

(T_A = 0 to 70°C, V_{CC} = 5.0 V +/− 5% or 10% depending on type)

	PARAMETER	MMN 4164 1		MMN 4164 2, 3		MMN 4164 4		UNIT	NOTES
		min.	max.	min.	max.	min.	max.		
t_{RLRL}	Random read or write cycle time	270	—	330	—	410	—	ns	6,7
t_{RLRL}	Read modify write cycle time	300	—	375	—	445	—	ns	6,7
t_{CLCL}	Page mode cycle time	170	—	200	—	280	—	ns	6,7
t_{RLQV}	Access time from RAS	—	150	—	200	—	250	ns	7,8
t_{CLQV}	Access time from CAS	—	100	—	110	—	150	ns	7,9
t_{CHQX}	Output buffer turn-off delay	—	50	—	50	—	50	ns	10
t_{THL} t_{TLH}	Transition time (rise and fall)	3	50	3	50	3	50	ns	5
t_{RHRL}	$\overline{RAS}$ precharge time	100	—	120	—	150	—	ns	
t_{RLRH}	$\overline{RAS}$ pulse width	150	10000	200	10000	250	10000	ns	
t_{CLRH}	$\overline{RAS}$ hold time	100	—	110	—	150	—	ns	
t_{RLCH}	$\overline{CAS}$ hold time	150	—	200	—	250	—	ns	
t_{CLCH}	$\overline{CAS}$ pulse width	100	10000	110	10000	150	10000	ns	
t_{RLCL}	$\overline{RAS}$ to $\overline{CAS}$ delay	25	50	45	90	75	100	ns	11

PARAMETER		MMN 4164.1		MMN 4164.2, .3		MMN 4164.4		UNIT	NOTES
		min.	max.	min.	max.	min.	max.		
t_{RHWL}	Read command hold time from $\overline{RAS}$	0	—	0	—	0	—	ns	12
t_{ZVAL}	Row address set-up time	0	—	0	—	0	—	ns	
t_{RLZX}	Row address hold time	15	—	30	—	45	—	ns	
t_{SVCL}	Column address set-up time	0	—	0	—	0	—	ns	
t_{CLSX}	Column address hold time	45	—	45	—	60	—	ns	
t_{RLSX}	Column address hold time from $\overline{RAS}$	95	—	135	—	160	—	ns	
t_{WHCL}	Read command set-up time	0	—	0	—	0	—	ns	
t_{CHWL}	Read command hold time from $\overline{CAS}$	0	—	0	—	0	—	ns	12
t_{CLWH}	Write command hold time	45	—	40	—	50	—	ns	
t_{RLWH}	Write command hold time from $\overline{RAS}$	95	—	130	—	155	—	ns	
t_{WLWH}	Write command pulse width	45	—	45	—	50	—	ns	
t_{WLRH}	Write command to $\overline{RAS}$ lead time	60	—	50	—	60	—	ns	
t_{WLCH}	Write command to $\overline{CAS}$ lead time	60	—	50	—	60	—	ns	
t_{IVCL}	Data-in set-up time from $\overline{CAS}$	0	—	0	—	0	—	ns	13
t_{IVWL}	Data-in set-up time from $\overline{WE}$	0	—	0	—	0	—	ns	13
t_{CLIX}	Data-in hold time	45	—	45	—	60	—	ns	13
t_{RLIX}	Data-in hold time from $\overline{RAS}$	95	—	135	—	160	—	ns	
t_{CHCL}	$\overline{CAS}$ precharge time for page mode only	60	—	80	—	120	—	ns	
t_{REF}	Refresh period	—	2	—	2	—	2	ms	
t_{WLCL}	Write command set-up time	0	—	0	—	0	—	ns	14
t_{CLWL}	$\overline{CAS}$ to $\overline{WE}$ delay	70	—	85	—	120	—	ns	14
t_{RLWL}	$\overline{RAS}$ to $\overline{WE}$ delay	120	—	175	—	220	—	ns	14
t_{CHCI}	$\overline{CAS}$ precharge time	25	—	45	—	90	—	ns	

NOTES:

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
3. An initial pause of 100 μs is required after power-up followed by 8 RAS cycles before proper device operation is achieved.
4. AC characteristics assume $t_T = 5$ ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. Load = 2 TTL loads and 100 pF.
8. Assumes that $t_{RLCL} \leq t_{RLCL}$ (max). If t_{RLCL} is greater than the maximum recommended value shown in this table, t_{RLOV} will increase by the amount that t_{RLCL} exceeds the value shown.
9. Assumes that $t_{RLOV} \geq t_{RLCL}$ (Max).
10. t_{CHOX} max defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

11. Operation within the t_{RLCL} (max) limit insures that t_{RLOV} (max) can be met t_{RLCL} (max) is specified as a reference point only is t_{RLCL} is greater than the specified t_{RLOV} (max) limit, then access is controlled exclusively by t_{CLOV}.
12. Either t_{RHWL} or t_{CHWL} must be satisfied for a read cycle.
13. These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in delayed write or read modify write cycles.
14. t_{WLCL}, t_{CLWL} and t_{RLWL} are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only if $t_{WLCL} \geq t_{WLCL}$ (min) the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CLWL} \geq t_{CLWL}$ (min) and $t_{RLWL} \geq t_{RLWL}$ (min) the cycle is a READ/WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until CAS goes back to V_{IH}) is indeterminate.
15. The transition time specification applies for all inputs signals. In addition to meeting the transition rate specification all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

OPERATION

The 16 address bits required to decode 1 of 65.536 cell locations within the MMN4164 are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock. Row Address Strobe (RAS), latches the 8 row addresses into the chip.

The high-to-low transition of the second clock, Column Address Strobe (CAS), subsequently latches the 8 column addresses into the chip. Each of these signals, RAS and CAS, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the CAS clock sequence are inhibited until the occurence of a delayed signal derived from the RAS clock chain. The "gated CAS" feature allows the CAS clock to be externally activated as soon as the Row Address Hold specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

The "gated CAS" feature permits CAS to be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of CAS which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if CAS is applied to the MMN4164 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from CAS (t_{CAS}) rather than from RAS (t_{RAS}), and RAS acces time will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and CAS while RAS is active. The latter of WRITE or CAS to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the WRITE input is brought low (active) prior to CAS being brought low (active), the D_{IN} is strobed by CAS, and the Input Data set-up and hold times are referenced to CAS. If the input data is not available at CAS time (late write) or if it is desired that the cycle be a read-write or read-modify-write cycle the WRITE signal should be delayed until after CAS has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of WRITE rather than CAS.

Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which both the RAS and CAS are low (active) Data read from the selected cell is available at the output port within the specified access time. The output data is the same polarity (not inverted) as the input data.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MMN4164 is the high impedance (open-circuit) state, any time CAS is high (inactive) the D_{OUT} pin will be floating .Once the output data port has gone active it will remain valid until CAS is taken to the precharge (inactive high) state. Note that CAS can be left active (low) indefinitely. This permits either RAS-only or RFSH refresh cycles to occur without invaliding D_{OUT}.

PAGE MODE OPERATION

The Page Mode feature of the MMN 4164 allows for succesive memory operations at multiple column locations within the same row address.This is done by strobing the row address into the chip and maintaining the RAS signal low (active) throughout all successive memory cycles in which the row address is common. The first access within a page mode operation will be available at t_{RAC} or t_{CAC} time whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at t_{CAC} time (referenced to CAS). With the MMN 4164 this results in as much as a 50% improvement in access times. Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MMN 4164 is limited to the 256 column locations determined by all combinations of the 8 column address bits. Operations within the page boundary need not be sequentially addressed and any combination of read write and read modify-write cycles are permitted within the page mode operation.

REFRESH

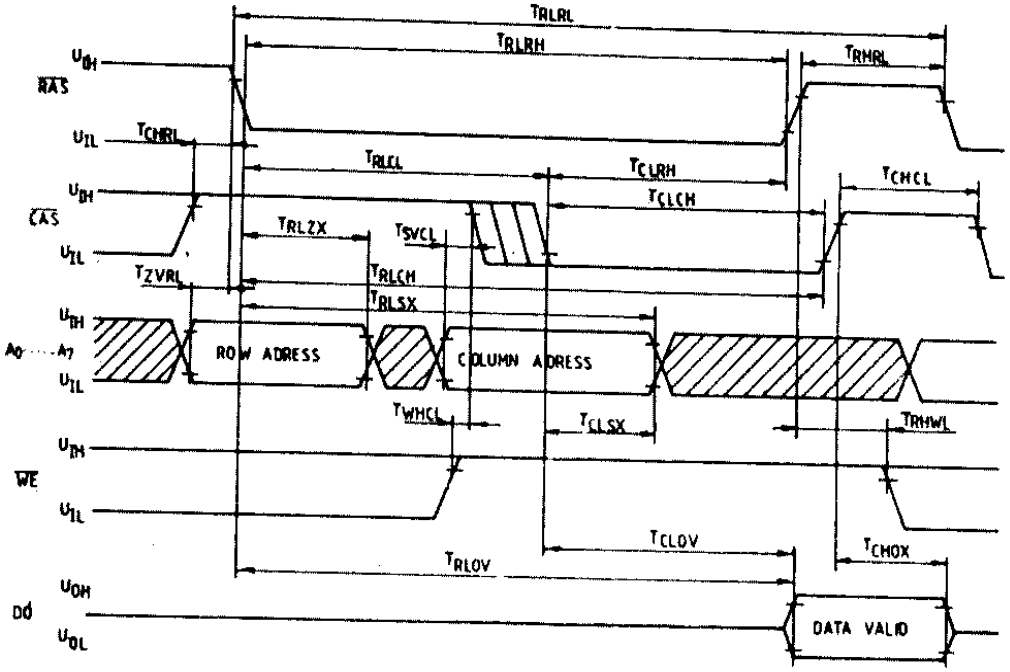
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2ms interval. Although any normal memory cycle will perform the required refreshing this function is easily accomplished by using either RAS-only or RFSH type refreshing.

RAS-ONLY REFRESH

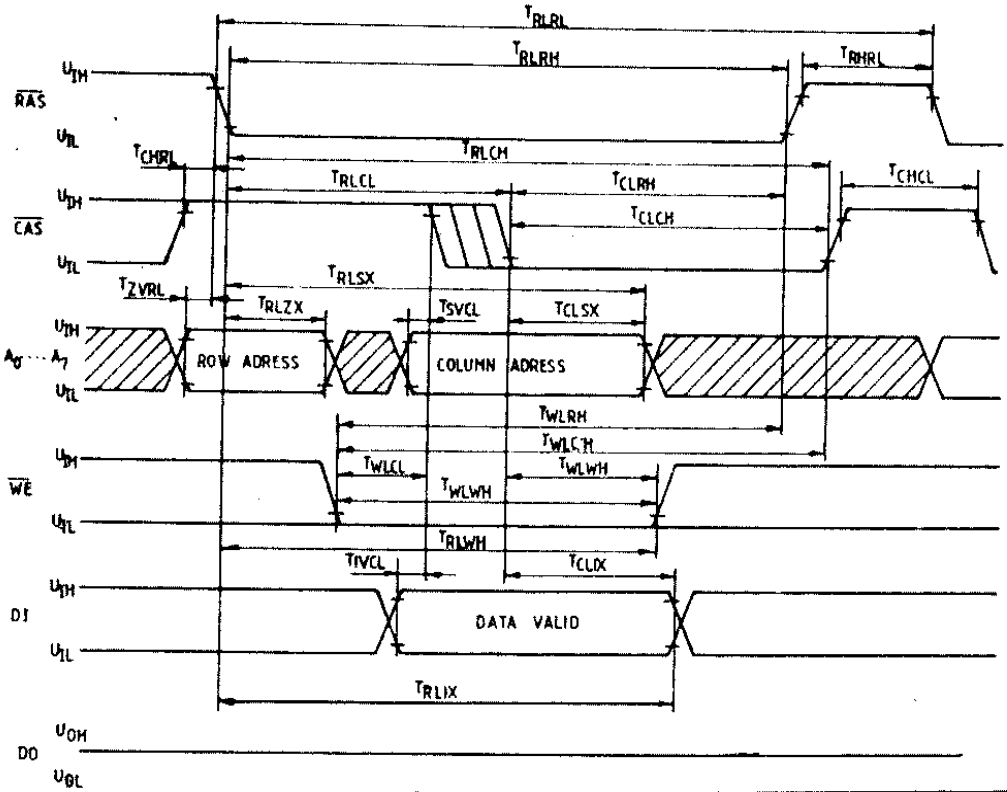
The RAS-only refresh cycle supported by the MMN

4164 requires that a 7 bit refresh address be valid at the device address inputs when RAS goes low (active). The state of the output data port during a RAS-only refresh is controlled by CAS. If CAS is high (inactive) during the entire time that RAS is asserted, the output will remain in the high impedance state. If CAS is low (active) the entire time that RAS is asserted, the output port will remain in the same state that it was prior to the issuance of the RAS signal. This is useful for single step operation. If CAS makes a low-to-high transition during the RAS-only refresh cycle, the output data buffer will assume the high impedance state.

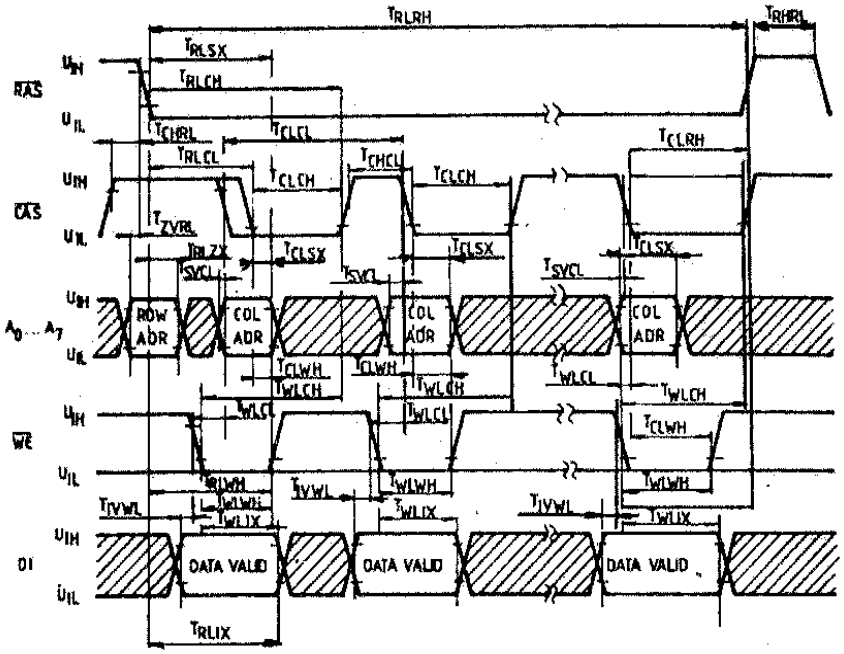
READ CYCLE



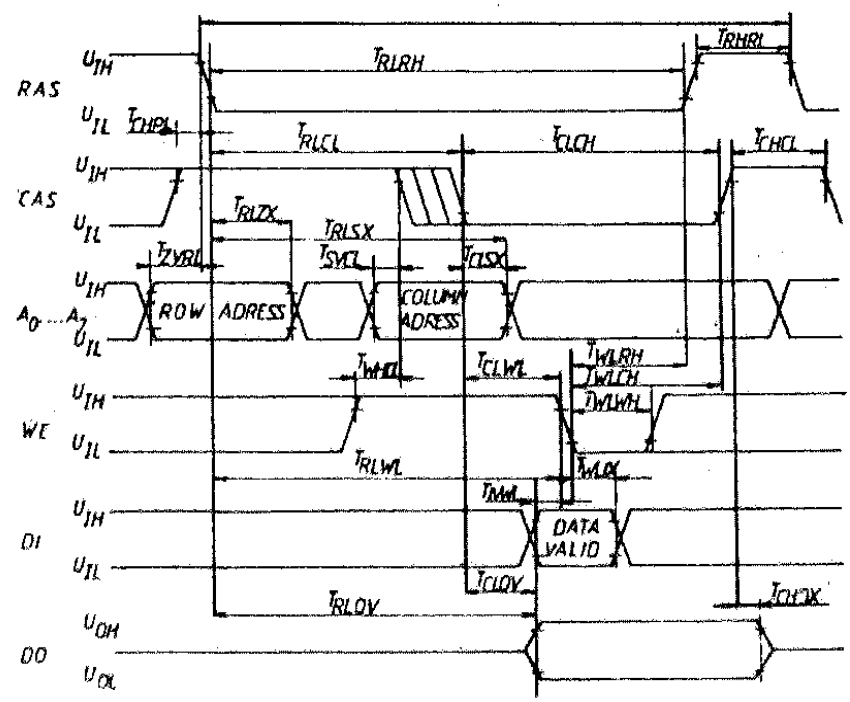
WRITE CYCLE



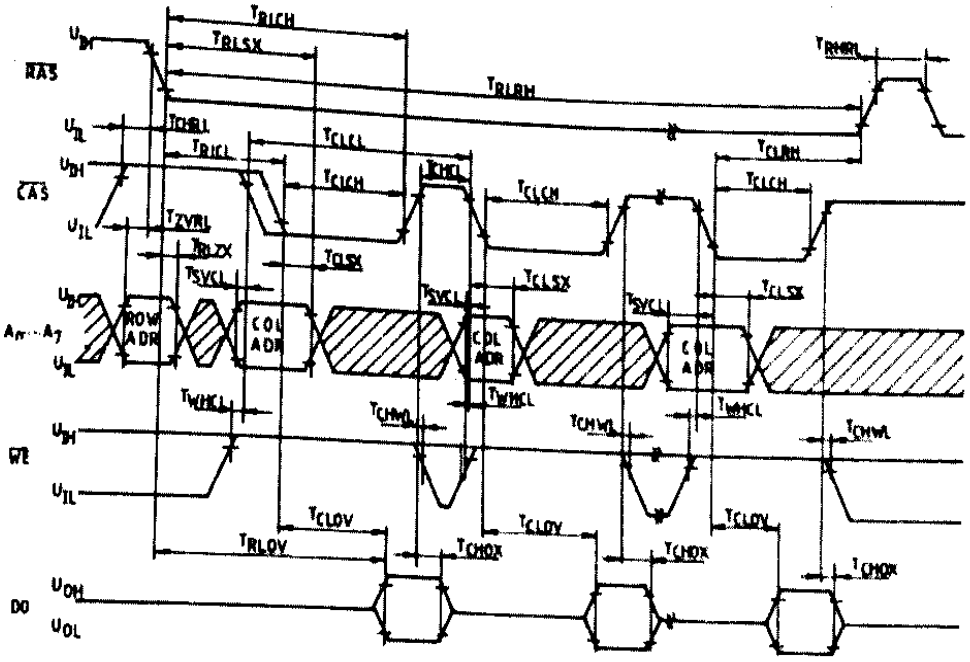
PAGE MODE WRITE CYCLE



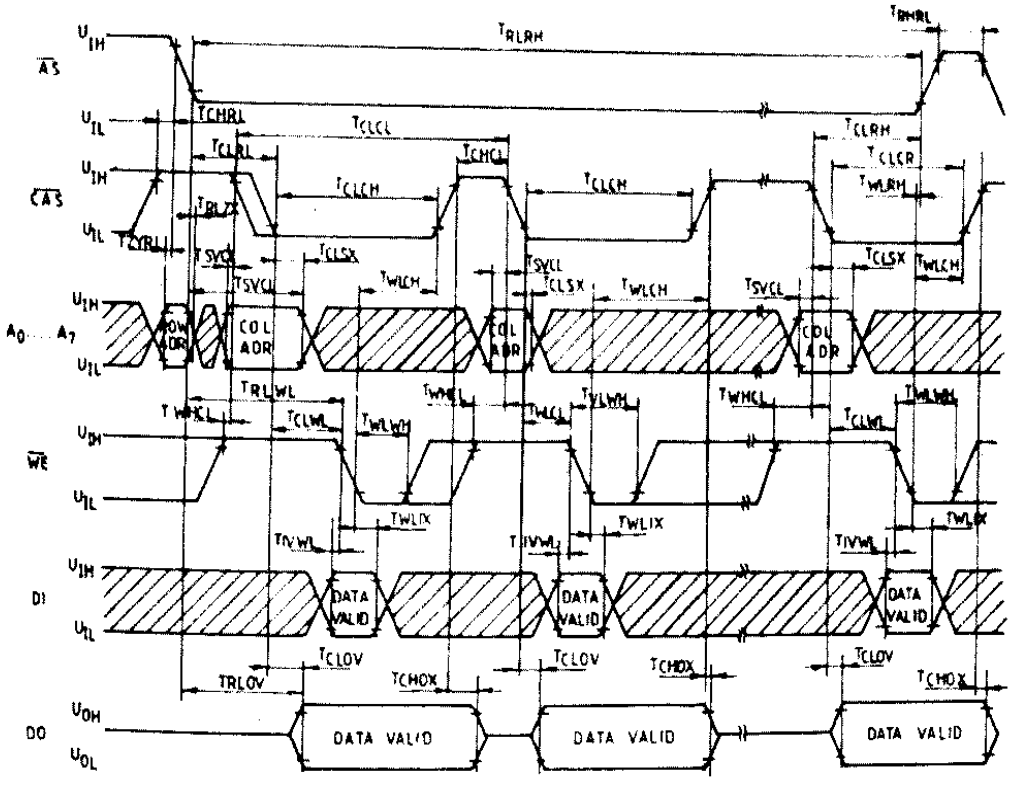
READ MODIFY WRITE CYCLE



PAGE MODE READ CYCLE



PAGE MODE READ MODIFY-WRITE CYCLE



RAS-ONLY-REFRESH CYCLE