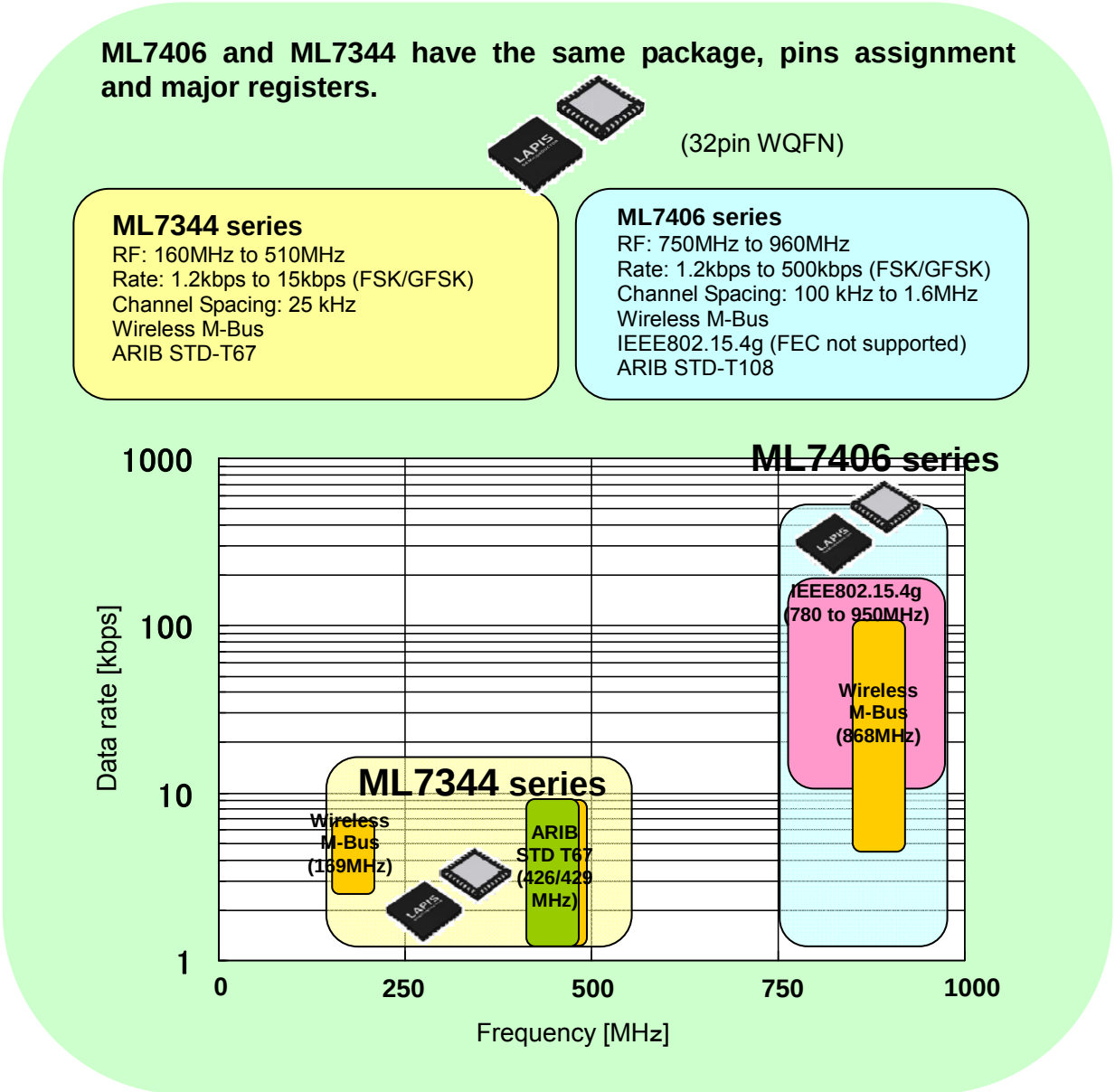
ML7406

868MHz SRD RF transceiver IC

■Overview

ML7406 is a low power consumption sub GHz RF transceiver, which includes RF, IF, MODEM, baseband processor, HOST interface. ML7406 can be used for mainly ISM(Industrial, Scientific and Medical) or SRD(Short Range Device). (EN13757-4:2011: Wireless M-BUS) packet format can be processed by on-chip hardware.



■Features

- Supported standard
  - ETSI EN 300 220 (Europe)
  - EN 13757-4:2011 (Wireless M-BUS)
  - IEEE802.15.4g
  - ARIB STD T108 (Japan)
- RF frequency: 750MHz to 960MHz
- Realized high resolution modulation by using fractional N type PLL direct GFSK modulation
- Modulation: GFSK/GMSK/FSK/MSK (MSK is a case that FSK modulation index = 0.5)
- Data transmission rate: 1.2 to 500 kbps
- Data encoding/decoding by HW: NRZ, Manchester, 3 out of 6
- Data whitening by HW
- Programmable frequency channel filters
- Programmable frequency deviation function
- TX/RX data inverse function
- 26 MHz oscillator circuits version (ML7406C)
- TCXO (26 MHz) direct input version (ML7406T)
- SPXO input(CMOS level) version (ML7406S)
- Oscillator capacitance fine tuning function
- On chip low speed RC oscillation circuit
- Low speed clock adjustment function
- frequency fine tuning function (using fractional N type PLL)
- Synchronous serial peripheral interface(SPI)
- On-chip TX PA. (20 mW / 10 mW / 1 mW selectable)
- TX power fine tuning function (±0.2 dB)
- TX power automatic ramping control
- External TX PA control function
- RSSI indicator and threshold judgment function
- High speed carrier checking function
- AFC function (IF frequency automatic adjustment by Fractional N type PLL adjustment)
- Antenna diversity function
- Automatic Wake UP, auto SLEEP function (external RTC input or internal RC oscillator selectable)
- General purpose timer (2ch)
- Test pattern generator (PN9 ,CW, 01 PATTERN, ALL"1", ALL"0" OUTPUT)
- Packet mode function
  - Wireless M-BUS packet format (Format A/B)
  - General purpose packet format (Format C)
  - Max.255 byte (Format A/B), 204t byte (Format C)
  - TX FIFO (64 byte), RX FIFO (64 byte)
  - RX Preamble pattern detection (Max.4 byte)
  - Automatic TX preamble length generation (Max.length 16383 byte)
  - SyncWord setting function (Max. 4byte × 2 type)
  - Program CRC function (CRC32/CRC16/CRC8 selectable, fully programmable polynomial)
  - Wireless M-BUS field checking function (C-field/M-field/A-field can be detected automatically)

    (Note) Proprietary packet format is possible depending on setting
- Supply voltage

  1.8 V to 3.6 V (TX power 1 mW mode)

  2.3 V to 3.6 V (TX power 10 mW mode)

  2.6 V to 3.6 V (TX power 20 mW mode)
- Operational temperature -40 ˚C to 85 ˚C

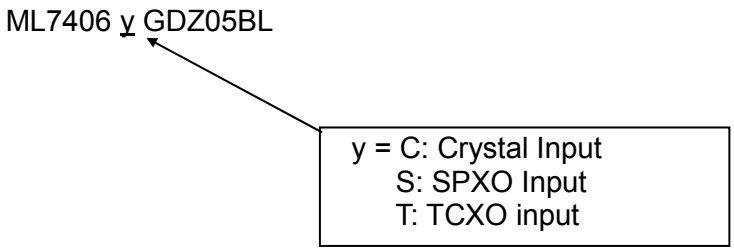
- Current consumption (868 MHz)

Deep sleep mode	0.1 μA (Typ.)	
Sleep mode2	0.56 μA (Typ.)	(retains registers, FIFO)
Idle mode	1.4 mA (Typ.)	
TX 20 mW	34 mA (Typ.)	
10 mW	24 mA (Typ.)	
1 mW	13 mA (Typ.)	
RX	15 mA (Typ.)	(@100kbps)

- Package

32pins WQFN (5mm × 5mm) P-WQFN32-0505-0.50
Lead free, RoHS compliance

■Product Name



■Description Convention

1) Numbers description
'0xnn' indicates hexa decimal. '0bnn' indicates binary.

Example: 0x11= 17(decimal), 0b11= 3(decimal)

2) Registers description
[<register name>: B<Bank No> <register address>] register

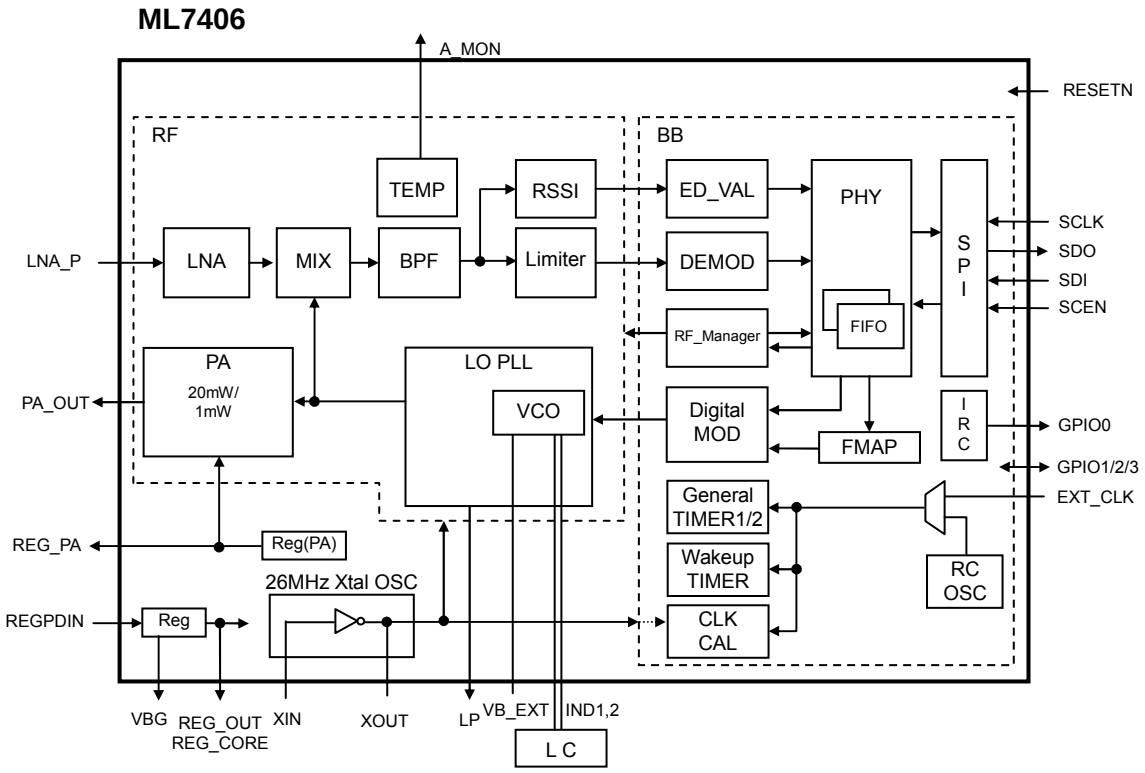
Example: [RF_STATUS: B0 0x0B] register
Register name: RF_STATUS
Bank No: 0
Register address: 0x0B

3) Bir name description
<bit name> ([<register name>: B<Bank No> <register address>(<bit location>)])

Example: **SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)])**
Bit name: SET_TRX
Register name: RF_STATUS
Bank No: 0
Register address: 0x0B
Bit location: bit3 to bit0

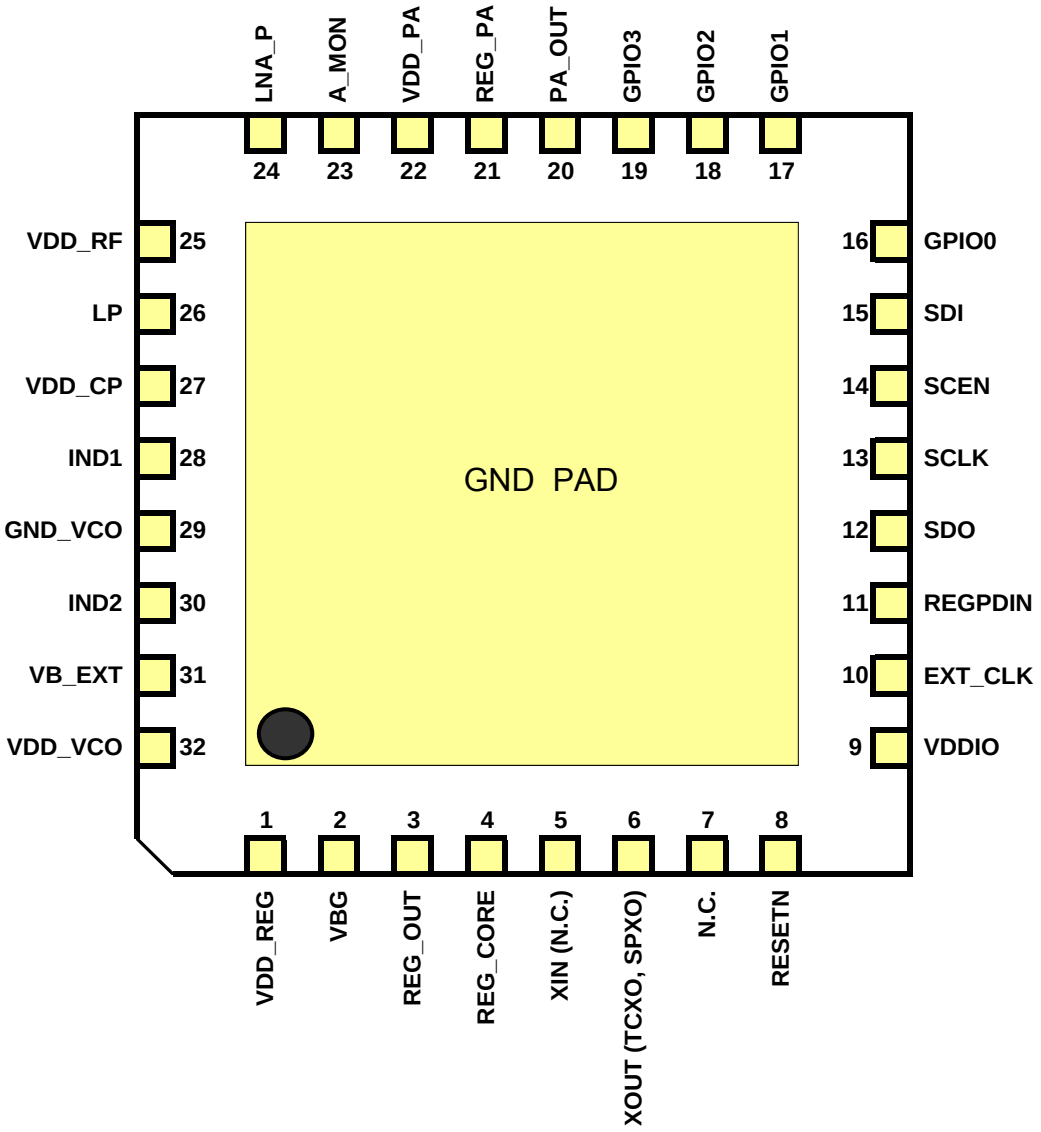
4) In this document
"TX" stands for transmittion.
"RX" stands for reception.

■Block Diagram



■PIN Configuration

32 pin WQFN



NOTE: GND pad in the middle of the LSI is reverse side (name:reversed side GND)

■PIN Definitions

Symbols
I : Digital input
O : Digital output
Is : Shmidt Trigger input
IO : Digital input/output
I_A : Analog input
O_A : Analog output 1
O_{AH} : Analog output 2
IO_A : Analog input/output
O_{RF} : RF output
V_{DDIO} : I/O power supply
V_{DDRF} : RF power supply
GND : Ground

●RF and Analog pins

Pin	Pin name	Reset state	I/O	Active Level	function
20	PA_OUT	−	O_{RF}	−	RF antenna output
23	A_MON	−	O_A	−	Temperature information output (*1)
24	LNA_P	−	I_A	−	RF antenna input
26	LP	−	IO_A	−	Pin for loop filter
28	IND1	−	IO_A	−	Pin for VCO tankl inductor
30	IND2	−	IO_A	−	Pin for VCO tank inductor
31	VB_EXT	−	IO_A	−	Pin for smothing capacitor for internal bias

*1 This pin can be configured by [MON_CTRL:B0 0x4D] register, no signal assigned as default setting.

●SPI Interface pins

Pin	Pin name	Reset state	I/O	Active Level	function
12	SDO	O/L	O	H or L	SPI data output or DCLK (*1)
13	SCLK	I	IS	P or N	SPI clock input
14	SCEN	I	IS	L	SPI chip enable L: enable H: disable
15	SDI	I	IS	H or L	SPI data input or DIO (*1)

*1 Please refer to “DIO function”

●Regulator pins

Pin	Pin name	Reset state	I/O	Active Level	function
2	VBG (*1)	−	O_{AH}	−	Pin for decouppling capacitor
3	REG_OUT (*1)	−	O_{AH}	−	Requlator1 ouput (typ. 1.5V)
4	REG_CORE	−	O_A	−	Requlator2 ouput (typ. 1.5V)
11	REGPDIN	I	I	H	Power down control pin for regulator Fix to 'L' for nomal use. "H" is for deep sleep mode.
21	REG_PA (*1)	−	O_{AH}	−	Regulator output for PA block

*1 These pin will output 0V in the sleep state.

●Miscellaneous

Pin	Pin name	Reset state	I/O	Active Level	function
5	XIN N.C.(*2)	I −	I_A −	P or N −	26MHz crystal pin1 (Note) In case of TCXO or SPXO, it must be open.
6	XOUT TCXO(*2) SPXO(*2)	O	O_A I_A I	P or N	26MHz crystal pin 2 or TCXO input, SPXO input
8	RESETN	I	I_S	L	Reset L: Hardware reset enable (Forcing reset state) H: Normal operation
10	EXT_CLK	I	IO	P or N	Digital I/O (*3) Reset state: External RTC (32kHz) input.
16	GPIO0	O/H	IO or OD(*1)	H or L	Digital GPIO (*4) Reset state: interrupt indication signal output
17	GPIO1	O/L	IO or OD(*1)	H or L	Digital GPIO (*5) Reset state: clock output
18	ANT_SW/ GPIO2	O/L	IO or OD(*1)	H or L	Digital GPIO (*6) Reset state: Antenna diversity selection control signal
19	TRX_SW/ GPIO3	O/L	IO or OD(*1)	H or L	Digital GPIO (*7) Reset state: TX –RX selection signal control

(Note)

*1 OD is open drain output.

*2 The following pin names are different depend on products.

Pin No.	ML7406C	ML7406S	ML7406T
5	XIN	N.C.	N.C.
6	XOUT	SPXO	TCXO

(Note)

In case of using TCXO/SPXO, set TCXO_EN or SPXO_EN =0b1. Please make sure only one of the register TCXO_EN, SPXO_EN, XTAL_EN_EN is set to 0b1.

*3 Please refer to [EXTCLK_CTR: B0 0x52] register.

*4 Please refer to [GPIO0_CTRL: B0 0x4E] register

*5 Please refer to [GPIO1_CTRL: B0 0x4F] register
*6 Please refer to [GPIO2_CTRL: B0 0x50] register
*7 Please refer to [GPIO3_CTRL: B0 0x51] register

●Power supply/GND pins

Pin	Pin name	Reset state	I/O	Active Level	function
1	VDD_REG	-	V_{DDIO}	-	Power supply pin for Regulator (input voltage: 1.8V to 3.3V)
9	VDDIO	-	V_{DDIO}	-	Power supply for digital I/O (input voltage: 1.8 to 3.6V)
22	VDD_PA	-	V_{DDIO}	-	Power supply for PA block (input voltage: 18 to 3.6V, depending on TX mode)
25	VDD_RF	-	V_{DDRF}	-	Power supply for RF blocks (REG-OUT is connected, typ.1.5V)
27	VDD_CP	-	V_{DDRF}	-	Power supply for charge pump (REG-OUT is connected, typ.1.5V)
32	VDD_VCO	-	V_{DDRF}	-	Power supply for VCO (REG_OUT is connected, typ.1.5V)
29	GND_VCO	-	GND	-	GND for VCO

●Unused pins treatment

Unused pins treatments are as follows:

Unused pins treatment

Pin name	Pins number	Recommended treatment
N.C.	5	Open
N.C.	7	GND or Open
EXT_CLK	10	GND
A_MON	23	GND
GPIO0	16	Open
GPIO1	17	Open
GPIO2	18	Open
GPIO3	19	Open

(Note)
*1 If input pins are high-impedence state and leave open, excess current could be drawn. Care must be taken that unused input pins and unused I/O pins should not be left open.
*2 Upon reset, GPIO1 pin is CLK_OUT function. If this function is not used, the clock must to be disabled by setting 0b000 to GPIO1_IO_CFG[2:0] ([GPIO1_CTRL: B0 0x4F (2-0)]). If this pin is left open while outputing clock signal, it may affect RX sensitivity.

■Electrical Characteristics

●Absolute Maximum Rating

Ta=-40˚C to +85˚C and GND=0V is the typical conditoin if not defined specific condition.

item	symbol	condition	Rating	unit
I/O Power supply	V_{DDIO}		-0.3 to +4.6	V
RF Power supply	V_{DDRF}		-0.3 to +2.0	V
RF input power	P_{RFI}	Antenna input in RX	0	dBm
RF output Voltage	V_{RFO}	PA_OUT(#20)	-0.3 to +4.6	V
Voltage on Analog Pins 1	V_A		-0.3 to +2.0	V
Voltage on Analog Pins 2	V_{AH}		-1.0 to +4.6	V
Voltage on Digital Pins	V_D		-0.3 to +4.6	V
Digital Input Current	IDI		-10 to +10	mA
Digital Output Current	IDO		-8 to +8	mA
Power Dissipation	Pd	Ta= +25˚C	1.2	W
Strage Temperature	Tstg	−	-55 to +150	˚C

●Recommended Operation Conditions

Item	Symbol	Condition	Min	Typ	Max	Unit
Power Supply (I/O)	VDDIO	VDDIO pin and VDD_REG pin (*1)	1.8	3.3	3.6	V
Power Supply (PA)	VDDPA	VDD_PA pin TX power 1mW mode	1.8	3.3	3.6	V
		VDD_PA pin TX Power 10mW mode	2.3	3.3	3.6	V
		VDD_PA pin TX Power 20mW mode	2.6	3.3	3.6	V
Operational Temperature	Ta	−	-40	+25	+85	˚C
Digital Input Rising Time	TIR	Digital Input pins (*1)	−	−	20	ns
Digital InputFalling Time	TIF	Digital Input pins (*1)	−	−	20	ns
Digital Output Output Load	CDL	All Digital Output pins	−	−	20	pF
Master Clock Frequency (XIN,XOUT,TCXO,SPXO pins)	FMCK1	−	(*2)	26	(*2)	MHz
Master Clock Accuracy (*2)	ACMCK1	−	-85	−	+85	ppm
TCXO Input Voltage	VTCXO	DC Cutoff TCXO Optionis selected	0.8	−	1.5	Vpp
SPI Clock InputFrequency	FSCLK	SCLK pin	0.032	2	16	MHz
SPI Clock Input Duty Cycle Ratio	DSCLK	SCLK pin	45	50	55	%
RF Frequency	FRF		750	−	960	MHz

*1 In the pin description, I or Is are specified as the I/O.

*2 Indicating frequency deviation during TX-RX operation. In order to support various standards, please apply the frequency accuracy for each standard to meet the requirements.

Specification	Required accuracy
Wireless M-Bus S mode	±60 ppm(Meter) ±25 ppm(Other)
Wireless M-Bus T mode	±60 ppm(Meter) ±25 ppm(Other)
Wireless M-Bus C mode	±25 ppm
ARIB STD-T108	±20 ppm

(Note) Below values are not taking individual LSI variations into consideration.

●Power Consumption

Item	Synbol	Condition	Min	Typ (*2)	Max (*5)	Unit
Power Consumption (*1)	IDD_DSLP	Deep Sleep mode (Not retaining Registers, all function halt)	−	0.1	9 (0.8)	μA
	IDD_SLP2	Sleep mode 2 (*3)	−	0.56	20 (3.2)	μA
	IDD_SLP3	Sleep mode 3 (*3)	−	0.7	20.2 (3.2)	μA
	IDD_SLP4	Sleep mode 4 (*3)	−	2.5	22 (5.1)	μA
	IDD_IDLE	Idle state	−	1.4	−	mA
	IDD_RX	RF RX state (*4)	−	15	−	mA
	IDD_TX1	RF TX state (1mW)(*4)	−	13	−	mA
	IDD_TX10	RF TX state (10mW) (*4)	−	24	−	mA
	IDD_TX20	RF TX state (20mW) (*4)	−	34	−	mA

*1 Power consumption is sum of current consumption of all power supply pins.
*2 “Typ” value is centre value under condition of VDDIO=3.3V, 25˚C.
*3 The definition od each sleep stae is shown in following table.

State.	Register	FIFO	RC Osc. (32kHz)	Low clock timer
Sleep mode 1	ML7406 does not support Sleep mode 1			
Sleep mode 2	Retain	Retain	OFF	-
Sleep mode 3	Retain	Retain	External Input	ON
Sleep mode 4	Retain	Retain	ON	ON

*4 Current consumption when RF Frequency is 868MHz.
*5 () means maximum value (reference value) under condition of 25˚C.

(Note)
It is inhibited the trnasiton from sleep modes to deep sleep mode in one power supply cycle.

●DC characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Voltage Input High	V_{IH1}	Digital Input pin	VDDIO × 0.75	−	VDDIO	V
	V_{IH2}	XIN pin	1.35	−	1.5	V
Voltage Input Low	V_{IL1}	Digital Input pin	0	−	VDDIO × 0.18	V
	V_{IL2}	XIN pin	0	−	0.15	V
SchmitTriggerThreshold High Level	V_{T+}	RESETN pin SDI, SCLK, SCEN pins	−	1.2	VDDIO × 0.75	V
		EXT_CLK pin				
SchmitTriggerThreshold Low Level	V_{T-}	RESETN pin SDI, SCLK, SCEN pins	VDDIO × 0.18	0.8	−	V
		EXT_CLK pin				
Input Leakage Current	I_{IH1}	Digital input pins	-1	−	1	µA
	I_{IH2}	XIN pin	-0.3	−	0.3	µA
	I_{IL1}	Digital input pins	-1	−	1	µA
	I_{IL2}	XIN pin	-0.3	−	0.3	µA
Tri-state output current leakage	I_{OZH}	Digital input pins	-1	−	1	µA
	I_{OZL}	Digital input pins	-1	−	1	µA
Voltage Output level H	V_{OH}	IOH=-4mA	VDDIO × 0.8	−	VDDIO	V
Voltage Output level L	V_{OL}	IOL=4mA	0	−	0.3	V
Regulator Output voltage	REG_{MAIN}	REG_CORE pin, REG_OUT pin, applicable to all states except SLEEP state	1.4	1.5	1.6	V
	REG_{SUB}	REG_CORE pin Sleep state	0.95	1.3	1.65	V
Pin capacitance	C_{IN}	Input pins	−	6	−	pF
	C_{OUT}	Output pins	−	9	−	pF
	C_{RFIO}	RF inout pins	−	9	−	pF
	C_{AI}	Analog input pins	−	9	−	pF

●RF characteristics

Modulated Data Rate : 1.2kbps to 500kbps
Modulation fomats : 2GFSK/2FSK
Channel spacing : 60kHz to 1.6MHz

The measurement point is at antenna end specified in the recommended circuits.

[RF Frequency]

Item	Condition	Min	Typ	Max	Unit
RF frequency	LNA_P, PA_OUT pins	750	−	960	MHz

(Note)
1)Frequency range can be adjusted from 750MHz to 960MHz by changing external components parameters.
2)If channel frequency is similar frequency range of Integral multiple of the master clock, it may not be able to use this mode. Please refer to the “channel frequency setting” section for detail.

[TX Characteristics]

Item	Condition	Min	Typ	Max	Unit
TX power	20mW(13dBm) mode	9	13	15	dBm
	10mW(10dBm) mode	6	10	12	dBm
	1mW(0dBm) mode	-4	0	4	dBm
Frequency deviation fine tuning range [Fdev] (*1)		0.025	−	400	kHz
Spurious emission level(10mW mode)	The sencod order harmonic	−	-35	-30	dBm
	The third order harmonic	−	-35	-30	dBm

*1. Depending on the frequency, max.frequency may be changed.

[RX Characteristics]

Item	Condition	Min	Typ	Max	Unit
Minimum RX sensitity BER<0.1%	32.768kbps mode	−	-108	−	dBm
	100kbps mode	−	-106	-100	dBm
Maximum RX input level	BER<0.1%	0	−	−	dBm
Minimum energy detection level (ED value)		−	-107	-100	dBm
Energy detection range	Dynamic range	60	70	−	dB
Energy detection accuracy		-6	−	+6	dB
Secondary emission level	Local frequency	−	-63	-57	dBm
	Frequency over 1000MHz	−	-57	-47	dBm

●RC oscillation circuits characteristics

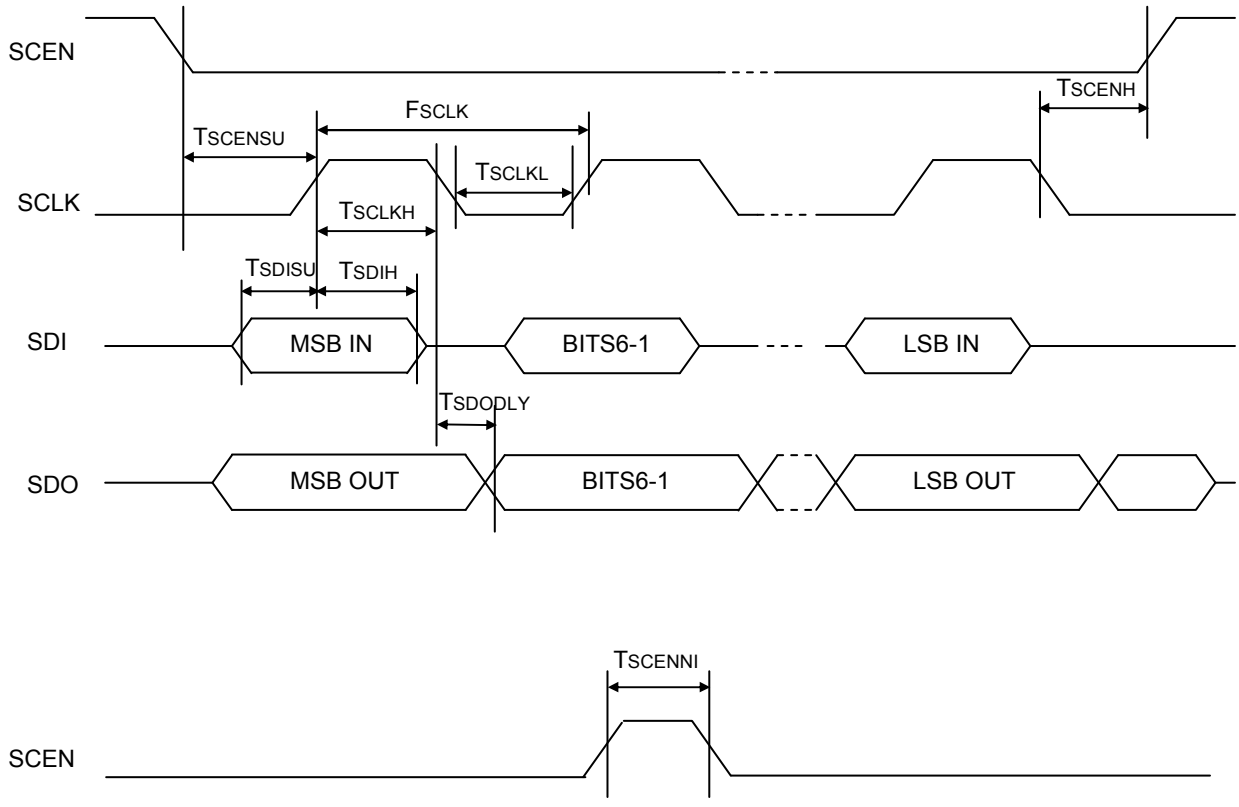
ML7406 has on-chip low speed RC clock generator. For details, please refer to “LSI state transition control/SLEEP setting” section.

Item	Symbol	Condition	Min	Typ	Max	Unit
RCOSC oscillation frequency	FRCOSC		−	44	−	kHz

●SPI interface characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
SCLK clock frequency	FSCLK	Load capacitance CL=20pF	0.032	2	16	MHz
SCEN input setup time	TSCENSU		30	−	−	ns
SCEN input hold time	TSCENH		30	−	−	ns
SCLK high pulse width	TSCLKH		28	−	−	ns
SCLK low pulse width	TSCLKL		28	−	−	ns
SDI input setup time	TSDISU		5	−	−	ns
SDI input hold time	TSDIH		15	−	−	ns
SCEN invert period	TSCENNI		200	−	−	ns
SDO output delay time	TSDODLY		−	−	22	ns

(Note) All measurement condition for the timings are VDDIO * 20% level and VDDIO * 80% level.

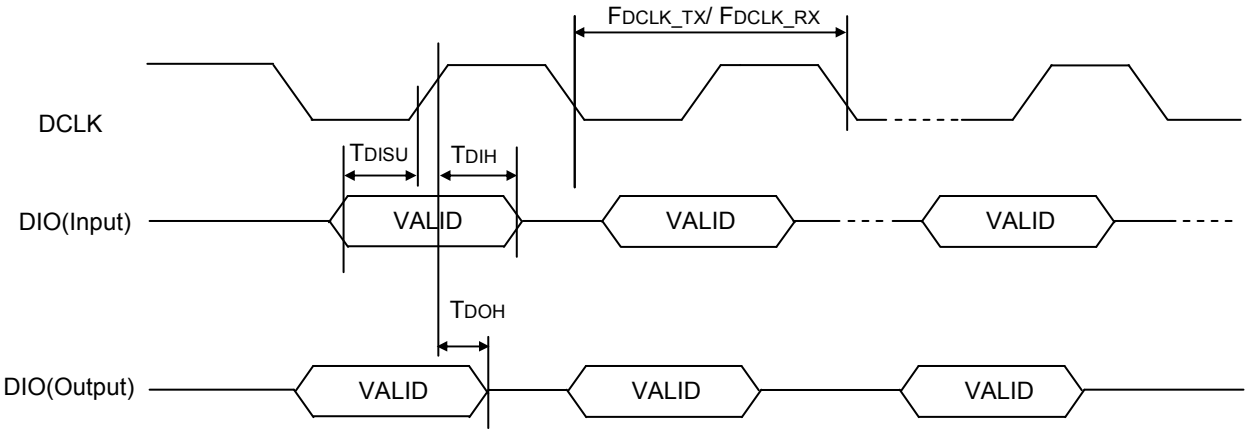


●DIO iInterface characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
DIO input setup time	TDISU	Load capacitance CL=20pF	1	−	−	μsec
DIO input hold time	TDIH		0	−	−	ns
DIO output hold time	TDOH		20	−	−	ns
DCLK frequency accuracy (*1) (TX)	FDCLK_TX		-clock frequency deviation	−	+clock frequency deviation	kHz
DCLK frequency accuracy (*2) (RX)	FDCLK_RX		-30	−	+30	%
DCLK output duty cycle (TX)	DDCLK_TX		45	−	55	%
DCLKoutput duty cycle (RX)	DDCLK_RX		30	−	70	%

*1 If there is no decimal point generated in the TX data rate setting caluclation, (see [TX_RATE_H: B1 0x02]), master clock frequency deviation is max.and min.of TX DCLK frequency.
*2 Max.and min.of RX DCLK frequency indicates jitter of recovered clock from RX signal upon synchronization.

(Note)
All timing measurement conditions are VDDIO * 20% and VDDIO * 80%.

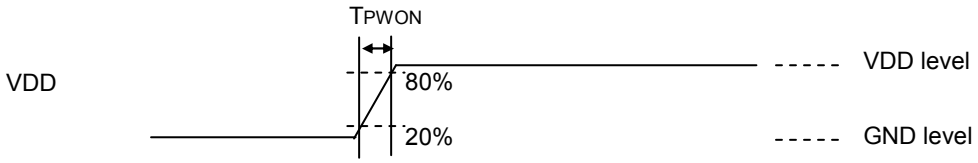


●Power-on characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Power-on stable time	TPWON	Power on state (all power pins)	-	-	5	ms

(Note)

All timing measurement conditions are VDDIO * 20% and VDDIO * 80%.

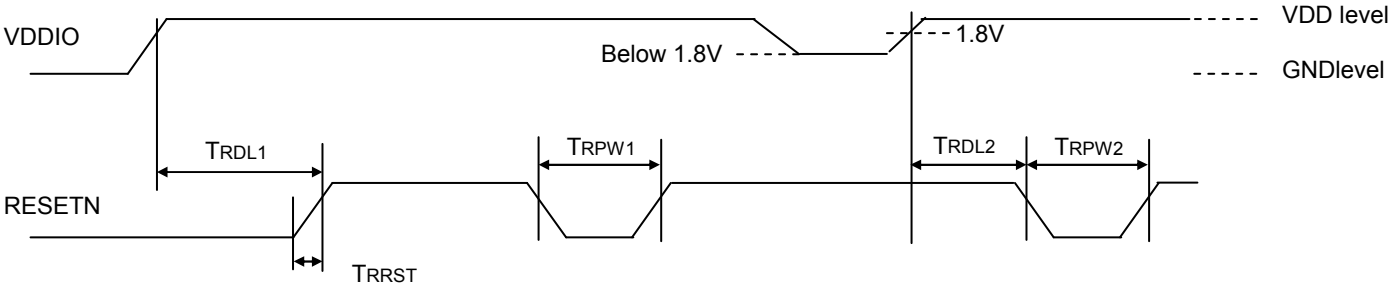


●Reset characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
RESETN release delay time (power on period)	TRDL1	All power pins After Power On	150	-	-	ms
RESETN pulse period (start-up from VDDIO=0V)	TRPW1		200	-	-	ns
RESETN pulse period 2(*1) (start-up from VDDIO≠0V)	TRPW2	After VDDIO>1.8V	150	-	-	ms
RESETN input delay time	TRDL2		1	-	-	µs
RESETN rising edge delay time	TRRST		-	-	1	ms

(Note)

All timing measurement conditions are VDDIO * 20% level and VDDIO * 80% level.

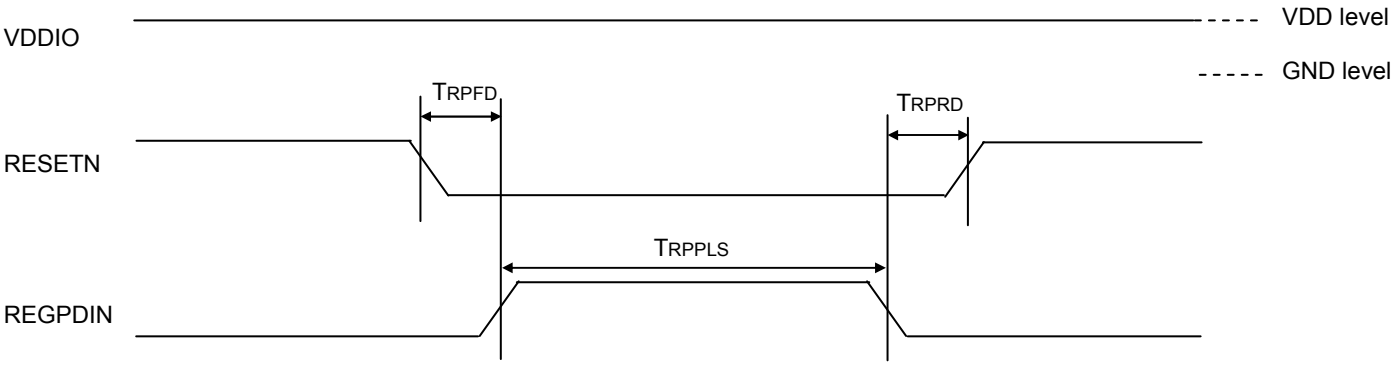


(*1) When starting from VDDIO≠0V, a pulse must be sent to VRESETN after DDIO exceeds 1.8V.

●Deep Sleep mode characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
REGPDIN rising edge delay time	TRPFD	VDDIO="H"	0	−	−	μs
REGPDIN assert time	TRPPLS	VDDIO="H"	1.2	−	−	ms
REGPDIN release delay time	TRPRD	VDDIO="H"	1.5	−	−	ms

(Note)
All timing measurement conditions are VDDIO × 20% and VDDIO × 80%.



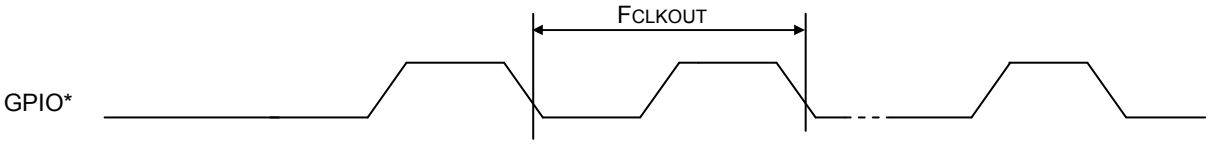
●Clock output characteristics

ML7406 has clock output function. Clock output can be controlled by DMON_SET([MON_CTRL: B0 0x4D(3-0)]) and [GPIOn_CTRL: B0 0x4E-0x51] registers (n=0 to 3). Upon reset, clock is output through GPIO1 pin.

Item	Symbol	Condition		Min	Typ	Max	Unit
Clock output frequency	FCLKOUT	Load capacitance CL=20pF		0.0064	3.33	26	MHz
Clock output duty cycle (*1)	DCLKOUT		8.66MHz	33	−	67	%
			All conditions except above	48	50	52	%

*1 Duty cycle is High:Low = 1:2 , only when 8.66MHz is used. Please refer to [CLK_OUT: B1 0x01] register.

(Note)
All timing measurement conditions are VDDIO × 20% and VDDIO × 80%.



■Functional Description

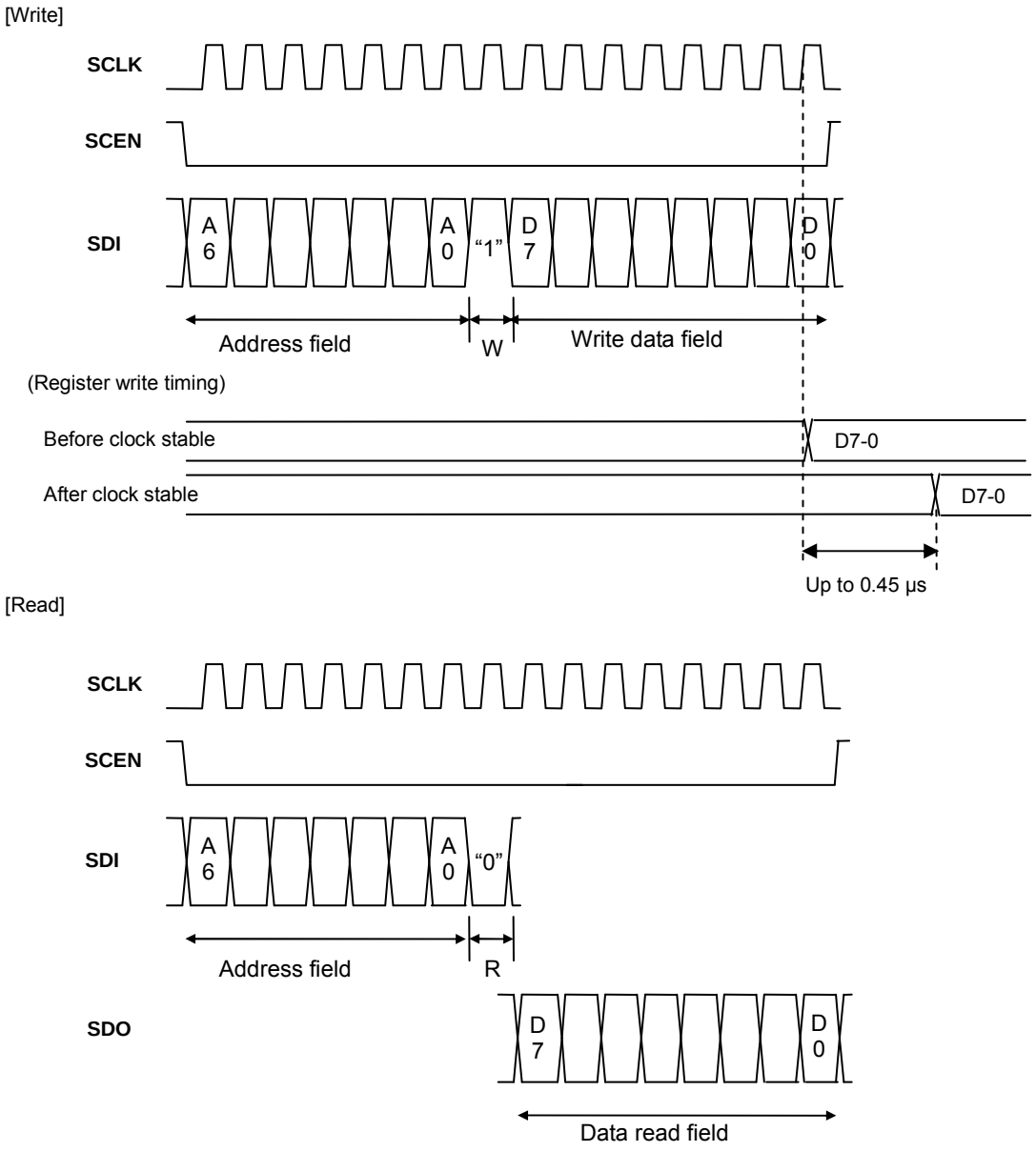
●Host Interface

○Serial Peripheral Interface (SPI)

ML7406 has a SPI, which supports slave mode. Host MCU can read/write to the ML7406 registers and on-chip FIFO using MCU clock. Single access mode and burst access mode are also supported.

[Single access mode timing chart]

In write operation, data will be stored into internal register at rising edge of clock which is capturing D0 dat. During write operation, if setting SCEN line to “H”, the data will not be stored into register. For more details of SCEN invert perios, please refer to the “SPI interface characteristics”. After the internal clock is stabilized, the data will be written into the register in synchronization with the internal clcok.

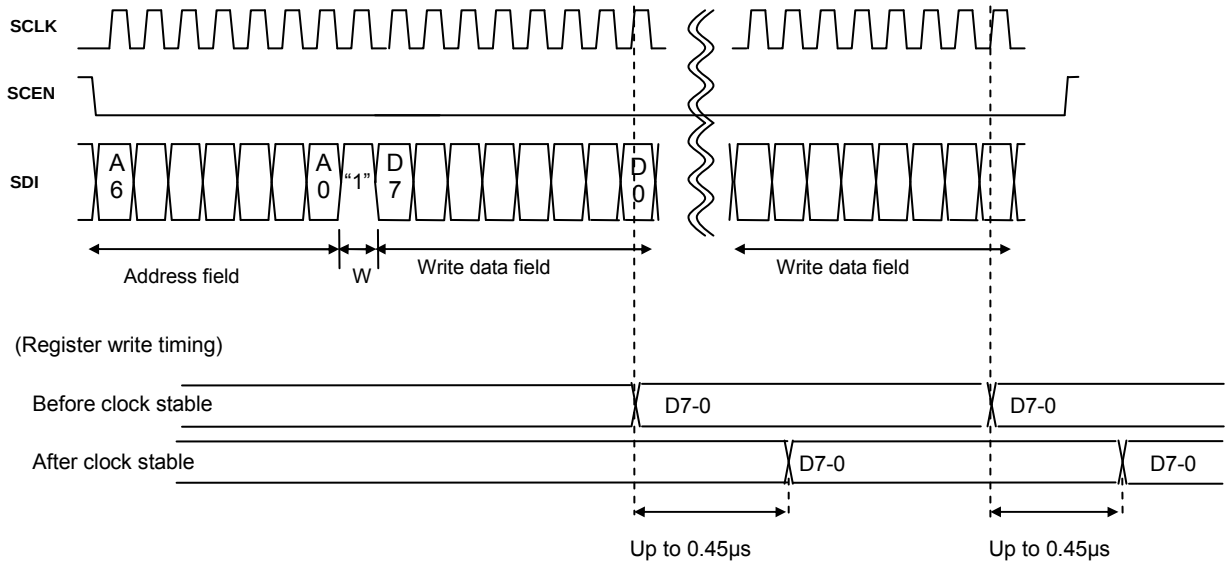


[Burst access mode timing chart]

By maintaining SCEN line as “L”, Burst access mode will be active. By setting SCEN line to “H”, exiting from the burst access mode. During burst access mode, address will be automatically incremented.
When SCEN line becomes “H” before Clock for D0 is input, data transaction will be aborted.

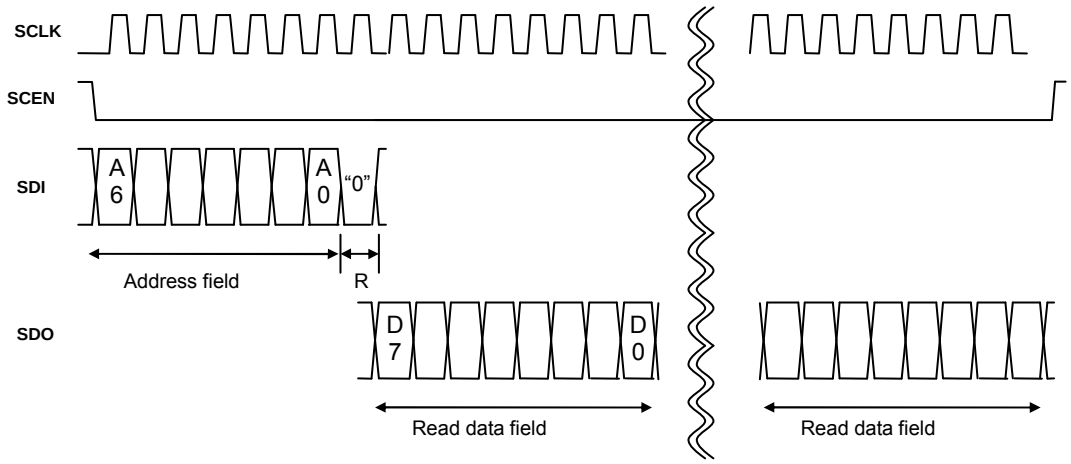
(Note)
If destination is [WR_TX_FIFO: B0 0x7C], [RD_FIFO: B0 0x7F], address will not be incremented. And continuous FIFO access is possible.

[Write]



(Register write timing)

[Read]



●LSI state transition control

○LSI state transition instruction

State can be controlled from MCU by setting registers below.

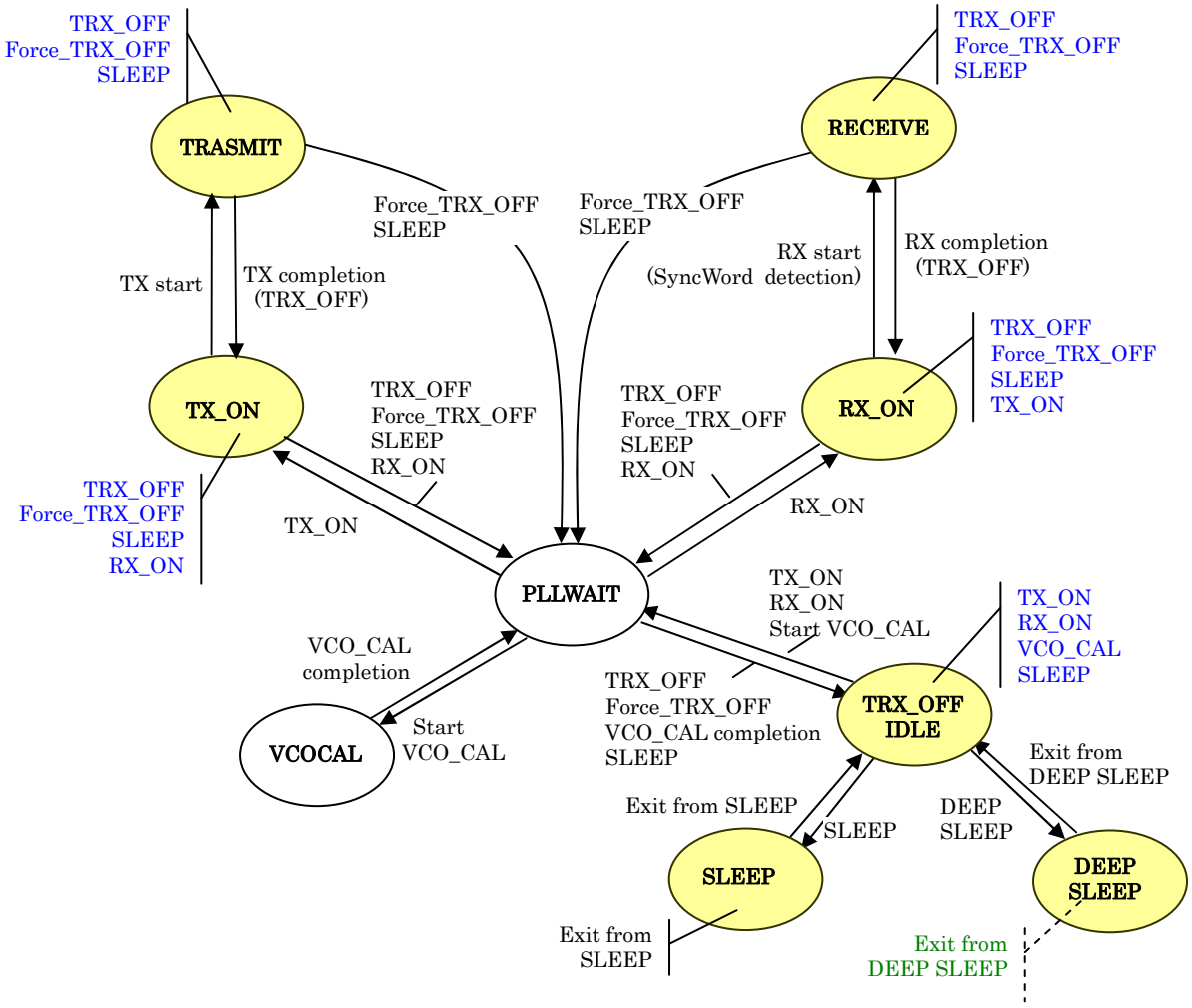
State transition command	Instruction
TX_ON	SET_TRX ([RF_STATUS: B0 0x0B(3-0)]) = 0b1001
RX_ON	SET_TRX ([RF_STATUS: B0 0x0B(3-0)]) = 0b0110
TRX_OFF	SET_TRX ([RF_STATUS: B0 0x0B(3-0)]) = 0b1000
Force_TRX_OFF	SET_TRX ([RF_STATUS: B0 0x0B(3-0)]) = 0b0011
SLEEP	SLEEP_EN([SLEEP/WU_SET: B0 0x2D(0)]) = 0b1
VCO_CAL	VCO_CA_LSTART([VCO_CAL_START: B0 0x6F(0)])= 0b1

State can be changed without command from MCU. If one of the following condition is met, state is changed automatically according to the following table. In order to enable these functions, the following registers must be programmed.

Function	Control bit name
Automatic TXON after FIFO write completion (AUTO_TX)	AUTO_TX_EN([RF_STATUS_CTRL: B0 0x0A(4)])
Automatic TXON during FIFO wrtie (FAST_TX)	FAST_TX_EN([RF_STATUS_CTRL: B0 0x0A(5)])
RF state setting after packet transmission completion	TXDONE_MODE([RF_STATUS_CTRL: B0 0x0A(1-0)])
RF state setting after packet reception completion	RXDONE_MODE([RF_STATUS_CTRL: B0 0x0A(3-2)])
Automatic RX_ON/TX_ON by Wake-up time	WAKEUP_MODE([SLEEP/WU_SET:B0 0x2D(6)]) WAKEUP_EN([SLEEP/WU_SET:B0 0x2D(4)])
Automatic VCO calibration after exit from SLEEP	AUTO_VCOCAL_EN([VCO_CAL_START: B0 0x6F(4)])
Automatic SLEEP by Timer	WU_DURATION_EN([SLEEP/WU_SET: B0 0x2D(5)])
Automatic SLEEP by high speed carrier checking mode	FAST_DET_MODE_EN([CCA_CTRL:B0 0x39(3)])
Force_TRX_OFF after PLL unlock detection during TX	PLL_LD_EN([PLL_LOCK_DETECT: B1 0x0B(7)])

○State Diagram

Each state transition control is decribed in the follwing state diagram.



[STATE]

DEEP SLEEP	: DEEP SLEEP
SLEEP	: SLEEP
TRX_OFF/IDLE	: IDLE (TX-RX stand-by)
PLL_WAIT	: PLL stand-by
TX_ON	: TX ready (TX data waiting)
TRANSMIT	: TX on-going
RX_ON	: RX stand-by (RX data waiting)
RECEIVE	: RX on-going
VCO_CAL	: VCO calibration

State transition instruction
Pins control
Normal sequence (state transition)
Command from Higher layer state
ML7406 Self controlled state transition

LSI state diagram

(Note)
The following state transition is inhibited;
DEEP SLEEP → any state → SLEEP

○SLEEP setting

DEEP_Sleep mode: Powers for all blocks except IO pins are turned off.
Sleep mode: Main regulator and 26MHz oscillation circuits are tured off. But sub-regulator is turned-on.
The following registers can be programmed to control SLEEP state.

Function	Control bit name
Power control	PDN_EN([SLEEP/WU_SET: B0 0x2D(1)])
Wake-up setting	WAKEUP_EN([SLEEP/WU_SET: B0 0x2D(4)])
Wake-up timer clock source setting	WUT_CLK_SOURCE([SLEEP/WU_SET: B0 0x2D(2)])
Internal RC oscillator control	RC32K_EN ([CLK_SET2: B0 0x03(3)])

Setting method and internal state for DEEP_SLEEP and various SLEEP modes are as follows:

SLEEP mode	Setting method	main regulator	Sub regulator	26MHz oscillator	RC oscilator	Low clock timer	FIFO
DEEP_SLEEP	RESETN pin="L" REGPDIN pin="H"	OFF	OFF	OFF	OFF	OFF	OFF
SLEEP1	not supported	-	-	-	-	-	-
SLEEP2	[SLEEP/WU_SET: B0 0x2D(4-0)] = 0b0_1001 (*2) [CLK_SET2: B0 0x03(3)] = 0b0 (default)	OFF	ON	OFF	OFF(*1)	OFF	ON
SLEEP3	[SLEEP/WU_SET: B0 0x2D(4-0)] = 0b1_1001 (*2) [CLK_SET2: B0 0x03(3)] = 0b0 (default)	OFF	ON	OFF	OFF	ON	ON
SLEEP4	[SLEEP/WU_SET: B0 0x2D(4-0)] = 0b1_1101 (*2) [CLK_SET2: B0 0x03(3)] = 0b1	OFF	ON	OFF	ON	ON	ON

(*1) Low speed clock is supplied from EXT_CLK pin.
(*2) Please set proper value to [SLEEP/WU_SET: B0 0x2D(3)].

(Note)
Contents of registers are not kept during DEEP_SLEEP. Contents of registers are kept during SLEEP2,SLEEP3,SLEEP4.

○Notes to set RF state

ML7406 is able to change the internal RF state transition autonomously (without commands from MCU) as well as RF state change commands from MCU. (please refer to ”LSI state transition instruction”). If both timing of operation (autonomous state and state change from MCU command) overlapped, unintentional RF state may occur. Timing of autonomous state RF change is described in the following table.
Care must be taken not to overlap the conditions.

Function	RF state change (before→after)	RF state transition timing (not from Host MCU command)	Recommended process
Automatic TX	TRX_OFF/RX_ON →TX_ON	After TX data transfer completion interrut occurs, { value [TX_RATE_H/L: B1 0x02/03)] * 2 / 26}[µs] period.	Write access to [RF_STATUS:B0 0x0B] is possible after RF state transition completion interrupt (INT[3] group1), or move to the state defined by GET_TRX ([RF_STATUS:B0 0x0B(7-4)]).
FAST_TX mode		When FIFO write access exceed trigger level +1, { value [RX_RATE1_H/L:B1 0x04/05] * 5 / 26}[µs] period.	
RF state setting after TX completion	TX_ON→TRX_OFF	After TX completion interrupt (INT[16] group3), { value [TX_RATE_H/L:B1 0x02/03] * 2 / 26} [µs] period	
	TX_ON→RX_ON		
	TX_ON→SLEEP		
RF state setting after RX completion	RX_ON→TRX_OFF	After data RX completion interrupt (INT[8] group2, { value [RX_RATE1_H/L:B1 0x04/05] * 2 / 26}[µs] period	
	RX_ON→TX_ON		
	RX_ON→SLEEP		
Wake-up timer	SLEEP→TX_ON	After wake-up timer completion interrupt (INT[6] group1), 1 clock cycle period defined by WUT_CLK_SET[3:0] ([WUT_CLK_SET:B0 0x2E (3-0)]).	
	SLEEP→RX_ON		
	SLEEP→VCO_CAL →TX_ON	After wake-up timer completion interrupt (INT[6]: group1), before VCO calibration completion interrupt (INT[1] group1).	Write access to [RF_STATUS:B0 0x0B] and BANK2 is possible after VCO calibration completion interrupt (INY[1] group1).
	SLEEP→VCO_CAL →RX_ON		
Continuous operation timer	TX_ON→SLEEP	After continuous operation timer completion, 1 clock cycle period defined by WUT_CLK_SET[3:0] ([WUT_CLK_SET:B0 0x2E (3-0)]).	Write access to [RF_STATUS:B0 0x0B] is possible after RF state transition completion interrupt (INT[3] group1), or move to the state defined by GET_TRX ([RF_STATUS:B0 0x0B(7-4)]).
	RX_ON→SLEEP		
High speed carrier checking	RX_ON→SLEEP	After CCA completion interrupt, duration 6.3[µs].	
PLL unlock detection	TX_ON→TRX_OFF	After PLL unlock detection interrupt (INT[2] group1) occurs, duration 147[µs].	Write access to [RF_STATUS:B0 0x0B] is possible 147µs after PLL unlock interrupt (INT[2] group1) detected.

●Packet Handling Function

○Packet format

ML7406 supports Wireless M-BUS frame FormatA/B, and Format C which is non Wireless M-BUS universal format. The following packet handling are supported in FIFO mode or DIO mode

1) Preamble and SyncWord automatic insertion (TX) --- DIO/FIFO mode
2) Preamble and SyncWord automatic detection (RX) --- DIO/FIFOmode
3) Preamble and SyncWord automatic deletion (RX) --- DIO/FIFO mode
4) CRC data insertion (TX) --- FIFO mode
5) CRC check and error notification (RX) --- DIO/FIFO mode

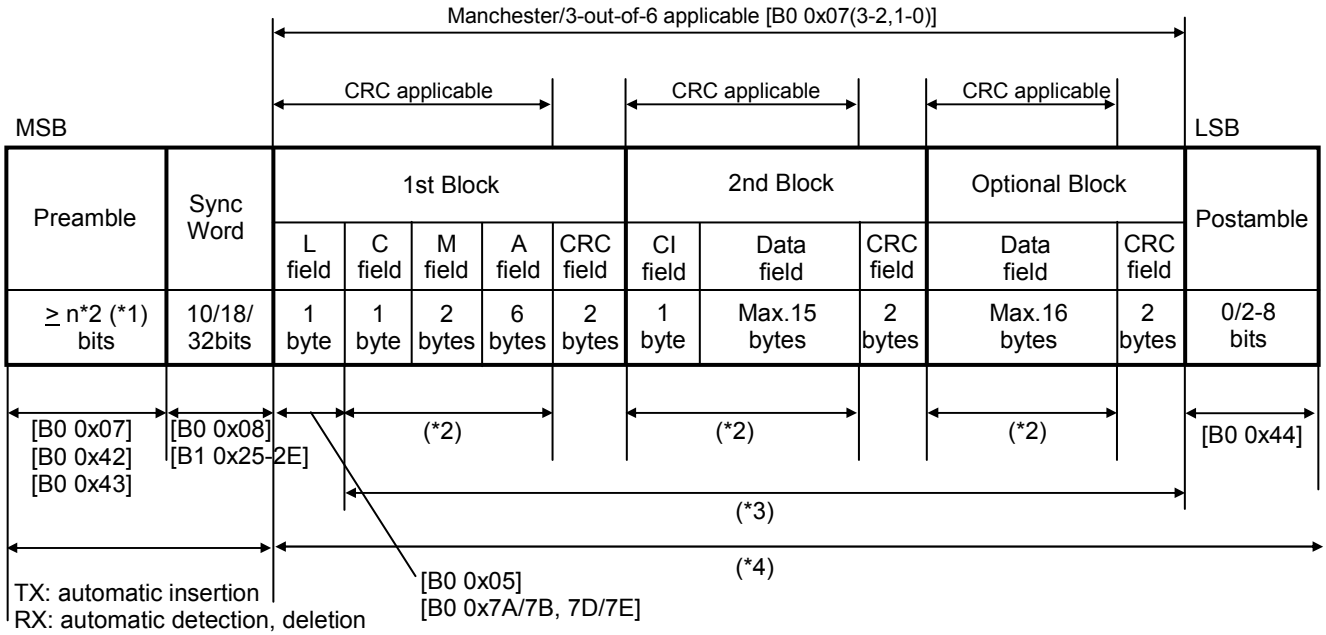
The following table shws control bits relative with the Packet format function.

Function	Control bit name
Packet formatsetting	PKT_FORMAT[1:0] ([PKT_CTRL1: B0 0x04(1-0)])
IEEE 802.15.4g setting	IEEE802_15_4G_EN ([PKT_CTRL1: B0 0x04(2)])
RX extended link layer mode disable	RX_EXTPKT_OFF ([PKT_CTRL1: B0 0x04(3)])
Data area bit order setting	DAT_LF_EN ([PKT_CTRL1: B0 0x04(4)])
Length area bit order setting	LEN_LF_EN ([PKT_CTRL1: B0 0x04(5)])
Extended link layer mode setting	EXT_PKT_MODE[1:0] ([PKT_CTRL1: B0 0x04(7-6)])
Length field setting	LENGTH_MODE ([PKT_CTRL2: B0 0x05(0)])

(1) Format A (Wireless M-BUS)

By setting PKT_FORMAT[1:0] ([PKT_CTRL1: B0 0x04(1-0)])=0b00, Wireless M-BUS Format A is selected.
Format A consists of 1st Block, 2nd Block and Optional Block(s). Each block has 2 bytes of CRC. "L-field" (1st byte of 1st Block) indicates packet length, which includes subsequenct user data bytes from "C-field". However, CRC bytes and postamble are excluded. Depending on "L-field" value, 2nd Block and Optional Block(s) are added.

The following [] indicates register address [bank #, address].



*1: Each mode has different minimum value of n.
*2: Indicates TX FIFO data storage area size.
*3: Indicates RX FIFO data storage area size.
*4: When RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b10, indicates DCLK/DIO output area.

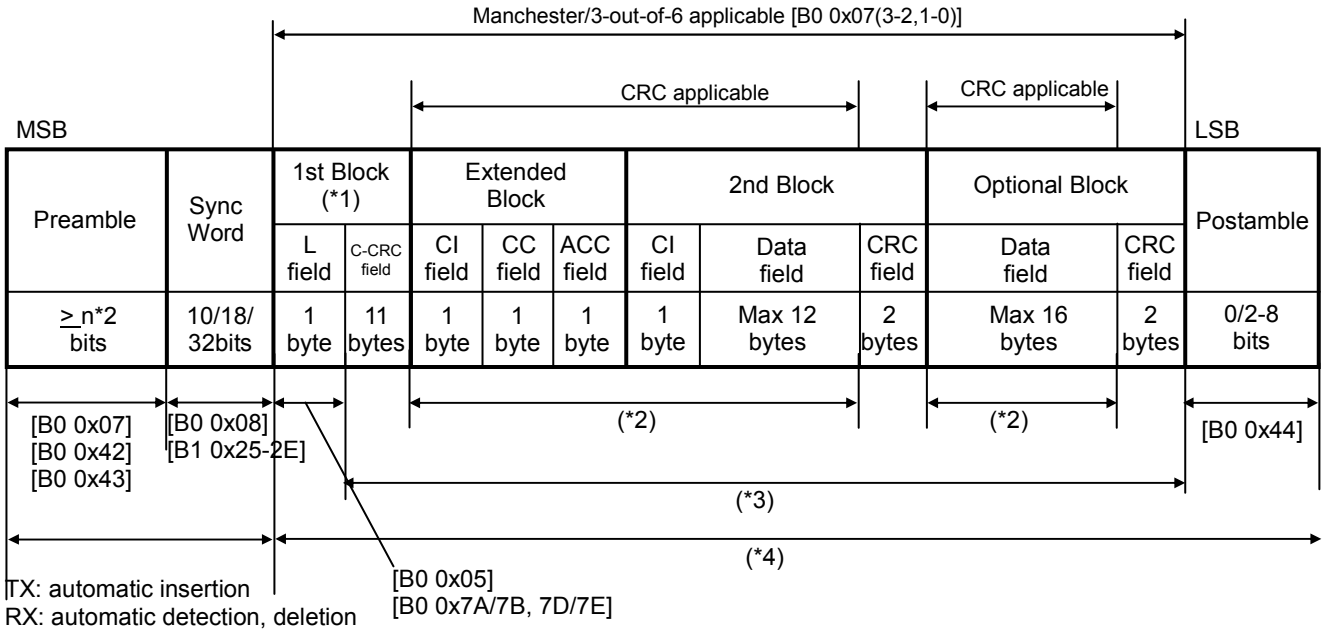
Extended Link Layer Format

If "CI-field" (1st byte of 2nd Block)=0x8C or 0x8D, Extended Link Layer is applied. The packet format is as follows:

(a) CI-field = 0x8C

For TX, if 2 bytes extention format is used, set EXT_PKT_MODE[1:0] ([PKT_CTRL1: B0 0x04(7-6)])=0b01.

For RX, if RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)])=0b0, ML7406 recognizes "CI-field" and RX operation is processed.



*1: 1st Block is identical to normal Format A..

*2: Indicates TX FIFO data storage area size.

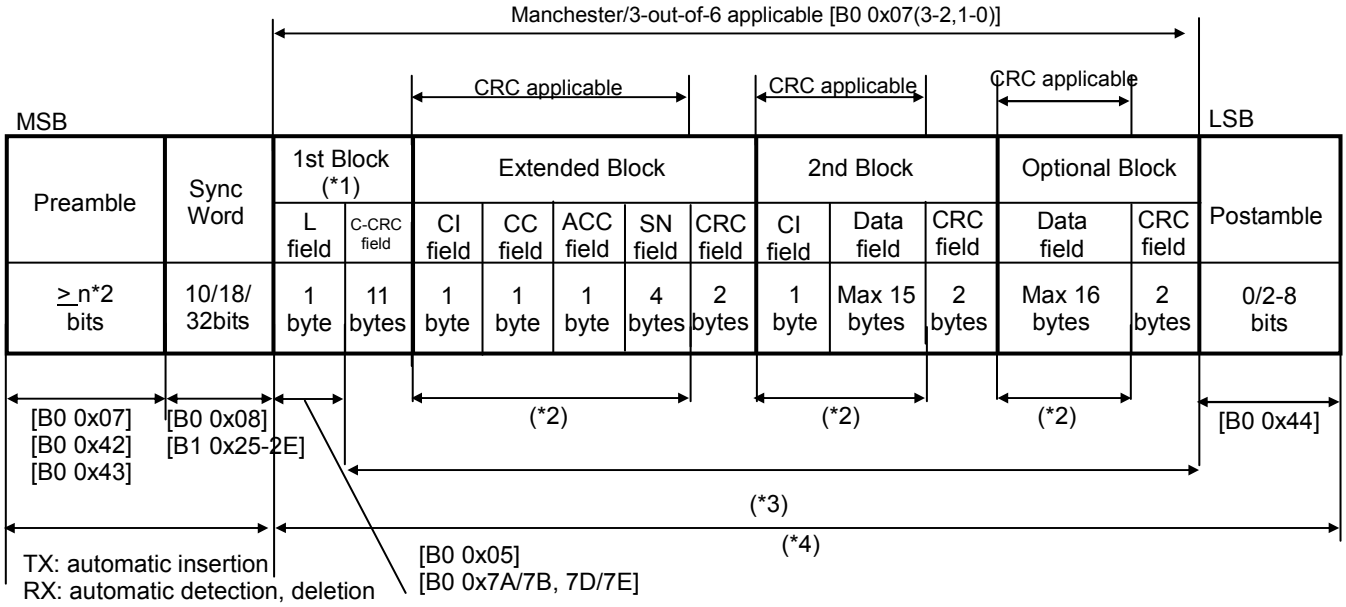
*3: Indicates RX FIFO data storage area size.

*4: When RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b10, indicating DCLK/DIO output area.

(b) CI-field = 0x8D

For TX, if 8 bytes extention format is used, set EXT_PKT_MODE[1:0] ([PKT_CTRL1: B0 0x04(7-6)])=0b10.

For RX, if RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)])=0b0, ML7406 recognizes “CI-field” and RX operation is processed.



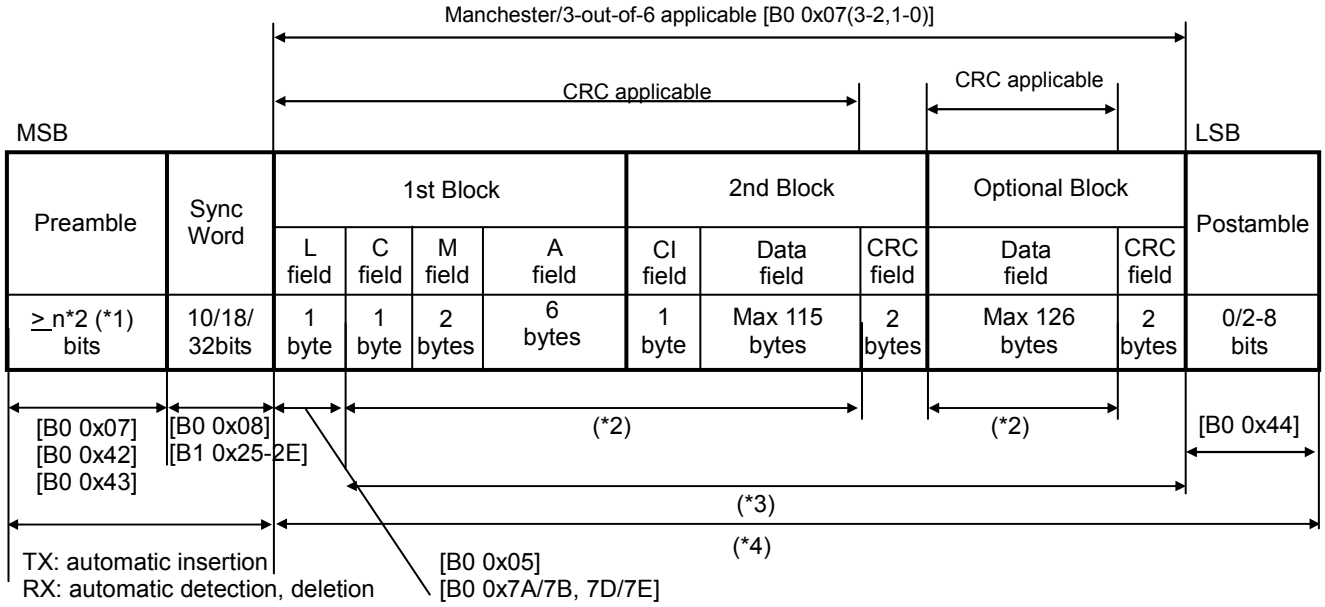
*1: 1st Block is identical to normal Format A..
*2: Indicating TX FIFO data storage area size.
*3: Indicating RX FIFO data storage area size.
*4: When RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b10, indicating DCLK/DIO output area.

(2) Format B (Wireless M-BUS)

By setting PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)])=0b01, Wireless M-BUS Format B is selected.

Format B consists of 1st Block, 2nd Block or Optional Block. Each block after 2nd Block has 2 bytes of CRC. "L-field" indicates packet length, which includes subsequent user data bytes from "C-field". However, unlike Format A, CRC bytes are included (Pastamble are exclueded). Depending on "L-field" value, 2nd Block and Optional Block(s) are added.

The following [] indicates register address [bank #, address].



*1: Each mode has different minimum value of n.
*2: Indicates TX FIFO data storage area size.
*3: Indicates RX FIFO data storage area size.
*4: When RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b10, indicating DCLK/DIO output area.

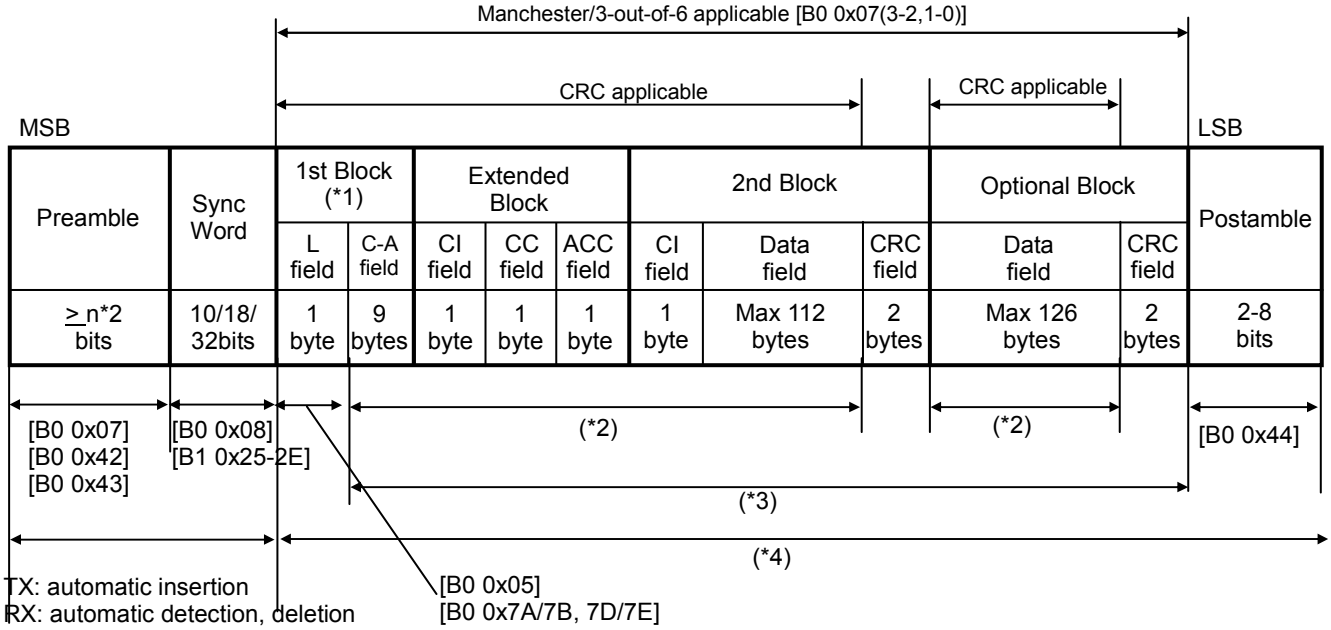
Extended Link Layer Format

If "CI-field" (1st byte of 2nd Block) = 0x8C or 0x8D, Extended Link Layer is applied. The packet format is as follows:

(a) CI-field = 0x8C

For TX, if 2bytes extention format is used, set EXT_PKT_MODE[1:0] ([PKT_CTRL1: B0 0x04(7-6)])=0b01.

For RX, if RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)])=0b0, ML7406 recognizes "CI-field" and RX operation is processed.

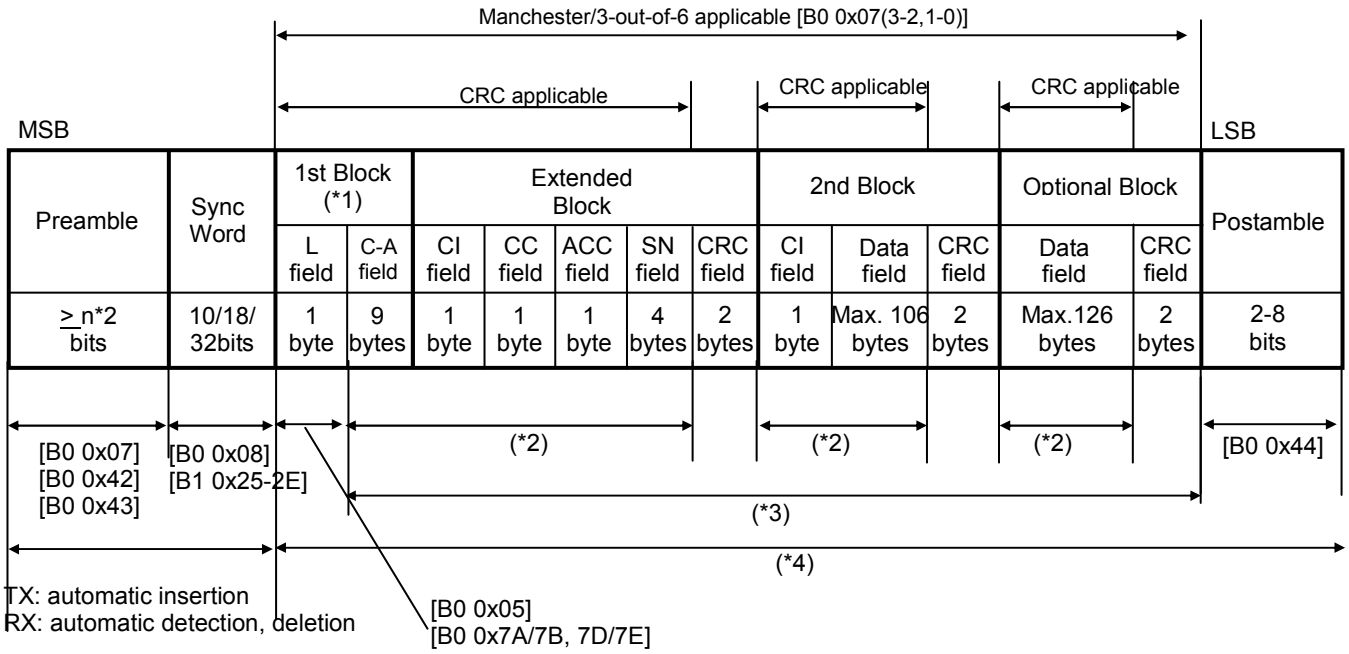


*1: 1st Block is identical to normal Format B..
*2: Indicating TX FIFO data storage area size.
*3: Indicating RX FIFO data storage area size.
*4: When RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b10, indicating DCLK/DIO output area.

(b) CI-field = 0x8D

For TX, if 8 bytes extention format is used, set EXT_PKT_MODE[1:0]([PKT_CTRL1: B0 0x04(7-6)])=0b10.

For RX, if RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)])=0b0, ML7406 recognizes “CI-field” and RX operation is processed.

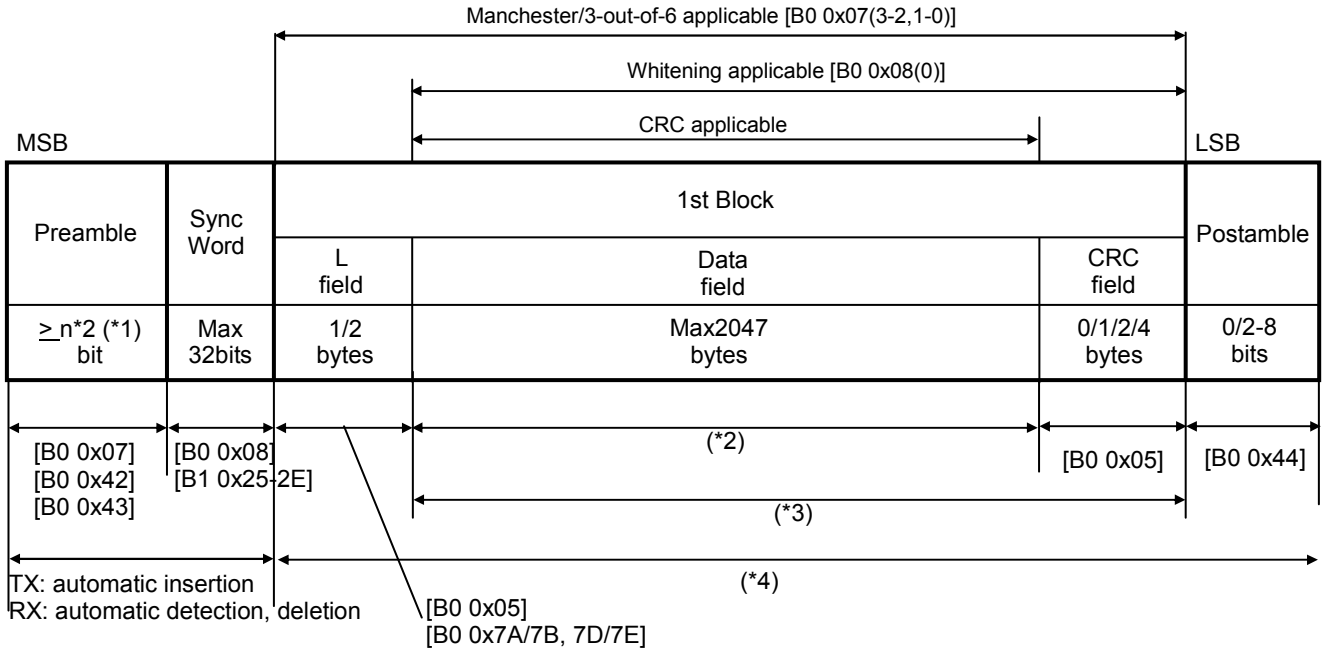


*1: 1st Block is identical to normal Format B..
*2: Indicating TX FIFO data storage area size.
*3: Indicating RX FIFO data storage area size.
*4: When RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b10, indicating DCLK/DIO output area.

(3) Format C (non Wireless M-BUS, general purpose format)

By setting PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)])=0b10, Format C, which is non Wireless M-BUS format, is selected. Format C consists of 1st Block only, which has 2 bytes of CRC. "L-field" indicates packet length, which includes subsequent user data bytes, including CRC bytes. The length of "L-field" is defined by LENGTH_MODE([PKT_CTRL2:B0 0x5(0]). Data Whitening function is supported.

The following [] indicates register address [bank #, address].



*1 Preamble length (n) is programmable by [TXPR_LEN_H/L: B0 0x42/43] registers.
*2 indicating TX FIFO data strorage area size.
*3 Indicating RX FIFO data storage area size.
*4 When RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)])=0b10, indicating DCLK/DIO output area.

○CRC function

ML7406 has CRC32,CRC16 and CRC8 function. CRC is calculated and appended to TX data. CRC is checked for RX data. The following modes are used for automatic CRC function.

●FIFO mode: RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b00
●DIO mode: RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b11

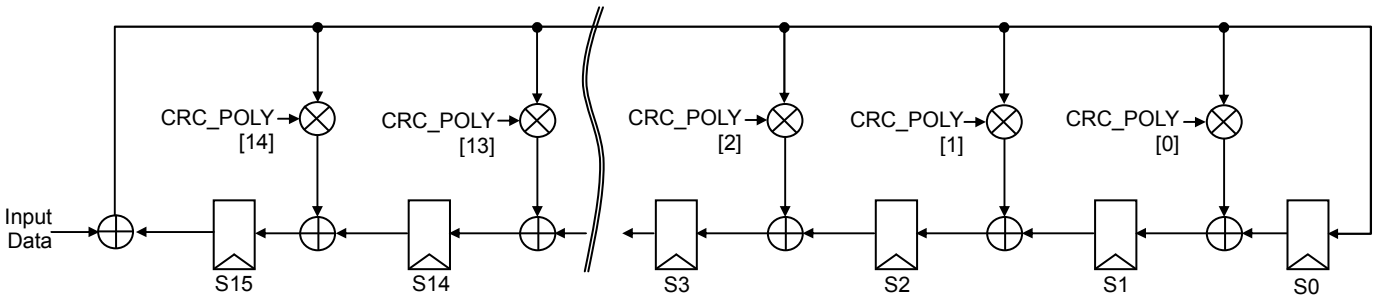
Function	Control bit name / Register
TX CRC setting	TX_CRC_EN([PKT_CTRL2: B0 0x05(2)])
RX CRC setting	RX_CRC_EN([PKT_CTRL2: B0 0x05(3)])
CRC length setting	CRC_LEN([PKT_CTRL2: B0 0x05(5-4)])
CRC complement value OFF setting	CRC_COMP_OFF([PKT_CTRL2: B0 0x05(6)])
CRC polynomial setting	[CRC_POLY3/2/1/0: B1 0x16/17/18/19] registers
CRC error status	[CRC_ERR_H/M/L: B0 0x13/14/15] registers

Any CRC polynomials for CRC32/CRC16/CRC8 can be specified. Reset value is as follows:

CRC16 polynomial = $x^{16} + x^{13} + x^{12} + x^{11} + x^{10} + x^8 + x^6 + x^5 + x^2 + 1$ (reset value)

(Note) CRC result data can be inverted by CRC complement value OFF setting,.

CRC data will be generated by the following circuits. By programming [CRC_POLY3/2/1/0] registers, any CRC polynomials can be supported. Generated CRC will be transfer from the left most bit (S15). If data length is shorter than CRC length (3 bytes of CRC32 only), data "0"s will be added for CRC calculation. CRC check result is stored in [CRC_ERR_H/M/L] registers.
Unlike Format C, Format A/B can include multiple CRC fields in one packet. For multiple CRCs check results, CRC value closest to L-field will be stored in CRC_ERR[0] ([CRC_ERR_L:B0 0x15(0)]). Subsequent bit will be stored in CRC_ERR from MSB order.



(Note) ⊕ :exclusive OR

CRC polynomial circuits

General CRC polynomial can be programmed by below [CRC_POLY3/2/1/0] register setting.
CRC length can be set by CRC_LEN.

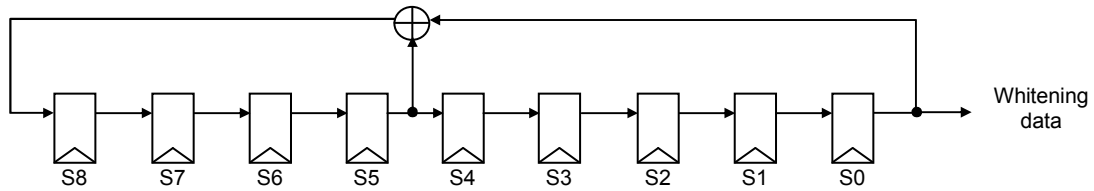
CRC polynomial		[CRC_POLY3/2/1/0]			
		(B1 0x16)	(B1 0x17)	(B1 0x18)	(B1 0x19)
CRC8	$x^8 + x^2 + x + 1$	0x00	0x00	0x00	0x03
CRC16	$x^{16} + x^{12} + x^5 + 1$	0x00	0x00	0x08	0x10
	$x^{16} + x^{15} + x^2 + 1$	0x00	0x00	0x40	0x02
	$x^{16} + x^{13} + x^{12} + x^{11} + x^{10} + x^8 + x^6 + x^5 + x^2 + 1$	0x00	0x00	0x1E	0xB2
CRC32	$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$	0x02	0x60	0x8E	0xDB

○Data whitening function (non Wireless M-BUS standard)

ML7406 supports Data whitening function. In packet format A/B, subsequent data followed by C-field can be processed data whitening. In packet format C, data Whitening is applied from data field. Data generated by the following 9 bit pseudo random sequence (PN9) will be "XOR" with TX data (encoded data if Manchester or 3-out-of 6 coding is selected) before transmission. Intialization value of the PN9 generation shift register can be defined by [WHT_INIT_H/L: B1 0x64/65] registers. PN9 polynomial can be programmed with [WHT_CFG: B1 0x66] register.

Function	Control bit name
Data Whiteing setting enable	WHT_SET ([DATA_SET2: B0 0x08(0)])
Data Whiteing initiazation value	WHT_INIT[8:0] ([WHT_INIT_H/L: B1 0x64(0)/65(7-0)])
Whitening polynomia	WHT_CFG[7:0] ([WHT_CFG: B1 0x66(7-0)])

In order to make feedback from S1 register, setting 0b1 to WHT_CFG0 ([WHT_CFG: B1 0x66(0)]). Similaly in order to make feedback from S2 register, setting 0b1 to WHT_CFG1 ([WHT_CFG: B1 0x66(1)]). Other bits of [WHT_CFG: B1 0x66] register has same function. Two or more bits can be also set to 0b1. Therefore any type of PN9 polinominal can be programmed.



(Note) ⊕ :exclusive OR

Whitening data generation circuits
(generator polynomial: $x^9 + x^5 + 1$)

General PN9 polynomial can be defined by [WHT_CFG].

PN9 polynomial	WHT_CFG[7:0] [WHT_CFG: B1 0x66]
$x^9 + x^4 + 1$	0x08
$x^9 + x^5 + 1$	0x10

○SyncWord detection function

ML7406 supports automatic SyncWord recognition function. By having two sets of SyncWord pattern storage area, it is possible to detect two different packet format (Format A/B) which are defined by Wireless M-Bus. (For details, please refer to Wireless M-BUS standard) Receiving packet format is indicated by SW_DET_RSLT([STM_STATE:B0 0x77(5)]). In Format C, it is possible to search for two SyncWords but detected result is not indicated.

1) TX

SyncWord pattern defined by SYNCWORD_SEL ([DATA_SET2: B0 0x08(4)]) will be selected. SyncWord length for TX is defined by SYNC_WORD_LEN[5:0] ([SYNC_WORD_LEN: B1 0x25(5-0)]). From high bit of each SyncWord pattern will be transmitted.

SYNCWORD_SEL	TX SyncWord pattern
0	SYNC_WORD1[31:0] ([SYNCWORD1_SET3/2/1/0: B1 0x27/28/29/2A])
1	SYNC_WORD2[31:0] ([SYNCWORD2_SET3/2/1/0: B1 0x2B/2C/2D/2E])

Example) SyncWord patten and SyncWord length

If the follwing registers are programmed, from higher bit of SYNC_WORD1[17:0] will be transmitted sequencially.
[SYNC_WORD_LEN: B1 0x25]=0x12
SYNCWORD_SEL ([DATA_SET2: B0 0x08(4)]) = 0b0

If the following registers are programmed, from higher bit of SYNC_WORD2[23:0] will be transmitted sequencially.
[SYNC_WORD_LEN: B1 0x25]=0x18
SYNCWORD_SEL ([DATA_SET2: B0 0x08(4)]) = 0b1

2) RX

By setting SYNCWORD_SEL and 2SW_DET_EN ([DATA_SET2: B0 0x08(4,3)]), One SyncWord pattern waiting or two SyncWord patterns waiting can be selected as follows: Packet format automatic detection is valid if 2SW_DET_EN=0b1 and Format A or Fromat B is selected by PKT_FORMAT[1:0] ([PKT_CTRL1:B0 0x04(1-0)]).

2SW_DET_EN	SYNCWORD_SEL	SyncWord pattern During Sync Detection	SyncWord Detection operation	Automatic packet format detection	Data process after SyncWord
0	0	SYNC_WORD1[31:0]	Waiting for 1 pattern	no	Process according to each Format setting
0	1	SYNC_WORD2[31:0]	Waiting for 1 pattern	no	Process according to each Format setting
1	–	SYNC_WORD1[31:0] SYNC_WORD2[31:0]	Waiting for 2 patterns	yes	[Format A or Format B setting] If matched with SYNC_WORD1, then process as Format A. If matched with SYNC_WORD2, then process as Format B. [Format C setting] Process as Format C

Length of SyncWord pattern can be defined by SYNC_WORD_LEN[5:0] ([SYNC_WORD_LEN: B1 0x25(5-0)]). In this case, SyncWord pattern defined by the length from low bit of SYNC_WORD1[31:0] or SYNC_WORD2[31:0] will be the pattern for checking.

Example) SyncWord length

If the following registers are set, 18 bit of SYNC_WORD1[17:0] or SYNC_WORD2[17:0] will be reference pattern for the SyncWord detection. Higher bits (bit31-18) are not checked.

[SYNC_WORD_LEN: B1 0x25]=0x12

[SYNC_WORD_EN: B1 0x26]=0x0F

32bit SyncWord pattern can be controlled by enabling/disabling by each 8bit, when receiving SyncWord. The following table describes enable/disable control and SyncWord pattern.

[SYNC_WORD_EN] (B1 0x26)	SYNC_WORD*				SyncWord detection operation
	[31:24]	[23:16]	[15:8]	[7:0]	
0000					No SyncWord detection
0001	D.C.(*1)			ON	Only [7:0] are valid. Upon [7:0] detection, SyncWord detection.
0010	D.C.		ON	D.C.	Only [15:8] are valid. Upon [7:0] detection, SyncWord detection.
0011	D.C.		ON	ON	[15:0] are valid. Upon [7:0] detection, SyncWord detection.
0100	D.C.	ON	D.C.		Only [23:16] are valid. Upon [7:0] detection, SyncWord detection.
0101	D.C.	ON	D.C.	ON	[23:16] and [7:0] are valid. Upon [7:0] detection, SyncWord detection.
0110	D.C.	ON	ON	D.C.	[23:8] are valid. Upon [7:0] detection, SyncWord detection.
0111	D.C.	ON	ON	ON	[23:0] are valid. Upon [7:0] detection, SyncWord detection.
1000	ON	D.C.			Only [31:24] are valid. Upon [7:0] detection, SyncWord detection.
1001	ON	D.C.		ON	[31:24] and [7:0] are valid. Upon [7:0] detection, SyncWord detection.
1010	ON	D.C.	ON	D.C.	[31:24] and [15:8] are valid. Upon [7:0] detection, SyncWord detection.
1011	ON	D.C.	ON	ON	[31:24] and [15:0] are valid. Upon [7:0] detection, SyncWord detection.
1100	ON	ON	D.C.		[31:16] are valid. Upon [7:0] detection, SyncWord detection.
1101	ON	ON	D.C.	ON	[31:16] and [7:0] are valid. Upon [7:0] detection, SyncWord detection.
1110	ON	ON	ON	D.C.	[31:8] are valid. Upon [7:0] detection, SyncWord detection.
1111	ON	ON	ON	ON	Whole [31:0] are valid. Upon [7:0] detection, SyncWord detection.

*1 D.C. stands for Don't Care.

*2 Preamble pattern can be added to the SyncWord detection conditions by RXPR_LEN[5:0]([SYNC_CONDITION1: B0 0x45(5-0)]).

○Field check function

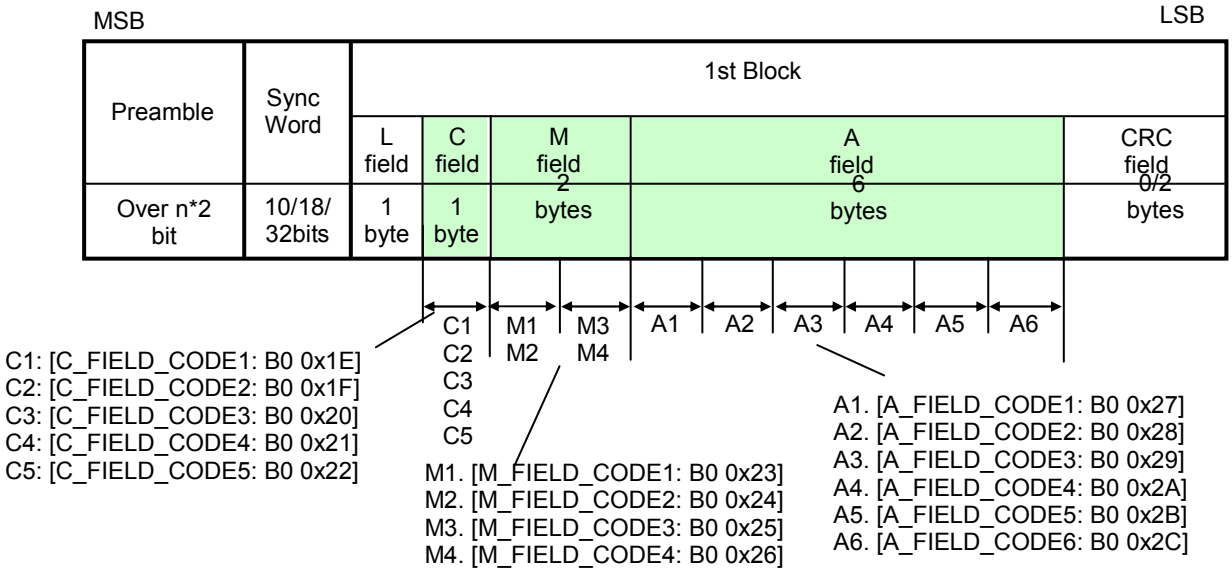
ML7406 has the function of caparing the 9 bytes following L-field (Format A/B: start from C-field, Format C: start from Data-field) in a receiving packet. Based on comparison with the expected data, possible to generate interrupts (Field check function). Field check can be possible with the following register setting. When using this function, RXDIO_CTRL[1:0] ([DIO_SET:B0 0x0C(7-6)]) =0b00 (FIFO mode) or 0b11 (data output mode 2) setting is required.

Function	Register
RX data process setting when Field check unmatched	[C_CHECK_CTRL: B0 0x1B(7)]
Field check interrupt setting	[C_CHECK_CTRL: B0 0x1B(6)]
C-field detection enable setting	[C_CHECK_CTRL: B0 0x1B(4-0)]
M-field detection enable setting	[M_CHECK_CTRL: B0 0x1C(3-0)]
A-field detection enable setting	[A_CHECK_CTRL: B0 0x1D(5-0)]
C-field code setting	[C_FIELD_CODE1: B0 0x1E] [C_FIELD_CODE2: B0 0x1F] [C_FIELD_CODE3: B0 0x20] [C_FIELD_CODE4: B0 0x21] [C_FIELD_CODE5: B0 0x22]
M-field code setting	[M_FIELD_CODE1: B0 0x23] [M_FIELD_CODE2: B0 0x24] [M_FIELD_CODE3: B0 0x25] [M_FIELD_CODE4: B0 0x26]
A-field code setting	[A_FIELD_CODE1: B0 0x27] [A_FIELD_CODE2: B0 0x28] [A_FIELD_CODE3: B0 0x29] [A_FIELD_CODE4: B0 0x2A] [A_FIELD_CODE5: B0 0x2B] [A_FIELD_CODE6: B0 0x2C]

The following describes the relation between each comparison code and incoming RX data.

[Format A/B(Wireless M-Bus)]

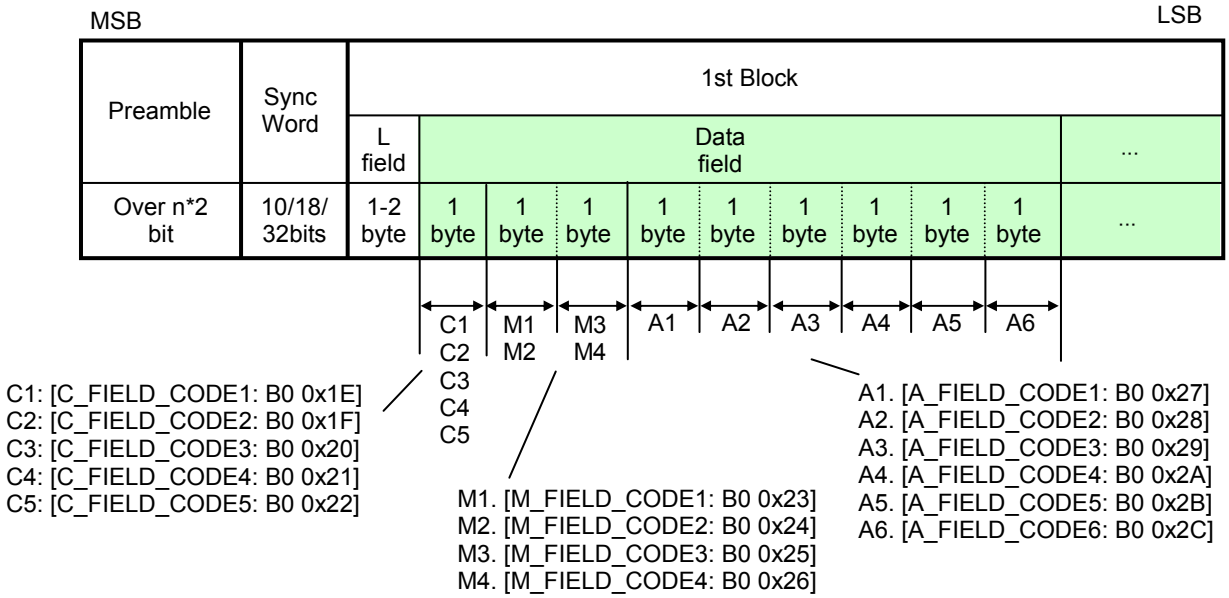
Field check can be controlled by setting disabled/enabled for each comparison code (1 byte). If all specified Field data (C-field/M-field/A-field) are matched, Field checking matching will be notified. However, if C-field data and C_FIELD_CODE5 are matched, even if other Field data (M-field/A-field) are not matched, Field check result will be notified as ”match”.



Check Field	Comaprison Code	Conditions for match
C-field	C_FIELD_CODE1 or C_FIELD_CODE2 or C_FIELD_CODE3 or C_FIELD_CODE4 or C_FIELD_CODE5	If one of the 5 comparison code is matched
M-field 1st byte	M_FIELD_CODE1 or M_FIELD_CODE2	If one of the 2 comparison code is matched.
M-field 2nd byte	M_FIELD_CODE3 or M_FIELD_CODE4	If one of the 2 comparison code is matched.
A-field	A_FIELD_CODE1/2/3/4/5/6	If comparison codes are matched.

[Format C]

Field check can be controlled by setting disabled/enabled for each comarison code (1 byte). If all specified Field data (specified table below) are matched, Field checking matching will be notified. However, if 1st byte of Data field and C_FIELD_CODE5 are matched, even if other Field data(from 2nd byte of Data field to 9th byte of Data field) are not matched, Field check result will be notified as "match".



Check Field	Comparison Code	Conditions for match
Data-field 1st byte	C_FIELD_CODE1 or C_FIELD_CODE2 or C_FIELD_CODE3 or C_FIELD_CODE4 or C_FIELD_CODE5	If one of the 5 comparison code is matched
Data-field 2nd byte	M_FIELD_CODE1 or M_FIELD_CODE2	If one of the 2 comparison code is matched.
Data-field 3rd byte	M_FIELD_CODE3 or M_FIELD_CODE4	If one of the 2 comparison code is matched.
Data-field 4th byte	A_FIELD_CODE1	If comparison code is matched.
Data-field 5th byte	A_FIELD_CODE2	If comparison code is matched.
Data-field 6th byte	A_FIELD_CODE3	If comparison code is matched.
Data-field 7th byte	A_FIELD_CODE4	If comparison code is matched.
Data-field 8th byte	A_FIELD_CODE5	If comparison code is matched.
Data-field 9th byte	A_FIELD_CODE6	If comparison code is matched.

●Packet processing as a result of Field checking

By setting CA_RXD_CLR ([C_CHECK_CTRL: B0 0x1B(7)])=0b1, if the result of Field check is unmatch, data packet will be aborted and wait for next packet data.

●Storing number of unmatched packets

Unmatched packets can be counted up to max. 2047 packets and result are stored in [ADDR_CHK_CTR_H: B1 0x62] and[ADDR_CHK_CTR_L: B1 0x63]. This count value can be cleared by STATE_CLR4 ([STATE_CLR: B0 0x16(4)]).

○FIFO control function

ML7406 has on-chip TX_FIFO(64Byte) and RX_FIFO(64Byte). As TX/RX_FIFO do not support multiple packets, packet should be processed one by one. If RX_FIFO keeps RX packet and next RX packet is received, RX_FIFO will be overwritten. It applies to TX_FIFO as well. However TX FIFO access error interrupt (INT[20] group3) will be generated. When receiving, RX data is stored in FIFO (byte by byte) and the host MCU will read RX data through SPI. When transmitting, host MCU write TX data to TX_FIFO through SPI and transmitting through RF.

Writing or reading to FIFO is through SPI with burst access. TX data is written to [WR_TX_FIFO: B0 0x7C] register. RX data is read from [RD_FIFO: B0 0x7F] register. Continuous access increments internal FIFO counter automatically. If FIFO access is suspended during write or read operation, address will be kept until the packet will be process again. Therefore, when resuming FIFO access, next data will be resumed from the suspended address.

FIFO control register are as follows:

Function	Register
TX FIFO Full level setting	[TXFIFO_THRH: B0 0x17]
TX FIFO Empty level setting	[TXFIFO_THRL: B0 0x18]
RX FIFO Full level setting	[RXFIFO_THRH: B0 0x19]
RX FIFO Empty level setting	[RXFIFO_THRL: B0 0x1A]
FIFO readout setting	[FIFO_SET: B0 0x78]
RX FIFO data usafe status indication	[RX_FIFO_LAST: B0 0x79]
TX packet Length setting	[TX_PKT_LEN_H/L: B0 0x7A/7B]
RX packet Length setting	[RX_PKT_LEN_H/L: B0 0x7D/7E]
TX FIFO	[WR_TX_FIFO: B0 0x7C]
FIFO read	[RD_FIFO: B0 0x7F]

TX – RX procedure using FIFO are as follows:

[TX]

i) TX data L-field value is set to [TX_PKT_LEN_H: B0 0x7A], [TX_PKT_LEN_L: B0 0x7B] register. If Length is 1 byte, [TX_PKT_LEN_L] register will be transmitted.
Length can be set to LENGTH_MODE([PKT_CTRL2: B0 0x05(0)]).

ii) TX data is written to [WR_TX_FIFO:B0 0x7C] register.

(Note)

1. If TX_FIFO write sequence is aborted during transmission, STATE_CLR0 [STATE_CLR:B0 0x16(0)] (TX FIFO pointer clear) must be issued. Otherwise data pointer is kept in the LSI and the next packet is not processed properly.
For example, TX FIFO access error interrupt (INT[20] group3) is generated. This interrupt can be generated when the next packet data is writren to the TX_FIFO before transmitting previous packet data or TX_FIFO overrun (FIFO is written when no TX_FIFO space) or underrun (attempt to transmit when TX_FIFO is empty)
2. Depending on the packet format, TX data Length value is different.
Format A: Length includs data area excluding L-field and CRC data.
Format B: Length includes data area excluding L-field.
Format C: Length includes data area excluding L-field.

[RX]

i) L-field (Length) is read from [RX_PKT_LEN_H: B0 0x7D], [RX_PKT_LEN_L: B0 0x7E] registers.

ii) Reading RX data from RX_FIFO. When reading from RX_FIFO, set FIFO_R_SEL([FIFO_SET: B0 0x78(0)])= 0b0.
If FIFO_R_SEL=0b1 , TX_FIFO will be selected. Data usage value of RX_FIFO is indicated by [RX_FIFO_LAST: B0 0x79] register.

(Note)

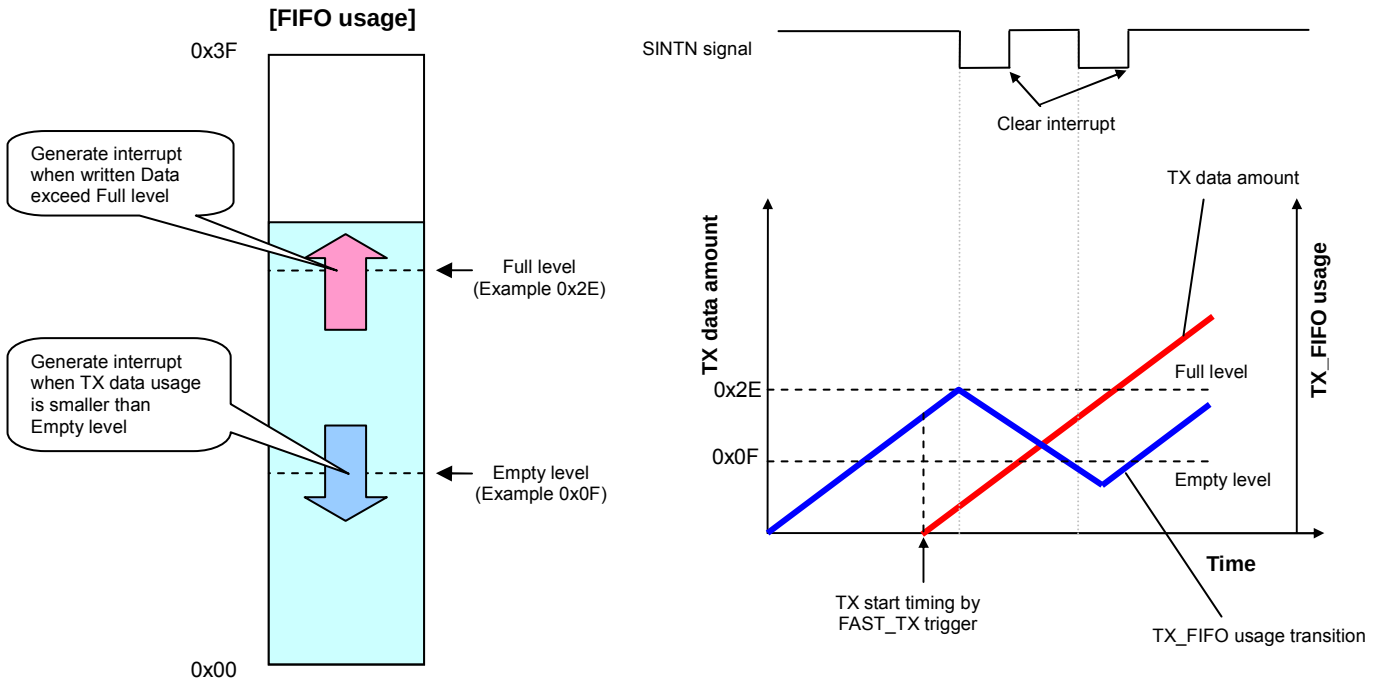
1. If reading FIFO data is terminated before reading all data, STATE_CLR1 [STATE_CLR: B0 0x16(1)] (RX FIFO pointer clear) must be issued. Otherwise If RX_FIFO is not cleared, the pointer controlling FIFO data keeps the same status. Next RX data will not be processed in the FIFO properly.
   For example, when RX_FIFO access error interrupt (INT[12] group2) is generated. This interrupt occurs when RX_FIFO overrun (data received when no space in RX_FIFO) or underrun (reading empty RX_FIFO).
2. If 1 packet data is kept in the RX_FIFO, next RX data will be overwritten.

IF TX/RX pack is larger than FIFO size, FIFO access can be controlled by FIFO-Full trigger or FIFO-Empty trigger.

(1) TX FIFO usage notification function

This function is to notice TX_FIFO usage to the MCU using interrupt (SINTN). If TX_FIFO usage (un-transmitted data in TX_FIFO) exceed the Full level threshold set by [TXFIFO_THRH: B0 0x17] register, interrupt will generate as FIFO-full interrupt (INT[5] group1). If TX_FIFO usage is smaller than Empty level threshold set by [TXFIFO_THRL: B0 0x18] register, FIFO-Empty interrupt will generate as FIFO-Empty interrout (INT[4] grou1). Interrupt signal (SINTN) can be output from GPIO* or EXT_CLK pin.

For output setting, please refer to [GPIO1_CTRL: B0 0x4E], [GPIO1_CTRL: B0 0x4F], [GPIO2_CTRL: B0 0x50], [GPIO3_CTRL: B0 0x51], [EXTCLK_CTRL: B0 0x52] registers for output setting.



(Reference Sequence)

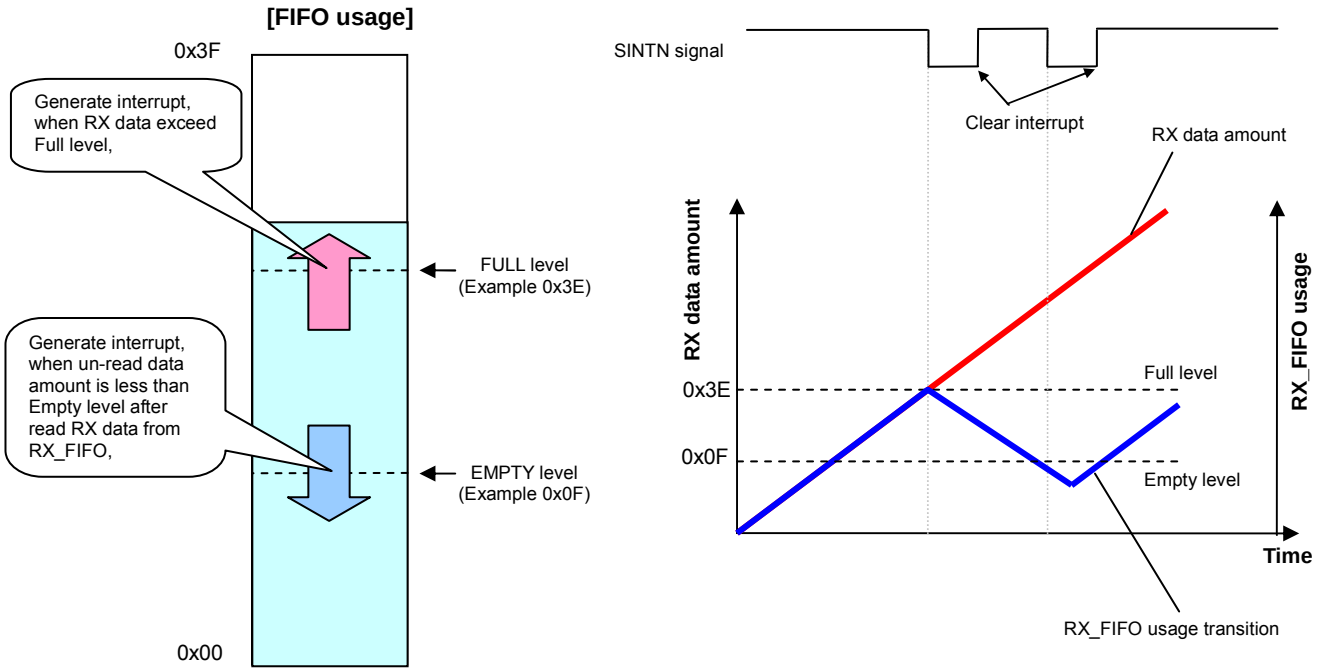
1. Set Full level threshold and Empy level threshold..Each threshold should set as TXFIFO_THRH[5:0] ([TXFIFO_THRH:B0 0x17(5-0)]) > TXFIFO_THRL[5:0] ([TXFIFO_THRL:B0 0x18(5-0)]). And enabling Full level threshold by TXFIFO_THRH_EN([TXFIFO_THRH:B0 0x17(7)=0b1.
2. Enabling FAST_TX mode by FAST_TX_EN([RF_STATUS_CTRL:B0 0x0A(5)])=0b1 and start writing TX data to the TX_FIFO[WR_TX_FIFO:B0 0x7C] until FIFO-Full interrupt (INT[5] group1) occurs.
3. After FIFO-Full interrupt is generated, Clear the interupt. Then disabling Full level threshold (TXFIFO_THRH_EN= 0b0) and enabling Empty level threshold (TXFIFO_THRL_EN([TXFIFO_THRL:B0 0x18(7)])=0b1).
4. After FIFO-Empty interrupt (INT[4] group1) is generated, Clear the interupt. Then disabling Empty level threshold (TXFIFO_THRL_EN=0b0) and enabling Full level threshold (TXFIFO_THRH_ EN=0b1). Then resume writing TX data to the TX_FIFO until next FIFO-Full interrupt occurs.
5. Repeat 3.-4. until completion of TX.

(Note)
When skip disabling threshold level at sequece 3. or 4., depending on TX data read (PHY block) and TX_FIFO write timing through SPI, in the middle of TX_FIFO writing, unwiilling FIFO-Full interrupt or FIFO-Empty interrupt may occurs.

(2) RX FIFO usage notification function

This function is to notify RX_FIFO usage amount by using interrupt (SINTN) to the MCU. If RX_FIFO usage (un-read data in RX_FIFO) exceed Full level threshold defined by [RXFIFO_THRH: B0 0x19] register, interrupt will generate as FIFO-Full interrupt (INT[5] group1). After MCU read RX data from RX_FIFO, un-read amount become smaller than Empty level threshold defined by [RXFIFO_THRL: B0 0x1A] register, interrupt will generated as FIFO-Empty (INT[4] group1). Interrupt signal (SINTN) can be output from GPIO* or EXT_CLK.

For output setting, please refer to [GPIO1_CTRL: B0 0x4E], [GPIO1_CTRL: B0 0x4F], [GPIO2_CTRL: B0 0x50], [GPIO3_CTRL: B0 0x51], [EXTCLK_CTRL: B0 0x52] registers.



(Reference Sequence)

1. Set Full level threshold and Empy level threshold..Each threshold should set as RXFIFO_THRH[5:0] ([RXFIFO_THRH:B0 0x19(5-0)]) > RXFIFO_THRL[5:0] ([RXFIFO_THRL:B0 0x1A(5-0)]). And enabling Full level threshold by RXFIFO_THRH_EN([RXFIFO_THRH:B0 0x19(7)=0b1.
2. After issuing RX_ON, wait FIFO-Full interrupt (INT[5] group1) generation.
3. After FIFO-Full interrupt is generated, Clear the interupt. Then disabling Full level threshold (RXFIFO_THRH_EN= 0b0) and enabling Empty level threshold (RXFIFO_THRL_EN([RXFIFO_THRL:B0 0x1A(7)])=0b1). And start reading RX data from RX_FIFO [RD_FIFO:B0 0x7F].
4. After FIFO-Empty interrupt (INT[4] group1) is generated, Clear the interupt. Then disabling Empty level threshold (TXFIFO_THRL_EN=0b0) and enabling Full level threshold (TXFIFO_THRH_ EN=0b1). Then resume writing TX data to the TX_FIFO until next FIFO-Full interrupt occurs.
5. Repeat 3.-4. until completion of RX data read out.

(Note)
When skip disabling threshold level at sequece 3. or 4., depending on RX data write (PHY block) and RX_FIFO read timing through SPI, in the middle of RX_FIFO reading, unwiilling FIFO-Full interrupt or FIFO-Empty interrupt may occurs.

○DIO function

Using GPIO0-3, EXT_CLK or SDI/SDO pins, TX/RX data can be input/output. Pins can be configured by [GPIO*_CTRL: B0 0x4E/0x4F/0x50/0x51], [EXTCLK_CTRL: B0 0x52] and [SPI/EXT_PA_CTRL: B0 0x53] registers.
Data format for TX/RX are as follows:

TX --- TX data (NRZ or Manchester/3-out-of-6coding) will be input.
RX --- pre-decoded RX data or decoded RX data will be output. (selectable by [DIO_SET: B0 0x0C] register)

DIO function registers are as follows:

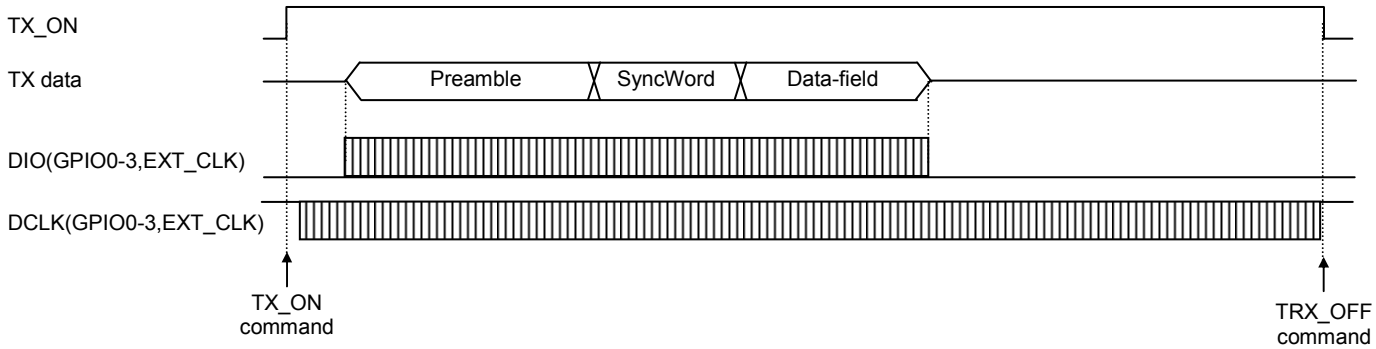
Function	Registers
DIO RX data output start setting	[DIO_SET: B0 0x0C(0)]
DIO RX completion setting	[DIO_SET: B0 0x0C(2)]
TX DIO mode setting	[DIO_SET: B0 0x0C(5-4)]
RX DIO mode setting	[DIO_SET: B0 0x0C(7-6)]

(1) In case of using GPIO*, EXT_CLK pins

If GPIO0-3 or EXT_CLK pins are used as DCLK/DIO, DCLK/DIO should be controlled as follow. (below DIO/DCLK vertical line part indicate output or input period)

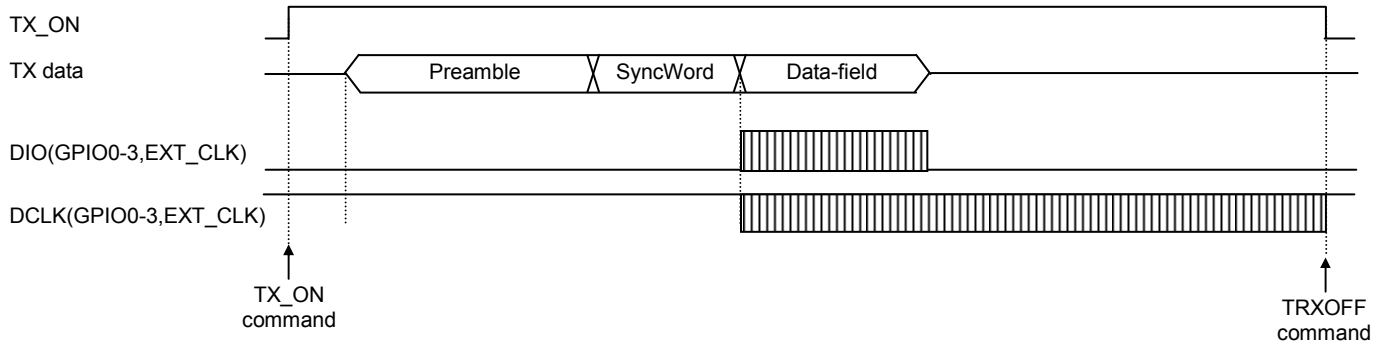
[TX]

i) Continuous input mode (from host)
Set TXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(5-4)]) =0b01.
After TX_ON(SET_TRX[3:0]([RF_STATUS: B0 0x0B(3-0)])=0x9), DCLK is output continuously. At falling edge of DCLK, TX data is input from DIO pin. TX data must be encoded data.



(Note) For details of timing, please refer to the “TX” in the “Timing Chart”.

ii) Data input mode (from host)
Set TXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(5-4)]) =0b10.
After TX_ON, DCLK is output during data input period after SyncWord. TX data is input at falling edge of DCLK through DIO input. Encoded TX data must be transferred from the host. Preamble and SyncWordis generated automatically according to the registers setting.



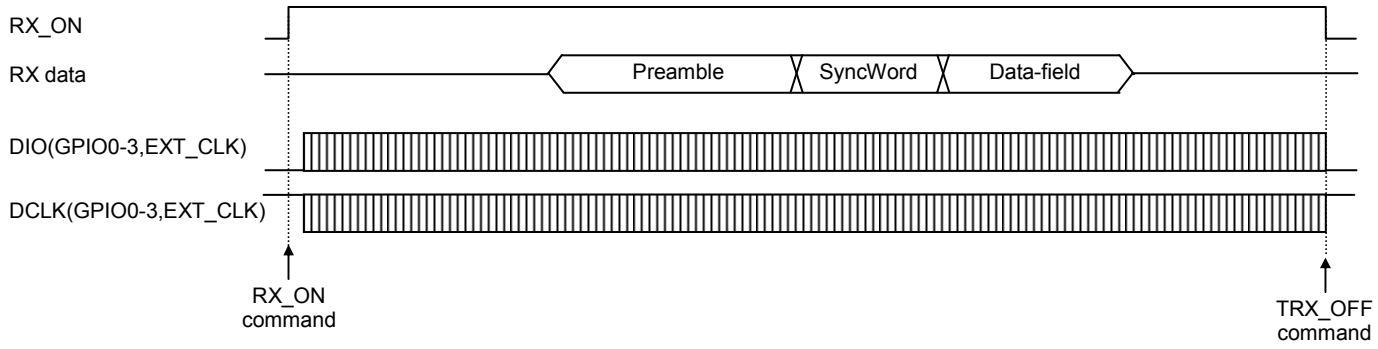
Preamble can be set by PB_PAT([DATA_SET1: B0 0x07(7)] and TXPR_LEN[15:0] ([TXPR_LEN_H/L: B0 0x42/43]). SyncWord can be set by SYNCWORD_SEL([DATA_SET1: B0 0x08(4)), SYNCWORD_LEN[5:0] ([SYNC_WORD_LEN: 1 0x25(5-0)]), SYNC_WORD_EN* ([SYNC_WORD_EN: B1 0x26(3-0)]), SYNC_WORD1[31:0] ([SYNCWORD1_SET3/2/1/0: B1 0x27/28/29/2A]), SYNC_WORD2[31:0] ([SYNCWORD2_SET3/2/1/0: B1 0x2B/2C/2D/2E]).

[RX]

i) Continuous output mode (to host)

Set RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b01.

After RX_ON(SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)])=0x6), DCLK is output continuously. RX data (demodulated data) is output from DIO pin at falling edge of DCLK. RX data is not stored in RX_FIFO.

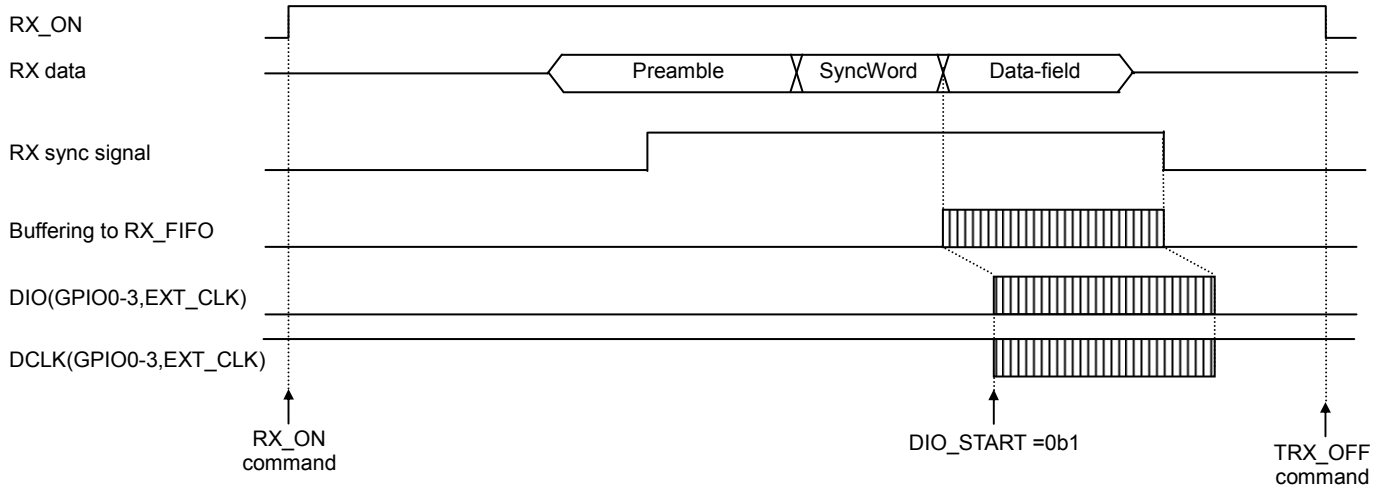


(Note) For details of timing, please refer to the “RX” in the “Timing Chart”.

ii) Data output mode 1 (to host)

Set RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) =0b10.

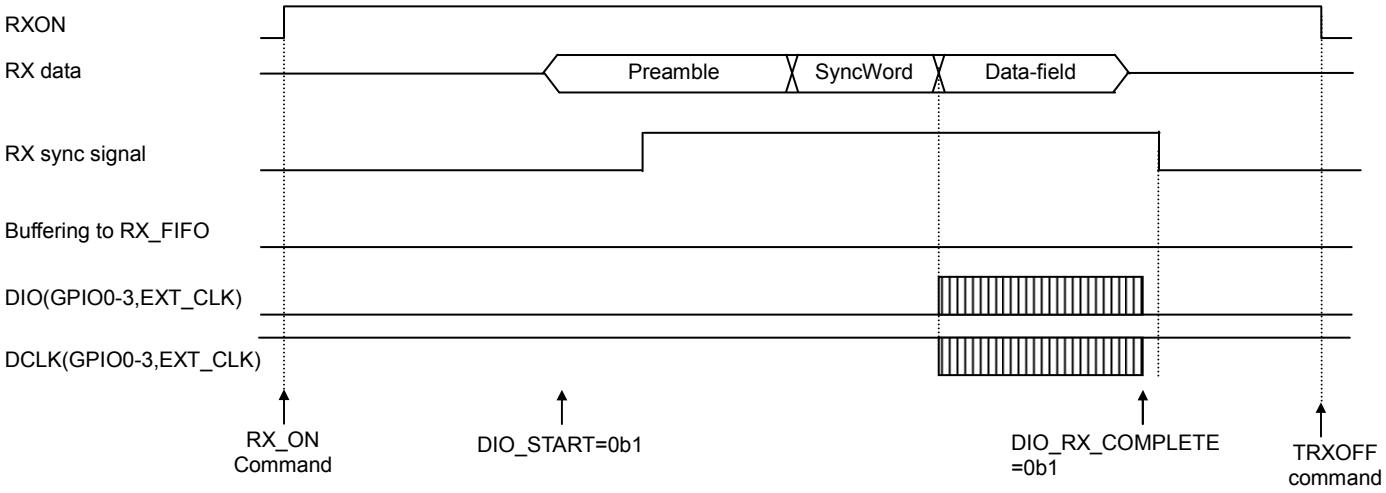
After SyncWord detection, RX data is buffered in RX_FIFO. RX data buffering will continue until RX sync signal (SYNC) becomes ”L”. By setting DIO_START ([DIO_SET: B0 0x0C(0)])=0b1, top data of buffered data will be output through DIO interface (DIO/DCLK). (RX data is output at falling edge of DCLK). However, if DIO_START setting is done after 64 byte timing, the top byte will be over written. If all buffered data is output until SYNC becomes ”L”, RX completion interrupt (INT[8] group 2) will be generated. After RX completion, ready to receive next packet.



(Note)

1. RX data buffering in RX_FIFO is accessed byte by byte. DIO_START should be issued after 1 byte access time upon SyncWord detection.
2. This mode does not process L-field. Field checking function is not supported.

If DIO_START is issued before SyncWord detection, data is not buffered in RX_FIFO and RX data after SyncWord detection will be output at falling edge of DCLK . In order to complete RX before SYNC becomes "L", DIO RX completion setting (DIO_RX_COMPLETE([DIO_SET: B0 0x0C(2)]=0b1) is necessary. After DIO_RX_COMPLETE setting, ready to receive the next packet.

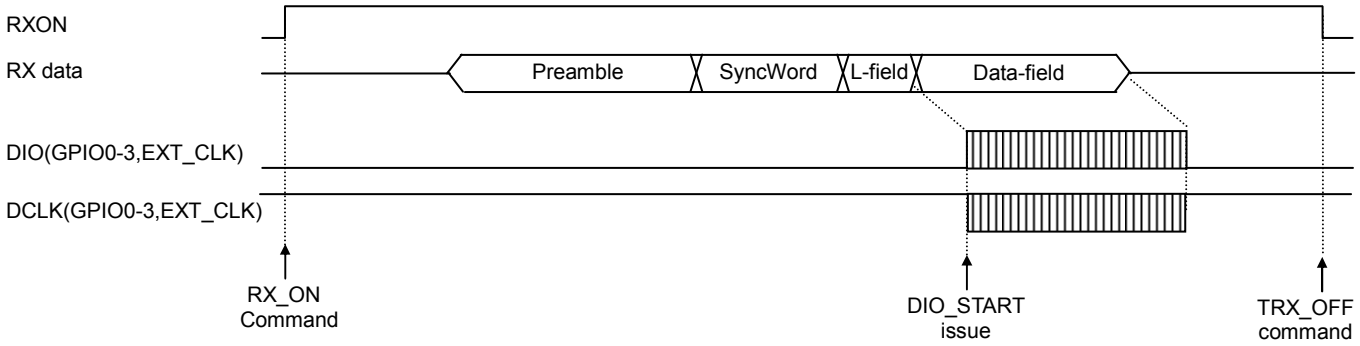


iii) Data output mode 2 (to host)

Set RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b11.

Only Data-field of RX data is buffered in RX_FIFO. RX data indicated by L-field is stored in RX_FIFO. By DIO_START([DIO_SET: B0 0x0C(0)])=0b1, top data of buffered data will be output through DIO interface (DIO/DCLK). (RX data is output at falling edge of DCLK).

However, if DIO_START setting is done after 64 byte timing, the top byte will be overwritten. If all data indicated by L-field is output, RX completion interrupt (INT[8] group2) will be generated. After RX completion, ready to receive next packet. Length information is stored in [RX_PKT_LEN_H/L: B0 0x7D/7E] registers. This mode support fileld check function.



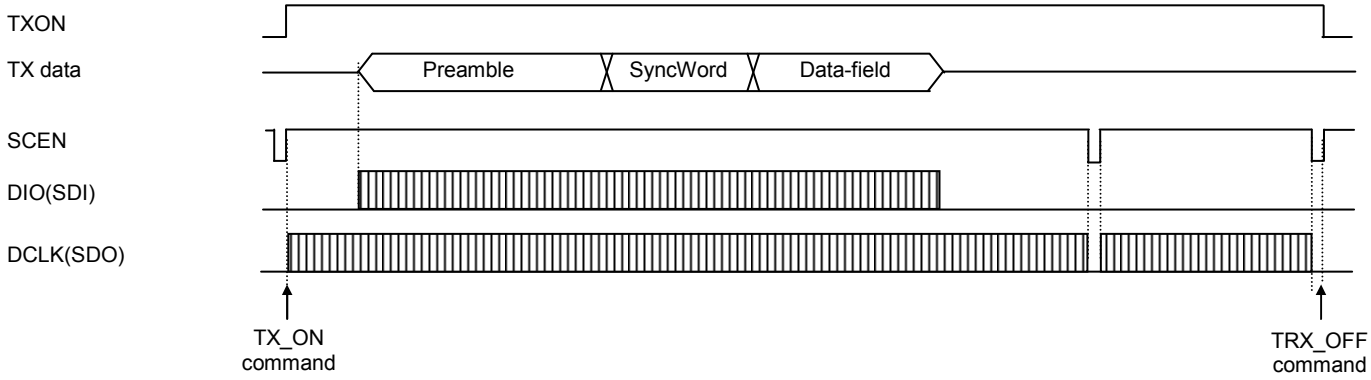
(Note)

RX data buffering in RX_FIFO is byte by byte access. DIO_START should be issued after elapsed time from SyncWord detection to L-field length + over 1byte access time.

(2) In case of using SDI/SDO pin (sharing with SPI interface)

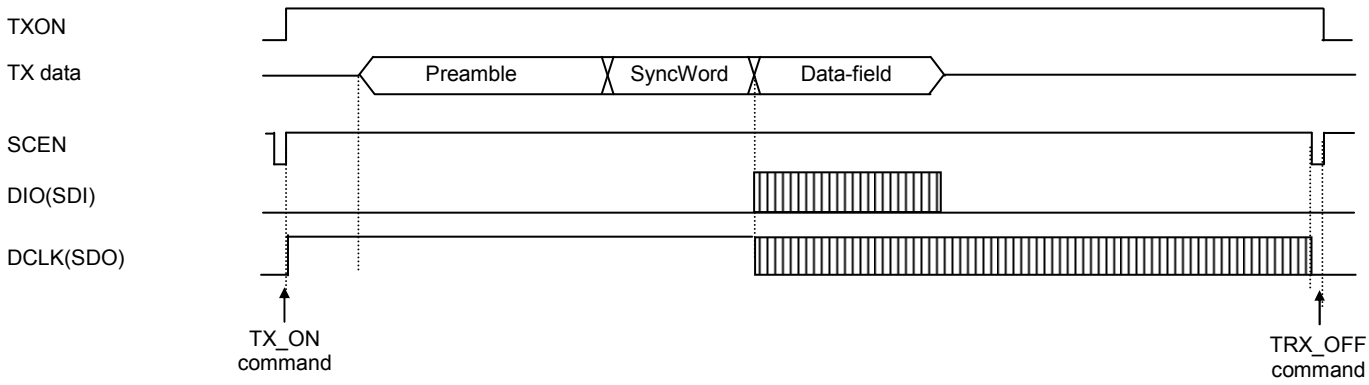
If SDI and SDO pins are used DCLK/DIO, DCLK/DIO is controlled as follow. (below DIO/DCLK vertical line part indicate output or input.) Both SDO_CFG and SDI_CFG ([SPI/EXT_PA_CTRL:B0 0x53 (5,4)]) should be set 0b1.

[TX]
i) Continuous input mode (from host)
Set TXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(5-4)])=0b01
After TX_ON(SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)])=0x9), during SCEN pin is "H", DCLK is output from SDO pin. TX data can be input from SDI pin at falling edge of DCLK. TX data must be encoded data. After TRX_OFF is issued (SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)])=0x8), input data from DIO pin are not valid. During DCLK output, if SCEN pin becomes "L", DCLK output will stop. (SPI access has priority)



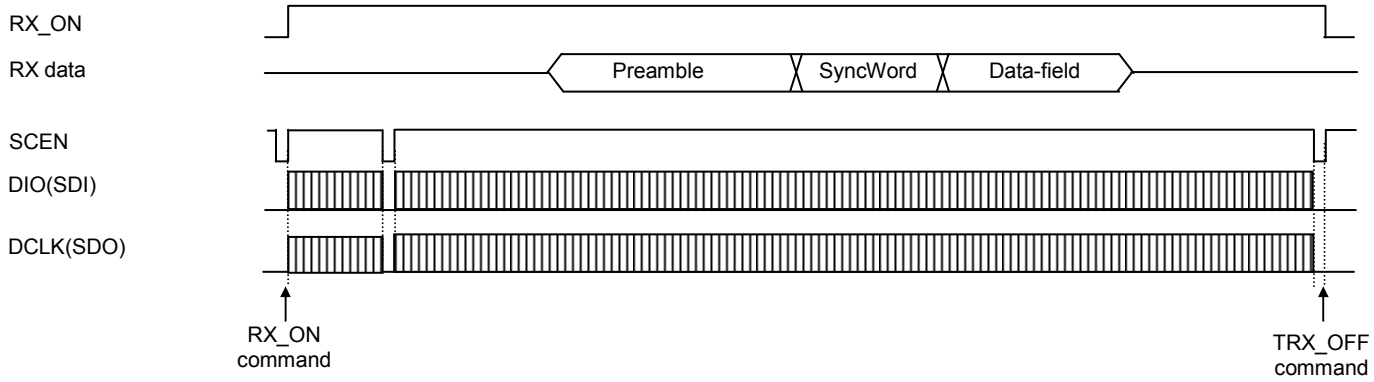
(Note)
Not to access SPI until TX completion. During packet transmission, if SPI access is attempted by the host, TX data error can be expected.

ii) Data input mode (from host)
Set TXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(5-4)])=0b10.
After TX_ON, when SCEN is "H", DCLK is output from SDO pin during data input period after SyncWord. At falling edge of DCLK, TX data should be input to SDI from the host. After TRX_OFF is issued (SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)])=0x8), TX data/clock input/output are invalid. During DCLK output period, if SCEN becomes "L", DCLK output will stop. (SPI access has a priority)



(Note)
Not to access SPI until TX completion. During packet transmission, if SPI access is attempted by the host, TX data error can be expected.

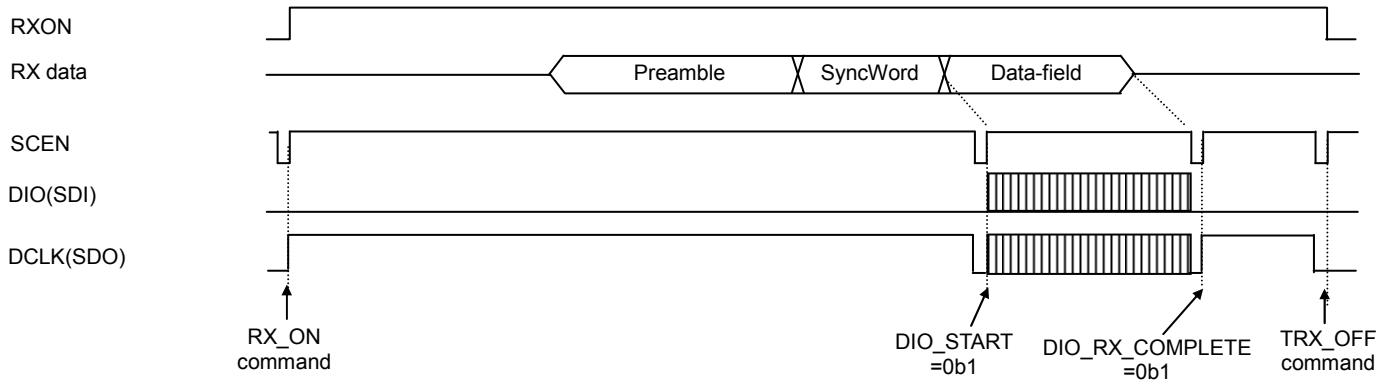
[RX]
i) Continuous output mode (to host)
Set RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b01.
After RX_ON (SET_TRX[3:0]([RF_STATUS: B0 0x0B(3-0)])=0x6) issued, during SCEN is ”H” period, DCLK is output from SDO pin, RX data is output from SDI pin at falling edge of DCLK. After TRX_OFF issuing(SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)])=0x8), DCLK/DIO output will stop. Even if DCLK/DIO are output, when SCEN becomes “L”, DCLK/DIO will stop. (SPI access has a higher priority)



(Note)
Not to access SPI until RX completion. During packet receiption, if SPI access is attemped by the host, RX data error can be expected. It is recommended

ii) Data ouput mode 1 or data output mode 2 (to host)
Set RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b10/11
After RX_ON, RX data upon SyncWord (output mode 1) or RX data upon L-fileld (output mode 2) is buffered in RX_FIFO. During SCEN is ”H”, by DIO_START([DIO_SET: B0 0x0C(0)])=0b1, top data of buffered data will be output through DIO interface (DIO/DCLK). (RX data is output at falling edge of DCLK). Other output condition is same as the case of using GPIO:/ECT_CLK pins. After TRX_OFF isuing, DCLK/DIO output will stop. Even during DCLK/DIO are output period, if SCEN becomes “L”, DCLK/DIO output will stop. (SPI access has a priority)

(In case of data output mode1)



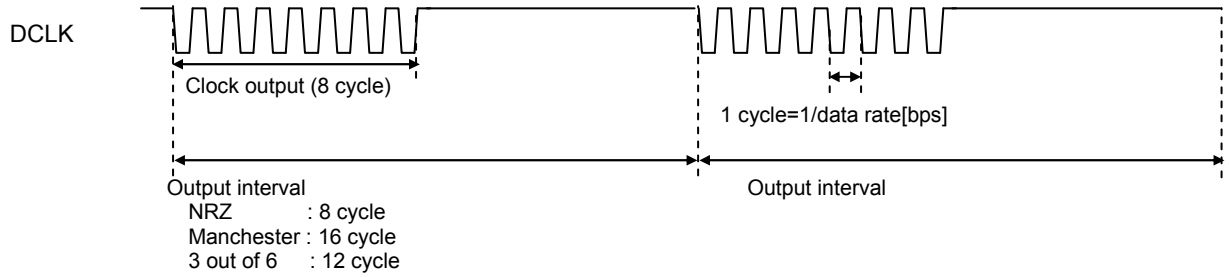
(Note)
Not to access SPI until RX completion. During packet receiption, if SPI access is attemped by the host, RX data error can be expected.

(3) DCLK output method

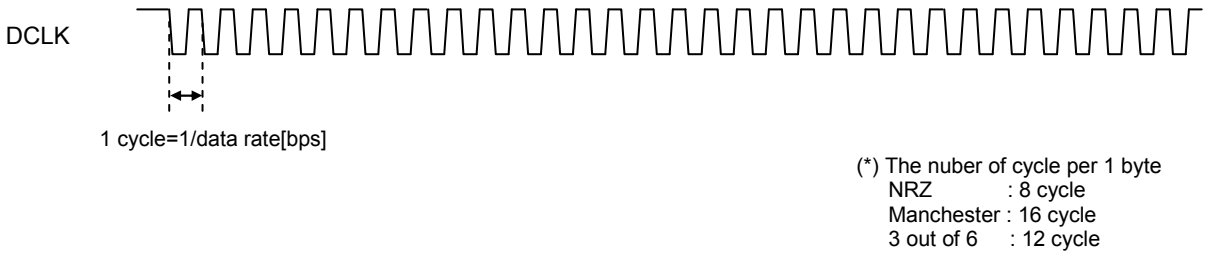
In Data output mode 2, decoded data is output. Therefore, The DCLK output section in a output interval changes with the coding method. DCLK output section is as follows.

In othe modes, undecoded data is input or output. DCLK is output continuously. Then, it is not depend on the coding method.

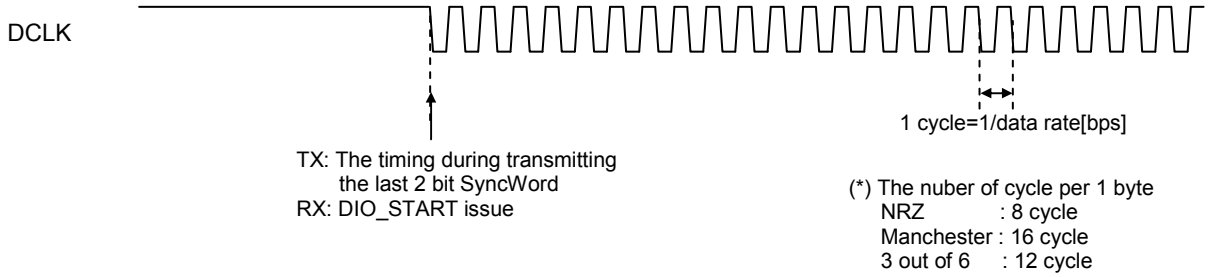
i) Data output mode 2



ii) TX continuous input mode or RX continuous mode



iii) TX Data input mode / RX Data output mode1



●Timer Function

○Wake-up timer

ML7406 has automatic wake-up function using wake-up timer. The following operations are possible by using wake-up timer.

- Upon timer completion, automatically wake-up from SLEEP state. After wake-up operation can be selected as RX_ON state or TX_ON state by WAKEUP_MODE ([SLEEP/WU_SET: B0 0x2D(6)]).
- By setting WUT_1SHOT_MODE ([SLEEP/WU_SET: B0 0x2D(7)]), continuous wake-up operation (interval operation) or one shot operation can be selected
- In interval operation, if RX_ON /TX_ON state is caused by wake-up timer, continuous operation timer is in operation..
- After moving to RX_ON state by wake-up timer, when continuous operation timer completed, move to SLEEP state automatically. However, if SyncWord is detected before timer completion, RX_ON state will be maintained. In this case, ML7406 does not go back to SLEEP state automatically. SLEEPsetting (SLEEP_EN[SLEEP/WU_SET: B0 0x2D(0)])=0b1) is necessary to go back to SLEEP state. However if RXDONE_ MODE[1:0]([RF_STATUS_CTRL:B0 0x0A(3-2)]) =0b11, after RX completion, move to SLEEP state automatically.
- After moving to TX_ON state by wake-up timer, when continuous operation timer completed, go back to SLEEPstate automatically.
- After wake-up by combining with high speed carrier checking mode, CCA is automatically performed, if IDLE is detected, able to move to SLEEP state immediately. For details, please refer to the “(3) high speede carrier detection mode”.
- By setting WU_CLK_SOURCE ([SLEEP/WU_SET:B0 0x2D(2)]), clock source for wake-up timer are selectable from EXT_CLK pin or on-chip RC OSC.

Wake-up intervalm, wake-up timer interval and continuous operation timer can be calculated in the following formula.

Wake-up interval [s] = Wake-up timer interval [s] + Continuous operation timer [s]

Wake-uptimer interval [s] = Wake-up timer clock cycle *
Division setting ([WUT_CLK_SET: B0 0x2E(3-0)]) *
Wake-up timer interval setting ([WUT_INTERVAL_H/L: B0 0x2F/0x30])

Continuous operation timer [s] = Wake-up timer clock cycle *
Division setting([WUT_CLK_SET: B0 0x2E(7-4)]) *
Continuous operation timer setting ([WU_DURATION: B0 0x31])

(Note)

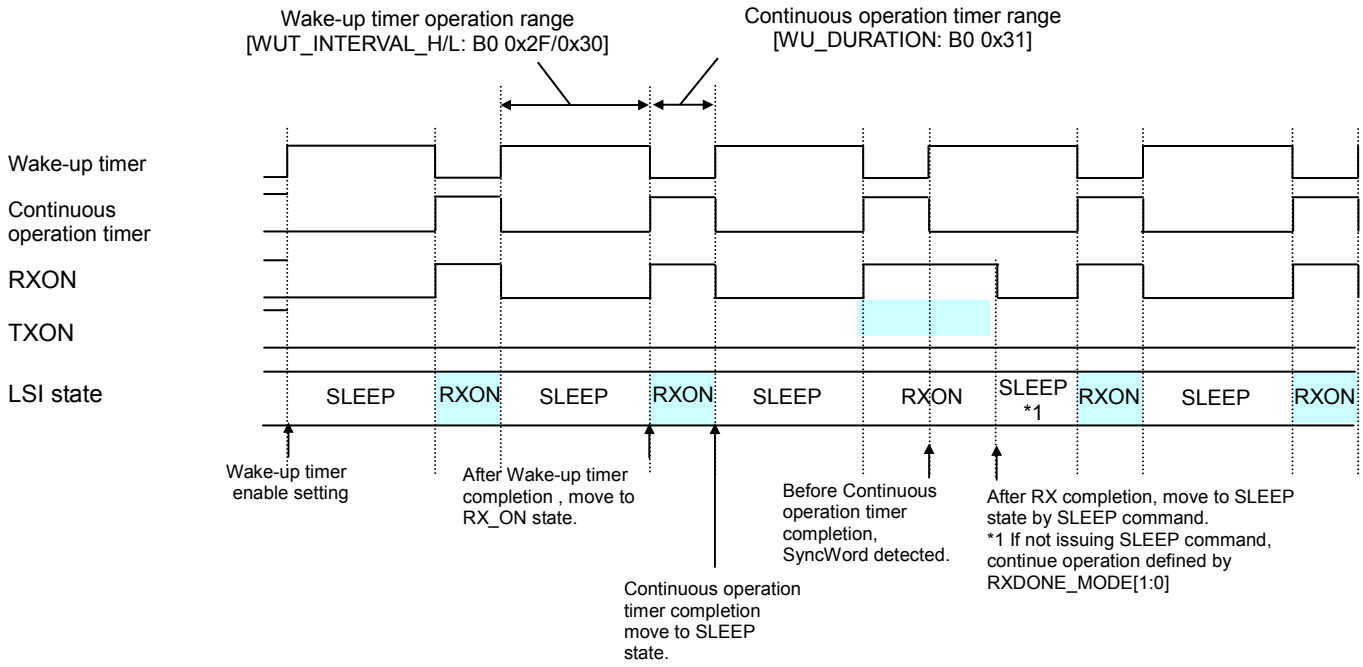
- In case of moving to TX_ON state after wake-up, move to SLEEP state when timer completed even in the middle of transmission. Continuous oeration timer should be set in such manner that timer completing after TX completion.
- WUDT_CLK_SET[3:0] ([WUT_CLK_SET: B0 0x2E(7-4)]) and WUT_CLK_SET[3:0] ([WUT_CLK_SET: B0 0x2E (3-0)]) can be set independently.
- Minimum value for wake-up timer interval setting ([WUT_INTERVAL_H/L: B0 0x2F/0x30]) is 0x02. And minimum value for continuous operation timer setting ([WU_DURATION: B0 0x31]) is 0x01.
- Be noted that the SyncWord detection is not issued when in DIO mode with RXDIO_CTRL([DIO_SET: B0 0x0C(7-6)])=0b01. Therefore, when continuous operation timer completed, forcibly move to SLEEP state.

(1) Interval operation

[RX]

After wake-up, RX_ON state. If continuous operation timer completed before SyncWord detection, automatically return to SLEEP state. If SyncWord detected, continue RX_ON. After RX completion, continue operation defined by RXDONE_ MODE[1:0] ([RF_STATUS_ CTRL: B0 0x0A(3-2)]) .

[SLEEP/WU_SET: B0 0x2D(6-4)]=0b011

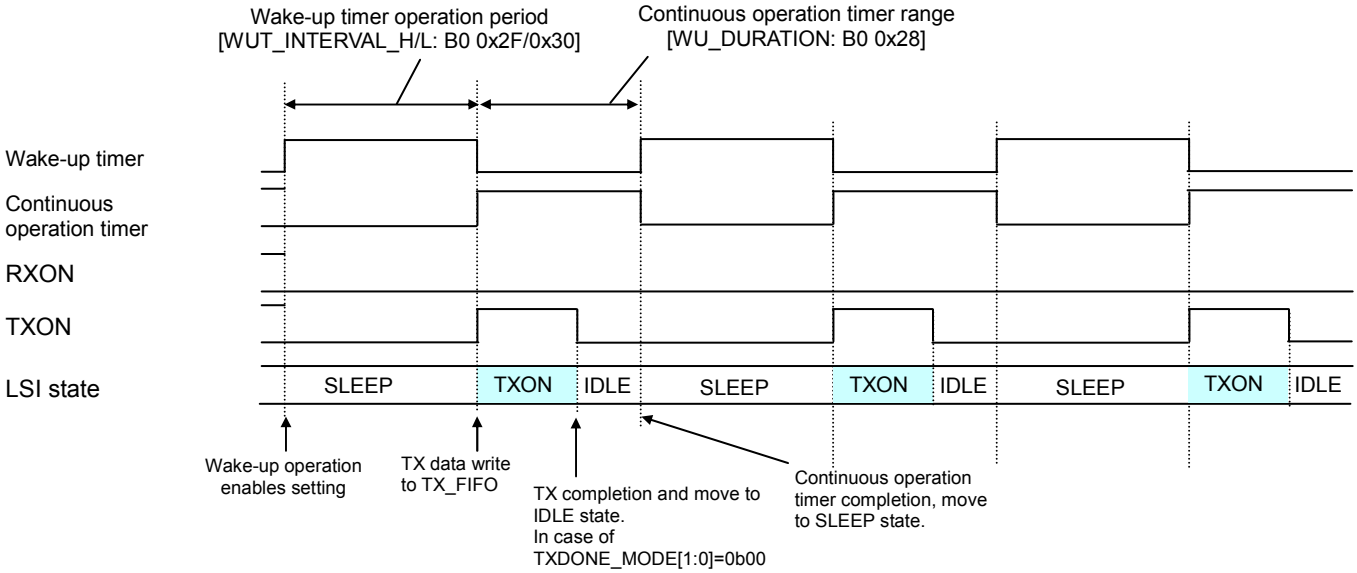


[TX]

After wake-up, TX_ON state. After TX completion, continue operation defined by TXDONE_MODE[1:0] ([RF_STATUS_ CTRL: B0 0x0A(1-0)]) .

If continuous operation timer completed, automatically return to SLEEP state. So continuous operation timer has to be set so that timer completion occur after TX completion.

[SLEEP/WU_SET: B0 0x2D(6-4)]=0b111

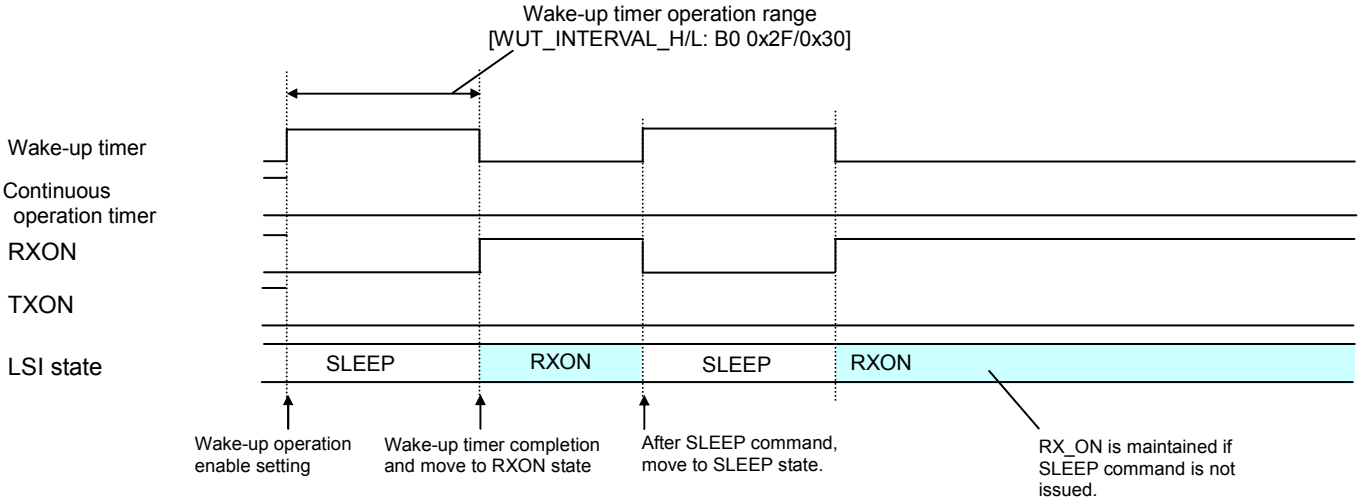


(2) 1 shot operation

[RX]

After wake-up timer completion, move to RX_ON state. And continue RX_ON state. Move to SLEEP state by SLEEP command. If wake-up timer interval ([WUT_INTERVAL_H/L: B0 0x2F/0x30]) is maintained, after re-issuing SLEEP command, 1 shot operation will be activated again. If RX completed during RX_ON, continue operation defined by RXDONE_ MODE[1:0] ([RF_STATUS_ CTRL: B0 0x0A(3-2)]) . Same manner in TX_ON state.

[SLEEP/WU_SET: B0 0x2D(7-4)]=0b1011

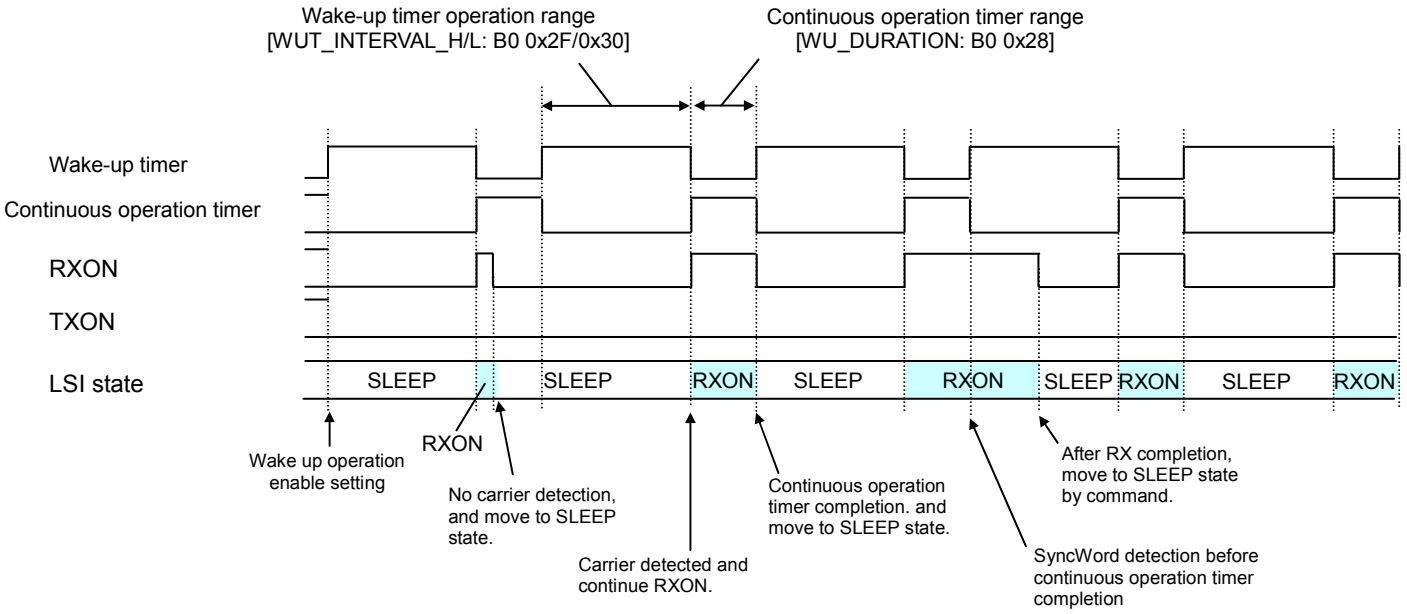


(3) Combination with high speed carrier detection

[Interval operation]

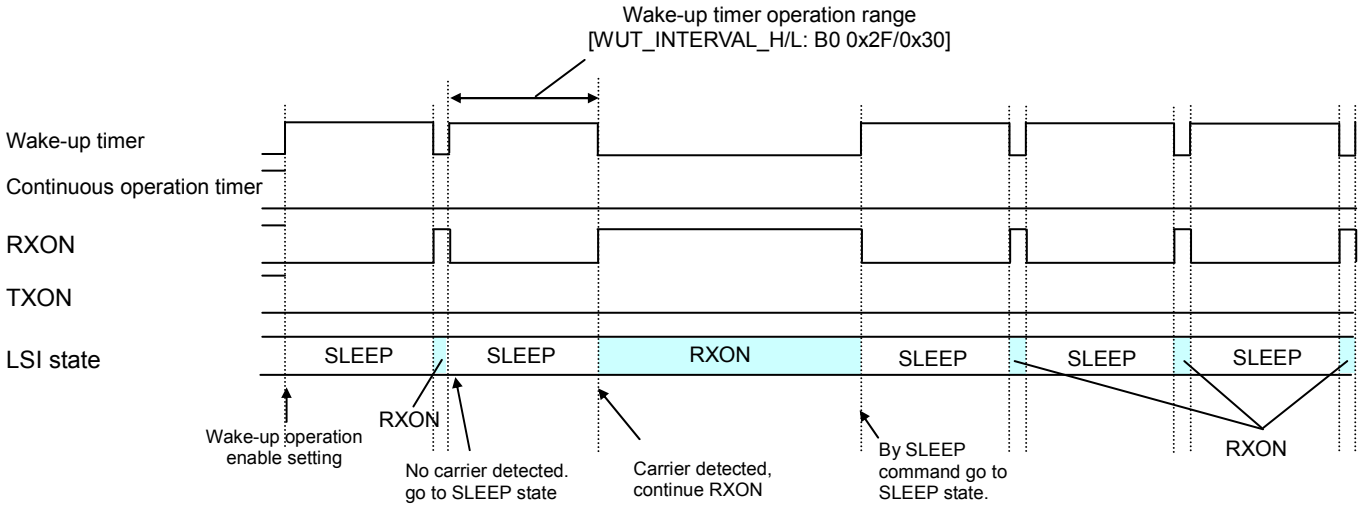
After wake-up timer completion, move to RX_ON state. Then perform CCA. If no carrier detected, automatically move to SLEEP state. If carrier detected, maintaining RX_ON state and perform SuncWord detection. If continuous operation timer completed before SyncWord detection, automatically move to SLEEP state. And If SyncWord detected, continue RX_ON state state.

[SLEEP/WU_SET: B0 0x2D(7-4)]=0b0011
FAST_DET_MODE_EN([CCA_CTRL: B0 0x39(3)])=0b1



[1 shot operation]
After wake-up timer completion, move to RX_ON state. And perform CCA to check carrier. If no carrier detected, go back to SLEEP state automatically. After wake-up timer completion, wake-up to check the carrier again. If carrier is detected, continue RX state. Able to go back to SLEEP by setting SLEEP parameters.

[SLEEP/WU_SET: B0 0x2D(7-4)]=0b1011
FAST_DET_MODE_EN([CCA_CTRL: B0 0x39(3)])=0b1



○General purpose timer

ML7406 has general purpose timer. 2 channel of timer are able to function independently. Clock sources, timer setting can be programmed independently. When timer is completed, General purpose timer 1 interrupt (INT[22] group3) or General purpose timer 2 interrupt (INT[23] group3) will be generated.

General timer interval can be programmed as the following formula.

General purpose timer interval[s] = general purpose timer clock cycle *
Division setting ([GT_CLK_SET: B0 0x33]) *
General purpose timer interval setting ([GT1_TIMER: B0 0x34] or [GT2_TIMER: B0 0x35])

By setting GT2/1_CLK_SOURCE ([GT_SET: B0 0x32(5,1)]), clock sources for general purpose timer can be selectable from wake-up timer clock or 2MHz.

●Frequency Setting Function

○Channel frequency setting

Maximum 256 channels can be selected (CH#0 -CH#255) by the following resisters.

Frequency		Register
CH#0 frequency	TX	[TXFREQ_I: B1 0x1B], [TXFREQ_FH: B1 0x1C], [TXFREQ_FM: B1 0x1D] and [TXFREQ_FL: B1 0x1E]
	RX	[RXFREQ_I: B1 0x1F], [RXFREQ_FH: B1 0x20], [RXFREQ_FM: B1 0x21] and [RXFREQ_FL: B1 0x22]
Channel space	-	[CH_SPACE_H: B1 0x23] and [CH_SPACE_L: B1 0x24]
Channel setting	-	[CH_SET: B0 0x09]

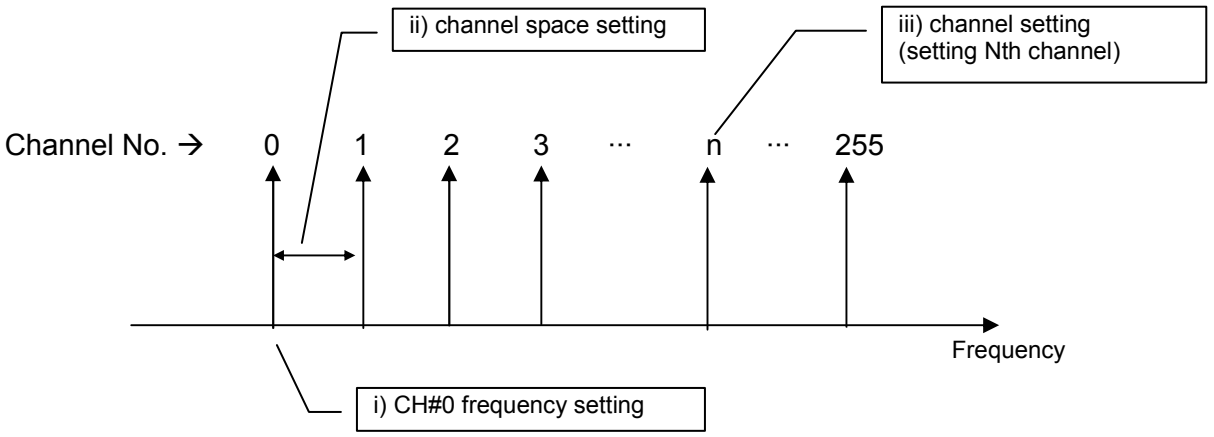
(1) Channel frequency setting overview

[Channel frequency setting]

Using above registers, channel frequency is defined as following formula.

Channel frequency = i) CH#0 frequency + ii) channel space * iii) channel setting

[Channel frequency allocation image]

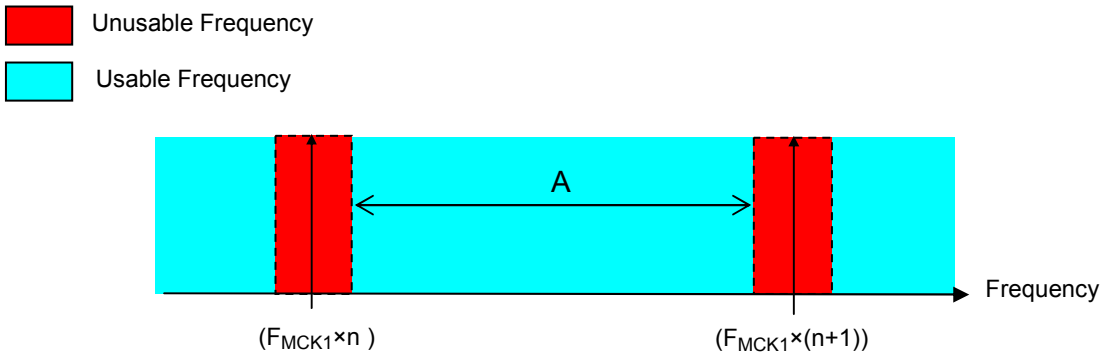


(Note)

The channel frequency to be selected must meet the following conditions. If the following conditions cannot be met, please change channel #0 frequency or use other channels. If this formula cannot be met, expected frequency is not functional or PLL may not be locked.

TX: (F_{MCK1}*n + 500kHz) ≤ channel frequency ≤ (F_{MCK1}*(n+1) – 500kHz)
RX: (F_{MCK1}*n +2.2MHz) ≤ channel frequency ≤ (F_{MCK1}*(n+1))

F_{MCK1}: Master clock frequency
n = integer



[Calculation example of above “A” range]
Condition: Master clock 26MHz, n=33

TX:(26*33+0.5)MHz ≤ channel frequency to be used ≤ (26*(33+1)-0.5)
→ 858.5MHz ≤ channel frequency to be used ≤883.5MHz

RX:(26*33+2.2)MHz ≤ channel frequency to be used ≤ (26*(33+1)-2.2)
→ 860.2MHz ≤ channel frequency to be used ≤881.8MHz

(Note)
“CH#0 frequency (Hz)” and “channle space (Hz)” may have error (Hz). Then the “channel frequency error (Hz)” is defined as following formula.

Channel frequency error (Hz) = CH#0 frequency error (Hz) + channel space error (Hz)* channel setting

When changing “channel frequency” by setting “channel setting” without “CH#0 frequency” change, the “channel frequency error” will become larger than by setting both “CH#0 frequency” and “channel setting”. If the “channle frequency error” is larger than expection, please consider to change “CH#0 frequency”.

(2) Channel #0 frequency setting

TX frequency can be set by [TXFREQ_I: B1 0x1B], [TXFREQ_FH: B1 0x1C], [TXFREQ_FM: B1 0x1D] and [TXFREQ_FL: B1 0x1E]. RX frequency can be set by [RXFREQ_I: B1 0x1F], [RXFREQ_FH: B1 0x20], [RXFREQ_FM: B1 0x21] and [RXFREQ_FL: B1 0x22].

Channel #0 frequency setting value can be caluculated using the following formula.

$$I = \frac{f_{rf}}{f_{ref}} \quad \text{(Integer part)}$$

$$F = \left\{ \frac{f_{rf}}{f_{ref}} - I \right\} \cdot 2^{20} \quad \text{(Integer part)}$$

Here

f_{rf} :channel #0 frequency

f_{ref} :PLL reference frequency (=master clock frequency: F_{MCK1})

I :Integer part of frequency setting

F :Fractional part of frequency setting

I (Hex) is set to [TXFREQ_I: B1 0x1B], [RXFREQ_I: B1 0x1F] registers.

F (Hex.) is set to the following registers.

For TX, from MSB, set in order of [TXFREQ_FH: B1 0x1C], [TXFREQ_FM: B1 0x1D], [TXFREQ_FL: B1 0x1E] registers.

For RX, from MSB, set in order of [RXFREQ_FH: B1 0x20], [RXFREQ_FM: B1 0x21], [RXFREQ_FL: B1 0x22] registers.

Frequency error (f_{err}) is calculated as follows :

$$f_{err} = \left\{ I + \frac{F}{2^{20}} \right\} \cdot f_{ref} - f_{rf}$$

[Example]

When set TX channel #0 frequency to 868MHz (master clock 26MHz), the calculations are as follows.

$$I = \frac{868MHz}{26MHz} \text{(Integer part)} = 33(0x21)$$

$$F = \left\{ \frac{868MHz}{26MHz} - I \right\} \cdot 2^{20} \text{ (Integer part)} = 403298(0x062762)$$

[TXFREQ_I: B1 0x1B] = 0x21
[TXFREQ _FH: B1 0x1C] = 0x06
[TXFREQ _FM: B1 0x1D] = 0x27
[TXFREQ _FL: B1 0x1E] = 0x62

Frequency error f_{err} is as follows:

$$f_{err} = \left\{ 33 + \frac{403298}{2^{20}} \right\} \cdot 26MHz - 868MHz = -11.45Hz$$

(3) Channel space setting

Channel space can be set by [CH_SPACE_H: B1 0x23], [CH_SPACE_L: B1 0x24] registers. Hexadecimal values calculated in the following formula should be set to [CH_SPACE_H: B1 0x23], [CH_SPACE_L: B1 0x24] registers. (MSB->LSB order)
Channel space is from the center frequency of given channel to adjacent channel center frequency.

Channel space setting value can be calculated using the following formula:

$$CH\_SPACE = \left\{ \frac{f_{sp}}{f_{ref}} \right\} \cdot 2^{20} \quad \text{(Integer part)}$$

Here

CH_SPACE : Channel space setting

f_{sp} : Channel space [MHz]

f_{ref} : PLL reference frequency (=master clock frequency : F_{MCK1})

[Example]
When set channle space to 60kHz (master clock 26MHz), the calculation is as follows.

$$CH\_SPACE = \left\{ \frac{0.06MHz}{26MHz} \right\} \cdot 2^{20} \quad \text{(Integer part)} \quad = 2419 \text{ (0x0973)}$$

[CH_SPACE_H: B1 0x23] = 0x09
[CH_SPACE_L: B1 0x24] = 0x73

○IF frequency setting

In order to support various data rate , RX filters have to be optimised. The RX filter can be selected according to the IF frequency. IF frequency is set by [IF_FREQ_H: B0 0x54],[IF_FREQ_L: B0 0x55] registers. IF frequency corresponds to each data rate must be selected as below.

	Data rate			
	4.8kbps	32.768kbps	50kbps	100kbps
IF frequency	500kHz	500kHz	500kHz	720kHz

For other data rate, please refer to "Initialization table".

If CCA is used to detect channel carrier power, required RX filter bandwidth may be different. [IF _FREQ_CCA_H: B1 0x56] and [IF_FREQ_CCA_L: B1 0x57] registers must be used for CCA purpose. IF frequency must be set according to the IF frequency.

IF frequency setting value can be calculated using the following formula:

$$IF\_FREQ = \left\{ \frac{(f_{IF} / 2)}{f_{ref}} \right\} \cdot 2^{20} \quad \text{(Integer part)}$$

Here

IF_FREQ : IF frequency setting

f_{IF} : IF frequency [MHz]

f_{ref} : PLL reference frequency (=master clock frequency: F_{MCK1})

[Example]

When set IF frequency to 720kHz (master ckock 26MHz), the calculation is as follows.

IF_FREQ= {(0.72MHz ÷ 2) ÷ 26MHz} $\times 2^{20}$ (Integer part) = 14518 (0x38B6)

[IF_FREQ_H: B0 0x54] = 0x38
[IF_FREQ_L: B0 0x55] = 0xB6

○BPF frequency band setting

For normal operation (including AFC) and CCA operation, optimized BPF setting to [BPF_CO: B0 0x5C] and [BPF_CO_CCA: B0 0x5D] registers are necessary. As indicated below table, proper value correspond to each data rate, must be programmed.

Data rate [kbps]	[DRATE_SET: B0 0x06]	Normal case [BPF_CO: B0 0x5C]		CCA [BPF_CO_CCA: B0 0x5D]	
		coefficient	Setting value	coefficient	Setting value
4.8	0b0010	1.44	0xB8	1.44	0xB8
32.768	0b1000	1.44	0xB8	1.44	0xB8
50	0b1010	1.44	0xB8	1.44	0xB8
100	0b1011	1	0x80	1	0x80

○Modulation setting

ML7406 supports GFSK modulation and FSK modulation.

(1) GFSK modulation setting

By setting GFSK_EN([DATA_SET1: B0 0x07(4)])=0b1, GFSK mode can be selected. In GFSK modulation, frequency deviation can be set by [GFSK_DEV_H: B1 0x30] and [GFSK_DEV_L: B1 0x31] registers and Gasusiaan filter can be set by [FSK_DEV0_H/GFIL0: B1 0x32] - [FSK_DEV3_H/GFIL6: B1 0x38] registers.

i) GFSK frequency deviation setting

F_DEV value can be calculated as the following formula:

$$F\_DEV = \left\{ \frac{f_{dev}}{f_{ref}} \right\} \cdot 2^{20} \quad \text{(Integer part)}$$

Here

F_DEV : Frequency deviation setting

f_{dev} : Frequency deviation [MHz]

f_{ref} : PLL reference frequency (= master clock frequency: F_{MCK1})

[Example]

When set frequency deviation to 50kH (master clock 26MHz), the calculation is as follows.

F_DEV = {0.05MHz ÷ 26MHz} $\times 2^{20}$ (Integer value) = 2016 (0x07E0)

[GFSK_DEV_H: B1 0x30] = 0x07
[GFSK_DEV_L: B1 0x31] = 0xE0

ii) Gaussian filter setting

BT value of Gaussian filter and setting value to related registers are shown in the below table.

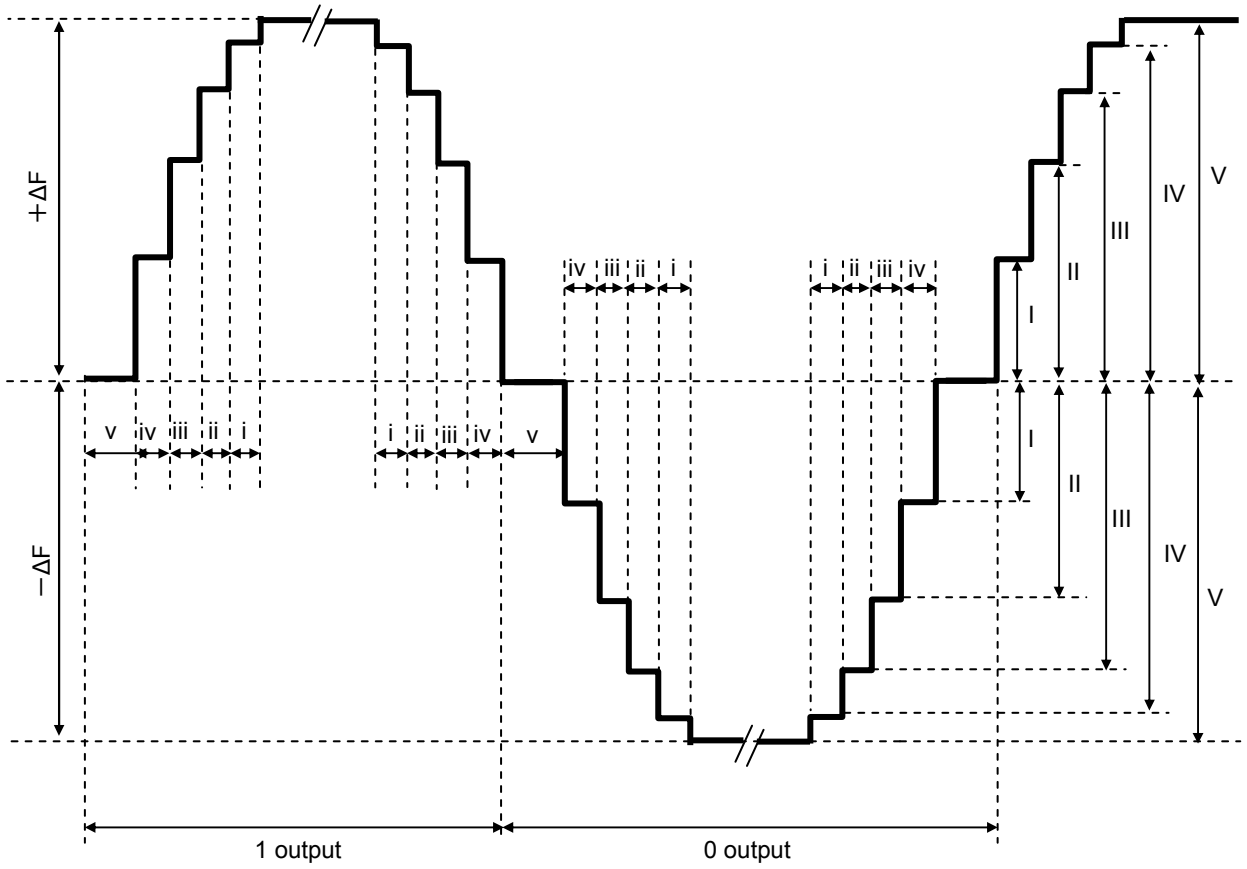
Register	BT value	
	0.5	1.0
[FSK_DEV0_H/GFIL0: B1 0x32]	0x49	0x00
[FSK_DEV0_L/GFIL1: B1 0x33]	0xA7	0x10
[FSK_DEV1_H/GFIL2: B1 0x34]	0x0F	0x04
[FSK_DEV1_L/GFIL3: B1 0x35]	0x14	0x0D
[FSK_DEV2_H/GFIL4: B1 0x36]	0x19	0x1E
[FSK_DEV2_L/GFIL5: B1 0x37]	0x1D	0x32
[FSK_DEV3_H/GFIL6: B1 0x38]	0x1E	0x3C

(Note)

GFSK filter coefficient setting register and FSK frequency deviation setting register are common. In GFSK mode, filter coefficient applies to this register. In FSK mode, frequency deviation applies to this register.

(2) FSK modulation setting

By setting GFSK_EN([DATA_SET1: B0 0x07(4)])=0b0, FSK mode can be selected. Fine frequency deviation can be set by [FSK_DEV0_H/GFIL0: B1 0x32] to [FSK_DEV4_L: B1 0x3B] registers. By adjusting [FSK_TIM_ADJ4-0: B1 0x3C-40] registers, FSK timing can be fine tuned.



TX_FSK_POL ([DATA_SET1:B0 0x07(6)]) = 0b0 setting

Frequency deviation setting				Timing setting			
symbol	Register name	address	function	symbol	Register name	address	function
I	FSK_FDEV0_H/GFIL0 FSK_FDEV0_L/GFIL1	B1 0x32/33	Frequency deviation Resolution: Approx.25Hz	i	FSK_TIM_ADJ4	B1 0x3C	Modulation timing 4.3MHz/13MHz counter value (*1)
II	FSK_FDEV1_H/GFIL2 FSK_FDEV1_L/GFIL3	B1 0x34/35		ii	FSK_TIM_ADJ3	B1 0x3D	
III	FSK_FDEV2_H/GFIL4 FSK_FDEV2_L/GFIL5	B1 0x36/37		iii	FSK_TIM_ADJ2	B1 0x3E	
IV	FSK_FDEV3_H/GFIL6 FSK_FDEV3_L	B1 0x38/39		iv	FSK_TIM_ADJ1	B1 0x3F	
V	FSK_FDEV4_H FSK_FDEV4_L	B1 0x3A/3B		v	FSK_TIM_ADJ0	B1 0x40	

(*1) Modulation timing resolution can be changed by FSK_CLK_SET ([FSK_CTRL: B1 0x2F(0)]).

(Note)
GFSK filter coefficient setting register and FSK frequency deviation setting register are common. In GFSK mode, filter coefficient applies to this register. In FSK mode, frequency deviation applies to this register.

●RX related function

○AFC function

ML7406 supports AFC function. Frequency deviation (max±85ppm) between remote device and local device can be compensated by this function. Using this function, stable RX sensitivity and interference blocking performance can be achieved. This function can be enabled by setting AFC_EN([AFC/GC_CTRL: B1 0x15(7)])=0b1.

○Energy detection value (ED value) acquisition function

ML7406 supports calculate Energy detection value (ED value) based on Receive signal strength indicator (RSSI).
ED value acquisition can be enabled by setting ED_CALC_EN ([ED_CTRL: B0 0x41(7)])=0b1 and as soon as trnasition to RX_ON state, automatically start acquiring ED value. During RX_ON state, ED value constantly updated.

ED value is not RSSI value at given timing, but average values. Number of average times can be specified by ED_AVG[2:0] ([ED_CTRL: B0 0x41(2-0)]). During diversity operation, DIV_ED_AVG[2:0] ([2DIV_MODE: B1 0x48(2-0)]) is used for setting. After acquiring specified average ED value, ED_DONE([ED_CTRL: B0 0x41(4)]) becomes ”0b1” and ED_VALUE[7:0] ([ED_RSLT: B0 0x3A]) is updated.

ED_DONE bit will be cleared if one of the following conditions are met.

1. Gain is switched.
2. Once stopping ED value acquisition and then resume it.
3. Antenna is switched. (when diversity is enabled)

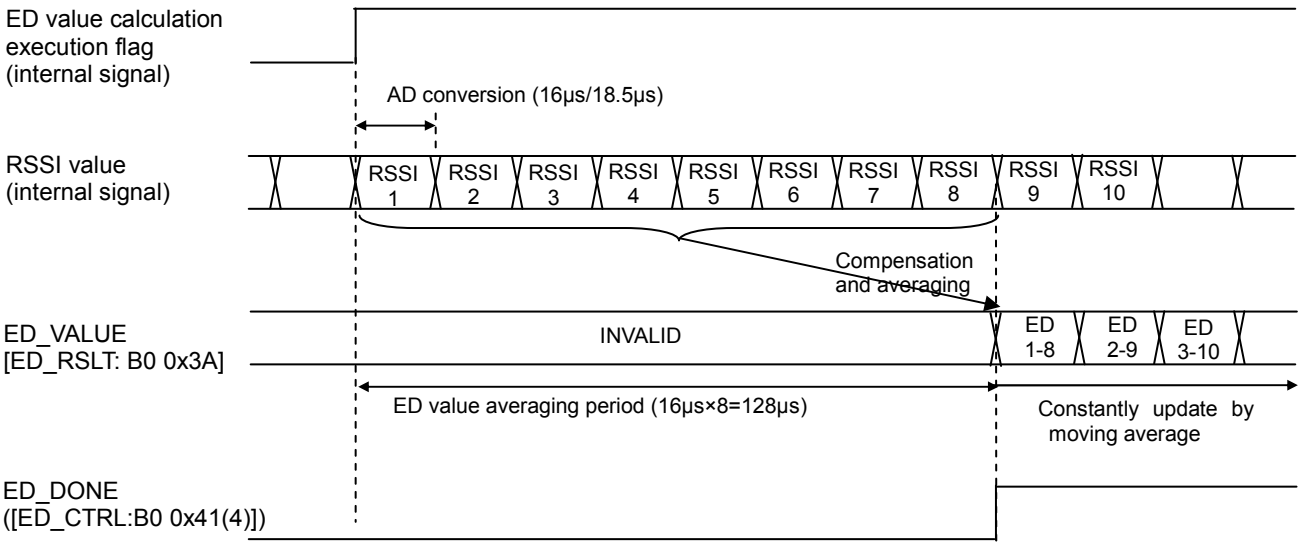
Timing from ED value starting point to ED value acquisition is calculated as below formula.

ED value average time = AD conversion time (16µs/17.8µs) * Number of average times.

(Note) AD conversion time can be set by ADC_CLK_SET([ADC_CLK_SET: B1 0x08(4)]). Reset value is 2MHz and AD conversion timer is 16µs.

The timing example is as follows:

[condition]
Set ADC_CLK_SEL([ADC_CLK_SEL: B1 0x08(4)])=0b1 (2MHz)
Set ED_AVG[2:0] ([ED_CTRL: B0 0x41(2-0)])=0b011 (8 times averaging)

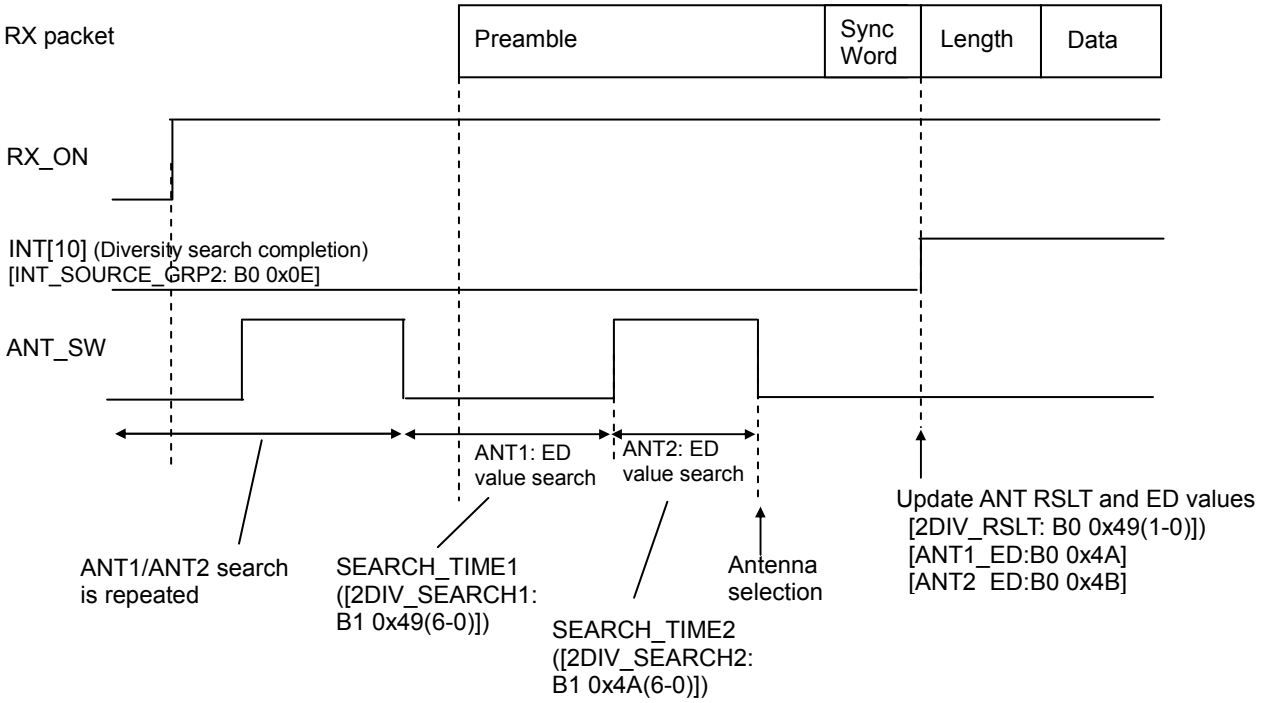


○Diversity function

ML7406 supports two antenna diversity function.

While setting 2DIV_EN([2DIV_CTRL: B0 0x48(0)])=0b1, as soon as RX_ON is set, diversity mode will start. When diversity mode is started, and upon RX data detection, each ED value will be acquired by switching two antennas. And then antenna with higher ED value will be selected automatically. As diversity uses preamble data for ED value acquisition, longer preamble length is desirable. If preamble is too short, accurate ED values may not be obtained.

The timing example is as below.



ED values acquired by the diversity operation are stored in [ANT1_ED: B0 0x4A] and [ANT2_ED: B0 0x4B] registers and antenna diversity result is indicated at 2DIV_RSLT[2:0] ([2DIV_RSLT: B0 0x49(1-0)]) when SyncWord is detected.

In diversity operation, the number of ED average times is specified by 2DIV_ED_AVG[2:0]([2DIV_MODE: B1 0x48(2:0)]). Search time for each antenna is defined by [2DIV_SEARCH1:B1 0x49] and [2DIV_SEARCH2:B1 0x4A] registers. And its time resolution can be defined by SEARCH_TIME_SET([2DIV_SEARCH1: B1 0x49(7)]).

If diversity search completion interrupt (INT[10] group2) is cleared, ED values and antenna diversity result are cleared.

(Note)

When an incorrect diversity completion caused by errornous detection due to thermal noize, ML7406 resume antenna diversity automatically. But when receiving a desired signal during the process of errounous detection, ED value obtained by [ANT1_ED:B0 0x4A] or [ANT2_ED:B0 0x4B] may indicate a low value different from the actual input level.

If this event occures, the actual ED value of desired signal can be achibed by reading [ED_RSLT:B0 0x3A] registers after SyncWord detection interrupt (INT[13] group2) generation.

(1) Antenna switching function

By using [2DIV_CTRL: B0 0x48], [ANT_CTRL: B0 0x4C], [SPI/EXT_PA_CTRL: B0 0x53] registers, TX-RX signal selection (TRX_SW), antenna switching signal (ANT_SW), external PA control signal(DCNT) can be controlled.

ML7406 can support both SPDT and DPDT antena swith control. ANT_SW signal and TRX_SW signal output considion for each antenna switch are explained below.

DPDT switch

Set 2PORT_SW([2DIV_CTRL: B0 0x48(1)])=0b1, ANT_CTRL1([2DIV_CTRL: B0 0x48(5)])=0b0. ANT_SW, TRX_SW output condition of each Idle, TX, RX state are as follow. (default setting) If INV_TRX_SW([2DIV_CTRL: B0 0x48(2)])=0b1, polarity of ANT_SW and TRX_SW are reversed.

TX/RX state	INV_TRX_SW=0b0 (default setting)		INV_TRX_SW=0b1 (reversed polarity)		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	H	L	L	H	Idle state
TX	L	H	H	L	TX state
RX	H	L	L	H	When Diversity disable or initial condition when diversity enable is set ([2DIV_CTRL: B0 0x48(0)]=0b1).
	L/H	H/L	H/L	L/H	If diversity enable is set, during searching, (ANT_SW=H, TRX_SW=L) and (ANT_SW=L, TRX_SW=H) are switched alternatively. After diversity completion, fix to one of the condition.

SPDT switch

Set 2PORT_SW([2DIV_CTRL: B0 0x48(1)])=0b0, ANT_CTRL1([2DIV_CTRL: B0 0x48(5)])=0b0. ANT_SW, TRX_SW output condition of each Idle, TX, RX state are as follow. (default setting) If INV_TRX_SW([2DIV_CTRL: B0 0x48(2)])=0b1, polarity of ANT_SW and TRX_SW are reversed.

TX/RX condition	INV_TRX_SW([2DIV_CTRL: B0 0x48(2)])=0 (default setting)		INV_TRX_SW([2DIV_CTRL: B0 0x48(2)])=1 (polarity reverse)		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	L	L	L	H	Idel state
TX	L	H	L	L	TX state
RX	L	L	L	H	When diversity disable or initial condition when diversity enable is set ([2DIV_CTRL: B0 0x48(0)]=0b1).
	H/L	L	H/L	H	If diversity enable is set,during searching (ANT_SW=H and (ANT_SW=L) is switched alternatively. After diversity completion , fix to one of the condition.

In the above setting, If INV_ANT_SW([2DIV_CTRL: B0 0x48(3)])=0b1, ANT_CTRL1([2DIV_CTRL: B0 0x48(5)])=0b1 are set, polarity of ANT_SW pin is reversed.

TX/RX state	INV_ANT_SW([2DIV_CTRL: B0 0x48(3)])=0 ANT_CTRL1([2DIV_CTRL: B0 0x48(5)])=any (default setting)		INV_ANT_SW([2DIV_CTRL: B0 0x48(3)])=1 ANT_CTRL1([2DIV_CTRL: B0 0x48(5)])=1		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	L	L	H	L	Idle state
TX	L	H	H	H	TX state
RX	L	L	H	L	When diversity disable or intial codition when diversity enable is set ([2DIV_CTRL: B0 0x48(0)]=0b1).
	H/L	L	L/H	L	If diversity enable is set, during searching (ANT_SW=H) and (ANT_SW=L) is switched alternatively. After diversity completion, fix to one of the condition.

(2) Antenna switch forced setting

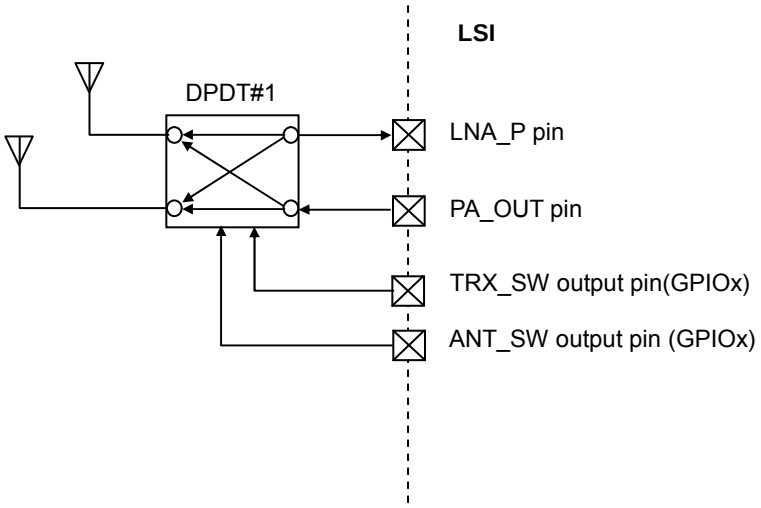
By [ANT_CTRL: B0 0x4C] register, ANT_SW pin output conditions can be set to fix.

TX: By TX_ANT_EN([ANT_CTRL: B0 0x4C(0)])=0b1, TX_ANT([ANT_CTRL: B0 0x4C(1)]) condition will be output.
RX: By RX_ANT_EN([ANT_CTRL: B0 0x4C(4)])=0b1, RX_ANT([ANT_CTRL: B0 0x4C(5)]) condition will be output.

However, output is defined by [GPIIO*_CTRL: B0 0x4E - 0x51] register , [GPIIO*_CTRL:B0 0x4E - 0x51] registers setting has higer priority.

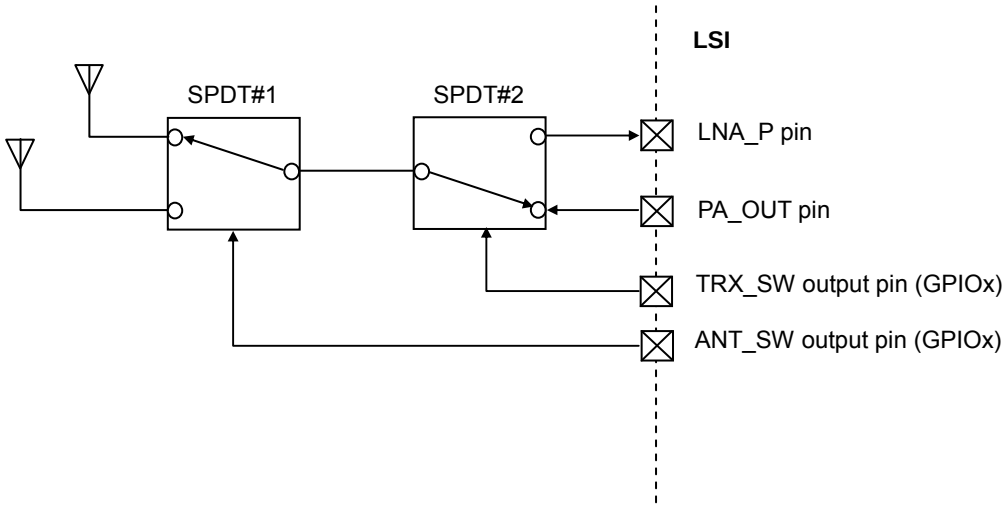
Antenna switching control signals can be also used as below.

Example 1) using one DPDT switch
Please set 2PORT_SW([2DIV_CTRL: B0 0x48(1)])=0b1.



(Note) altenate external PA control signal exists (GOIPn or EXT_CLK pin).
(Note) external circuits around LNA_P pin, PA_OUT pin and antenna switch (DPDT#1) are omitted in this example.

Example 2) using 2 SPDT switches
Please set 2PORT_SW([2DIV_CTRL: B0 0x48(1)])=0b0.



(Note) altenate external PA control signal exsits. (GPIOx or EXT_CLK pin)
(Note) external circuits around LNA_P pin, PA_OUTpin and antenna switch(SPDT#2) are omitted in this example.

○CCA (Clear Channel Assessment) function

ML7406 supports CCA function. CCA function is to make a judment wheher the specified frequency channel is in-use or available. Normal mode, continuous mode and IDLE detection mode are supported as following table.

[CCA mode setting]

	[CCA_CTRL: B0 0x39]		
	Bit4 (CCA_EN)	Bit5 (CCA_CPU_EN)	Bit6 (CCA_IDLE_EN)
Normal mode	0b1	0b0	0b0
Continuous mode	0b1	0b1	0b0
IDLE detection mode	0b1	0b0	0b1

(1) Normal mode

Normal mode determines IDLE or BUSY. CCA (Normal mode) will be executed when RX_ON is issued while CCA_EN(CCA_CTRL: B0 0x39(4)])=0b1, CCA_CPU_EN(CCA_CTRL: B0 0x39(5)])=0b0 and CCA_IDLE_EN (CCA_CTRL: B0 0x39(6)])=0b0 are set.

Judgement of CCA is determined by average ED value and CCA threshold value defined by [CCA_LVL: B0 0x37] register. IF average ED value in [ED_RSLT: B0 0x3A] register exceeds the CCA threshold value, it is considered as “BUSY”. And CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)]) =0b01 is set

If average ED value is smaller than CCA threshold value and maintains IDLE detection period which is defined by IDLE_WAIT[9:0] of the [IDLE_WAIT_L: B0 0x3B], [IDLE_WAIT_H: B0 0x3C] registers. it is considered as “IDLE”. And CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)])=0b00 is set. For details operation of CCA_IDLE_WAIT[9:0], please refer to ”IDLE detection for long time period”

If BUSY or IDLE state is detected, CCA completion interrupt (INT[18] group3) is generated, CCA_EN bit is cleared to 0b0 automatically.

Upon clearing CCA completion interrupt, CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)]) are reset to 0b00. Therefore CCA_RSLT[1:0] should be read before clearing CCA completion interrupt.

If ED value exceeds the value defined by [CCA_IGNORE_LVL: B0 0x36] register, and as long as a given ED value is included in the averaging target of ED value calculation, IDLE judgement is not performed. In this case if average ED value exceeds CCA threshold value, it is considered as “BUSY” and CCA is terminated.

If average ED value is smaller than CCA threshold valu, IDLE judgement is not determined. And CCA_RSLT[1:0] ([CCA_CTRL: B0 0x39(1-0)]) indicates 0b11. CCA operation continues until BUSY is determined or gievn ED value is out of averaging target and IDLE is determined. For details operation of ED value exeeeding [CCA_IGNORE_LVL: B0 0x36] register, please refer to ”IDLE determination exclusion under strong signal input”.

Timming from CCA command issue to CCA completion is in the formula below.

[IDLE detection]
CCA execution timing = (ED value average times + IDLE_WAIT setting) * AD conversion time

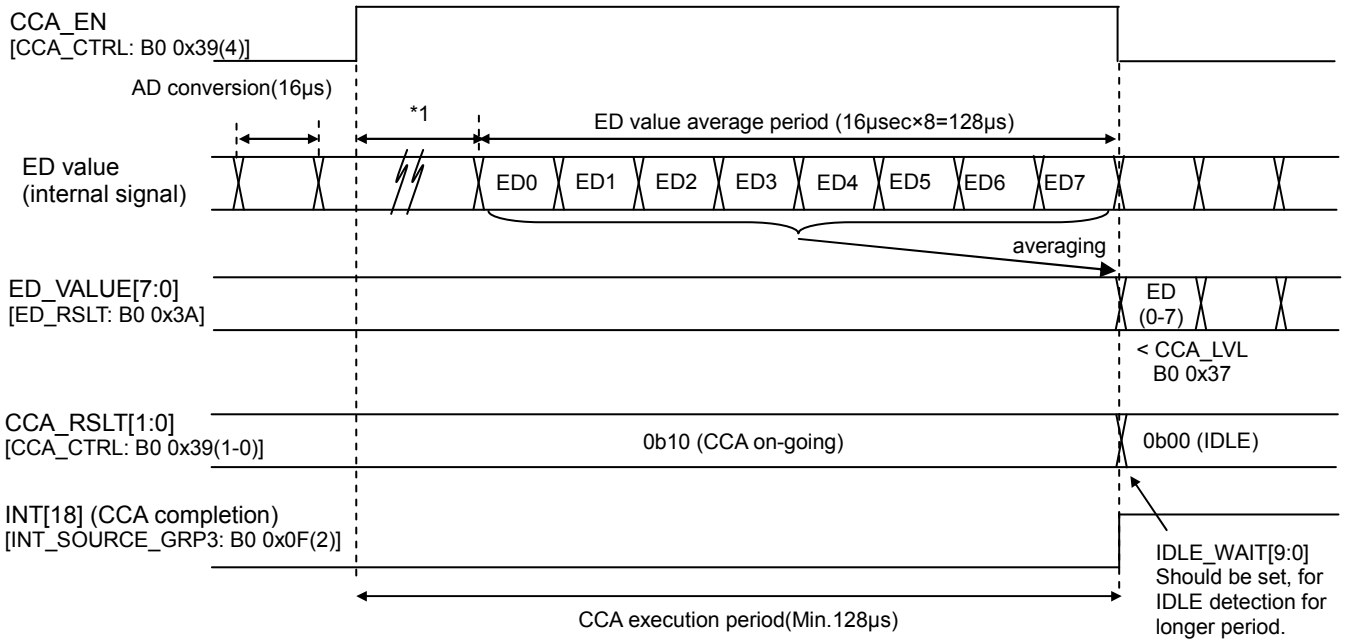
[BUSY detection]
CCA execution time = ED value average time * AD conversion time

(Note)
1. Above formula does not consider IDLE judgement exclusion based on [CCA_IGNORE_LVL: B0 0x36] register. For details, please refer to ”IDLE detection exclusion under strong signal input”.
2. AD conversion time can be slected by ADC_CLK_SEL([ADC_CLK_SET: B1 0x08(4)]). ADC_CLK_SEL=0b0:17.7µs , 0b1:16µs(default)

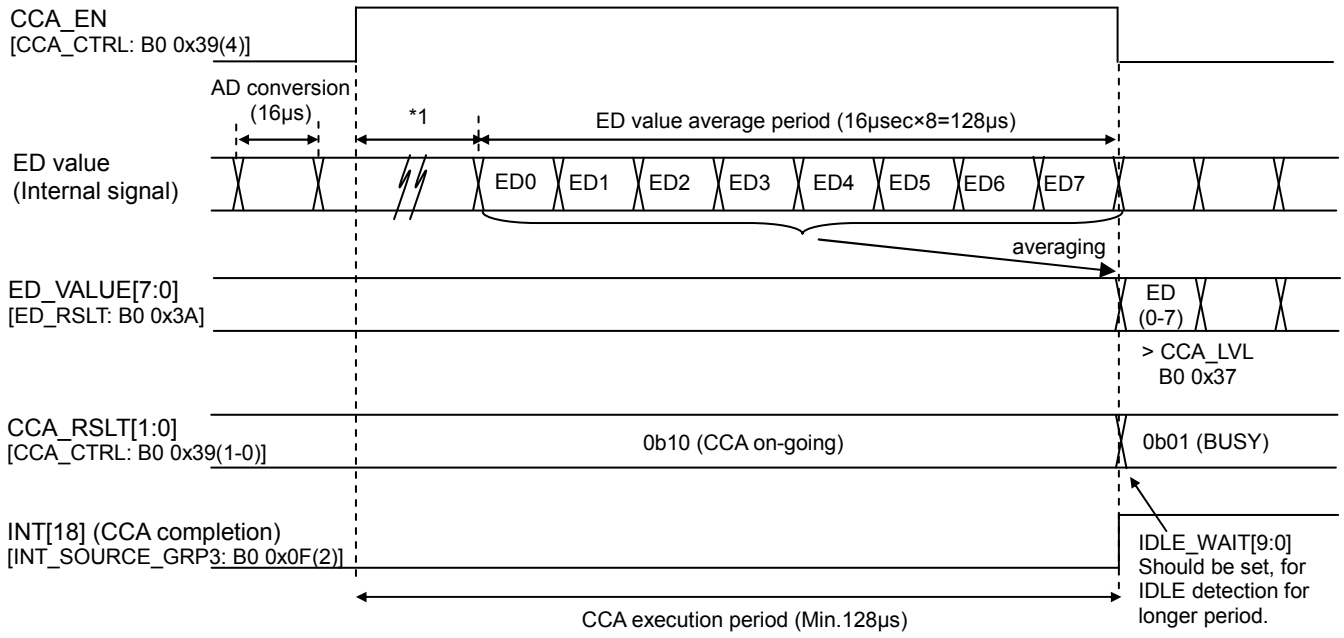
The following is timing chart for normal mode.

[Condition]
ADC_CK_SEL([ADC_CLK_SET: B0 0x08(4)])=0b1 (2MHz)
ED_AVG[2:0] ([ED_CTRL: B0 0x41(2-0)])=0b011 (ED value 8 times average)
IDLE_WAIT[9:0] ([IDLE_WAIT_L/H: B0 0x3C/3B(1-0)])=0b00_0000_0000 (IDLE detection 0µs)

[IDLE detection case]



[BUSY result case]



(Note)
*1 During CCA operation, if set bandwidth to be extended (default is not extended), enabling filter stabilization time by setting CCA_MASK_EN([CCA_MASK_SET: B2 0x7E(4)]) = 0b1. Stabilization time should be 1 ADC conversion time. If this register is enabled, input operation is suspended until filter become stable.

(2) Continuous mode

Continuous mode continues CCA untill terminated by the host MCU. CCA continuous mode will be executed when RX_ON is issued while CCA_EN(CCA_CTRL: B0 0x39(4)])=0b1, CCA_CPU_EN(CCA_CTRL: B0 0x39(5)])=0b1 and CCA_IDLE_EN(CCA_CTRL: B0 0x39(6)])=0b0 are set.

Like normal mode, CCA judgement is determined by average ED value and CCA threshold defined by [CCA_LVL: B0 0x37] register. IF average ED value in [ED_RSLT: B0 0x3A] register exceed the CCA threshold value, it is considered as “BUSY”. And CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)]) = 0b01 is set.
If average ED value is smaller than CCA threshold value and maintains IDLE detection period which is defined by IDLE_WAIT[9:0] of the [IDLE_WAIT_L: B0 0x3B], [IDLE_WAIT_H: B0 0x3C] registers, it is considered as “IDLE”. And CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)])=0b00 is set. For details operation of CCA_IDLE_WAIT[9:0], please refer to ”IDLE detection for long time period”.

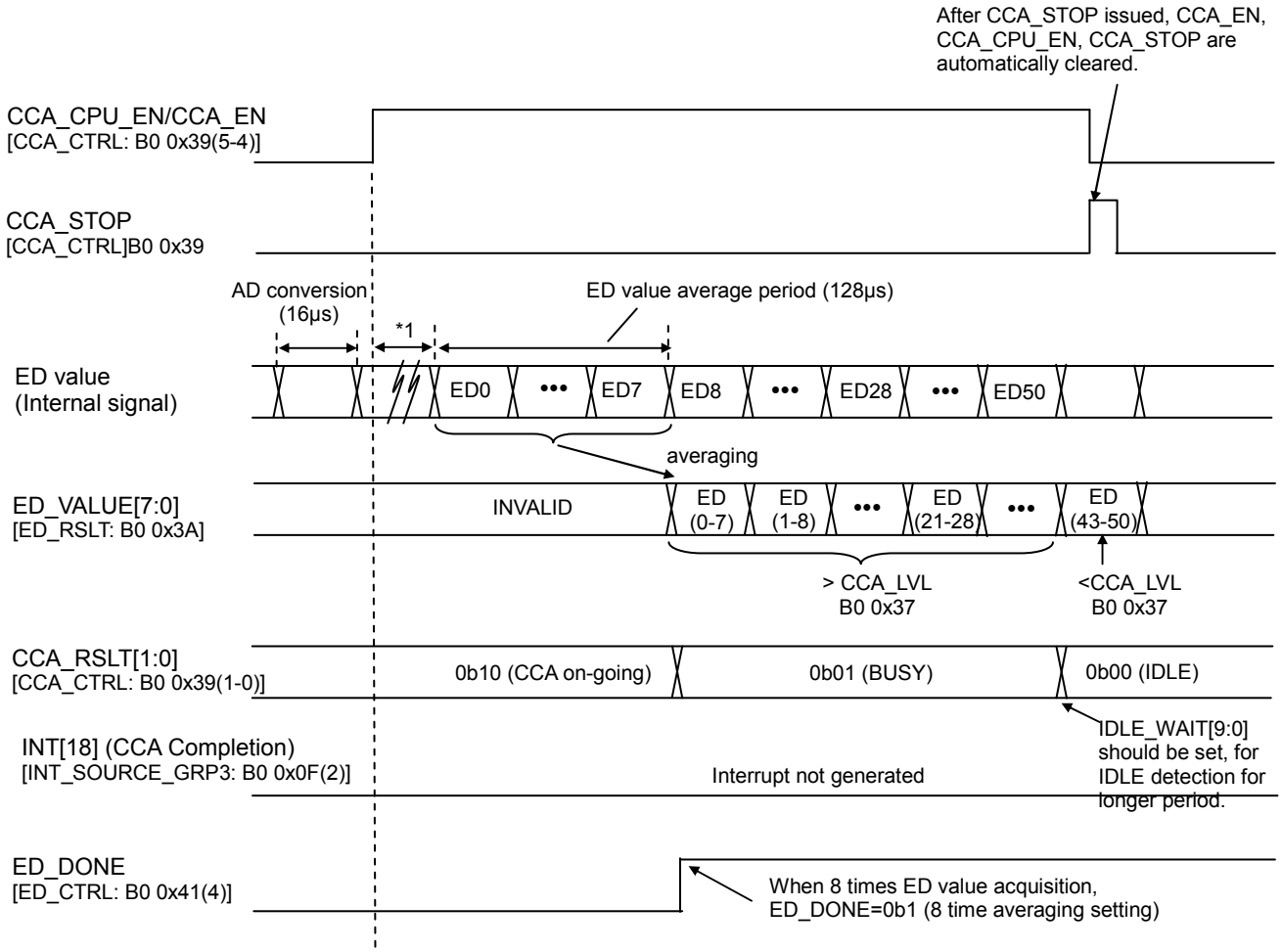
If ED value exceeds the value defined by [CCA_IGNORE_LVL: B0 0x36] register, as long as a given ED value is included in the averaging target of ED value calculation, IDLE judgement is not performed. In this case if average ED value exceed CCA threshold level, it is considered as “BUSY” and CCA_RSLT[1:0] ([CCA_CTRL: B0 0x39(1-0)]) indicates 0b01. If average ED value is smaller than CCA threshold level, IDLE judgement is not determined. And CCA_RSLT[1:0] ([CCA_CTRL: B0 0x39(1-0)]) indicates 0b11. For details operation of ED value exeeceding [CCA_IGNORE_LVL: B0 0x36] register, please refer to ”IDLE determination exclusion under strong signal input”.

Continuous mode does not stop when BUSY or IDLE is detected. CCA operation continues until 0b1 is set to CCA_STOP([CCA_CTRL: B0 0x39(7)]). Result is updated every time ED value is acquired. CCA completion interrup (INT[18] group3) will not be generated.

The follwing is timing chart for continuous mode.

[Condition]
ADC_CK_SEL([ADC_CLK_SET: B0 0x08(4)])=0b1 (2MHz)
ED_AVG[2:0] ([ED_CTRL: B0 0x41(2-0)])=0b011 (ED value 8 times average)
IDLE_WAIT[9:0] ([IDLE_WAIT_L/H: B0 0x3C/3B(1-0)])=0b00_0000_0000 (IDLE detection period 0µs)

[BUSY to IDLE transition, terminated with CCA_STOP]



(Note)
*1 During CCA operation, if set bandwidth to be extended (default is not extended), enabling filter stabilization time by setting CCA_MASK_EN([CCA_MASK_SET: B2 0x7E(4)]) = 0b1. Stabilization time should be 1 ADC conversion time. If this register is enabled, input operation is suspended until filter become stable.

(3) IDLE detection mode

IDLE detection mode continues CCA until IDLE detection. IDLE detection CCA will be executed when RX_ON is issued while CCA_EN(CCA_CTRL: B0 0x39(4)])=0b1, CCA_CPU_EN(CCA_CTRL: B0 0x39(5)])=0b0 and CCA_IDLE_EN (CCA_CTRL: B0 0x39(6)])=0b1 are set.

Like normal mode, CCA judgement is determined by average ED value and CCA threshold defined by [CCA_LVL: B0 0x37] register. IF average ED value in [ED_RSLT: B0 0x3A] register exceed the CCA threshold value, it is considered as "BUSY". And CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)]) =0b01 is set.
If average ED value is smaller than CCA threshold value and maintains IDLE detection period which is defined by IDLE_WAIT[9:0] of the [IDLE_WAIT_L: B0 0x3B], [IDLE_WAIT_H: B0 0x3C] registers. it is considered as "IDLE". And CCA_RSLT[1:0]([CCA_CTRL:B0 0x39(1-0)]) =0b00 is set. For details operation of CCA_IDLE_WAIT[9:0], please refer to "IDLE detection for longer period".

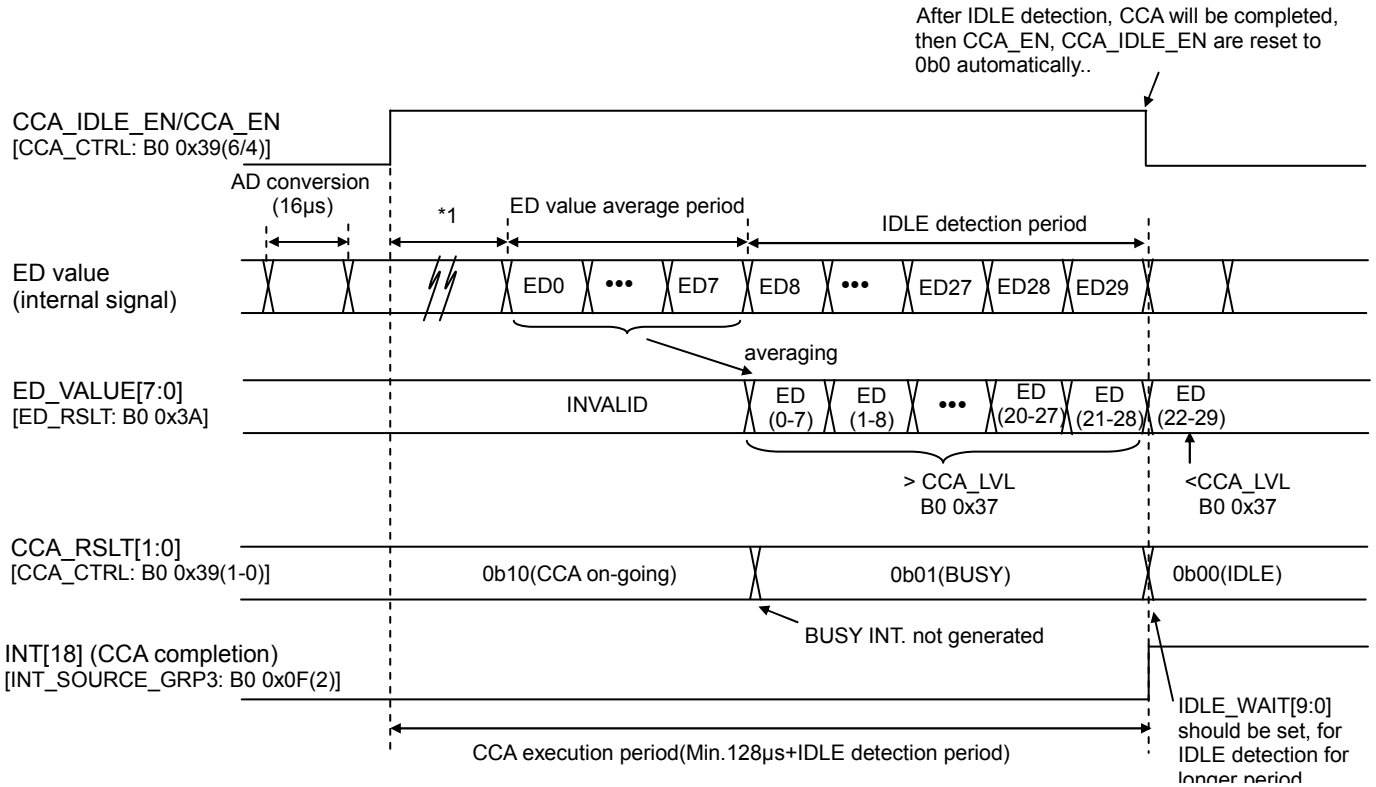
In IDLE detection mode, only when IDLE is detected, CCA completion interrupt (INT[18] group3 is generated. After IDLE detection, CCA_EN and CCA_IDLE_EN are reset to 0b0.
Upon clearing CCA completion interrupt, CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)]) are reset to 0b00. CCA_RSLT[1:0] should be read before clearing CCA completion interrupt.

If ED value exceeds the value defined by [CCA_IGNORE_LVL: B0 0x36] register, as long as a given ED value is included in the averaging target of ED value calculation, IDLE judgement is not performed. In this case, if average ED value is smaller than CCA threshold level, IDLE determination is not performed and CCA_RSLT[1:0] ([CCA_CTRL: B0 0x39(1-0)]) indicates 0b11. CCA operation continues until given ED value is out of averaging target and IDLE is determined. For details of ED value exceeding [CCA_IGNORE_LVL: B0 0x36] register, please refer to "IDLE determination exclusion under strong signal input".

The follwing is timing chart for IDLE detection.

[Upon BUSYdetection, continue CCA and IDLE detection case]

[Condition]
ADC_CK_SEL([ADC_CLK_SET: B0 0x08(4)])=0b1 (2MHz)
ED_AVG[2:0]([ED_CTRL: B0 0x41(2-0)])=0b011 (ED value 8 times average)
IDLE_WAIT[9:0] ([IDLE_WAIT_L/H: B0 0x3C/3B(1-0)])=0b00_0000_0000 (IDLE detection period 0μs)



(Note)
*1 During CCA operation, if set bandwidth to be extended (default is not extended), enabling filter stabilization time by setting CCA_MASK_EN([CCA_MASK_SET: B2 0x7E(4)]) = 0b1. Stabilization time should be 1 ADC conversion time. If this register is enabled, input operation is suspended until filter become stable.

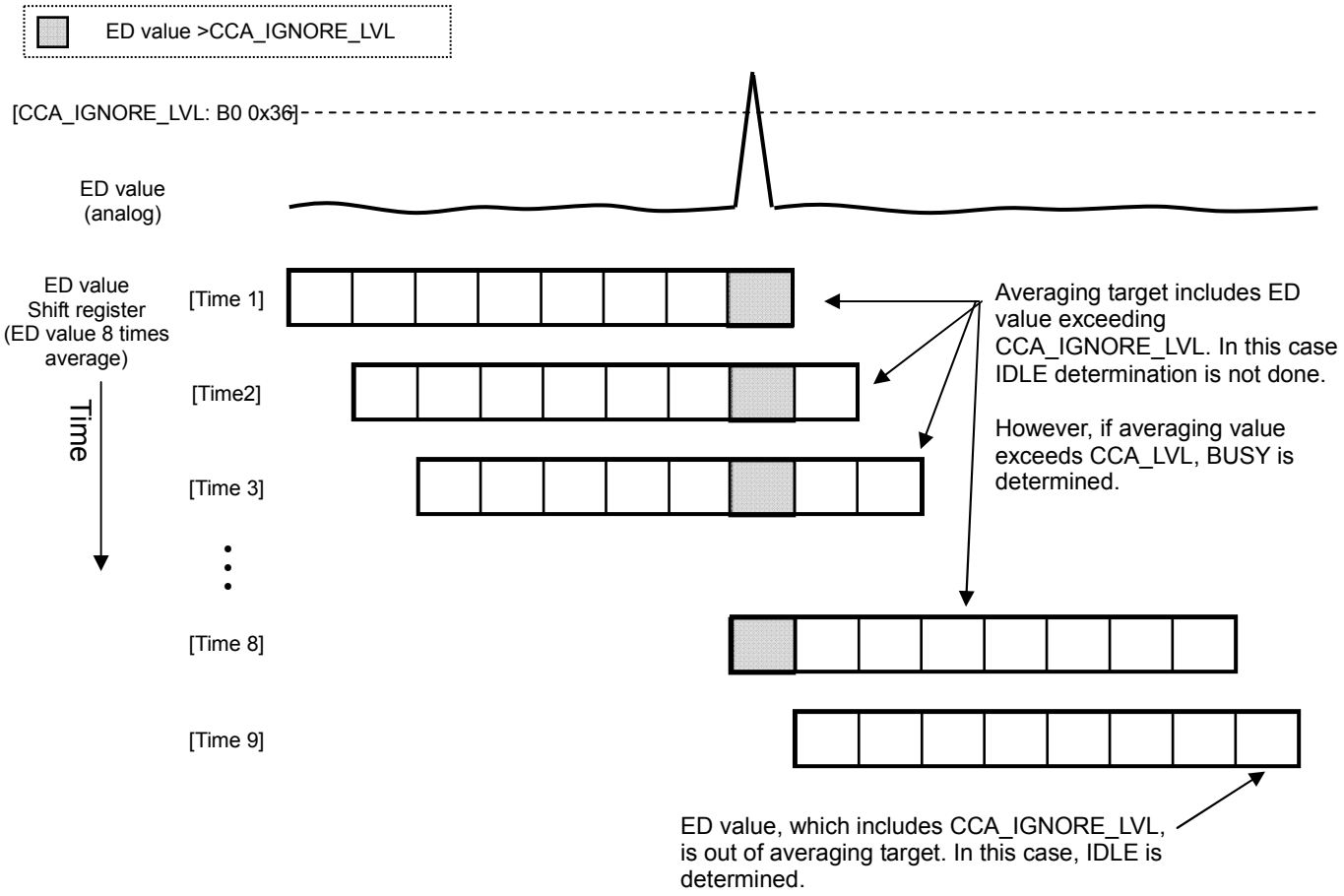
(4) IDLE determination exclusion under strong signal input

If acquired ED value exceeds [CCA_IGNORE_LVL: B0 0x36] register, IDLE dertermination is not performed as lon as a given ED value is included in the averaging target range. If average ED value including this strong ED value indicated in [ED_RSLT: B0 0x39] rehgiser exceeds the CCA threshold value defined by [CCA_LVL: B0 0x37] register, it is considered as ”BUSY”. And CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)])=0b01 is set.

If average ED value is smaller than CCA threshold value, IDLE determination is not performed and CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)]) indicates 0b11 ”CCA evaluation under going (ED value excluding CCA judgement acquisition)”. CCA will continue until IDLE or BUSY determination (in case of IDLE detection mode, IDLE is determined. In case of continuous mode, CCA_STOP([CCA_CTRL: B0 0x39(7)]) is issued.)

(Note)
CCA completion interrupt (INT[18] group3) is generated CCA only when IDLE or BUSY is determined. Therefore, if data whose ED value exceeds CCA_IGNORE_LVL are input intermittently, neither IDLE or BUSY cane be determined and CCA may continues.

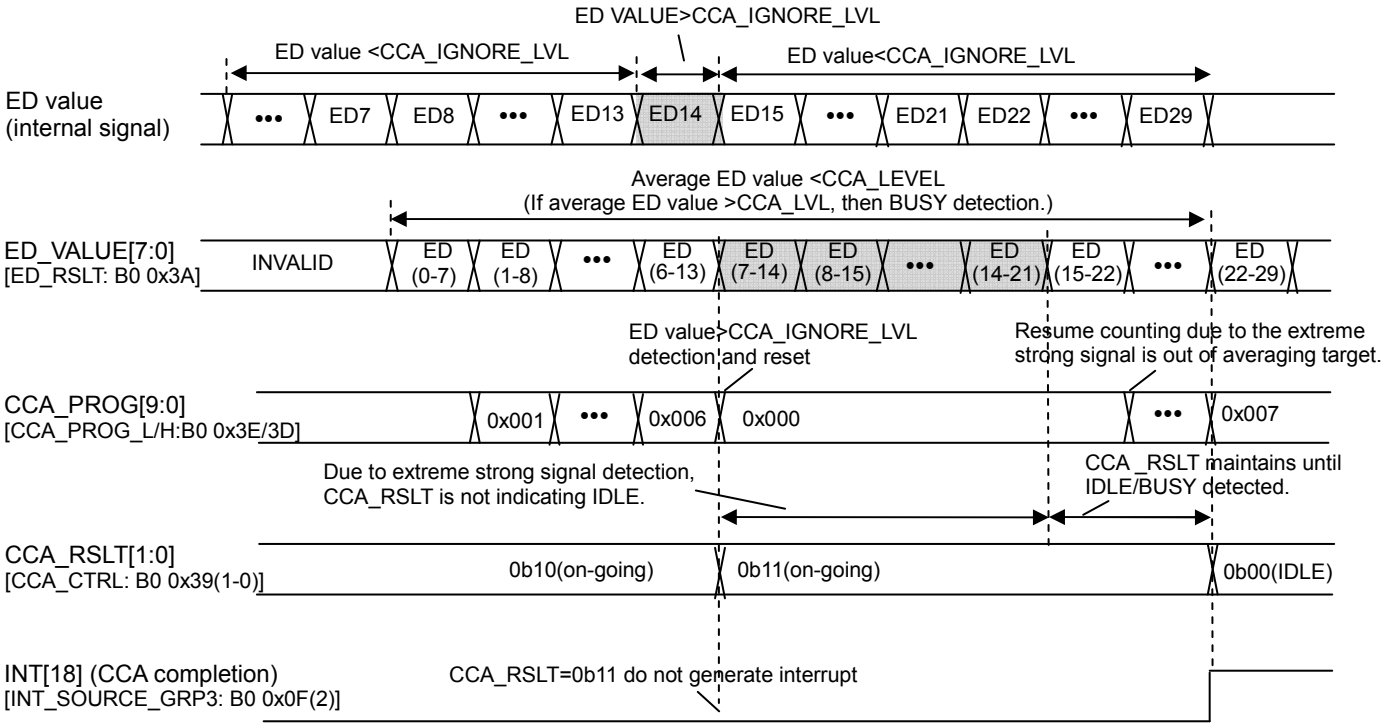
[ED value acquisition under extrem strong signal]



The follwing is timing chart for CCA determination exclusion under strong signal.

[During IDLE_WAIT counting, detected extremly strong signal. After the given signal is out of averaging target, IDLE detection case]

[Condition]
CCA normal mode
ADC_CK_SEL([ADC_CLK_SET: B0 0x08(4)])=0b1 (2MHz)
ED_AVG[2:0]([ED_CTRL: B0 0x41(2-0)])=0b011 (ED value 8 times average)
IDLE_WAIT[9:0]([IDLE_WAIT_L/H: B0 0x3C/3B(1-0)])=0b00_0000_0111(IDLE detection period 112μs)



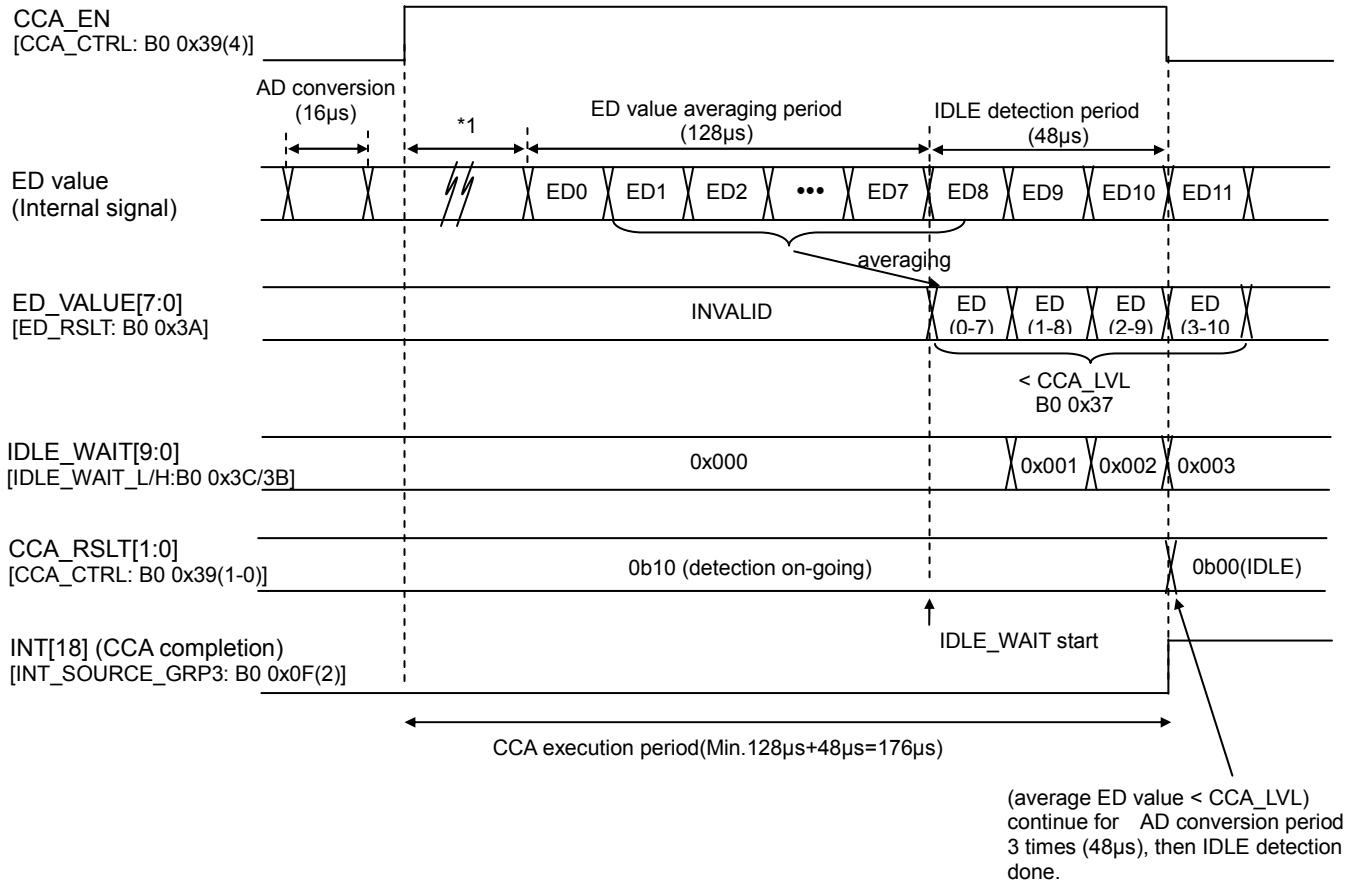
(5) IDLE detection for longer time period

When CCA IDLE detection is performed for longer time period, IDLE_WAIT[9:0]([IDLE_WAIT_L/H:B0 0x3C/3B(1-0)] can be used. By setting IDLE_WAIT [9:0], averaging period longer than the period (for example, AD conversion16µs, 8 times average setting 128µs) can be possible.
This function can be used for IDLE determination – by counting times when average ED value becomes smaller than CCA threshold defined by [CCA_LVL: B0 0x37] register. When counting exceed IDLE_WAIT [9:0], IDLE determination is done. If average ED value exceeds CCA threshold level, imemediately "Busy" is determined without wait for IDLE_WAIT [9:0] period.

The following timing chart is IDLE detection setting IDLE_WAIT[9:0].

[ED value 8 timesv average IDLE detection case]

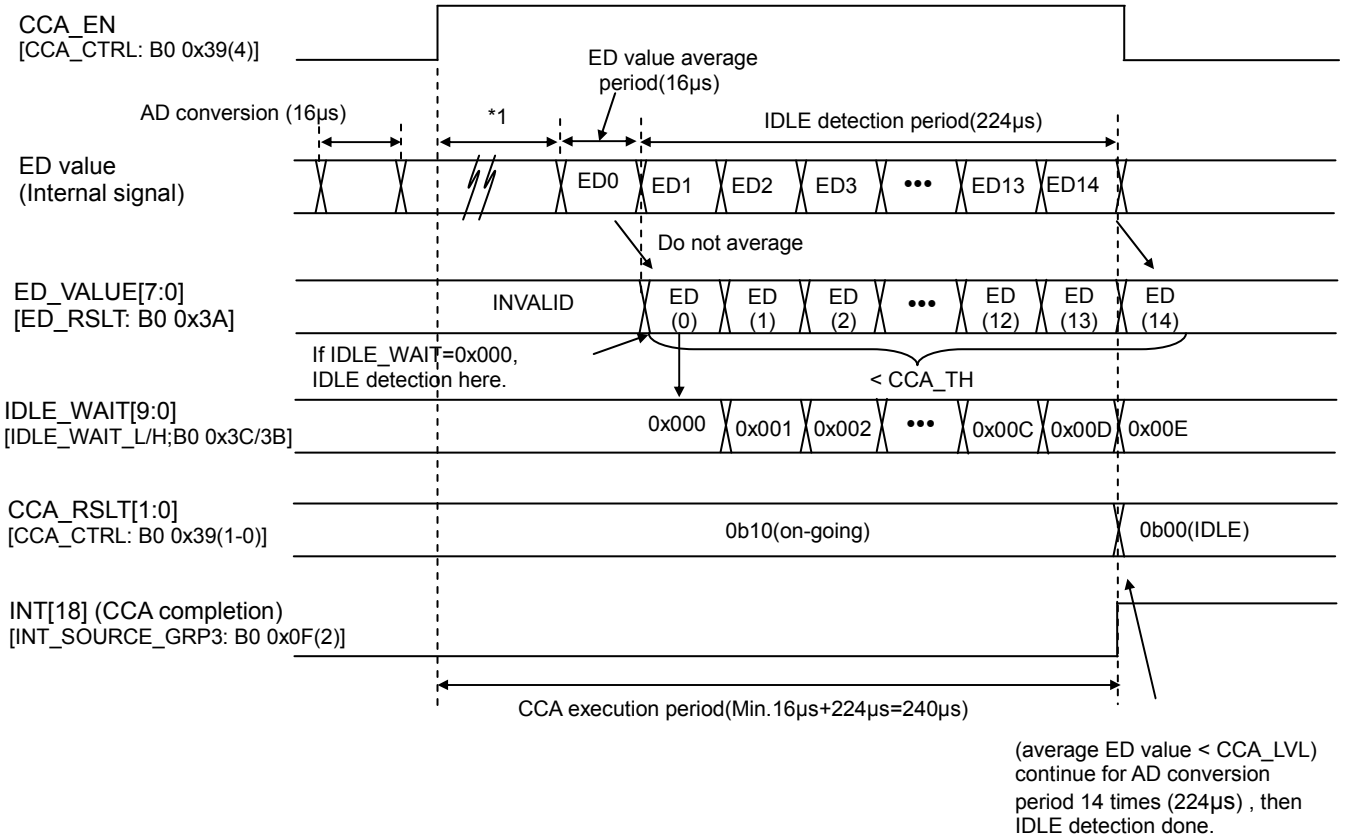
[Condition]
CCA normal mode
ADC_CK_SEL([ADC_CLK_SET: B0 0x08(4)])=0b1 (2MHz)
ED_AVG[2:0]([ED_CTRL: B0 0x41(2-0)])=0b011 (ED value 8 times average)
IDLE_WAIT[9:0]([IDLE_WAIT_L/H: B0 0x3C/3B(1-0)])=0b00_0000_0011 (IDLE detection period 48µs)



(Note)
*1 During CCA operation, if set bandwidth to be extended (default is not extended), enabling filter stabilization time by setting CCA_MASK_EN([CCA_MASK_SET: B2 0x7E(4)]) = 0b1. Stabilization time should be 1 ADC conversion time. If this register is enabled, input operation is suspended until filter become stable.

[ED value 1time IDLE detection case]

[Condition]
CCA normal mode
ADC_CK_SEL([ADC_CLK_SET: B0 0x08(4)])=0b1 (2MHz)
ED_AVG[2:0]([ED_CTRL: B0 0x41(2-0)])=0b000 (ED value 1 time average)
IDLE_WAIT[9:0]([IDLE_WAIT_L: B0 0x3C/H: B0 0x3C/3B(1-0)])=0b00_0000_1110 (IDLE detection period 224µs)



(Note)
*1 During CCA operation, if set bandwidth to be extended (default is not extended), enabling filter stabilization time by setting CCA_MASK_EN([CCA_MASK_SET: B2 0x7E(4)]) = 0b1. Stabilization time should be 1 ADC conversion time. If this register is enabled, input operation is suspended until filter become stable.

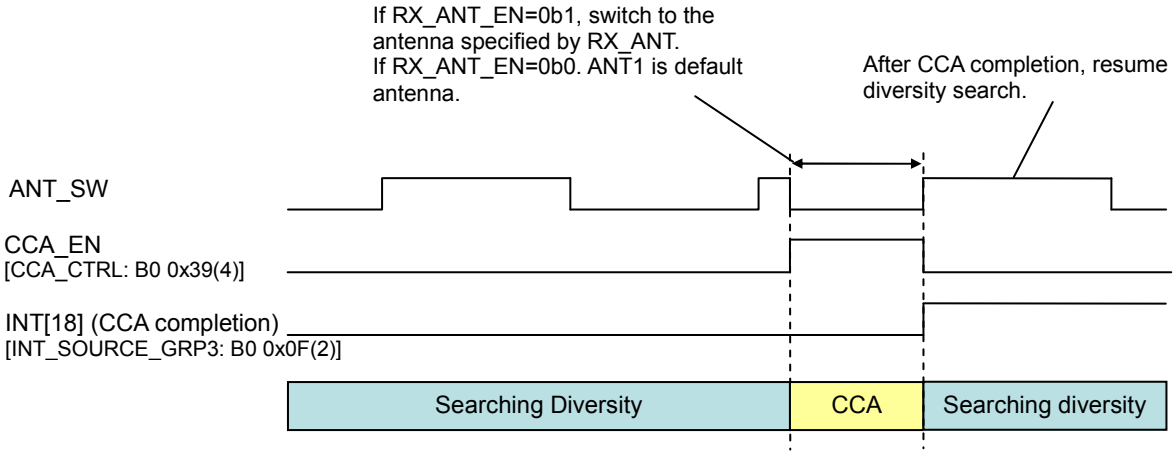
(6) CCA operation during diversity

CCA operation during antenna diversity

During diversity, if CCA command is issued, diversity terminated and CCA starts.

Upon CCA starting, antenna is fixed to reset value(*1), maintaining until next diversity search. However, if RX_ANT_EN([ANT_CTRL:B0 0x4C(4)])=0b1 is set, antenna is specified by RX_ANT([ANT_CTRL: B0 0x4C(5)]). After CCA completion, diversity will be executed agaim.

*1 Please refer to the “Antenna switching function”. According to the default setting, ANT_SW and TRX_SW signals are set.



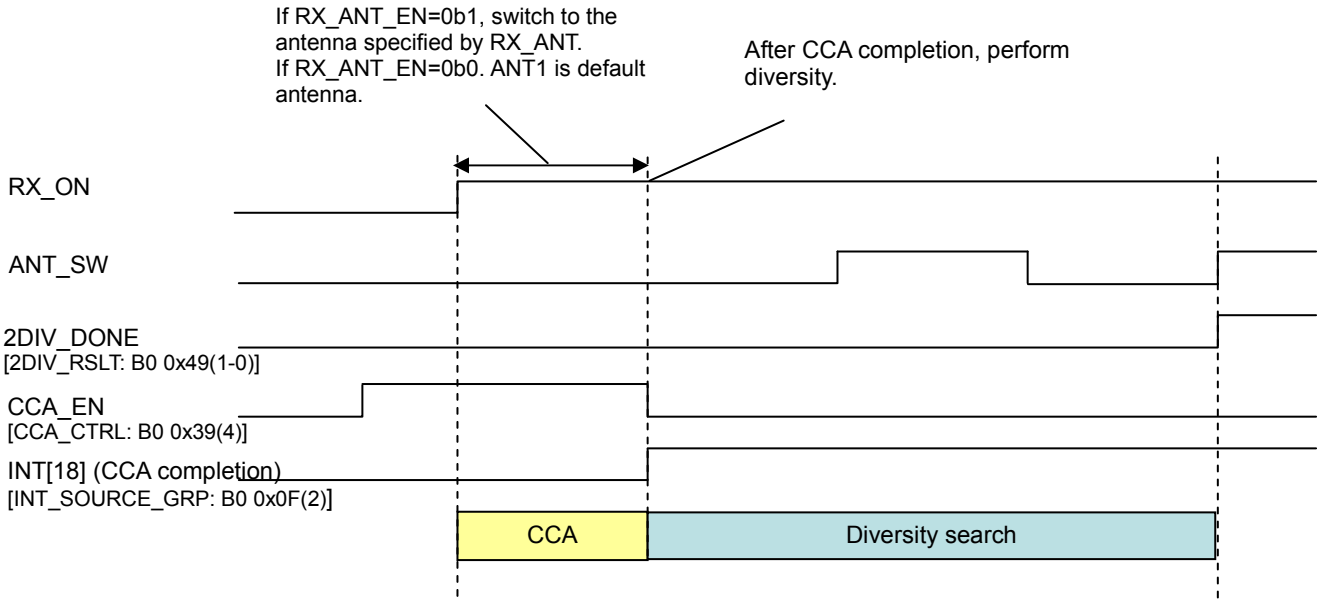
(Note)

During CCA operation, RX operation is performed at the same time, even if CCA completion interrupt (INT[18] group3) is not generated, SyncWord detection interrupt (INT[13] group2), RX FIFO access error interrupt (INT[12] group2), RX length error interrupt (INT[11] group2), CRC error interrupt (INT[9] group2), RX completion interrupt (INT[8] group2) or FIFO-Full interrupt (INT[5] group1) can be generated.

For details diversity function, please refer to the ”diversity function”.

During diversity , before RX_ON state, CCA is performed.

If diversity ON setting and CCA operation setting is enabled before RX_ON state, after RX_ON state transition, diversity will not perform, but CCA will start. After CCA completion, diversity will be performed.



(7) CCA threshold setting

CCA threshold value defined by [CCA_LVL: B0 0x37] register, should be considered desired input leve (ED value), components variation, temperature fluctuation, loss at antenna and matching circuits. Input level and ED value are described in the follow table.

ED value = 255 / 70 * (107 + input level[dBm])

However, if BPF setting modified and CCA is executed, ED value become bigger than normal case. CCA threshold can be set as below , taking this compensation and variations into account.

CCA threshold = 255 / 70 * (107 + input level[dBm] - variations – other losses) + CCA compensation

Item	Value
Variation (individual, temp.)	6dB
Other loss	Antenna, matchich circuits loss
CCA compensation	12@100kbps, 15@200kbps, 0@other rate

Example) When input level threshold is set to -75dBm
conditions:other losses 1dB, 100kbps

CCAthreshold = 255 / 70 * (107 - 75 - 6 - 1) + 12
≈ 103
= 0x67

In order to validate whether CCA threshold is optimised or not, CCA should be executed and confirmimg level changing from IDLE to BUSY, every time input level is changed,

●Other Functions

○Data rate setting function

(1) Data rate change setting

ML7406 supports various TX/RX data rate setting defined by the following registers.
TX: [TX_RATE_H: B1 0x02] and [TX_RATE_L: B1 0x03] registers
RX: [RX_RATE1_H: B1 0x04], [RX_RATE1_L: B1 0x05] and [RX_RATE2: B1 0x06] registers
TX/RX data rate can be defined in the following formula.

[TX]

TX data rate [bps] = round (26MHz / 13/ TX_RATE[11:0])

Recommended values for each data rate are in the table below. Registers value below are automatically set to [TX_RATE_H],[TX_RATE_L] registers by setting TX_DRATE[3:0] ([DRATE_SET: B0 0x06(3-0)]).

TX data rate [kbps]	[TX_RATE_H][TX_RATE_L] register setting value	Data rate deviation [%] *1
1.2	1667d	-0.02
2.4	833d	0.04
4.8	417d	-0.08
9.6	208d	0.16
32.768	61d	0.06
50	40d	0.00
100	20d	0.00
200	10d	0.00
300	7d	3.17
400	5d	0.00
500	4d	0.00

*1 Data rate deviation is assumption that frequency deviation of master clock(26MHz crystal oscillator or TCXO or SPXO) is 0ppm.

[RX]

RX data rate [bps] = round (26MHz / {RX_RATE1[11:0] ×[RX_RATE2[6:0]})

Recommended values for each data rate are in the table below. Registers value below are automatically set to [RX_RATE1_H][RX_RATE1_L] [RX_RATE2] registers by setting RX_DRATE[3:0]([DRATE_SET:B0 0x06(7-4)]).

RX dta rate [kbps]	[RX_RATE1_H][RX_RATE1_L] register setting value	[RX_RATE2] register setting
1.2	169d	0d
2.4	85d	0d
4.8	42d	0d
9.6	21d	0d
32.768	11d	72d
50	8d	65d
100	4d	65d
200	5d	26d
300	3d	29d
400	2d	32d
500	2d	26d

(Note)
When LOW_RATE_EN([CLK_SET2:B0 0x03(0)])=0b1, [RX_RATE1_H/L] and [RX_RATE2] registers are not set automatically by setting RX_DRATE[3:0]. Please calcurate appropriate values by replacing the 8.66MHz to 26MHz in the above formula and set them to each register.

(2) Other register setting associate with data rate change

Data rate can be cahnged by RX_DRATE[3:0] ([DRATE_SET(7-4)]) and TX_DRATE[3:0] ([DRATE_SET(3-0)]), below registers may have to be changed.

(Note)
1. Depending on data rate, the following chage may not be necessary. For details, please refer to each register description.
2. Please change data rate setting in TRX_OFF state.
3. After change of data rate setting, please execute RST1 [RST_SET: B0 0x01(1)] (MODEM Reset).

Parameters	Registers	
	Name	Address
Data rate	DRATE_SET	B0 0x06
Channel space	CH_SPACE_H	B1 0x23
	CH_SPACE_L	B1 0x24
Frequency deviation(GFSK)	GFSK_DEV_H	B1 0x30
	GFSK_DEV_L	B1 0x31
Frequencydeviation (FSK)	FSK_DEV0_H/GFIL0	B1 0x32
	FSK_DEV0_L/GFIL1	B1 0x33
	FSK_DEV1_H/GFIL2	B1 0x34
	FSK_DEV1_L/GFIL3	B1 0x35
	FSK_DEV2_H/GFIL4	B1 0x36
	FSK_DEV2_L/GFIL5	B1 0x37
	FSK_DEV3_H/GFIL6	B1 0x38
	FSK_DEV3_L	B1 0x39
	FSK_DEV4_H	B1 0x3A
	FSK_DEV4_L	B1 0x3B
Frequency deviation time(FSK)	FSK_TIM_ADJ4	B1 0x3C
	FSK_TIM_ADJ3	B1 0x3D
	FSK_TIM_ADJ2	B1 0x3E
	FSK_TIM_ADJ1	B1 0x3F
	FSK_TIM_ADJ0	B1 0x40
IF frequency	IF_FREQ_H	B0 0x54
	IF_FREQ_L	B0 0x55
If frequency during CCA	IF_FREQ_CCA_H	B0 0x56
	IF_FREQ_CCA_L	B0 0x57
BPF coefficient	BPF_CO	B0 0x5C
BPF coefficient during CCA	BPF_CO_CCA	B0 0x5D
Demodulator DC level adjustment	IFF_ADJ_H	B0 0x5E
	IFF_ADJ_L	B0 0x5F
Demodulator DC level adjustment during CCA	IFF_ADJ_CCA_H	B0 0x60
	IFF_ADJ_CCA_L	B0 0x61
Demodulator adjustment1	DEMOD_SET1	B1 0x57
Demodulator adjustment2	DEMOD_SET2	B1 0x58
Demodulator adjustment3	DEMOD_SET3	B1 0x59
Demodulator adjustment4	DEMOD_SET4	B1 0x5A
Demodulator adjustment5	DEMOD_SET5	B1 0x5B
Demodulator adjustment6	DEMOD_SET6	B1 0x5C
Demodulator adjustment7	DEMOD_SET7	B1 0x5D
Demodulator adjustment8	DEMOD_SET8	B1 0x5E
Demodulator adjustment9	DEMOD_SET9	B1 0x5F

○Interrupt generation function

ML7406 support interrupt generation function. When interrupt occurs, interrupt notification signal (SINTN) become “L” to signal interrupt to the Host. Interrupt elements are divided in to the 3 groups, [INT_SOURCE_GRP1: B0 0x0D], [INT_SOURCE_GRP2: B0 0x0E] and [INT_SOURCE_GRP3: B0 0x0F]. Each interrupt element can be maskalable using [INT_EN_GRP1: B0 0x10]. [INT_EN_GRP2: B0 0x11] and [INT_EN_GRP3: B0 0x12] registers. Interrupt notification signal (SINTN) can be output from GPIO* or EXT_CLK. For output setting, please refer to [GPIO1_CTRL: B0 0x4E], [GPIO1_CTRL: B0 0x4F], [GPIO2_CTRL: B0 0x50], [GPIO3_CTRL: B0 0x51] and [EXTCLK_CTRL: B0 0x52] registers.

(Note)
If one of the unmask interrupt event occurs, SINTN maintains Low.

(1) Interrupt events table

Each interrupt event is described below table.

Register	Interrupt name	Description
INT_SOURCE_GRP1	INT[0]	Clock stabilizaion completion interrupt
	INT[1]	VCO calibration completion interrupt/ FUSE access completion interrupt
	INT[2]	PLL unlock interrupt
	INT[3]	RF state transition completion interrupt
	INT[4]	FIFO-Empty interrupt
	INT[5]	FIFO-Full interrupt
	INT[6]	Wake-up timer completion interrupt
	INT[7]	Clock calibration completion interrupt
INT_SOURCE_GRP2	INT[8]	RX completion interrupt
	INT[9]	CRC error interrupt
	INT[10]	Diversity search completion interrupt
	INT[11]	RX Length error interrupt
	INT[12]	RX FIFO access error interrupt
	INT[13]	SyncWord detection interrupt
	INT[14]	Field checking interrupt
	INT[15]	Sync error interrupt
INT_SOURCE_GRP3	INT[16]	TX completion interrupt
	INT[17]	TX Data request accept completion interrupt
	INT[18]	CCA completion interrupt
	INT[19]	TX Length error interrupt
	INT[20]	TX FIFO access error interrupt
	INT[21]	Reserved
	INT[22]	General purpose timer 1 interrupt
	INT[23]	General purpose timer 2 interrupt

(2) Interrupt generation timing

In each interrupt generation, timing from reference point to interrupt generation (notification) are described in the following table. Timeout procedure for interrupt notification waiting are also described below.

(Note)
(1)The values are described in units of "bit cycle" in the below tablee is the value at 100kbps. If using other data rate,, please esitimate with appropriate "bit cycle".

(2)Below table uses the following format for TX/RX data.

10 byte	2 byte	1 byte	24 byte	2byte
Preamble	SyncWord	Length	User data	CRC

(3)Even if each interrupt notification is masked, in case of interrupt occurence, interrupt elements are stored internally. Therefore, as soon as interrupt notification is unmasked, interrupt will generate.

Interrupt notice		Reference point	Timing From reference point to interrupt generation or interrupt generation timing
INT[0]	CLK stabilization completion	RESETN release (upon power-up)	50µs
		SLEEP release (recovered from SLEEP)	50µs
INT[1]	VCO calibration completion	VCO calibration start	230µs
	FUSE access completion	RESETN release	48µs
INT[2]	PLL unlock detection	-	(TX) during TX after PA enable. (RX) during RX enable after RX enable.
INT[3]	RF state transition completion	TX_ON command	(IDLE) 210µs (RX) 192µs
		RX_ON command	(IDLE) 119µs (RX) 244µs
		TRX_OFF command	(TX) 147µs (RX) 4µs
		Force_TRX_OFF Command	(TX) 147µs (RX) 4µs
INT[4]	FIFO-Empty detection	(TX) TX_ON command (*1)	NRZ coding, Empty trigger level is set to 0x02. RFwake-up(210µs)+35byte(preamble to 22nd Data byte) ×8bit × 10(bit cycle) =3010µs
		(RX) -	By FIFO read, remaining FIFO data is under trigger level
INT[5]	FIFO-Full detection	(TX) -	By FIFO write, FIFO usage exceed trigger level
		(RX) SyncWord detection	NRZ coding, Full trigger level is set to 0x05. 6byte (Length to 5th Data byte) ×8bit ×10µs(bit cycle) = 480µs
INT[6]	Wake-up timer completion	SLEEP setting	Wake-up timer is completed. For details, please refer to "wake-up timer"
INT[7]	Clock calibration completion	Calibration start	Calibration timer is completed. For details, please refer to "low speed clock shift detection function".
INT[8]	RX completion	SyncWord detection	NRZ coding 27byte (L-ength to CRC) ×8bite ×10(bit cycle)=2160µs
INT[9]	CRC error detection	SyncWord detection	(Format A/B) each RX CRC block calculation completion (Format C) RX completion
INT[10]	Diversity search completion	-	SyncWord detection during diversity enable setting
INT[11]	RX Length error detection	SyncWord detection	80µs (L-field 1byte) 160µs (L-field 2byte)
INT[12]	RX FIFO access error detection	-	(1)overflow occurs because FIFO read is too slow. (2)underflow occurs because too many FIFO data is read
INT[13]	SyncWord detection	-	SyncWord detection
INT[14]	Field check completion	-	Match or mismatch detected in Field check

(*1) Before issuing TX_ON, writing full length TX data to the TX_FIFO.

Interrupt notice		Reference point	Timing From reference point to interrupt generation or interrupt generation timing
INT[15]	Sync error detection	-	During RX after SyncWord detection, out-of-sync detected. (When RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) =0b00 or 0b11.)
INT[16]	TX completion	TX_ON command (*1)	RF wake-up+[TX data+3](bit) =210μs+(39byte ×8 +3) bit × 10μs (bit cycle)=3360μs after
INT[17]	TX Data request accept completion	-	After full length data are written to the TX_FIFO.
INT[18]	CCA completion	CCA execution start	(1)Normal mode (ED value calculation averaging times +IDLE_WAIT setting [IDLE_WAIT_H/L:B0 0x3B,3C]) ×AD conversion time (2) IDLE detection mode ○IDLE judgment case (ED value calculation averaging times +IDLE_WAIT setting [IDLE_WAIT_H/L:B0 0x3B,3C]) ×AD conversion time ○BUSY judgment case (ED value calculation averaging times) ×AD conversion time AD conversion time period can be changed by AD clock frequency ([ADC_CLK_SEL:B1 0x08]) . AD clock frequency = 1.88MHz: 17.7μs, 2.0MHz: 16μs. For details, please refer to the “CCA (Clear Channel Assessment) function”.
INT[19]	TX Length error detection	-	After set length value to [TX_PKT_LEN_H/L: B0 0x7A/7B] registers
INT[20]	TX FIFO access error detection	-	(1) When the next packet data is writren to the TX_FIFO before transmitting previous packet data. (2) FIFO overflow when writing (3) FIFO underflow (no data) when transmitting
INT[21]	Reserved	-	-
INT[22]	General purpose timer 1 completion	Timer start	General purpose timer 1 completion General purpose timer clock cycle ×Division setting [GT_CLK_SET: B0 0x33] × general purpose timer interval setting [GT1_TIMER:B0 0x34] For details, please refer to the “General purpose timer”.
INT[23]	General purpose timer 2 completion	Timer start	General purpose timer 2 completion General purpose timer clock cycle ×Division setting [GT_CLK_SET: B0 0x33] × general purpose timer interval setting [GT2_TIMER:B0 0x35] For details, please refer to the “General purpose timer”.

(*1) Before issuing TX_ON, writing full length TX data to the TX_FIFO.

(3) Clearing interrupt conditions

The following table shows the condition of clearing each intereupt. As a procedure to clear the interrup, it is recommended that the interrupt to be cleared after masking the interrupt.

Interrupt notification		Conditions for clearing interrupts
INT[0]	CLK stabilization completion	After interrupt generated
INT[1]	VCO calibration completion /FUSE access completion	After interrupt generated
INT[2]	PLL unlock	After interrupt generated
INT[3]	RF state transition completion	After interrupt generated
INT[4]	FIFO-Empty	After interrupt generated (must clear before next FIFO-Empty trigger timing)
INT[5]	FIFO-Full	After interrupt generated (must clear before next FIFO-Full trigger timing)
INT[6]	Wake-up timer completion	After interrupt generated
INT[7]	Clock calibration completion	After interrupt generated
INT[8]	RX completion	After interrupt generated
INT[9]	CRC error	After interrupt generated
INT[10]	Diversity search completion	After RX completion interrupt (INT[8]), must clear together with RX completion interrupt. (Note) During data reception, clearing is prohibited.
INT[11]	RX Length error	After interrupt generated
INT[12]	RX FIFO access error	After interrupt generated
INT[13]	SyncWord detection	After interrupt generated
INT[14]	Field checking	After interrupt generated
INT[15]	Sync error	After interrupt generated
INT[16/]	TX completion	After interrupt generated
INT[17]	TX Data request accept completion	After interrupt generated
INT[18]	CCA completion	After interrupt generated (Note) clearing interrupt erase CCA result as well.
INT[19]	TX Length error	After interrupt generated
INT[20]	TX FIFO access error	After interrupt generated
INT[21]	Reserved	
INT[22]	General purpose timer 1	After interrupt generated
INT[23]	General purpose timer 2	After interrupt generated

○Temperature measurement function

ML7406 has temperature measurement function. This temperature information can be from A_MON pin (pin#23) as analog output or digital information using[TEMP: B1 0x09] register. Analog or digital can be switched by [MON_CTRL: B0 0x4D] register.

(Note)
Please do not set TEMP_OUT([MON_CTRL: B0 0x4D(4)]) and TEMP_ADC_OUT([MON_CTRL: B0 0x4D(5)]) at the same time. Correct value reading may not be guaranteed.

[Analog output]
ML7406 has current source circuits and its current flow through 75kΩ connected to A_MONpin (pin#23). From voltage information, temperature information can be obtained.

Current from current source circuits are 10μA at 25˚C. The following formula can be used to calculate temperature from the current.

Itemp = (273+ Temp) / (273+25) * 10 (μA)

Therefore, if 75kΩ resister is connected, temperature can be calculated using the following formula.

Vamon = (273+ Temp) / (275+25) * 10E-6 * 75000

If temperature is -40˚C to 85˚C, Vamon will be 0.59V to 0.9V.
The following formula can be used to calculate temperature from voltage .

Temp = Vamon * 397.3 - 273

[Digital output]
Digital temperature information is using 6 bit ADC to convert from the above analog information. Internally, 4samples information are added and indicates as 8bit information in [TEMP: B1 0x09] register. Ignoring low 2 bits, upper 6bitare used for average temperature information.
Temperature information is updated every 16μs([ADC_CLK_SET: B1 0x08] register. If 1.73MHzis selected, it is updated every 18.5μs.

○Low speed clock shift detection function

ML7406 has low speed shift detection function to compensate inaccurate clock generated by RC oscillator (external clock or internal RC oscillation circuits). By detecting frequency shift of the wake up timer, host can set wake-up timer parameters which taking frequency shift into consideration. More accurate timer operation is possible by adjusting wake-up timer interval setting ([WUT_INTERVAL_H/L: B0 0x2F/0x30]) or continuous operation timer interval ([WU_DURATION: B0 0x31]).

Setting	Register
Frequency shift detection clock frequency setting	[CLK_CAL_SET: B0 0x70]
Clock calibration time	[CLK_CAL_TIME: B0 0x71]
Clock calibration result value	[CLK_CAL_H: B0 0x72], [CLK_CAL_L: B0 0x73]

This function is to measure low speed wake-up timer cycle by using accurate high speed internal clock and count result will be stored in [CLK_CAL_H/L: B0 0x72/0x73] registers. Above setting and count numbers are as follows:

High speed clock counter = {Wakeup timer clock cycle[SLEEP/WU_SET:B0 0x2D(2)] *
Clcok calibration time setting ([CLK_CAL_TIME:B0 0x71(5-0)]) /
{master clock cycle (26MHz) / clock division setting value ([CLK_CAL_SET: B0 0x70(7-4)])}

Clock calibration time is as follows:

Clock calibration time[s] = Wakeup timer clock cycle * Clock calibration time setting

[Example]
Assuming no division in the internal high speed clock, calibration time is set as 10 cycle. Set 1,000 to Wake-up interval timer:

condition: wake-up timer clock frequency = 32.768kHz
detection clock division setting CLK_CAL_DIV[3:0][CLK_CAL_SET: B0 0x70(7-4)] = 0b0000
clock calibration time setting [CLK_CAL_TIME] = 0x0A
wake-up timer interval [WUT_INTERVAL_H/L:B0 0x2F,30] = 0x03E8

Theorical high speed clock count = (1/32.768kHz) * 10 / (1/26MHz)
= 7934(0x1EFE)

If getting [CLK_CAL_H/L:B0 0x72,73] = 0x1E17 (7703)
Counter difference = 7703 - 7934 = -231
Frequency shift = 1/[{1/32.768kHz + (-231) / 10 * 1/26MHz } - 1/32.768kHz] = 0.983 kHz
Then finding wake-up timer clock frequency accuracy is +3% higher. And the compensation vale (C) is calcurared as below:

C= Wake-up timer interval([WUT_INTERVAL_H/L:B0 0x2F,30]) * frequecy shift / 32.768
= 1000 * 0.983kHz / 32.768kHz
=30

Therefore, setting [WUT_INTERVAL_H/L:B0 0x2F,30] = 1000 +30 = 1030 = 0x0406 to achive more accurate inteval timinig.

(Note)
If calibration time is too short or if high speed counter is divided into low speed clock, calibration may not be accurate.

■LSI adjustment items and adjustment method

●PA adjustment

ML7406 has output circuits for 1mW and 20mW (10mW as well).
Output circuits can be selected by PA_MODE[1:0] ([PA_MODE: B0 0x67(5-4)]).

PA_MODE[1:0]	Output circuit
0b00	1mW
0b01	10mW
0b10	20mW
0b11	Not allowed

Output power can be adjusted by the following 3 registers.

Coarse adjustment 1	PA_REG[3:0] ([PA_MODE: B0 0x67(3-0)]) 16 resolutions
Coarse adjustment 2	PA_ADJ[3:0] ([PA_ADJ: B0 0x69(3-0)]) 16 resolutions
Fine adjustment	PA_REG_FINE_ADJ[4:0] ([PA_REG_FINE_ADJ: B0 0x68(4-0)]) 32 resolutions

Coarse adjustment 1: PA regulator voltage adjustment
Setting regulator voltage according to the desired output level.
However, please set PA regulator voltage to less than [VDD_PA(pin#22) – 0.3V].

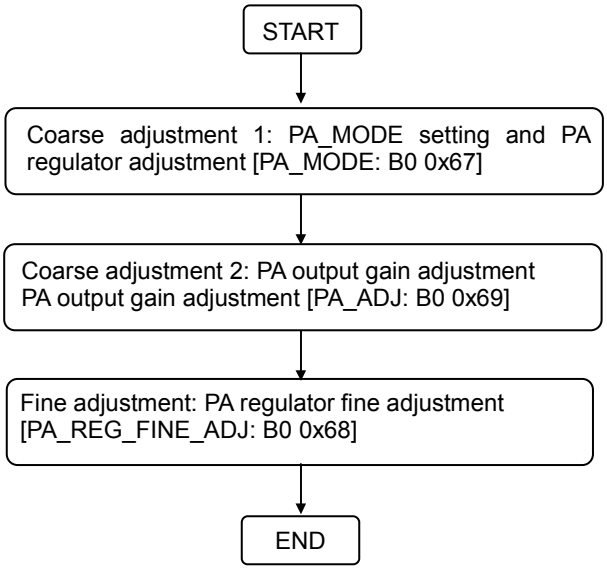
PA_REG[3:0] [PA_MODE:B0 0x67]	PA regulator voltage[V]
0b0000	1.20
0b0001	1.32
0b0010	1.44
0b0011	1.56
0b0100	1.68
0b0101	1.80
0b0110	1.92
0b0111	2.04
0b1000	2.16
0b1001	2.28
0b1010	2.40
0b1011	2.52
0b1100	2.64
0b1101	2.76
0b1110	2.88
0b1111	3.00

Coarse adjustment 2: PA output gain adjustment
Controlling output power by adjusting PA gain. Adjustment steps are 0.4dB to 1.5dB.
[PA_ADJ: B0 0x69]=0x0F: output PA gain maximum.
[PA_ADJ: B0 0x69]=0x00: output gain minimum.

Fine adjustment: PA regulator voltage fine adjustment
Fine tuning output power by adjusting PA regulator voltage. Adjustment step is less than 0.2dB.
[PA_REG_FINE_ADJ B0 0x68]=0x1F: maximum
[PA_REG_FINE_ADJ B0 0x68]=0x00: minimum

(Note)
In order to achieve the most optimized result, Matching circuits may vary depending on the output mode.

○PA output adjustment flow



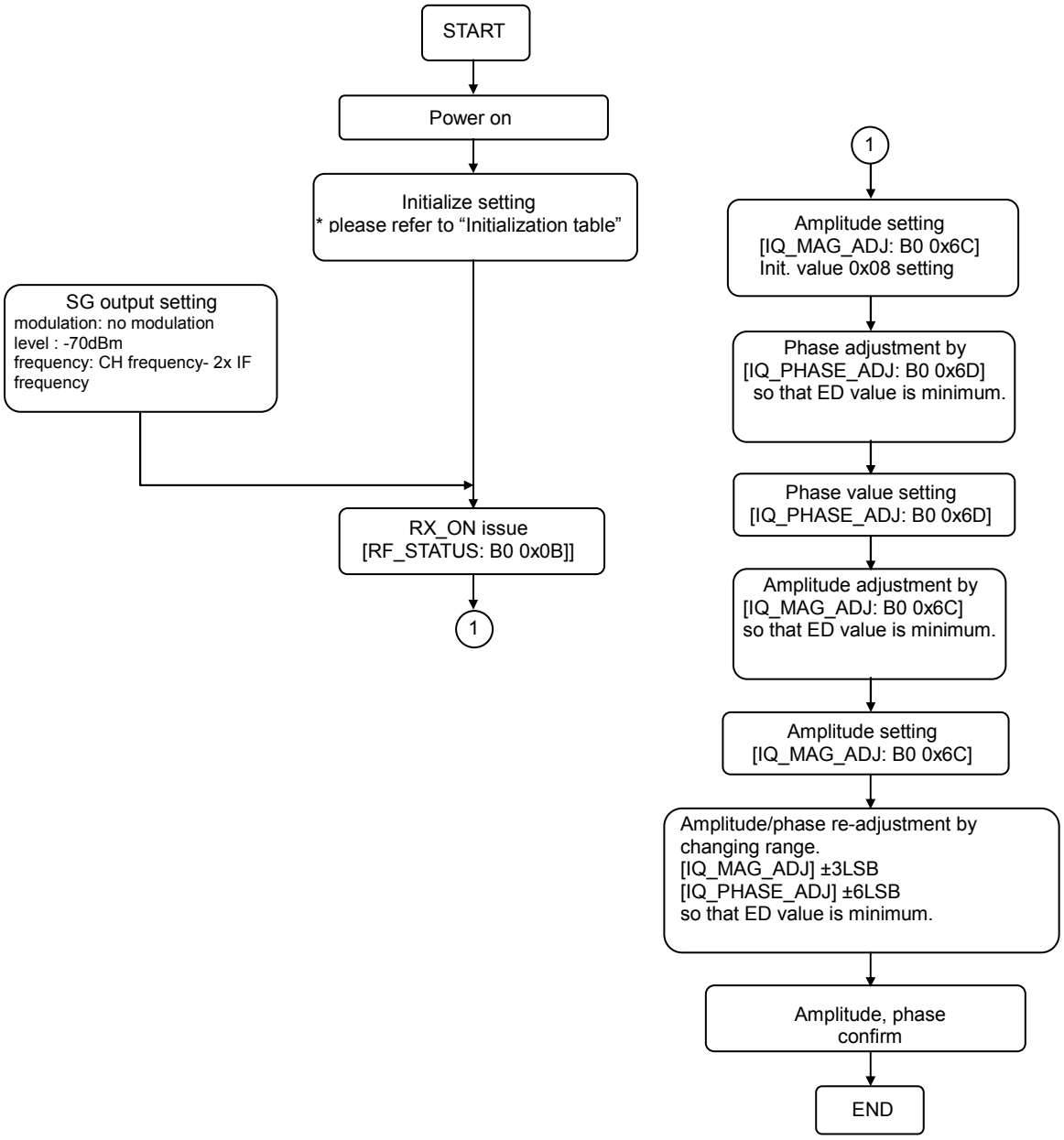
●I/Q adjustment

Image rejection ratio can be adjusted by tuning IQ signal balance. The adjustment procedure is as follows:

1. From SG, image frequency signal is input to ANT pin.
   Input signal source: no modulation.wave
   Input frequency: channel frequency - (2×IF frequency)
   In case of 100kbps, IF frequency = 720kHz: please refer to the “IF frequency setting”.
   Input level: -70dBm

2. Issuing RX_ON by [RF_STATUS:B0 0x7B] register, by adjusting [IQ_MAG_ADJ: B0 0x6C] and [IQ_PHASE_ADJ: B0 0x6D] registers, Finding setting value so that ED value [ED_RSLT: B0 0x3A] is minimum.

○I/Q adjustment flow

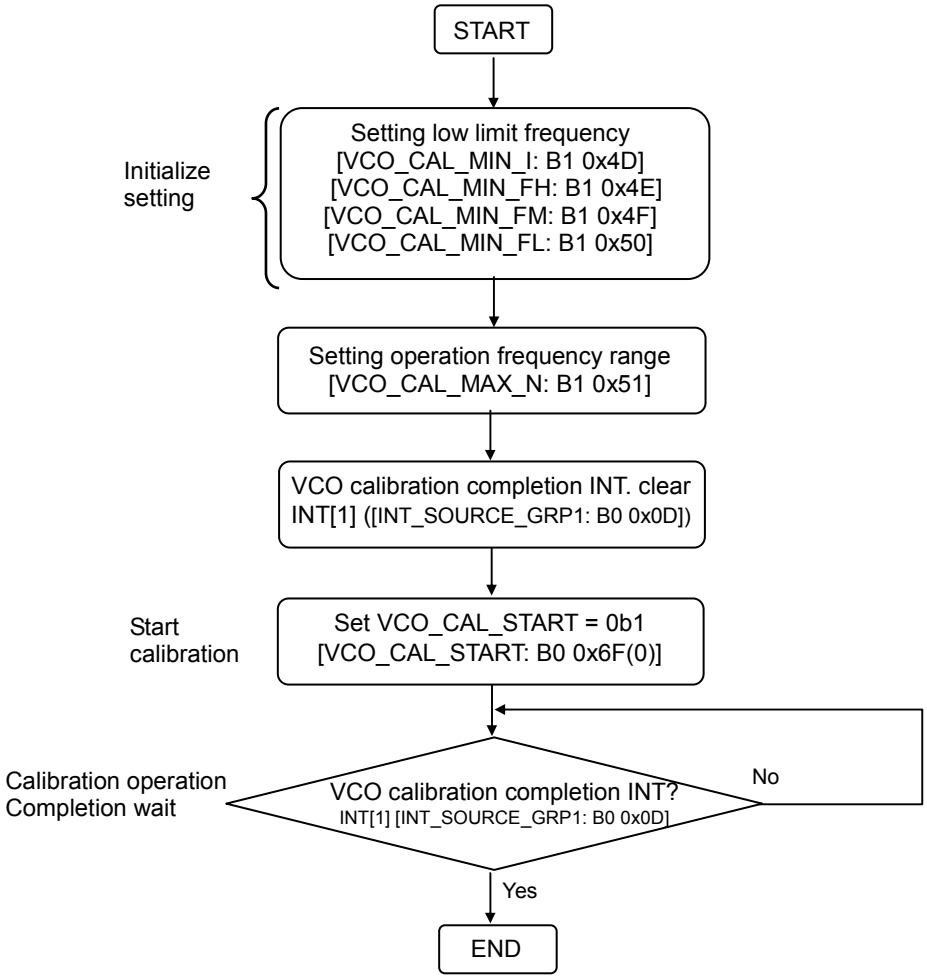


●VCO adjustment

In order to compensate VCO operation margin, optimized capacitance compensation value should be set in each TX/RX operation and frequency. This capacitance compensation value can be acquired by VCO calibration.
By performing VCO calibration when power-up or reset, acquired capacitance compensation values for upper limit and lower limit of operation frequency range (for both TX/RX), based on this value optimised capacitance value is applied during TX/RX operation.

○VCO adjustment flow

The following flow is the procedure for acquiring capacitance compensation value when power-up or reset.



(Note)
VCO calibration should be performed only during IDLE state .

VCO calibration is necessary every 0.6ms to 3.9ms.
After completion, capacitance compensation values are stored in the following registers.
Capacitance compensation value at low limit frequency: [VCAL_MIN: B1 0x52]
Capacitance compensation value at upper limit frequency: [VCAL_MAX: B1 0x53]

In actual operation, based on the 2 compensation values, the most optimized capacitance value for the frequency is calculated and applied. The calculated value is stored in [VCO_CAL: B0 0x6E].

By evaluation stage, if below values are stored in the MCU memory and uses these values upon reset or power-up, calibration operation can be omitted.

Registers to be saved in the MCU memory.
[VCO_CAL_MIN_I: B1 0x4D]
[VCO_CAL_MIN_FH: B1 0x4E]
[VCO_CAL_MIN_FM: B1 0x4F]
[VCO_CAL_MIN_FL: B1 0x50]]
[VCO_CAL_MAX_N: B1 0x51]
[VCAL_MIN: B1 0x52]
[VCAL_MAX: B1 0x53]

(Note)
1. For low limit frequency, please use frequency at least 2.2MHz lower than operation frequency.
2. Upper limit frequency should be selected so that operation frequency is in the frequency range.
3. In case of like a channel change, if the setting frequency is outside of calibration frequency range, calibration has to be performed again with proper frequency.
4. If PLL unlock occures, PLL unlock interrupt (INT[02] group1) will geneate. The following shows the ML7406 opereation related with LSI state and PLL_LD_EN([PLL_LOCK_DETECT:B1 0x0B(7)]) setting, after interrupt generation.

LSI state	check timig of PLL unlock detection	PLL lock detection control setting and ML7406 operation after interrupt generation	
		PLL_LD_EN=0b1 [PLL_LOCK_DETECT:B1 0x0B(7)]	PLL_LD_EN=0b0 [PLL_LOCK_DETECT:B1 0x0B(7)]
TX	PA_ON ="H"	interrupt occurs and TX stops forcibly	interrupt occurs and TX is continued
RX	RX enable ="H"	interrupt occurs and RX is continued	interrupt occurs and RX is continued

○VCO low limit frequency setting

VCO low limit frequency can be set as described in the "channel frequency setting". I is set to [VCO_CAL_MIN_I:B0 0x4D] register, F is set to [VCO_CAL_MIN_FH:B0 0x4E], [VCO_CAL_MIN_FM:B0 0x4F], [VCO_CAL_MIN_FL:B0 0x50] registers in MSB – LSB order.

example) If operation low limit frequency is 870MHz, setting value should be lower than 2.2MHz, Then in following example, low limit frequency is set to 866MHz, master clock frequency is 26MHz.

I = 866MHz/26MHz (Integer part) = 33(0x21)
F =(866MHz/26MHz-33)×2^{20} (Integer part) = 12905550 (0xC4EC4E)

Setting values for each register is as follows:

[VCO_CAL_MIN_I] = 0x21
[VCO_CAL_MIN_FH] = 0xC4
[VCO_CAL_MIN_FM] = 0xEC
[VCO_CAL_MIN_FL] = 0x4E

○VCO upper limit frequency setting

VCO upper limit frequency is calculated as following formula, based on low limit frequency value and VCO_CAL_MAX_N[3:0] ([VCO_CAL_MAX_N: B1 0x51(3-0)]).

VCO calibration upper limit frequency = VCO calibration low limit frequency (B1 0x4E-0x50) + ΔF(B1 0x51)

ΔF is defined in the table below.

VCO_CAL_MAX_N[3:0]	ΔF[MHz]
0b0000	0
0b0001	0.8125
0b0010	1.625
0b0011	3.25
0b0100	6.5
0b0101	13
0b0110	26
0b0111	52
0b1000	82.875
0b1001	104
Other than above	prohibited

●Energy detection value (ED value) adjustment

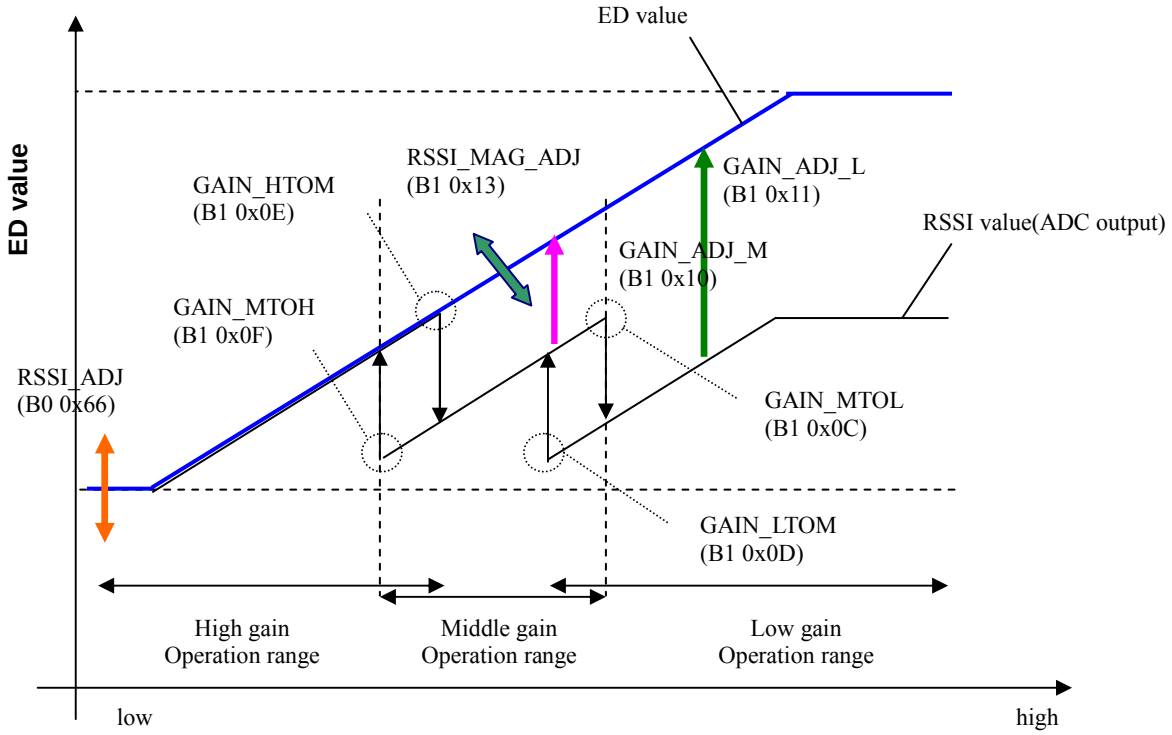
[ED value adjustment]

ED value is calculated by RSSI signal (analog signal) from RF part,. By performing the following adjustment, it is possible to correct the variation in LSIs.

The gain adjustment and related registers are described below.

In order to cover wider input range, gain should be changed at given point. Threshold for gain change points are set to [GAIN_LTOM: B1 0x0C], [GAIN_MTOH: B1 0x0F]. [GAIN_ADJ_M: B1 0x10] and [GAIN_ADJ_L: B1 0x11] registers are used to addition values to maintain linearity when changing gain. RSSI slope can be set to [RSSI_MAG_ADJ: B1 0x13] register so that ED value can be between 0x00(min) and 0xFF(max). Please set to these registers based on the "Initialization table", do not change the setting for these registers for tuning.

Adjusting the input level variation for the same input level can be set to [RSSI_ADJ: B0 0x66] register. It must compensate the slope before compensation defined by [RSSI_MAG_ADJ:B0 0x13] register. However, if positive value is set , ED value cannot be decreased down to 0x00 at low input signal level. If negative value is set, ED value cannot be increased up to 0xFF.



Operation in the High gain range:	RSSI value>GAIN_HtoM, and move to Middle gain.
Operation in the Middle gain range:	RSSI value>GAIN_MtoL, and move to Low gain.
	GAIN_MtoH≥RSSI value, and move to High gain.
Operation in the Low gain range:	GAIN_LtoM≥RSSIvalue, and move to Middle gain.

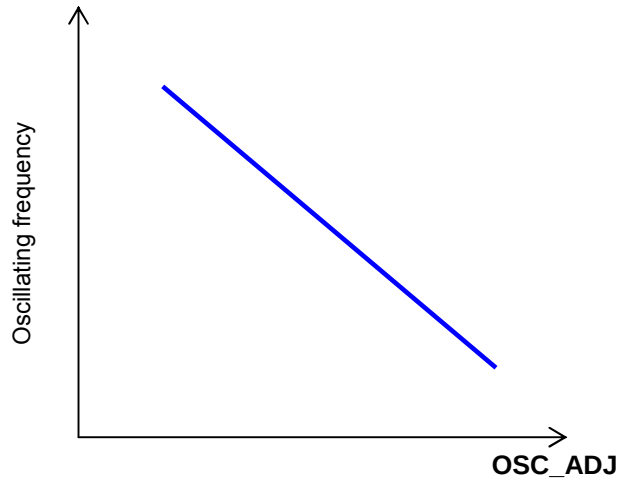
●Oscillation circuit adjustment

In case of using a crystal oscillator (ML7406C), crystal oscillator frequency deviation can be tuned by adjusting load capacitance of XIN pin (pin#5) and XOUT pin (pin #6). Load capacitance can be adjusted by [OSC_ADJ1: B0 0x62] and [OSC_ADJ2: B0 0x63].

Adjustable capacitance is as follows:

[OSC_ADJ1] Coarse adjustment of load capacitance: **0.7pF/step (setting range: 0x00 to 0x0F)**

[OSC_ADJ2] Fine adjustment of load capacitance: **0.02pF/step (setteing range: 0x00 to 0x77)**



■Registers

●Registers map

Addressing range for each register BANK are 0x00-0x7F(128 bytes). Grey colours in the table are unused bits or reserved bits . Please use the initial setting value, as reserved bits may be used for functions not open to the customers. It may cause unexpected operation.

Each BANK can be selected by [BANK_SEL] register (B0 0x00, B1 0x00, B2 0x00, B3 0x00), enabling each bank in bit7-4 (B*_ACEN) and specified BANK number to bit3-0.

If registers value is specified in the description, do not change.

BANK0

address [HEX]	Register name	description	bit							
			7	6	5	4	3	2	1	0
00	BANK_SEL	Register access bank selection								
01	RST_SET	Software reset setting								
02	CLK_SET1	Clock cofiguration 1								
03	CLK_SET2	Clock configuration 2								
04	PKT_CTRL1	Packet configuration 1								
05	PKT_CTRL2	Packet configuration 2								
06	DRATE_SET	Data rate setting								
07	DATA_SET1	TX/RX data configulation 1								
08	DATA_SET2	TX/RX data configulation 2								
09	CH_SET	RF channel setting								
0A	RF_STATUS_CTRL	RFauto status transition control								
0B	RF_STATUS	RFstate setting and status indication								
0C	DIO_SET	DIO mode configuration								
0D	INT_SOURCE_GRP1	Interrupt status for INT0 to INT7								
0E	INT_SOURCE_GRP2	Interrupt status for INT8 to INT15 (RX)								
0F	INT_SOURCE_GRP3	Interrupt statsu for INT16 to INT23 (TX)								
10	INT_EN_GRP1	Interrupt mask for INT0 to INT7								
11	INT_EN_GRP2	Interrupt mask for INT8 to INT15								
12	INT_EN_GRP3	Interrupt mask for INT16 to INT23								
13	CRC_ERR_H	CRC error status (high byte)								
14	CRC_ERR_M	CRC error status (middle byte)								
15	CRC_ERR_L	CRC error status (low byte)								
16	STATE_CLR	State clear control								
17	TXFIFO_THRH	TX FIFO-Full level setting								
18	TXFIFO_THRL	TX FIFO-Emptythreshold, FAST_TXenable thresold								
19	RXFIFO_THRH	RX FIFO-Full thresold								
1A	RXFIFO_THRL	RX FIFO-Empty threshold								
1B	C__CHECK_CTRL	Control field (C-field) detection setting								
1C	M__CHECK_CTRL	Manufactute ID field (M-field) detection setting								
1D	A__CHECK_CTRL	Address field (A-field) detection setting								
1E	C_FIELD_CODE1	C-field setting code #1								
1F	C_FIELD_CODE2	C-field setting code #2								
20	C_FIELD_CODE3	C-field setting code #3								
21	C_FIELD_CODE4	C-field setting code #4								
22	C_FIELD_CODE5	C-field setting code #5								
23	M_FIELD_CODE1	M-field 1st byte setting code #1								
24	M_FIELD_CODE2	M-field 1st byte setting code #2								
25	M_FIELD_CODE3	M-field 2nd byte setting code #1								
26	M_FIELD_CODE4	M-field 2nd byte setting code #2								
27	A_FIELD_CODE1	A-field 1st byte setting								
28	A_FIELD_CODE2	A-field 2nd byte setting								
29	A_FIELD_CODE3	A-field 3rd byte setting								
2A	A_FIELD_CODE4	A-field 4th byte setting								
2B	A_FIELD_CODE5	A-field 5th byte setting								
2C	A_FIELD_CODE6	A-field 6th byte setting								
2D	SLEEP/WU_SET	SLEEP execution and Wake-up operation setting								
2E	WUT_CLK_SET	Wake-up timer clock division setting								
2F	WUT_INTERVAL_H	Wake-up timer interval setting (high byte)								
30	WUT_INTERVAL_L	Wake-up timer interval setting (low byte)								
31	RX_DURATION	Continue operation timer (after Wake-up) setting								
32	GT_SET	General purpose timer configuration								
33	GT_CLK_SET	General purposetimer clock division setting								
34	GT1_TIMER	General purpose timer #1 setting								
35	GT2_TIMER	General purpose timer #2 setting								

address [HEX]	Register name	description	bit							
			7	6	5	4	3	2	1	0
36	CCA_IGNORE_LVL	ED threshold level setting for excluding CCA judgement								
37	CCA_LVL	CCA threshold level setting								
38	CCA_ABORT	Timing setting for forced termination of CCA operation								
39	CCA_CTRL	CCA control setting and result indication								
3A	ED_RSLT	ED value indication								
3B	IDLE_WAIT_H	IDLE detection period setting during CCA (high 2 bits)								
3C	IDLE_WAIT_L	IDLE detection period setting during CCA (low byte)								
3D	CCA_PROG_H	IDLE detection elapsed time display (during CCA high byte)								
3E	CCA_PROG_L	IDLE detection elapsed time display during CCA(low byte) I								
3F-40	Reserved									
41	ED_CTRL	ED detection control setting								
42	TXPR_LEN_H	TX preamble length setting (high byte)								
43	TXPR_LEN_L	TX preamblelength setting (low byte)								
44	POSTAMBLE_SET	Postamble length and pattern setting								
45	SYNC_CONDITION1	RX preamble setting and ED control setting								
46	SYNC_CONDITION2	ED threshold setting during synchronization								
47	SYNC_CONDITION3	Tolerance of bit error setting in RX preamble and SyncWord detection								
48	2DIV_CTRL	Antenna diversity setting								
49	2DIV_RSLT	Antenna diversity result								
4A	ANT1_ED	ANT1 ED value during antenna diversity								
4B	ANT2_ED	ANT2 ED value during antenna diversity								
4C	ANT_CTRL	Antenna control setting for TX, CCA or RX								
4D	MON_CTRL	Monitor function setting								
4E	GPIO0_CTRL	GPIO0 pin (pin#16) configuration setting								
4F	GPIO1_CTRL	GPIO1 pin (pin#17) configuration setting								
50	GPIO2_CTRL	GPIO2 pin (pin#18) configuration setting								
51	GPIO3_CTRL	GPIO3 pin (pin#19) configuration setting								
52	EXTCLK_CTRL	EXT_CLK pin (pin #10) control setting								
53	SPI/EXT_PA_CTRL	SPI interface IO configurattion /external PA control setting								
54	IF_FREQ_H	IF frequency setting (high byte)								
55	IF_FREQ_L	IF frequency setting (low byte)								
56	IF_FREQ_CCA_H	IF frequency setting during CCA operation (high byte)								
57	IF_FREQ_CCA_L	IF frequency setting during CCA operation (low byte)								
58	BPF_ADJ_H	Bandpass filter capacitance adjustment (high 2 bits)								
59	BPF_ADJ_L	Bandpass filter capacitance adjustment (low byte)								
5A-5B	Reserved									
5C	BPF_CO	BPF coefficient								
5D	BPF_CO_CCA	BPFcoefficient (CCA)								
5E	IFF_ADJ_H	Demodulator DC level adjustment (high 2 bits)								
5F	IFF_ADJ_L	Demodulator DC level adjustment (low byte)								
60	IFF_ADJ_CCA_H	Demodulator DC level adjustment during CCA (high 7 bits)								
61	IFF_ADJ_CCA_L	Demodulator DC level adjustment during CCA (low byte)								
62	OSC_ADJ1	Coarse adjustment of load capacito for oscillation circuits								
63	OSC_ADJ2	Fine adjustment of load capaciatnce for oscillation circuits								
64	OSC_ADJ3	Oscillation circuits bias adjustment								
65	OSC_ADJ4	Oscillation circuits bias adjustment (high speed start-up)								
66	RSSI_ADJ	RSSI value adjustment								
67	PA_MODE	PA mode setting/PA regulator coarse adjustment								
68	PA_REG_FINE_ADJ	PA regulator fine adjustment								
69	PA_ADJ	PA gain adjustment								
6A	Reserved									
6B	Reserved									
6C	IQ_MAG_ADJ	IF I/Q amplitude balance adjustment								
6D	IQ_PHASE_ADJ	IF I/Q phase balance adjustment								

address [HEX]	Register name	description	bit							
			7	6	5	4	3	2	1	0
6E	VCO_CAL	VCO calibration setting or status indicarion								
6F	VCO_CAL_START	VCO calibration execution								
70	CLK_CAL_SET	Clock calibration setting								
71	CLK_CAL_TIME	Clock calibration time setting								
72	CLK_CAL_H	Clock calibration value readout (high byte)								
73	CLK_CAL_L	Clock calibration value readout (low byte)								
74	Reserved									
75	SLEEP_INT_CLR	Interrupt clear setting during SLEEP state								
76	RF_TEST_MODE	TX test pattern setting								
77	STM_STATE	Sate machine status and synchronization status indication								
78	FIFO_SET	FIFO readout setting								
79	RD_FIFO_LAST	RX FIFO data usage status indication								
7A	TX_PKT_LEN_H	TX packet length setting (high byte)								
7B	TX_PKT_LEN_L	TX packet length setting (low byte)								
7C	WR_TX_FIFO	TX FIFO								
7D	RX_PKT_LEN_H	RX packet length indication (high byte)								
7E	RX_PKT_LEN_L	RX packet length indication (low byte)								
7F	RD_FIFO	FIFO read								

BANK1

address [HEX]	Register name	description	bit							
			7	6	5	4	3	2	1	0
00	BANK_SEL	BANK selection								
01	CLK_OUT	CLK_OUT (GPIOn) output frequency setting								
02	TX_RATE_H	TX data rate conversion setting (high 4 bits)								
03	TX_RATE_L	TX data rate conversion setting (low byte)								
04	RX_RATE1_H	RX data rate conversion setting1 (high 4 bits)								
05	RX_RATE1_L	RX data rate conversion setting1 (low byte)								
06	RX_RATE2	RX data rate conversion setting2								
07	Reserved									
08	ADC_CLK_SET	RSSI ADC clock frequency setting								
09	TEMP	Temperature digital value indication								
0A	Reserved									
0B	PLL_LOCK_DETECT	PLL lock detection setting								
0C	GAIN_MTOL	Threshold level setting for switching middle gain to low gain								
0D	GAIN_LTOM	Threshold level setting for switching low gain to middle gain								
0E	GAIN_HTOM	Threshold level setting for switching high gain to middle gain								
0F	GAIN_MTOH	Threshold level setting for switching middle gain to high gain								
10	RSSI_ADJ_M	RSSI offset value setting during middle gain opoeration								
11	RSSI_ADJ_L	RSSI offset value setting during low gain operation								
12	RSSI_STABLE_TIME	RSSI stabilization wait time setting								
13	RSSI_MAG_ADJ	Scale factor setting for ED value conversion								
14	RSSI_VAL	RSSI value indication								
15	AFC/GC_CTRL	AFCcontrol/gain controlmode setting								
16	CRC_POLY3	CRC polynomial setting 3								
17	CRC_POLY2	CRC polynomial setting 2								
18	CRC_POLY1	CRC polynomial setting 1								
19	CRC_POLY0	CRC polynomial setting 0								
1A	Reserved									
1B	TXFREQ_I	TX frequency setting (I counter)								
1C	TXFREQ_FH	TX frequency setting (F counter high 4bit)								
1D	TXFREQ_FM	TX frequency setting (F counter middle byte)								
1E	TXFREQ_FL	TX frequency setting (F counter low byte)								
1F	RXFREQ_I	RX frequency setting (I counter)								
20	RXFREQ_FH	RX frequency setting (F counter high 4bit)								
21	RXFREQ_FM	RX frequency setting (F counter middle byte)								
22	RXFREQ_FL	RX frequency setting (F counter low byte)								
23	CH_SPACE_H	Channel space setting (high byte)								
24	CH_SPACE_L	Channel space setting (low byte)								
25	SYNC_WORD_LEN	SyncWord lenght setting								
26	SYNC_WORD_EN	SyncWord enable setting								
27	SYNCWORD1_SET0	SyncWord #1 setting (bit24-31)								
28	SYNCWORD1_SET1	SyncWord #1 setting (bit16-23)								
29	SYNCWORD1_SET2	SyncWord #1 setting (bit8-15)								
2A	SYNCWORD1_SET3	SyncWord #1 setting (bit0-7)								
2B	SYNCWORD2_SET0	SyncWord #2 setting (bit24-31)								
2C	SYNCWORD2_SET1	SyncWord #2 setting (bit16-23)								
2D	SYNCWORD2_SET2	SyncWord #2 setting (bit8-15)								
2E	SYNCWORD2_SET3	SyncWord #2 setting (bit0-7)								
2F	FSK_CTRL	GFSK/FSK mudulation timing resolution setting								
30	GFSK_DEV_H	GFSK frequency deviation setting (high 6 bits)								
31	GFSK_DEV_L	GFSK frequency deviation setting (low byte)								
32	FSK_DEV0_H/GFIL0	FSK 1st frequency deviation setting (high 6 bits) / Gaussian filter coefficient setting 0								
33	FSK_DEV0_L/GFIL1	FSK 1st frequency deviation setting (low byte) / Gaussian filter coefficient setting 1								
34	FSK_DEV1_H/GFIL2	FSK 2nd frequency deviation setting (high 6 bits) / Gaussian filter coefficient setting 2								

BANK1(continue)

address [HEX]	Register name	description	bit							
			7	6	5	4	3	2	1	0
35	FSK_DEV1_L/GFIL3	FSK 2nd frequency deviation setting (low byte) / Gaussian filter coefficient setting 3								
36	FSK_DEV2_H/GFIL4	FSK 3rd frequency deviation setting (high 6 bits) / Gaussian filter coefficient setting 4								
37	FSK_DEV2_L/GFIL5	FSK 3rd frequency deviation setting (low byte) / Gaussian filter coefficient setting 5								
38	FSK_DEV3_H/GFIL6	FSK 4th frequency deviation setting (high 6 bits) / Gaussian filter coefficient setting 6								
39	FSK_DEV3_L	FSK 4th frequency deviation setting (low byte)								
3A	FSK_DEV4_H	FSK 5th frequency deviation setting (high 6 bits)								
3B	FSK_DEV4_L	FSK 5th frequency deviation setting (low byte)								
3C	FSK_TIM_ADJ4	FSK 4th frequency deviation hold timing seting								
3D	FSK_TIM_ADJ3	FSK 3rd frequency deviation hold timing seting								
3E	FSK_TIM_ADJ2	FSK 2nd frequency deviation hold timing seting								
3F	FSK_TIM_ADJ1	FSK 1st frequency deviation hold timing seting								
40	FSK_TIM_ADJ0	FSK no-deviation frequency (carrier frequency) hold timing seting								
41-47	Reserved									
48	2DIV_MODE	Antenna diversity mode setting								
49	2DIV_SEARCH1	Antenna diversity search time setting 1								
4A	2DIV_SEARCH2	Antenna diversity search time setting 2								
4B	2DIV_FAST_LVL	ED threshold setting during Antenna diversity FAST mode								
4C	Reserved									
4D	VCO_CAL_MIN_I	VCO Calibration low limit frequency setting (I counter)								
4E	VCO_CAL_MIN_FH	VCO Calibration low limit frequency setting (F counter high 4 bits)								
4F	VCO_CAL_MIN_FM	VCO Calibration low limit frequency setting (F counter middle byte)								
50	VCO_CAL_MIN_FL	VCO Calibration low limit frequency setting (F counter low byte)								
51	VCO_CAL_MAX_N	VCO_CAL Max frequency setting								
52	VCAL_MIN	VCO calibration low limit value indication and setting								
53	VCAL_MAX	VCO calibration upper limit value indication and setting								
54-55	Reserved									
56	DEMOD_SET0	Demodulator configulation 0								
57	DEMOD_SET1	Demodulator configulation 1								
58	DEMOD_SET2	Demodulator configulation 2								
59	DEMOD_SET3	Demodulator configulation 3								
5A	DEMOD_SET4	Demodulator configulation 4								
5B	DEMOD_SET5	Demodulator configulation 5								
5C	DEMOD_SET6	Demodulator configulation 6								
5D	DEMOD_SET7	Demodulator configulation 7								
5E	DEMOD_SET8	Demodulator configulation 8								
5F	DEMOD_SET9	Demodulator configulation 9								
60	DEMOD_SET10	Demodulator configulation 10								
61	DEMOD_SET11	Demodulator configulation 11								
62	ADDR_CHK_CTR_H	Address check counter indication (high 3 bit)								
63	ADDR_CHK_CTR_L	Address check counter indication (low byte)								
64	WHT_INIT_H	Whitening initializing state setting (high 1bit)								
65	WHT_INIT_L	Whiteningi initializing state setting (low 8bit)								
66	WHT_CFG	Whitening polynomial generation setting								
67-7E	Reserved									
7F	ID_CODE	ID code indication								

BANK2

address [HEX]	Register name	description	bit							
			7	6	5	4	3	2	1	0
00	BANK_SEL	BANK selection								
7E	CCA_MASK_SET	Filter stabilization setting during CCA								

BANK3

address [HEX]	Register name	description	bit							
			7	6	5	4	3	2	1	0
00	BANK_SEL	BANK selection								
23	2MODE_DET	2 modes detection setting (MODE-T and MODE-C)								

(Note)

1. Other registers are closed register and access is limited. Accessible registers are written in the “initialization table”.calibration operation, do not access BANK1 registers.

■Application circuits example

The below diagram does not show decoupling capacitors for LSI power pins.
10uF decoupling capacitor should be placed to common 3.3V power pins .
MURATA LQW15series inductors are recommended.

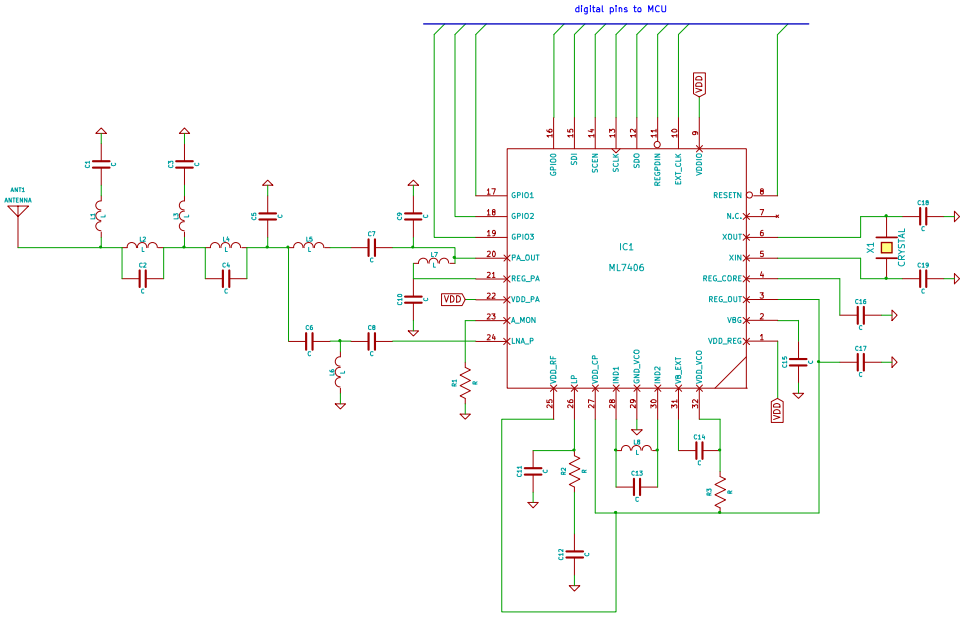


Figure.Direct-Tie exmaple

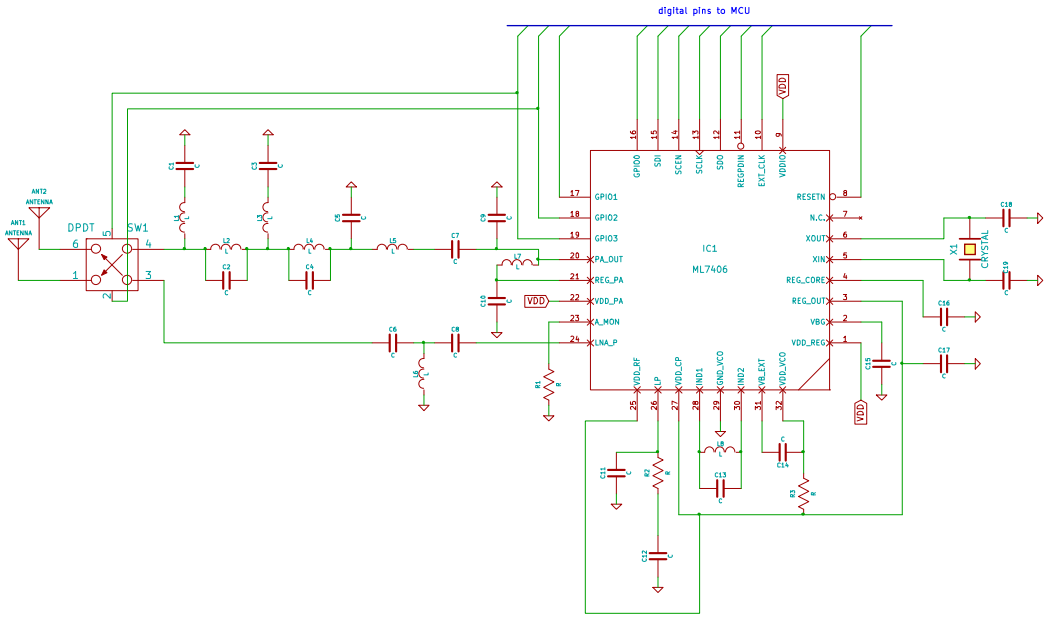
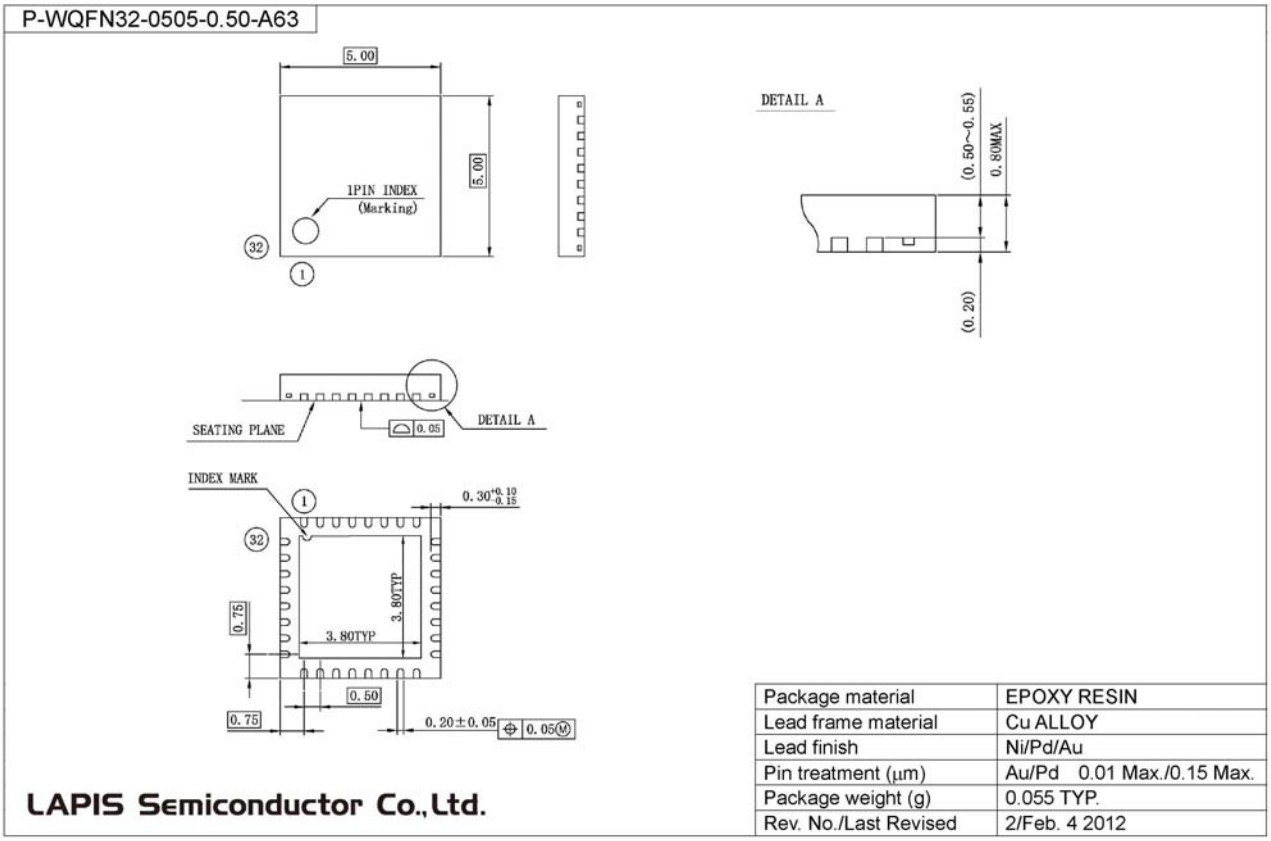


Figure. Diversity exmaple

■Package Dimensions



Package material	EPOXY RESIN
Lead frame material	Cu ALLOY
Lead finish	Ni/Pd/Au
Pin treatment (μm)	Au/Pd 0.01 Max./0.15 Max.
Package weight (g)	0.055 TYP.
Rev. No./Last Revised	2/Feb. 4 2012

Remarks for surface mount type package

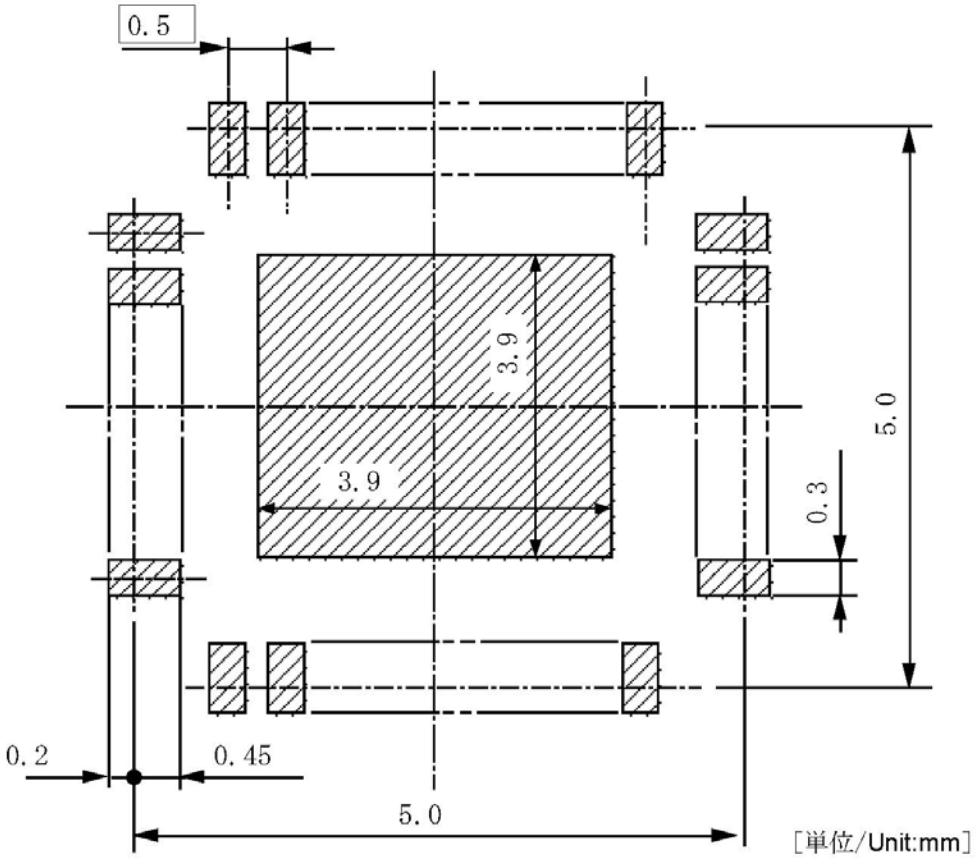
Surface mount type package is very sensitive affected by heating from reflow process, humidity during storaging Therefore, in case of reflow mouting process, please contact sales representative about product name, package name, number of pin, package code and required reflow process condition (reflow method, temperature, number of reflow process), storage condition.

■Footprint Pattern (Recommendation)

When laying out PC boards, it is important to design the foot pattern so as to give consideration to ease of mounting, bonding, positioning of parts, reliability, wiring, and elimination of slder bridges.

The optimum design for the foot pattern varies with the materials of the substrate, the sort and thichness of used soldering paste, and the way of soldering. Therefore when laying out the foot pattern on the PC boards, refer to this figure which mean the mounting area that the package leads are allowable for soldering PC boards.

P-WQFN32-0505-0.50-A63



■Revision History

Document No.	Release data	page		Revision description
		Before revision	After revision	
PEDL7406-01	Sep 14, 2012	-	-	Preliminary version
FJDL7406-01	June 12, 2013	-	-	Initial release
FJDL7406-02	July 9, 2013	-	-	2nd revision

(Note) Corrections in spelling , improvements in the description are not included in the Revision history.

NOTES

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