AN2836
Application note

L6225, L6226, L6227 dual full-bridge drivers

1 Introduction

Modern motion control applications need more flexibility that can be addressed only with specialized IC products. The L6225, L6226, L6227 are dual full-bridge driver ICs specifically developed to drive a wide range of motors. These ICs are one-chip, cost-effective solutions that include several unique circuit design features. These features allow the devices to be used in many applications including DC and stepper motor driving. The principal aim of this development project was to produce easy-to-use, fully-protected power ICs. In addition several key functions such as protection circuit and PWM current control drastically reduce the number of external components to meet requirements for many different applications.

The L6225, L6226, L6227 are highly integrated, mixed-signal power ICs that allow the user to easily design a control system for two-phase bipolar stepper motors, multiple DC motors and a wide range of inductive loads. *Figure 1* to *Figure 3* show the block diagrams of the L6225, L6226, L6227 . Each IC integrates eight power DMOS plus other added features for safe operation and flexibility. The L6227 also features a constant tOFF PWM current control technique (synchronous mode) for each of the two full bridges

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2 References

1. "A New Fully Integrated Stepper Motor Driver IC", Proceedings of PCIM 2001, September 2001, Intertech Communication
2. "Stepper Motor Driving" (AN235)
3. "Controlling Voltage Transients in Full bridge Driver Applications" (AN280)
4. "A New High Power IC Surface Mount Package Family" (AN668)
5. "L6205, L6206, L6207 dual full bridge drivers" (AN1762).

3 Main differences between L6225, L6226, L6227

The L6225, L6226 and L6227 are DMOS dual full-bridge ICs.

The L6225 (see *Figure 1*) includes logic for CMOS/TTL interface, a charge pump that provides auxiliary voltage to drive the high-side DMOS, non-dissipative overcurrent protection circuitry on the high-side DMOS, with a fixed trip point set at 2.8 A (see *Section 4.13*), overtemperature protection, undervoltage lockout for reliable startup.

In addition, the L6226 (see *Figure 2*) gives the possibility of adjusting the trip point of the overcurrent protection for each of the two full bridges (through two external resistors), and its internal open-drain MOSFETs (see *Section 4.13*) are not internally connected to EN pins but to separate OCD pins, allowing easier external diagnostics and overcurrent management.

The L6227 (see *Figure 3*) has an overcurrent protection function with a fixed trip point set at 2.8 A and internal open-drain MOSFETs connected to EN pins, as the L6225, but it also integrates two PWM current controllers for each of the two full bridges (see *Section 4.11*).

Figure 1. L6225 block diagram

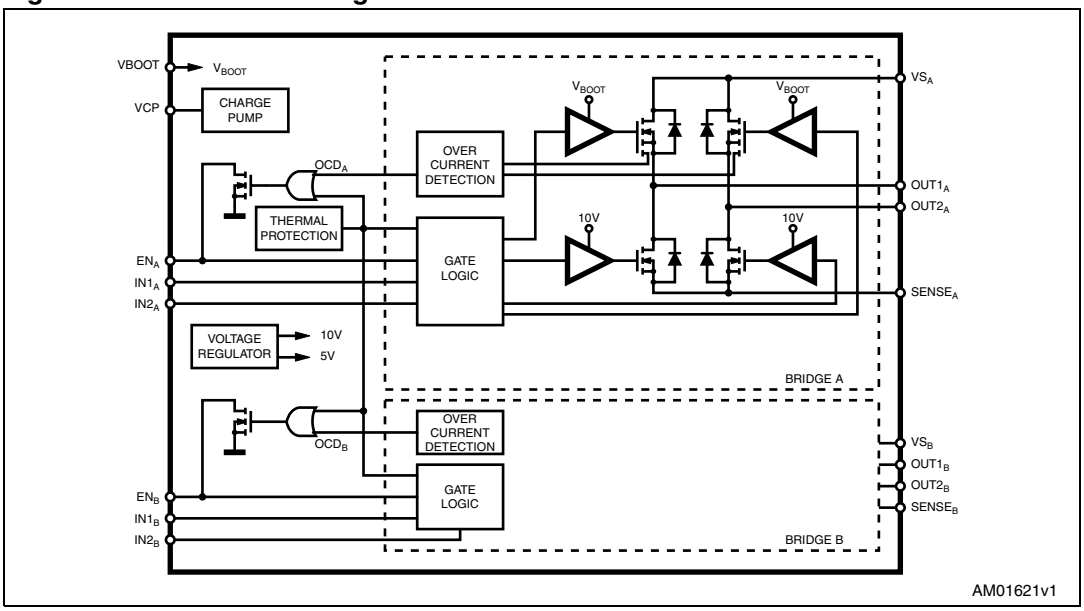


Figure 2. L6226 block diagram

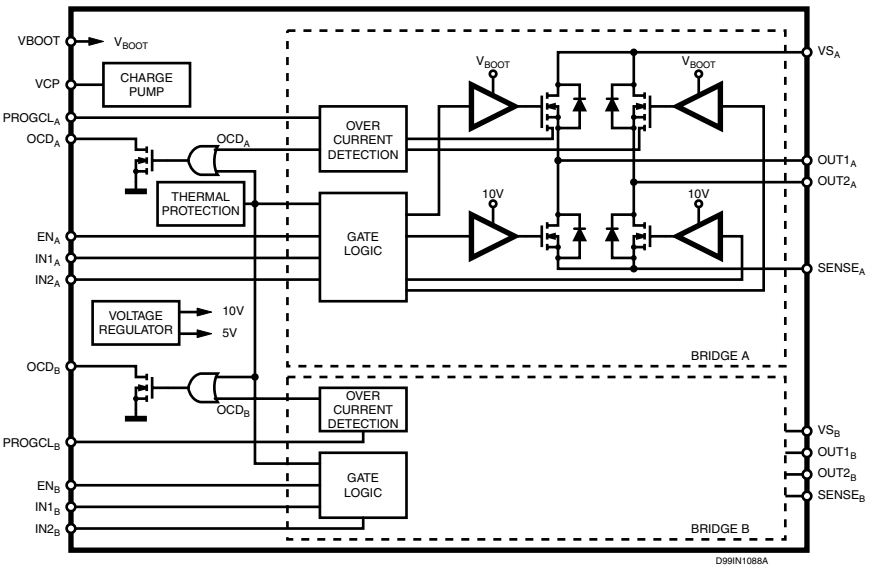
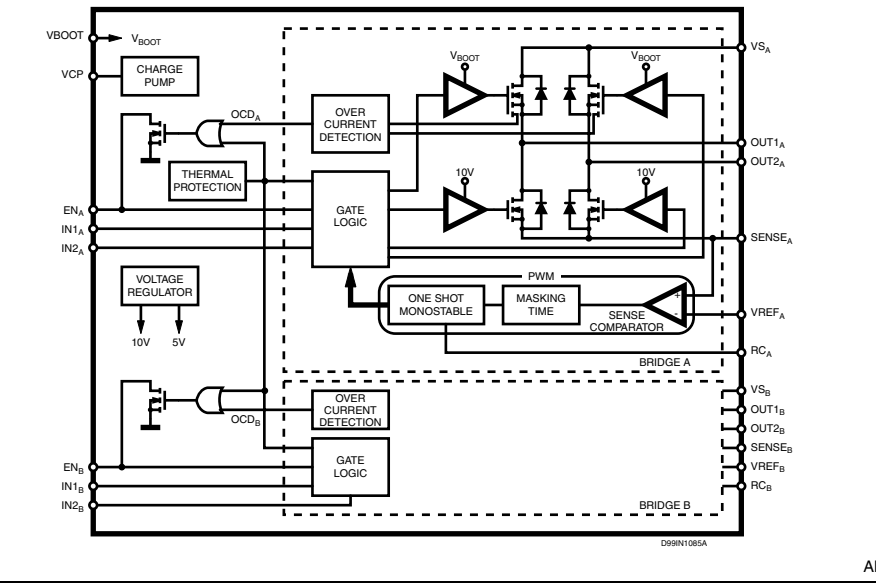


Figure 3. L6227 block diagram



4 Designing an application with L6225, L6226, L6227

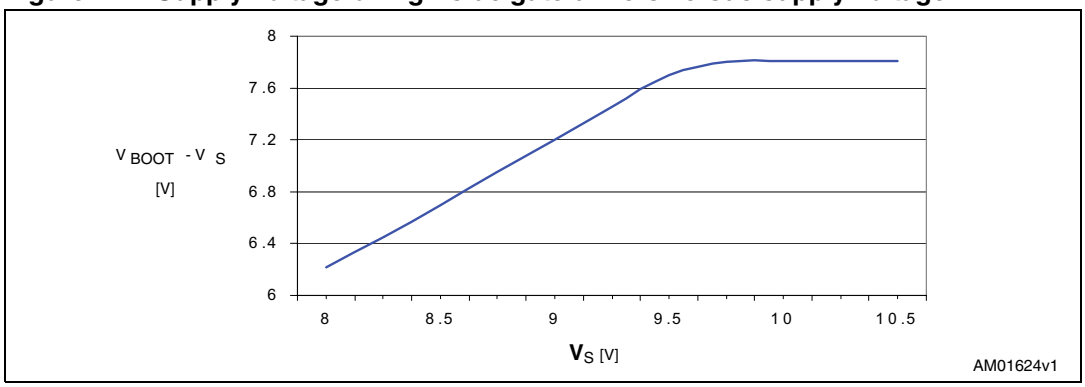
4.1 Current ratings

With MOSFET (DMOS) devices, unlike bipolar transistors, current under short-circuit conditions is, at first approximation, limited by the $R_{DS(on)}$ of the DMOS themselves and could reach very high values. L6225, L6226, L6227 OUT pins and the two V_{SA} and V_{SB} pins are rated for a maximum of 1.4 Arms and 2.8 A peak (typical values), corresponding to a total (for the whole IC) 2.8 Arms (5.6 A peak). These values are meant to avoid damaging metal structures, including the metallization on the die and bond wires. In practical applications, though, maximum allowable current is less than these values, due to power dissipation limits (see *Section 4.16*). The devices have a built-in overcurrent detection (OCD) that provides protection against short circuits between the outputs and between an output and ground (see *Section 4.13*).

4.2 Voltage ratings and operating range

The L6225, L6226, L6227 require a single supply voltage (V_S), for the motor supply. Internal voltage regulators provide the 5 V and 10 V required for the internal circuitry. The operating range for V_S is 8 to 52 V. To prevent working from an undesirable low supply voltage an undervoltage lockout (UVLO) circuit shuts down the device when the supply voltage falls below 5.5 V. To resume normal operating conditions, V_S must then exceed 6.3 V. The hysteresis is provided to avoid false intervention of the UVLO function during fast V_S ringings. It should be noted, however, that $R_{DS(on)}$ of the DMOS is a function of the V_S supply voltage. Actually, when V_S is less than 10 V, $R_{DS(on)}$ is adversely affected, and this is particularly true for the high-side DMOS that are driven from V_{BOOT} supply. This supply is obtained through a charge pump from the internal 10 V supply, which tends to reduce its output voltage when V_S goes below 10 V. *Figure 4* shows the supply voltage of the high-side gate drivers (V_{BOOT} - V_S) versus the supply voltage (V_S).

Figure 4. Supply voltage of high-side gate drivers versus supply voltage



Note that V_S must be connected to both V_{SA} and V_{SB} since the bootstrap voltage (at V_{BOOT} pin) is the same for the two H-bridges. The integrated DMOS have a rated drain-source breakdown voltage of 60 V. However V_S should be kept below 52 V, since in normal working conditions the DMOS see a V_{ds} voltage that exceeds V_S supply. In particular, during a phase change (when each output of the same H-bridge switches from V_S to GND or vice versa, for example to reverse the current in the load) at the beginning of the deadtime (when all the DMOS are off) the SENSE pin sees a negative spike due to a non-negligible parasitic

inductance of the PCB path from the pin to GND. This spike is followed by a stable negative voltage due to the drop on R_{SENSE}. One of the two OUT pins of the bridge sees a similar behavior, but with a slightly larger voltage due to the forward recovery time of the integrated freewheeling diode and the forward voltage drop across it (see *Figure 5*). Typical duration of this spike is 30 ns. At the same time, the other OUT pin of the same bridge sees a voltage above V_S, due to the PCB inductance and voltage drop across the high-side (integrated) freewheeling diode, as the current reverses direction and flows into the bulk capacitor. It turns out that the highest differential voltage can be observed between the two OUT pins of the same bridge, during the deadtime at a phase change, and this must always be kept below 60 V [*3*].

Figure 5. Currents and voltages during the deadtime at a phase change

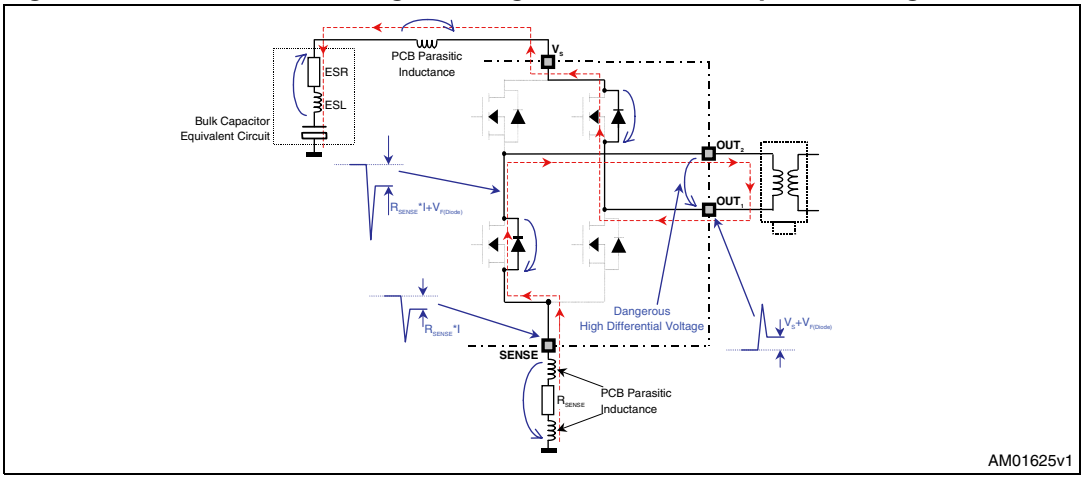
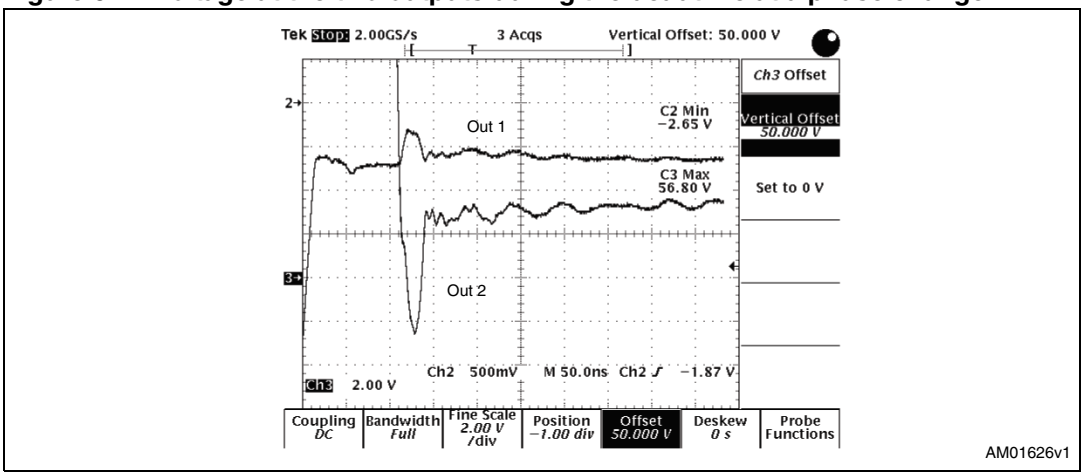


Figure 6 shows the voltage waveforms at the two OUT pins referring to an application, with a peak output current of 1.4 A, V_S = 52 V, R_{SENSE} = 0.33 Ω, T_J = 25 °C (approximately) and a good PCB layout. Below ground spike amplitude is –2.65 V for one output, the other OUT pin is at about 57 V. In these conditions, total differential voltage reaches almost 60 V, which is the absolute maximum rating for the DMOS. Keeping differential voltage between two output pins belonging to the same full bridge within rated values is a must that can be accomplished with proper selection of bulk capacitor value and equivalent series resistance (ESR), according to current peaks and chopping style and adopting good layout practices to minimize PCB parasitic inductances (see below) [*3*].

Figure 6. Voltage at the two outputs during the deadtime at a phase change



4.3 Choosing the bulk capacitor

Since the bulk capacitor, placed between V_S and GND pins, is charged and discharged during the IC operation, its AC current capability must be greater than the RMS value of the charge/discharge current. In case of PWM current regulation, the current flows from the capacitor to the IC during the on-time (t_{ON}) and from the IC (implementing a fast decay current recirculation technique) or from the power supply (implementing a slow decay current recirculation technique) to the capacitor during the off-time (t_{OFF}). The RMS value of the current flowing into the bulk capacitor depends on peak output current, output current ripple, switching frequency, duty cycle and chopping style. It also depends on power supply characteristics. A power supply with poor high-frequency performances (or long, inductive connections to the IC) causes the bulk capacitor to be recharged slowly: the higher the current control switching frequency, the higher the current ripple in the capacitor. RMS current in the capacitor, however, does not exceed the RMS output current. Bulk capacitor value (*C*) and the ESR determine the amount of voltage ripple on the capacitor itself and on the IC. In slow decay, neglecting the deadtime and output current ripple, and assuming that during the on-time the capacitor is not recharged by the power supply, the voltage at the end of the on-time is:

Equation 1

$$V_S - I_{OUT} \cdot \left(ESR + \frac{t_{ON}}{C} \right),$$

so the supply voltage ripple is:

Equation 2

$$I_{OUT} \cdot \left(ESR + \frac{t_{ON}}{C} \right)$$

where I_{OUT} is the output current. With fast decay, instead, recirculating current recharges the capacitor, causing the supply voltage to exceed the nominal voltage. This can be very dangerous if the nominal supply voltage is close to the maximum recommended supply voltage (52 V). In fast decay the supply voltage ripple is about:

Equation 3

$$I_{OUT} \cdot \left(2 \cdot ESR + \frac{t_{ON} + t_{OFF}}{C} \right)$$

always assuming that the power supply does not recharge the capacitor, and neglecting the output current ripple and the deadtime. Usually (if C > 100 µF) the capacitance role is much less than the ESR, then supply voltage ripple can be estimated as:

Equation 4

$$I_{OUT} \cdot ESR \qquad \text{in slow decay}$$

Equation 5

$$2 \cdot I_{OUT} \cdot ESR \qquad \text{in fast decay}$$

For example, if a maximum ripple of 500 mV is allowed and I_{OUT} = 1 A, the capacitor ESR should be lower than:

Equation 6

$$ESR < \frac{0.5V}{1A} = 500m\Omega$$ In slow decay

Equation 7

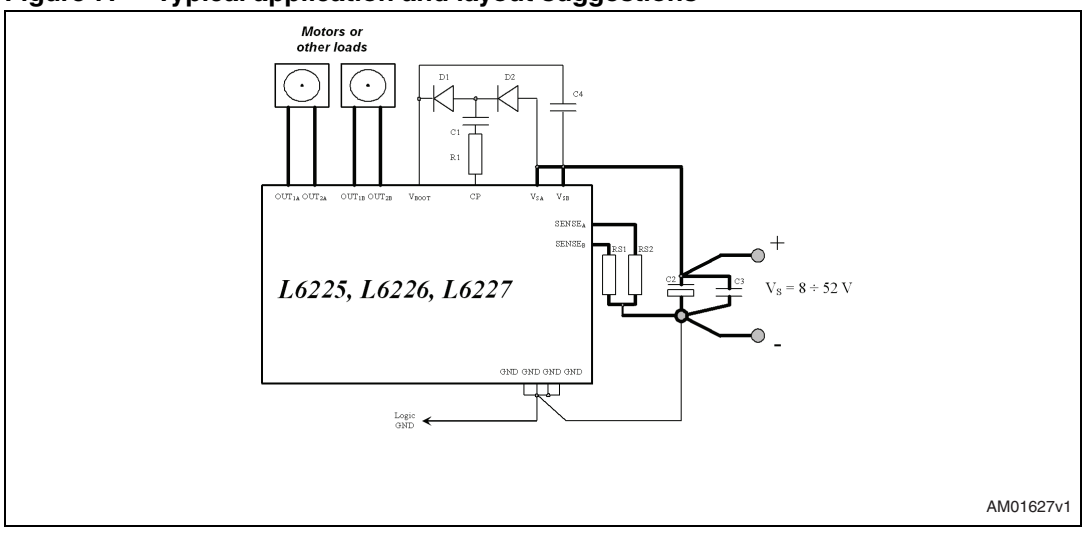
$$ESR < \frac{1}{2} \cdot \frac{0.5V}{1A} = 250m\Omega$$ In fast decay

Actually, current sunk by the V_{SA} and V_{SB} pins of the device is subject to higher peaks due to the reverse recovery charge of the internal freewheeling diodes. The duration of these peaks is, though, very short, and can be filtered using a small value (100÷200 nF), good quality ceramic capacitors, connected as close as possible to the V_{SA}, V_{SB} and GND pins of the IC. The bulk capacitor will be chosen with maximum operating voltage 25% greater than the maximum supply voltage, considering also power supply tolerances. For example, with a 48 V nominal power supply, with 5% tolerance, maximum voltage is 50.4 V, then operating voltage for the capacitor should be at least 63 V.

4.4 Layout considerations

Working with devices that combine high power switches and control logic in the same IC, special attention has to be paid to the PCB layout. In extreme cases, power DMOS commutation can induce noise that could cause improper operation in the logic section of the device. Noise can be radiated by high dV/dt nodes or high dI/dt paths, or conducted through GND or supply connections. Logic connections, especially high-impedance nodes (actually all logic inputs, see further), must be kept far from switching nodes and paths. With the L6225, L6226, L6227, in particular, external components for the charge pump circuitry should be connected together through short paths, since these components are subject to voltage and current switching at relatively high frequency (600 kHz). The primary means to minimize conducted noise is to have a good GND layout (see *Figure 7*).

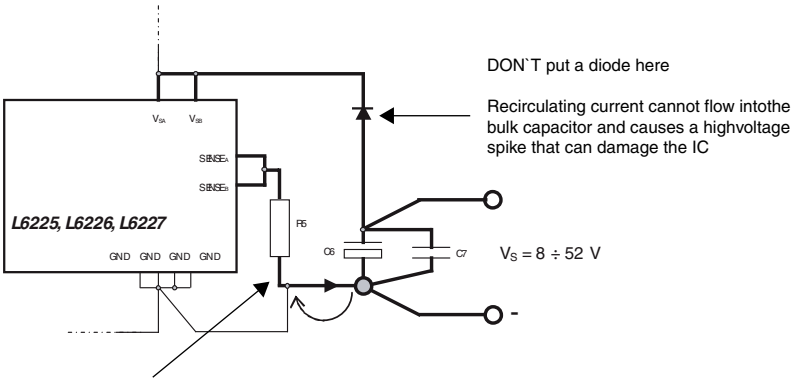
Figure 7. Typical application and layout suggestions



High-current GND tracks (i.e. the tracks connected to the sensing resistors) must be connected directly to the negative terminal of the bulk capacitor. A good quality, high-frequency bypass capacitor is also required (typically a 100 nF÷200 nF ceramic would suffice), since electrolytic capacitors show a poor high frequency performance. Both bulk electrolytic and high-frequency bypass capacitors have to be connected with short tracks to V_{SA}, V_{SB} and GND. On the L6225, L6226, L6227 GND pins are the logic GND, since only the quiescent current flows through them. Logic GND and power GND should be connected together in a single point, the bulk capacitor, to keep noise in the power GND from affecting logic GND. Specific care should be paid layouting the path from the SENSE pins through the sensing resistors to the negative terminal of the bulk capacitor (power ground). These tracks must be as short as possible in order to minimize parasitic inductances that can cause dangerous voltage spikes on the SENSE and OUT pins (see *Section 4.2: Voltage ratings and operating range*). For the same reason the capacitors on V_{SA}, V_{SB} and GND should be very close to the GND and supply pins. Refer to *Section 4.5: Sensing resistors* for information on selecting the sense resistors. Traces connected to V_{SA}, V_{SB}, $SENSE_A$, $SENSE_B$, and the four OUT pins must be designed with adequate width, since high currents are flowing through these traces, and layer changes should be avoided. Should a layer change prove necessary, multiple and large via holes have to be used. A wide GND copper area can be used to improve heat removal, thus reducing thermal resistance.

Figure 8 shows two typical situations that must be avoided. An important consideration about the location of the bulk capacitors is the ability to absorb the inductive energy from the load, without allowing the supply voltage to exceed the maximum rating. The diode shown in *Figure 8* prevents the recirculation current from reaching the capacitors and results in a high voltage on the IC pins that can damage the device. Having a switch or a power connection that can disconnect the capacitors from the IC, while there is still current in the motor, also results in a high-voltage transient since there is no capacitance to sink the recirculation current.

Figure 8. Two situations that must be avoided



4.5 Sensing resistors

Each motor winding current flows through the corresponding sensing resistor, causing a voltage drop that can be used by the logic (integrated in the L6227; an external logic can be used with L6225 and L6226) to control the peak value of the load current. Two issues must be taken into account when choosing the R_{SENSE} value:

The sensing resistor dissipates energy and provides dangerous negative voltages on the SENSE pin during the current recirculation. For this reason the resistance of this component should be kept low.

The voltage drop across R_{SENSE} is compared with a reference voltage (on V_{ref} pin) by the internal comparator (L6227 only): the lower the R_{SENSE} value, the higher the peak current error due to noise on the V_{ref} pin and to the input offset of the current sense comparator. Small values of R_{SENSE} must be avoided.

A good compromise is to calculate the sensing resistor value so that the voltage drop, corresponding to the peak current in the load (I_{peak}), is about 0.5 V: $R_{SENSE} = 0.5\ V / I_{peak}$.

It should be clear that the sensing resistor must absolutely be non-inductive in order to avoid dangerous negative spikes on the SENSE pins. Wire-wound resistors cannot be used here, while metallic film resistors are recommended for their high peak current capability and low inductance. For the same reason the connections between the SENSE pins, C6, C7, V_{SA}, V_{SB} and GND pins (see *Figure 7*) must be made as short as possible (see also *Section 4.4: Layout considerations*).

The average power dissipated by the sensing resistor is:

- Fast decay recirculation: $P_R \approx I_{rms}^2 \cdot R_{SENSE}$
- Slow decay recirculation: $P_R \approx I_{rms}^2 \cdot R_{SENSE} \cdot D$

where D is the duty cycle of the PWM current control and I_{rms} is the RMS value of the load current.

Nevertheless, the sensing resistor power rating should be chosen, taking into account the peak value of the dissipated power:

Equation 8

$$P_R \approx I_{pk}^2 \cdot R_{SENSE}$$

where I_{pk} is the peak value of the load current.

Using multiple resistors in parallel helps to obtain the required power rating with standard resistors, and reduces the inductance.

The R_{SENSE} tolerance reflects on the peak current error: 1% resistors should be preferred. *Table 1* shows the R_{SENSE} recommended values (for a 0.5 V drop) and power ratings for typical examples of current peak values.

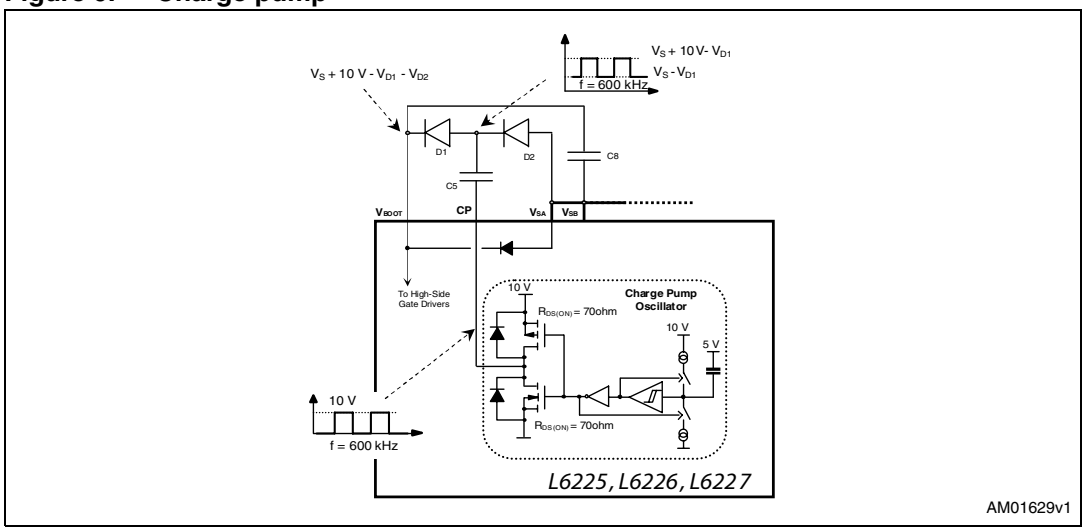
Table 1. R_{SENSE} recommended values

Ipk	R_{SENSE} value [Ω]	R_{SENSE} power rating [W]	Alternatives
0.25	2	0.125	
0.5	1	0.25	
1	0.5	0.5	2 X 1 Ω, 0.25 W paralleled

4.6 Charge pump external components

An internal oscillator, with its output at the CP pin, switches from GND to 10 V with a typical frequency of 600 kHz (see *Figure 9*).

Figure 9. Charge pump



When the oscillator output is at ground, C_5 is charged by V_S through D_2. When it rises to 10, D_2 is reverse biased and the charge flows from C_5 to C_8 through D_1, so the V_{BOOT} pin, after a few cycles, reaches the maximum voltage of V_S + 10 V - V_{D1} - V_{D2}, which supplies the high-side gate drivers.

With a differential voltage between V_S and V_{BOOT} of about 9 V and both the bridges switching at 50 kHz, the typical current drawn by the V_{BOOT} pin is 1.85 mA.

Care must be taken in establishing the PCB layout of the C5, D1, D2 connections in order to minimize interferences with the rest of the circuit (see also *Section 4.4*). Recommended values for the charge pump circuitry are:

- D1, D2: 1N4148
- C5: 10 nF 100 V ceramic
- C8: 220 nF 25 V ceramic

Due to the high charge pump frequency, fast diodes are required. Connecting the cold side of the bulk capacitor (C8) to V_S instead of GND, the average current in the external diodes during operation is less than 10 mA. At IC power-up the current in the external diodes is less than 200 mA. The reverse voltage of the charge pump diodes is about 10 V in all

conditions. The 1N4148 diodes withstand about 200 mA DC (1 A peak), and the maximum reverse voltage is 75 V, so they should fit for the majority of applications.

4.7 Sharing the charge pump circuitry

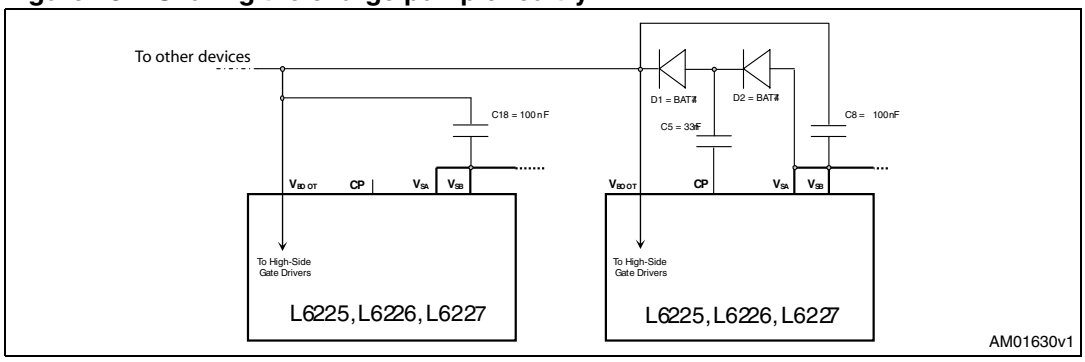
If more than one device is used in the application, it's possible to use the charge pump from one L6225, L6226 or L6227 to supply the V_{BOOT} pins of several ICs. The unused CP pins on the slave devices are left unconnected, as shown in *Figure 10*. A 100 nF capacitor (C8) should be connected to the V_{BOOT} pin of each device. Supply voltage pins (V_S) of the devices sharing the charge pump must be connected together.

The higher the number of devices sharing the same charge pump, the lower the differential voltage available for the gate drive (V_{BOOT} - V_S), causing a higher $R_{DS(on)}$ for the high-side DMOS, thus higher dissipating power.

Better performance can also be obtained using a 33 nF capacitor for C5 and using Schottky diodes (for example BAT47 are recommended).

Sharing the same charge pump circuitry for more than 3÷4 devices is not recommended, since it reduces the V_{BOOT} voltage increasing the high-side MOS on-resistance and thus power dissipation.

Figure 10. Sharing the charge pump circuitry

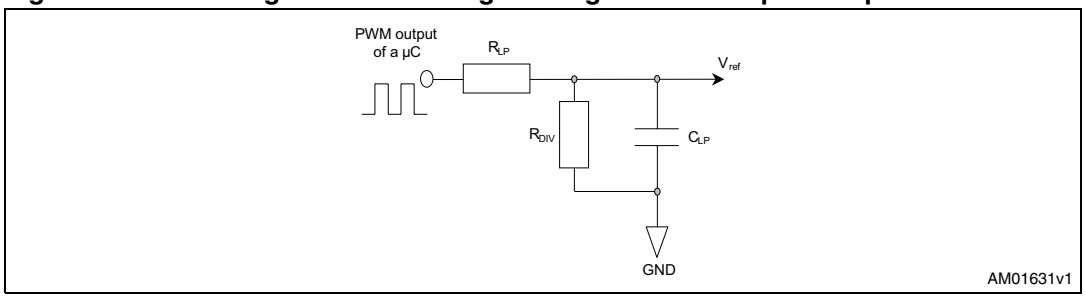


4.8 Reference voltage for PWM current control (L6227 only)

The L6227 has two analog inputs, $VREF_A$ and $VREF_B$, connected to the internal sense comparators, to control the peak value of the motor current through the integrated PWM circuitry. In typical applications these pins are connected together, in order to obtain the same current in the two motor windings. A fixed reference voltage can be easily obtained through a resistive divider from an available 5 V voltage rail (maybe the one supplying the µC or the rest of the application) and GND.

A very simple way to obtain a variable voltage without using a DAC is to low-pass filter a PWM output of a µC (see *Figure 11*).

Figure 11. Obtaining a variable voltage through a PWM output of a µC



Assuming that the PWM output swings from 0 to 5 V, the resulting voltage is:

Equation 9

$$V_{ref} = \frac{5V \cdot D_{\mu C} \cdot R_{DIV}}{R_{LP} + R_{DIV}}$$

where $D_{\mu C}$ is the duty cycle of the PWM output of the µC.

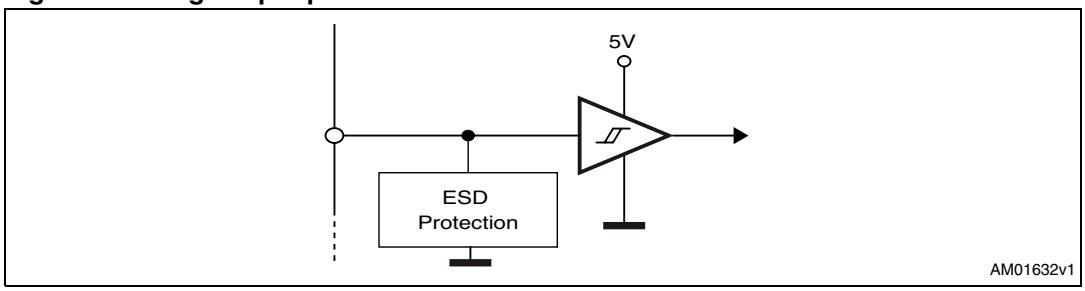
Assuming that the µC output impedance is lower than 1 kΩ, with R_{LP} = 56 kΩ, R_{DIV} = 15 kΩ, C_{LP} = 10 nF and a µC PWM switching from 0 to 5 V at 100 kHz, the low-pass filter time constant is about 0.12 ms and the remaining ripple on the V_{ref} voltage is about 20 mV. Using higher values for R_{LP}, R_{DIV} and C_{LP} reduces the ripple, but the reference voltage takes more time to vary after changing the duty cycle of the µC PWM, and too high values of R_{LP} also increase the impedance of the V_{ref} net at low frequencies, causing a poor noise immunity.

As sensing resistor values are typically kept small, a small noise on the V_{ref} input pins might cause a considerable error in the output current. It's then recommended to decouple these pins with ceramic capacitors of some tens of nF, placed very close to the V_{ref} and GND pins. Note that the V_{ref} pins cannot be left unconnected, while, if connected to GND, zero current is not guaranteed due to the voltage offset in the sense comparator. The best way to cut down the IC power consumption and clear the load current is to pull down the EN pins. With very small reference voltage, PWM integrated circuitry can lose control of the current due to the minimum allowed duration of t_{ON} (see *Section 4.11*).

4.9 Input logic pins

$IN1_A$, $IN2_A$, $IN1_B$, $IN2_B$ are CMOS/TTL compatible logic input pins. The input comparator has been configured with hysteresis to ensure the required noise immunity. Typical values for turn-on and turn-off thresholds are $V_{th,ON}$ = 1.8 V and $V_{th,OFF}$ = 1.3 V. As shown in *Figure 12*, these pins are ESD-protected (2 kV human-body electro-static discharge), and can be directly connected to the logic outputs of a µC. A series resistor is generally not recommended, as it could help inducted noise to disturb the inputs. All logic pins enforce a specific behavior and cannot be left unconnected.

Figure 12. Logic input pins

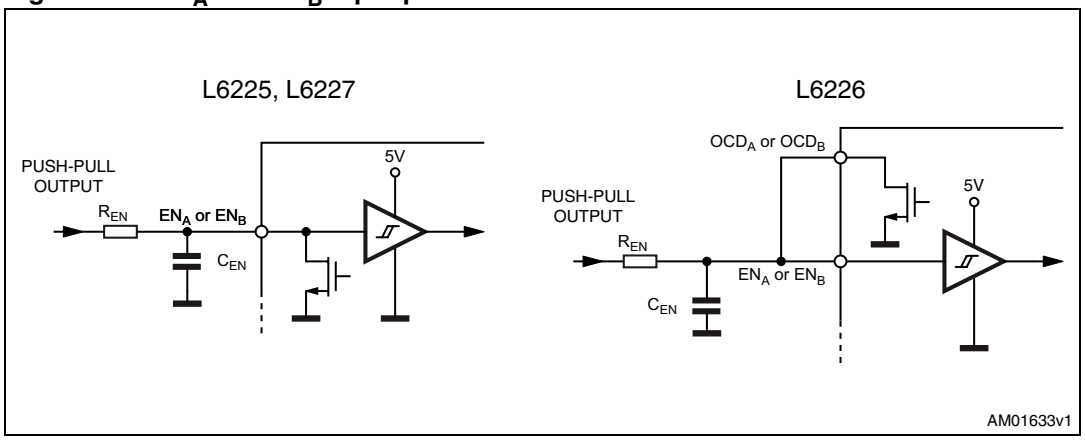


4.10 EN pins

The EN_A, EN_B pins are, actually, bi-directional. As an input, with a comparator similar to the other logic input pins (TTL/CMOS with hysteresis), they control the state of the power DMOS. When each of the two pins is at a low logic level, all the power DMOS of the corresponding H-bridge (A or B) are turned off. In L6225 and L6227 the EN pins are also connected to the two corresponding open-drain outputs of the protection circuits that pull the pins to GND if overcurrent in the corresponding H-bridge or overtemperature conditions exist. In L6226 the open-drain outputs are on separate pins, OCD_A and OCD_B, allowing easier external diagnostics and overcurrent management. For this reason, with L6225 and L6227 (and L6226 if EN pins are connected to DIAG pins), EN pins must be driven through a series resistor of 2.2 kΩ minimum (for 5 V logic), to allow the voltage at the pin to be pulled below the turn-off threshold.

A capacitor (C_{EN} in *Figure 13*) connected between each EN pin and GND is also recommended, to reduce the RMS value of the output current when overcurrent conditions persist (see *Section 4.13*). The EN pin must not be left unconnected.

Figure 13. EN_A and EN_B input pins



4.11 Programmable off-time monostable (L6227 only)

The L6227 includes a constant off-time PWM current controller for each of the two bridges. The current control circuit senses the bridge current by sensing the voltage drop across an external sense resistor connected between the source of the two lower power MOSFET transistors and ground, as shown in *Figure 14*. As the current in the load builds up, the voltage across the sense resistor increases proportionally. When the voltage drop across the sense resistor becomes greater than the voltage at the reference input ($VREF_A$ or $VREF_B$), the sense comparator triggers the monostable, switching the low-side MOSFET off. The low-side MOSFET remains off for the time set by the monostable and the motor current recirculates in the upper path. When the monostable times out, the bridge again turns on. Since the internal deadtime, used to prevent cross conduction in the bridge, delays the turn- on of the power MOSFET, the effective off-time is the sum of the monostable time plus the deadtime.

Figure 14. PWM current control circuitry (L6227 only)

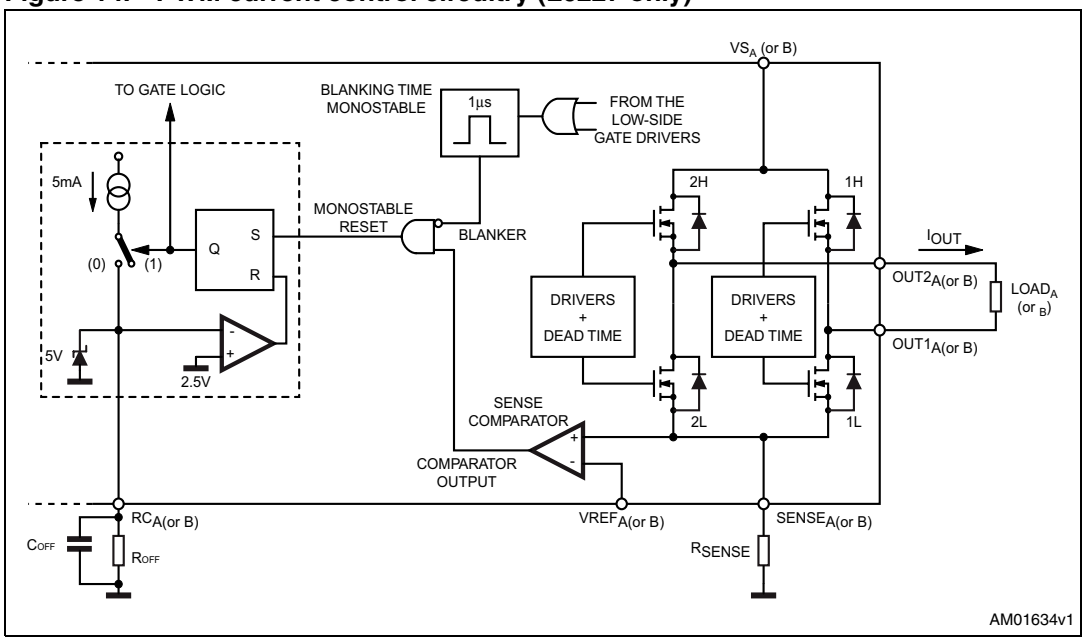


Figure 15 shows the typical operating waveforms of the output current, the voltage drop across the sensing resistor, the RC pin voltage and the status of the bridge. Immediately after the low-side power MOSFET turns on, a high peak current flows through the sensing resistor due to the reverse recovery of the freewheeling diodes. The L6227 provides a 1 µs blanking time t_{BLANK} that inhibits the comparator output so that this current spike cannot prematurely re-trigger the monostable.

Figure 15. PWM output current regulation waveforms (L6227 only)

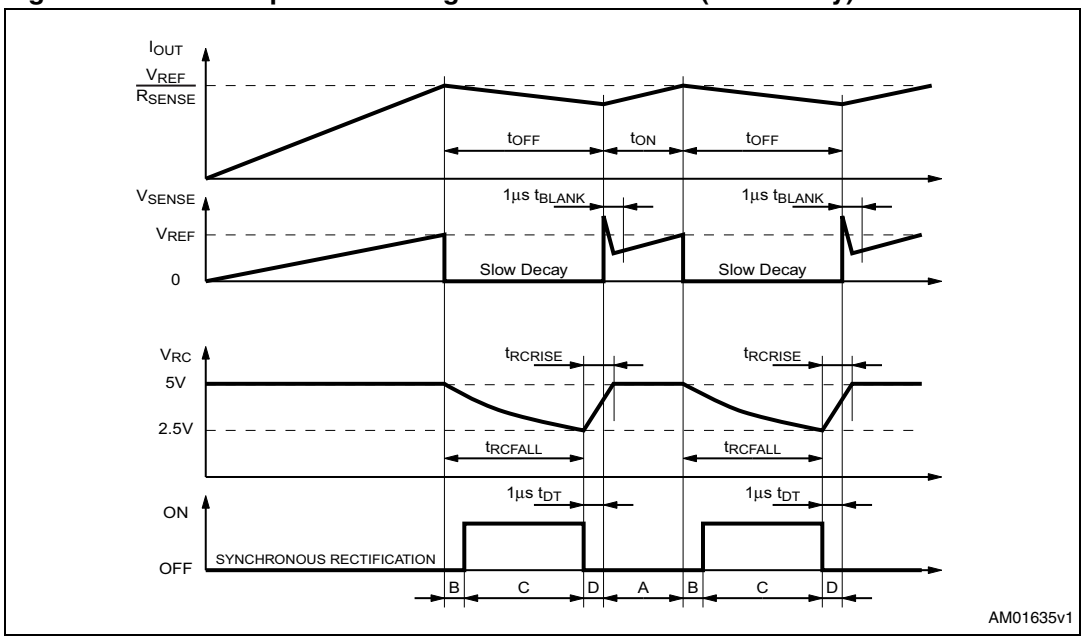


Figure 16 shows the magnitude of the OFF time t_{OFF} versus C_{OFF} and R_{OFF} values. It can be approximately calculated from the equations:

- $t_{RCFALL} = 0.6 \cdot R_{OFF} \cdot C_{OFF}$
- $t_{OFF} = t_{RCFALL} + t_{DT} = 0.6 \cdot R_{OFF} \cdot C_{OFF} + t_{DT}$

where R_{OFF} and C_{OFF} are the external component values and t_{DT} is the internally generated deadtime with:

- $20\ k\Omega \leq R_{OFF} \leq 100\ k\Omega$
- $0.47\ nF \leq C_{OFF} \leq 100\ nF$
- $t_{DT} = 1\ \mu s$ (typical value)

Therefore:

- $t_{OFF(MIN)} = 6.6\ \mu s$
- $t_{OFF(MAX)} = 6ms$

These values allow a sufficient range of t_{OFF} to implement the drive circuit for most motors.

The capacitor value chosen for C_{OFF} also affects the rise time t_{RCRISE} of the voltage at the pin RC_A (or RC_B). The rise time t_{RCRISE} is only an issue if the capacitor is not completely charged before the next time the monostable is triggered. Therefore, the on-time t_{ON}, which depends on motor and supply parameters, has to be longer than t_{RCRISE} in order to allow a good current regulation by the PWM stage. Furthermore, the on-time t_{ON} cannot be shorter than the minimum on-time $t_{ON(MIN)}$.

Equation 10

$$\begin{cases} t_{ON} > t_{ON(MIN)} = 1.5\mu s \text{ (typ. value)} \\ t_{ON} > t_{RCRISE} - t_{DT} \end{cases}$$

Equation 11

$$t_{RCRISE} = 600 \cdot C_{OFF}$$

4.12 Off-time selection and minimum on-time (L6227 only)

Figure 17 also shows the lower limit for the on-time t_{ON} for having a good PWM current regulation capacity. It has to be said that t_{on} is always longer than $t_{ON(MIN)}$ because the device imposes this condition, but it can be shorter than t_{RCRISE} - t_{DT}. In this last case the device continues to work, but the off-time t_{OFF} is no longer constant.

So, a small C_{OFF} value gives more flexibility for the applications (allows shorter on-time and, therefore, higher switching frequency), but the smaller the value for C_{OFF}, the more influential the noise on the circuit performance.

Figure 16. Typical off-time vs. C_{OFF} for several values of R_{OFF}

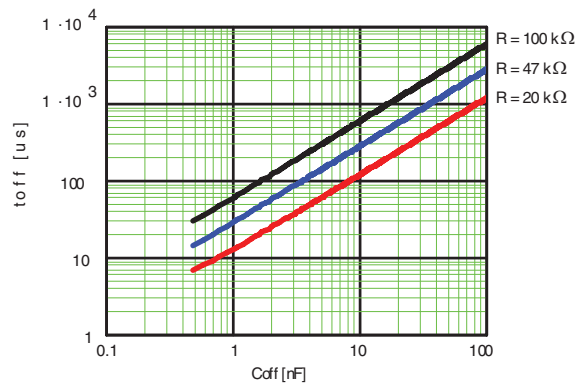
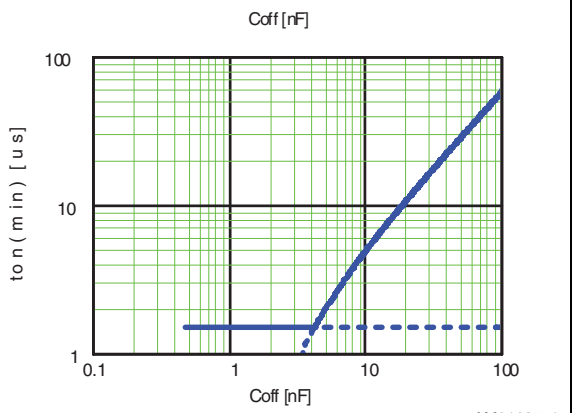


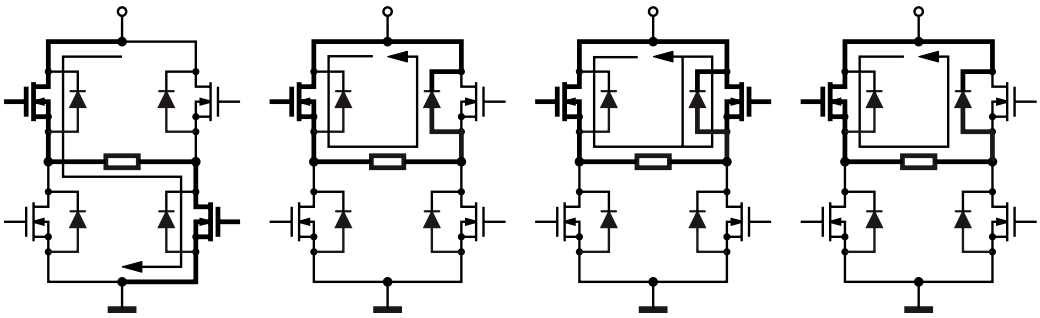
Figure 17. Minimum on-time vs. C_{OFF}



4.12.1 Slow decay mode (L6227 only)

Figure 18 shows the operation of the bridge in the slow decay mode. At the start of the off time, the lower power MOSFET is switched off and the current recirculates around the upper half of the bridge. Since the voltage across the coil is low, the current decays slowly. After the deadtime the upper power MOSFET is operated in the synchronous rectification mode. When the monostable times out, the lower power MOSFET is turned on again after a delay set by the deadtime to prevent cross conduction.

Figure 18. Slow decay mode output stage configurations



In some conditions (short off-time, very low regulated current, high motor winding L / R) the system may need an on-time shorter than 1.5 µs in which case the PWM current controller can lose the regulation.

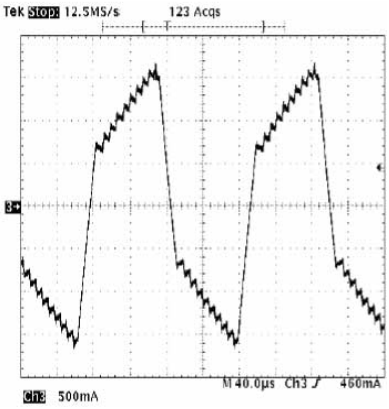
Figure 19 shows the operation of the circuit in this condition. When the current first reaches the threshold, the bridge is turned off for a fixed time and the current decays. During the following on-time, the current increases above the threshold, but the bridge cannot be turned off until the minimum 1.5 µs on-time expires. Since the current increases more in each on-time than it decays during the off-time, it keeps growing during each cycle, with a steady state asymptotic value set by the duty cycle and load DC resistance. The resulting peak current is:

Equation 12

$$I_{pk} = V_S \cdot \frac{D}{R_{LOAD}}$$

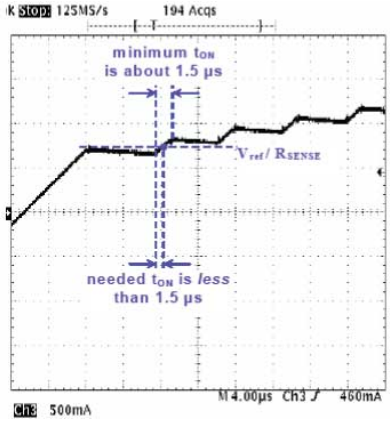
where $D = t_{ON} / (t_{ON} + t_{OFF})$ is the duty cycle and R_{LOAD} is the load DC resistance.

Figure 19. PWM controller loses the current regulation due to minimum on-time (L6227 only)



AM01639v1

Figure 20. PWM controller loses the current regulation due to minimum on-time (L6227 only) - detail



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4.13 Overcurrent protection

To implement an overcurrent protection, a dedicated overcurrent detection (OCD) circuitry (see *Figure 21* and *22* for a simplified schematic) senses the current in each high side. Power DMOS are actually made of thousands of individual identical cells, each carrying a fraction of the total flowing current. The current sensing element, connected in parallel to the power DMOS, is made only of a few such cells, having a 1:N ratio compared to the power DMOS. The total drain current is split between the output and the sense element according to the cell ratio. Sensed current is, then, a small fraction of the output current and does not contribute significantly to power dissipation.

Figure 21. L6225 and L6227 overcurrent detection simplified circuitry

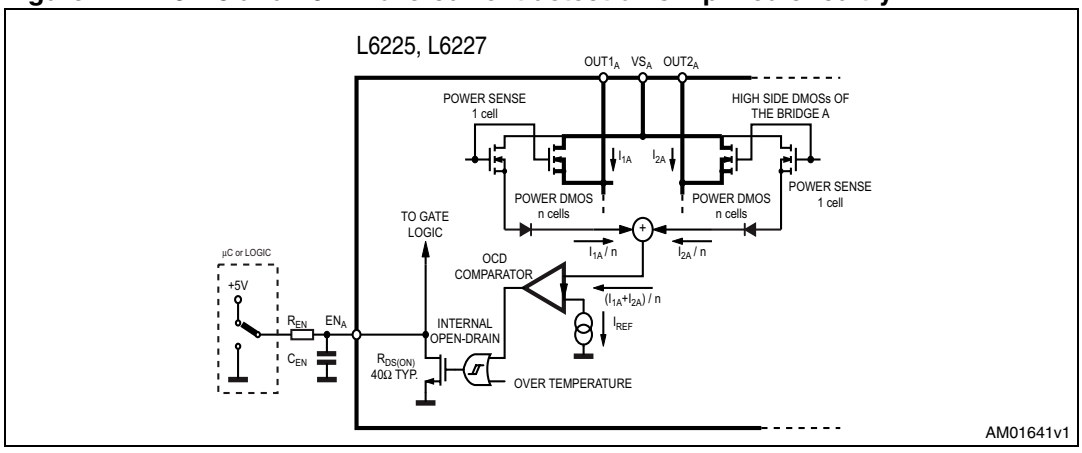

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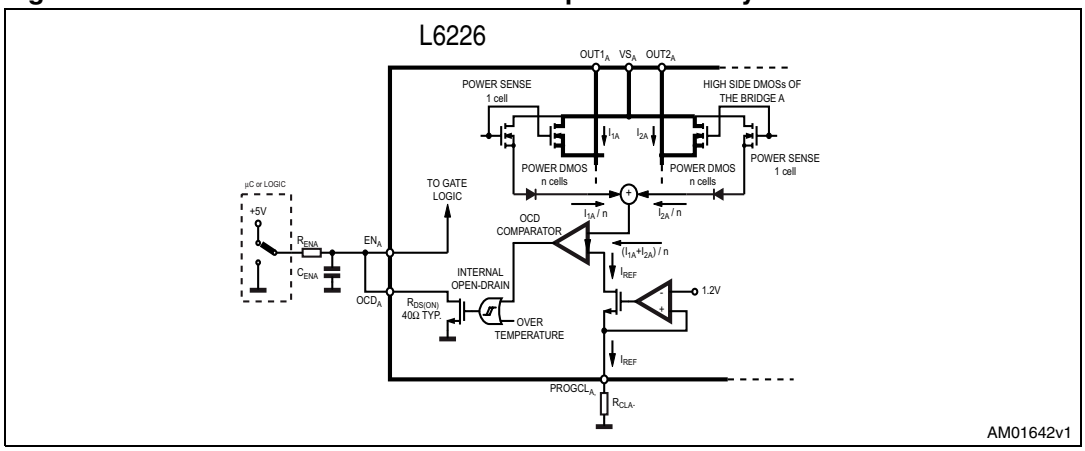
Figure 22. L6226 overcurrent detection simplified circuitry



This sensed current is compared to an internally-generated reference (adjustable through the external resistors R_{CLA} and R_{CLB} for L6226) to detect an overcurrent condition. An internal open-drain MOSFET turns on when the sum of the currents in the bridges 1A and 2A or 1B and 2B reaches the threshold (2.8 A typical value for L6225 and L6227; adjustable through the external resistors R_{CLA} and R_{CLB} for L6226). In L6225 and L6227 the open drain is internally connected to the EN pins. With L6226 the OCD pins should be connected to the EN pins to allow the protection to function. To ensure an overcurrent protection, connect these pins to an external RC network (see *Figure 21* and *22*).

Figure 23 and *24* show the device operating in overcurrent condition (short to ground). When an overcurrent is detected, the internal open-drain MOSFET pulls the EN pin to GND, switching off all 4 power DMOS of the bridge and allowing the current to decay. Under a persistent overcurrent condition, like a short to ground or a short between two output pins, the external RC network on the EN pin (see *Figure 21* and *22*) reduces the RMS value of the output current by imposing a fixed disable time after each overcurrent occurrence. The values of R_{EN} and C_{EN} are selected to ensure proper operation of the device under a short-circuit condition. When the current flowing through the high-side DMOS reaches the OCD threshold (2.8 A typ. for L6225 and L6227, adjustable for L6226), after an internal propagation delay ($t_{OCD(ON)}$) the open drain starts discharging C_{EN}. When the EN pin voltage falls below the turn-off threshold ($V_{TH(OFF)}$), all the power DMOS turn off after the internal propagation delay ($t_{D(OFF)EN}$). The current begins to decay as it circulates through the freewheeling diodes. Since the DMOS are off, there is no current flowing through them and no current to sense, so the OCD circuit, after a short delay ($t_{OCD(OFF)}$), switches the internal open-drain device off, and R_{EN} can charge C_{EN}. When the voltage at the EN pin reaches the turn-on threshold ($V_{TH(ON)}$), after the $t_{D(ON)EN}$ delay, the DMOS turns on and the current restarts. Even if the maximum output current is very high, the external RC network provides a disable time ($t_{DISABLE}$) to ensure a safe RMS value (see *Figure 23* and *24*).

Figure 23. Overcurrent operation: timing 1

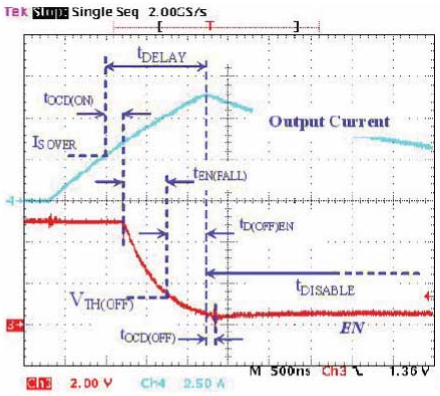


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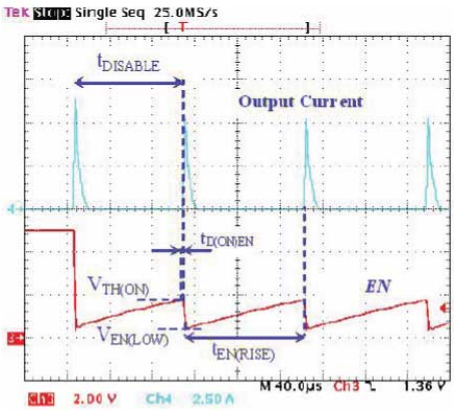
Figure 24. Overcurrent operation: timing 2



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The maximum value reached by the current depends on its slew rate, thus on the state of the short-circuit, the supply voltage, and on the total intervention delay (t_{DELAY}). It can be noticed that after the first current peak, the maximum value reached by the output current becomes lower, because the capacitor on the EN pins is discharged starting from a lower voltage, resulting in a shorter t_{DELAY}.

The following approximate relations estimate the disable time and the first OCD intervention delay after the short-circuit (worst case).

The time the device remains disabled is:

Equation 13

$$t_{DISABLE} = t_{OCD(OFF)} + t_{EN(RISE)} + t_{D(ON)EN}$$

where:

Equation 14

$$t_{EN(RISE)} = R_{EN} \cdot C_{EN} \cdot \ln \frac{V_{DD} - V_{EN(LOW)}}{V_{DD} - V_{TH(ON)}}$$

$V_{EN(LOW)}$ is the minimum voltage reached by the EN pin, and can be estimated by the relation:

Equation 15

$$V_{EN(LOW)} = V_{TH(OFF)} \cdot e^{-\frac{t_{D(OFF)EN} + t_{OCD(OFF)}}{R_{OPDR} \cdot C_{EN}}}$$

The total intervention time is:

Equation 16

$$t_{DELAY} = t_{OCD(ON)} + t_{EN(FALL)} + t_{D(OFF)EN}$$

where

Equation 17

$$t_{EN(FALL)} = R_{OPDR} \cdot C_{EN} \cdot \ln \frac{V_{DD}}{V_{TH(OFF)}}$$

$t_{OCD(OFF)}$, $t_{OCD(ON)}$, $t_{D(ON)EN}$, $t_{D(OFF)EN}$, and R_{OPDR} are device intrinsic parameters, V_{DD} is the pull-up voltage applied to R_{EN}.

The external RC network, C_{EN} in particular, must be chosen in order to obtain a reasonably fast OCD intervention (short t_{DELAY}) and a safe disable time (long $t_{DISABLE}$).

Figure 25 and *26* show both $t_{DISABLE}$ and t_{DELAY} as a function of C_{EN}: at least 100 µs for $t_{DISABLE}$ are recommended, keeping the delay time below 1÷2 µs at the same time.

The internal open drain can also be turned on if the device experiences an overtemperature (OVT) condition. The OVT causes the device to shut down when the die temperature exceeds the OVT threshold (T_J >165 °C typ.). Since the OVT is also connected directly to the gate drive circuits (see *Figure 1* to *Figure 3*), all the power DMOS shut down, even if the EN pin voltage is still over $V_{th(OFF)}$. When the junction temperature falls below the OVT turn-off threshold (150 °C typ.), the open drain turns off, CEN is recharged up to $V_{TH(ON)}$ and then the power DMOS are turned back on.

Figure 25. Typical disable time vs. C_{EN} for several values of R_{EN}

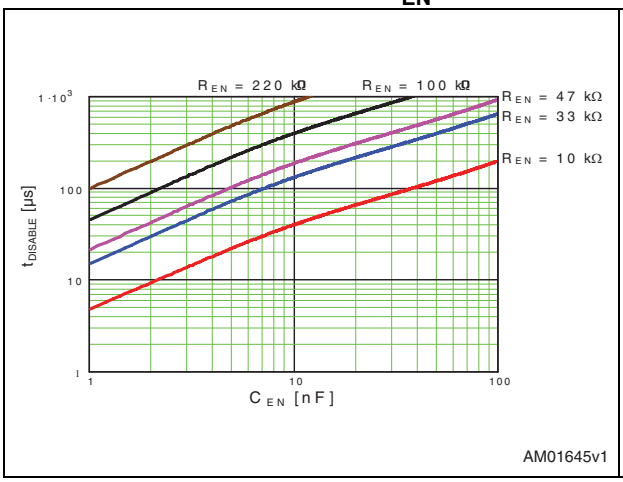
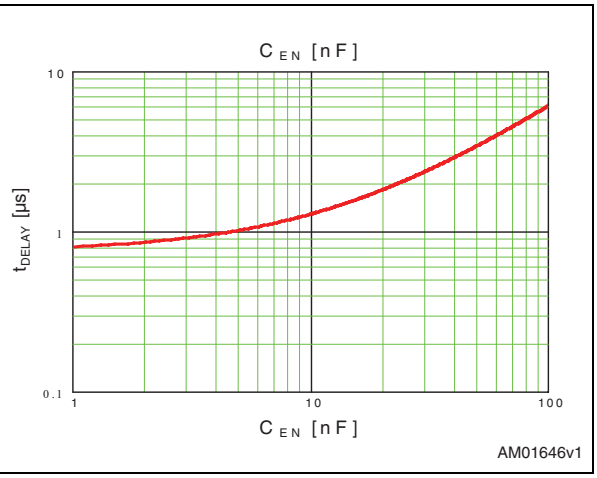


Figure 26. Typical delay time vs. C_{EN}



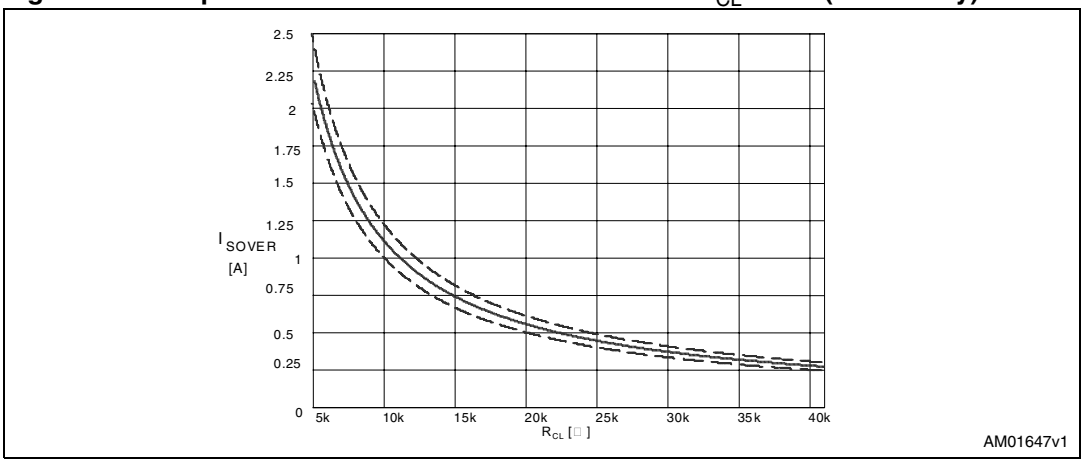
4.14 Adjusting the overcurrent detection trip point (L6226 only)

The L6226 allows the user to set the overcurrent detection threshold separately for the two full bridges connecting two resistors (R_{CL}) to pins $PROGCL_A$ and $PROGCL_B$. The OCD threshold (I_{SOVER}) follows the equations:

- I_{SOVER} = 2.8 A ±30% at -25 °C < T_j < 125 °C if R_{CL} = 0 Ω (PROGCL connected to GND)
- $I_{SOVER} = \frac{11050}{R_{CL}}$ ±10% at -25 °C < T_j < 125 °C if 5 kΩ < R_{CL} < 40 kΩ

Figure 27 shows the OCD threshold versus the R_{CL} value in the range from 5 kΩ to 40 kΩ.

Figure 27. Output current detection threshold versus R_{CL} value (L6226 only)

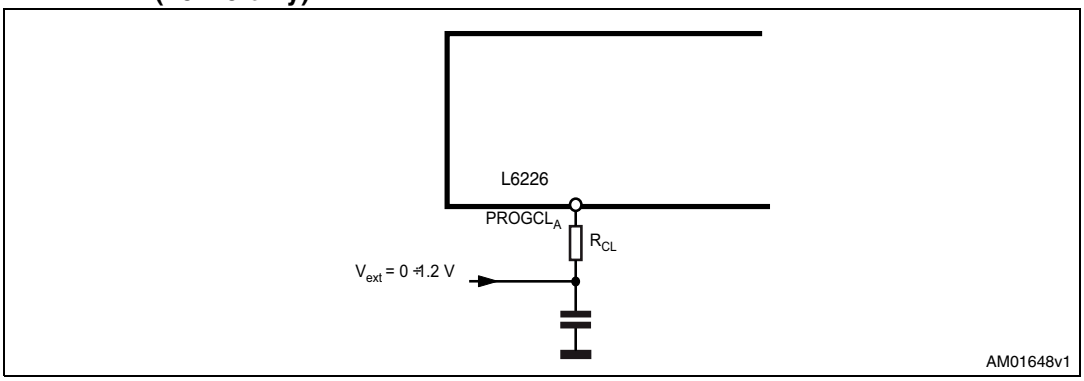


The overcurrent detection threshold can also be adjusted through an external reference voltage, as shown in *Figure 28*. The external reference voltage source should be able to sink current (about 300 µA maximum). Moreover, if the supply voltage is provided to the L6226 before V_{EXT}, and its EN pins are at a high logic level, the device starts working with minimum OCD threshold (actually the capacitor placed at the bottom of R_{CL} allows a short startup time with a higher OCD threshold). V_{EXT} can also be obtained through a PWM output of a µC, adding a series resistor to obtain a low-pass filter.

The OCD threshold (I_{SOVER}) follows the equation:

- $I_{SOVER} = \frac{9208.3(1.2V - Vext)}{R_{CL}}$ ±10%, at -25 °C < T_j < 125 °C if 0.25 A < I_{SOVER} < 2.25 A

Figure 28. Adjusting the OCD threshold through an external reference voltage (L6226 only)



4.15 Paralleling two full bridges

4.15.1 Paralleling two full bridges to get a single full bridge

The outputs of L6225, L6226, L6227 can be paralleled to increase the output current capability or reduce the power dissipation in the device at a given current level. It must be noted, however, that the internal wire bond connections from the die to the power or sense pins of the package must carry current in both of the associated half bridges (see *Figure 29* and *30*). When the two halves of one full bridge (for example $OUT1_A$ and $OUT2_A$) are connected in parallel, the peak current rating is not increased since the total current must still flow through one bond wire on the power supply or sense pin. In addition, the overcurrent detection senses the sum of the current in the upper devices of each bridge (A or B), so connecting the two halves of one bridge in parallel does not increase the overcurrent detection threshold.

Figure 29. V_S and SENSE pins maximum sourced current handling

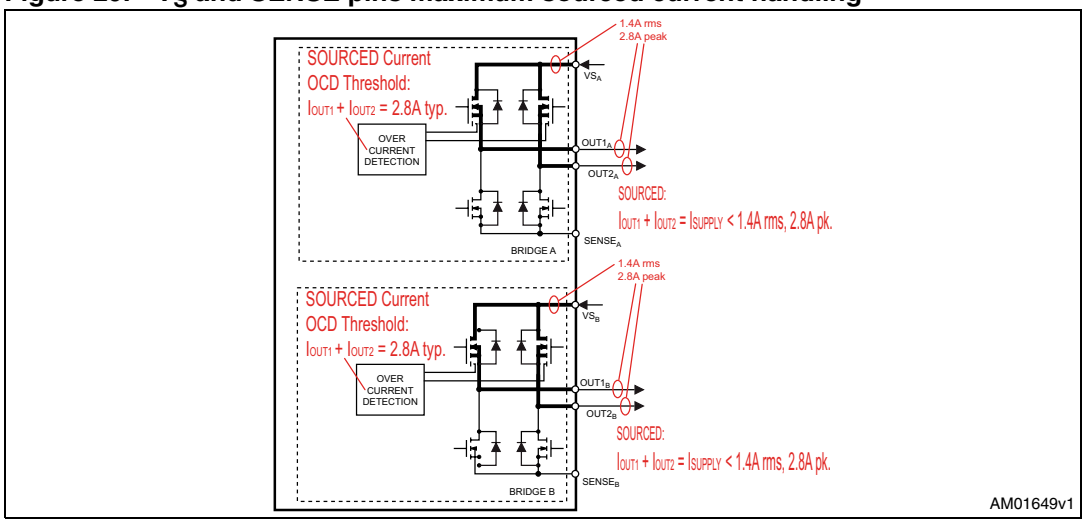
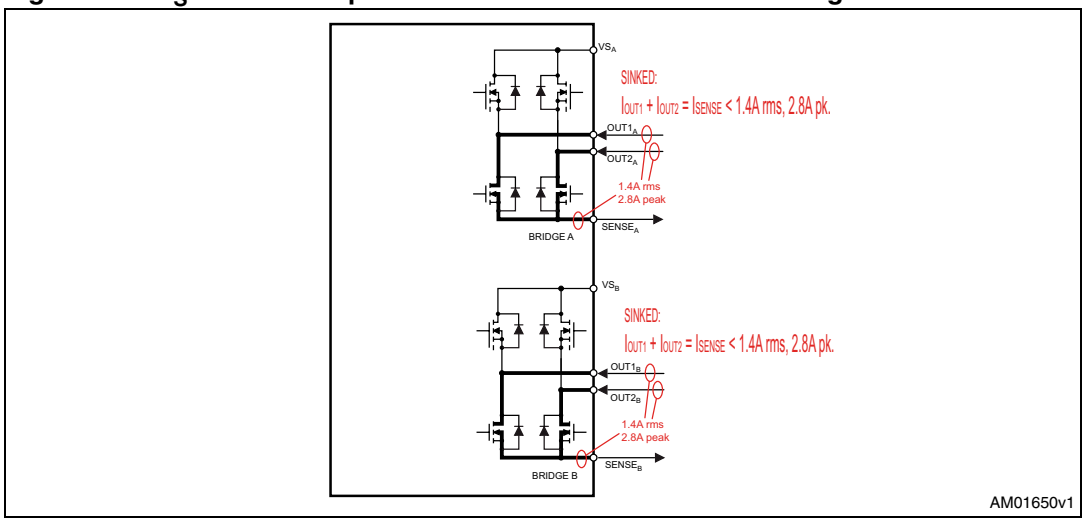


Figure 30. V_S and SENSE pins maximum sinked current handling



This configuration has to be used when two separate loads are driven, since the ICs have only two ENABLE inputs, one for the full bridge A and the other for the bridge B. In this case pulling to GND one of the two ENABLE pins disables only one load (see *Figure 31* to *33*).

This configuration can also be used if a 2.8 A OCD threshold is desired (instead of 5.6 A).

Half-bridge 1 and the half-bridge 2 of the bridge A are connected in parallel and the same is done for the bridge B as shown in *Figure 31* to *33*. In this configuration, the peak current for each half bridge is still limited by the bond wires for the supply and sense pins so the dissipation in the device is reduced, but the peak current rating is not increased. Using this configuration with L6226, two separate resistors connected to pins $PROGCL_A$ and $PROGCL_B$ must be used. With L6227, two separate RC networks should be used on the RC pins. When two different loads are driven (see *Figure 33*) by the two equivalent half bridges, two separate sensing resistors are needed, while if the two equivalent half bridges drive two separate loads, they must be connected from the OUT pins to V_S (see *Figure 33*) to make the PWM current control work properly.

In this configuration, the resulting bridge has the following characteristics (typical values).

- Equivalent device: full bridge
- $R_{DS(on)\ HS} + R_{DS(on)\ LS}$ 0.73 Ω typ. value at T_J = 25°C
- 1.4 A max RMS load current
- 2.8 A OCD threshold

Figure 31. L6225 parallel connection with lower overcurrent threshold

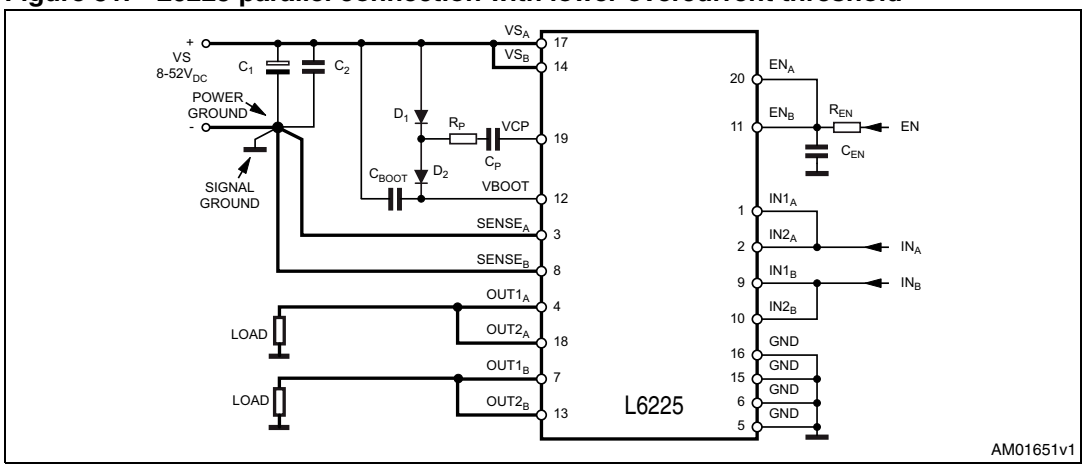


Figure 32. L6226 parallel connection with lower overcurrent threshold

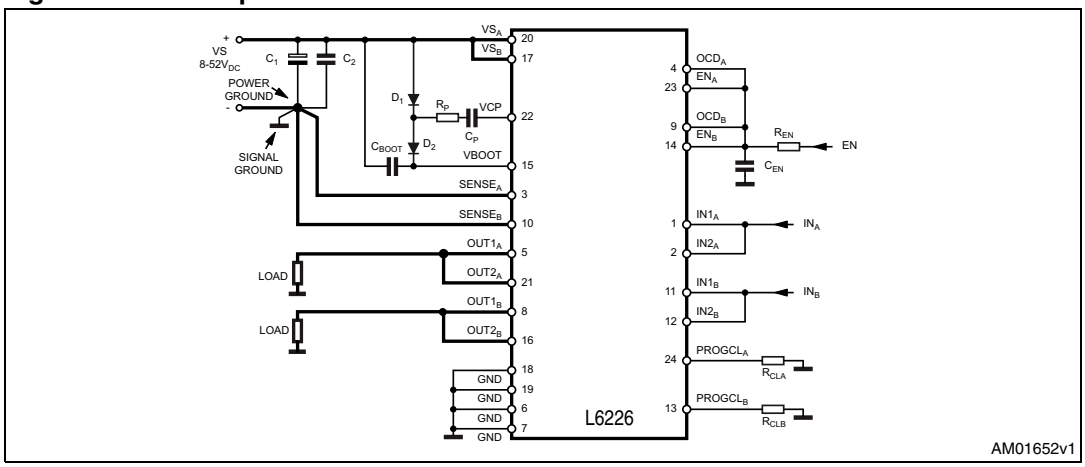
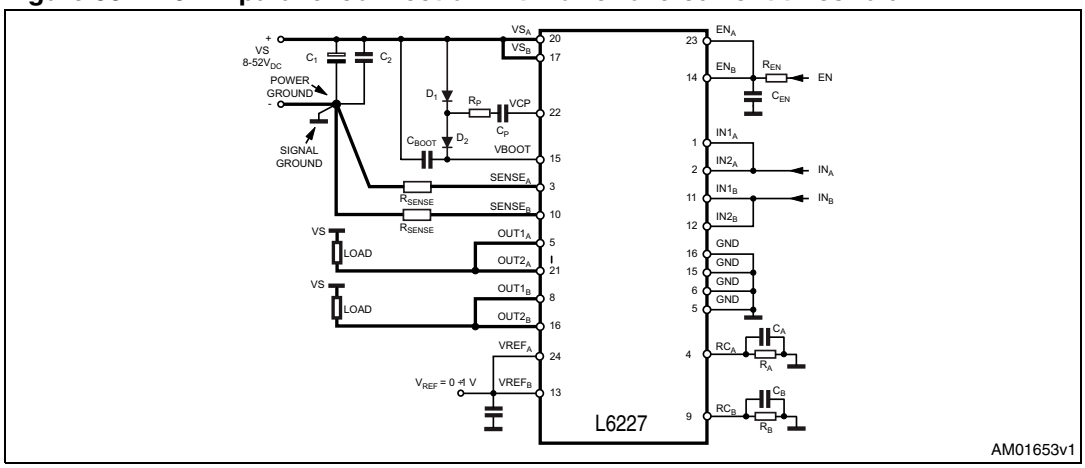


Figure 33. L6227 parallel connection with lower overcurrent threshold



For some applications the recommended configuration is half bridge 1 of bridge A paralleled with the half-bridge 1 of the bridge B, and the same for the half-bridges 2 as shown in *Figure 34* and *35*.

Figure 34. L6225 parallel connection for higher current

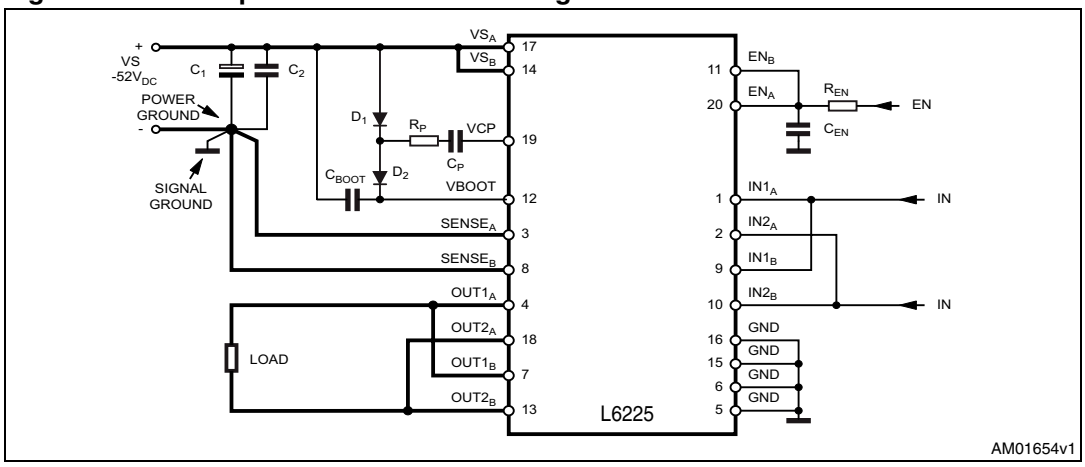
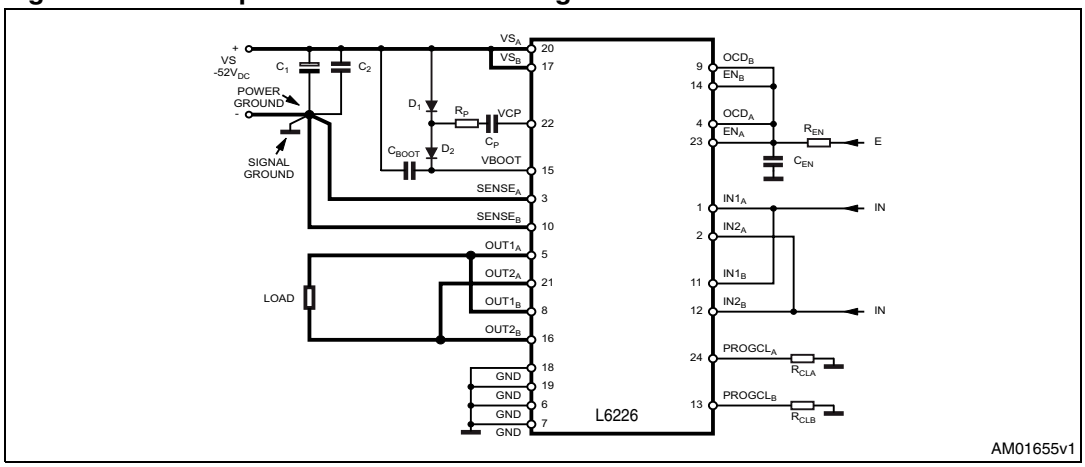


Figure 35. L6226 parallel connection for higher current



This configuration cannot be used with L6227, because of its internal PWM current controllers that work separately for bridge A and bridge B. Using this configuration with the L6227 may damage the device.

In this configuration the resulting bridge has the following characteristics (typical values):

- Equivalent device: full bridge
- $R_{DS(on)\ HS} + R_{DS(on)\ LS}$ 0.73 Ω typ. value at T_J = 25 °C
- 2.8 A max RMS load current
- 5.6 A OCD threshold

It should be noted that using two separate loads for the two equivalent half bridges the maximum current cannot be sourced or sinked simultaneously by the two equivalent half bridges (for example to drive two separate loads), due to the 2.8 A maximum current limit for the V_S and SENSE pins (see *Figure 29* and *30*). When a single load is driven (see *Figure 34* and *35*), the R_{CLA} and R_{CLB} resistors connected to the PROGCL pins of L6226 should have the same value.

4.15.2 Paralleling the four half bridges to get a single half bridge

It is also possible to parallel the four half bridges to obtain a simple half bridge as shown in *Figure 36* and *37*.

This configuration cannot be used with L6227, because of its internal PWM current controllers that work separately for bridge A and bridge B. Using this configuration with the L6227 may damage the device.

The resulting half bridge has the following characteristics (typical values):

- Equivalent device: half bridge
- $R_{DS(on)\ HS} + R_{DS(on)\ LS}$ 0.36 Ω typ. value at T_J = 25 °C
- 2.8 A max RMS load current
- 5.6 A OCD threshold

When the L6226 is used in this configuration, R_{CLA} and R_{CLB} resistors connected to PROGCL pins must have the same value.

Figure 36. L6225 paralleling the four half bridges

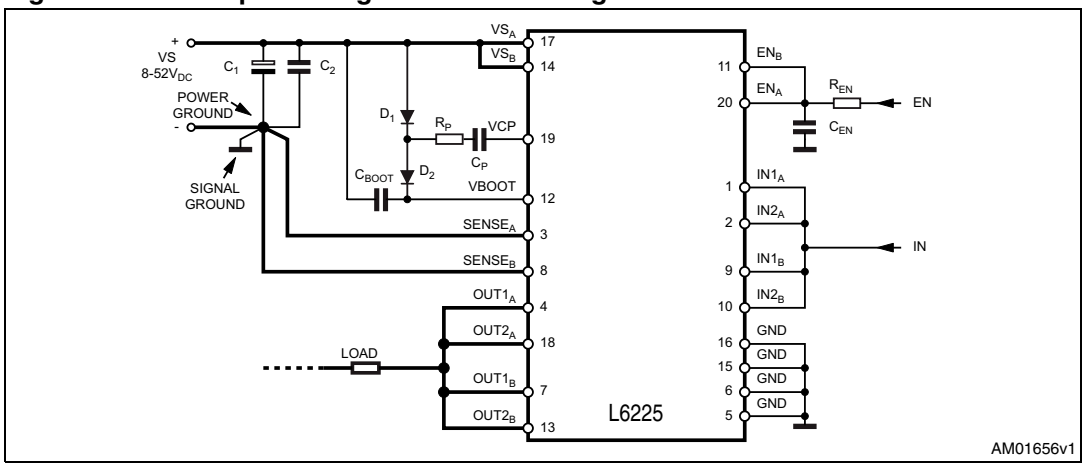
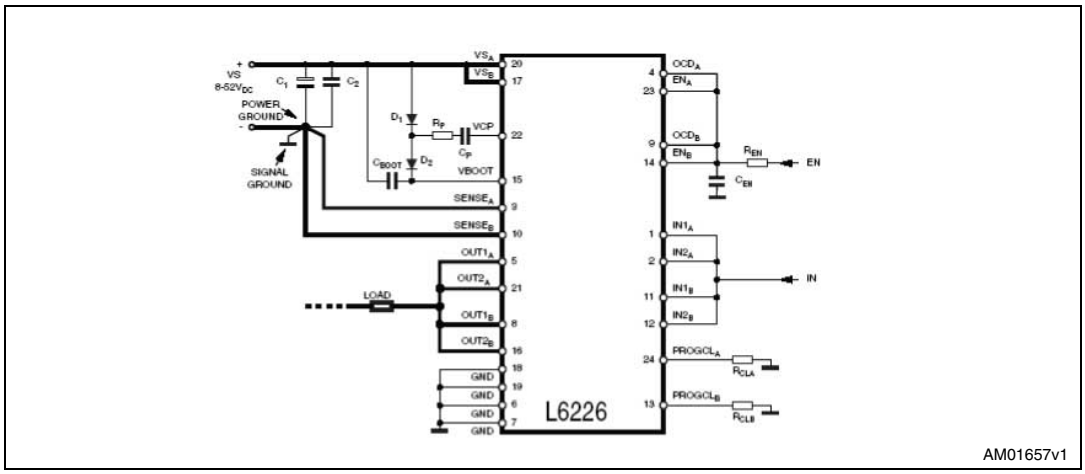


Figure 37. L6226 paralleling the four half bridges



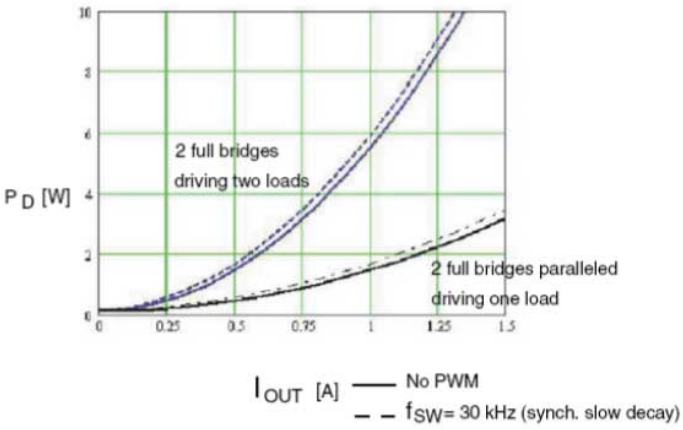
4.16 Power management

Even when operating at current levels well below the maximum ratings of the device, the operating junction temperature must be kept below 125 °C.

Figure 38 shows the IC dissipated power versus the RMS load current, in the case of:

- a single IC driving two loads (for instance 2 DC motors or a two-phase stepper motor)
- or a single IC, with two full bridges paralleled (see *Section 4.15: Paralleling two full bridges*) driving one load (for instance 1 DC motor or one phase of a two-phase stepper motor) and assuming the supply voltage is 24 V.

Figure 38. IC dissipated power versus output current

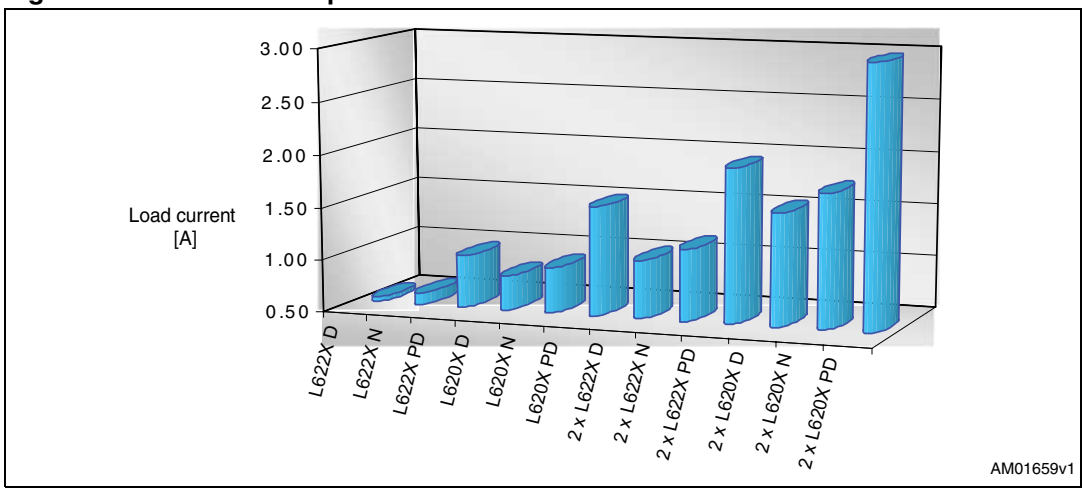


4.16.1 Maximum output current vs. selectable devices

Figure 39 shows a comparison of performance between different devices of the powerSPIN™ family, for different packages and in a parallel configuration, with the following assumptions:

- Each equivalent full bridge drives a load
- Supply voltage: 24 V; switching frequency: 30 kHz
- T_{amb} = 25 °C, T_J = 125 °C
- Maximum $R_{DS(on)}$ (taking into account process spread) has been considered, at 125 °C
- Maximum quiescent current I_Q (taking into account process spread) has been considered
- PCB is an FR4 with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm) for SO and PowerDIP packages (D, N suffixes)
- PCB is an FR4 with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm), 16 via holes and a ground layer for the PowerSO package (PD suffix)
- For each device configuration (on the x-axis) the y-axis shows the maximum output (load) current
- 2 x 'device' means that the two loads are driven by two equivalent full bridges obtained by paralleling two full bridges for each of the two ICs used. The current reported in *Figure 39* is the maximum output current of an equivalent full bridge (a paralleled IC).

Figure 39. Maximum output current vs. selectable devices



4.16.2 Power dissipation and thermal analysis with PractiSPIN™ software

The PractiSPIN™ software includes a power dissipation and thermal analysis section that helps in calculating the IC power dissipation and estimating its junction temperature, through a simulation.

This section is intended to help to give a fast evaluation of the device, package and dissipating copper area required by the user's application, and to be a good starting point for designing an application (from the power dissipation and thermal point of view). Software results, especially thermal results, need to be confirmed on the bench.

The input data for simulation are divided in three sections:

a) Application data: to select the motor characteristics and its configuration, the driving parameters and the analysis type (steady state, single pulse or repeated pulse analysis).

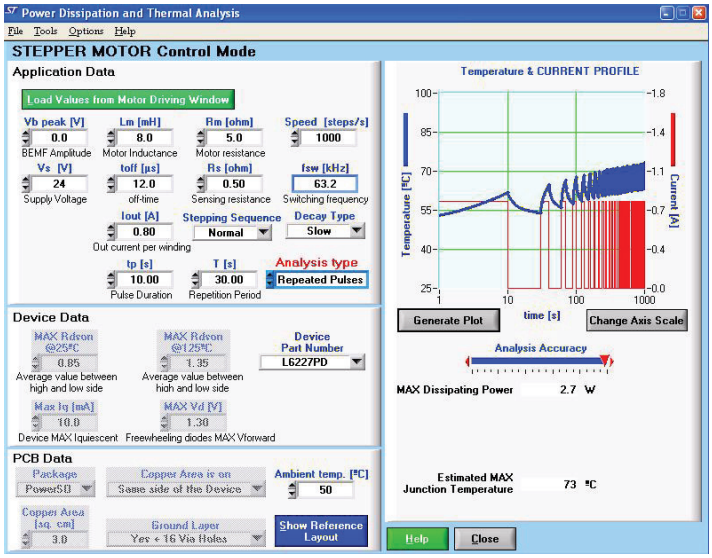
b) Device data: to choose the device part number and to edit some available IC parameters.

c) PCB data: to select the package, the PCB dissipating charcteristics and ambient temperature.

The output data include the waveforms of temperature and current profile, the estimated IC power dissipation and junction temperature.

For more details on the formulas used in the software, please refer to the "Help" menu of "Power Dissipation and Thermal Analysis".

Figure 40. Power dissipation and thermal analysis with PractiSPIN™ software



5 Application example (L6227)

Table 2. Application data

Application data	Value
Rotation speed	300 rpm (f_{CK}=1 kHZ)
Winding peak current	0.5 A
Maximum ripple	50 mA
Supply voltage	24 V ± 5 %
Sequence	Wave mode
OFF time	15 µs

Table 3. Motor data

Motor data	Value
Winding resistance	6.6 Ω
Winding inductance	7.9 mH
Step angle	1.8° / step
Maximum BEMF at 300 rpm	15 V

The bulk capacitor needs to withstand at least 24 V + 5% + 25% ≅ 32 V. A 50 V capacitor is used. Allowing a voltage ripple of 200 mV, the capacitor ESR should be lower than 200 mV / 0.5 A = 400 mΩ. The AC current capability should be about 0.5 A.

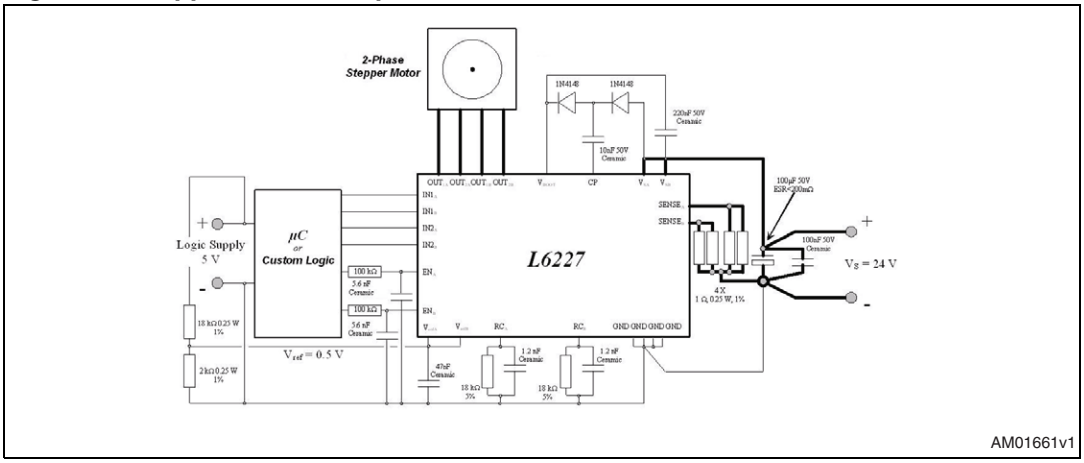
Providing a reference voltage of 0.5 V, a sensing resistor of 1 Ω is needed.

Loading the input data on the power dissipation and thermal analysis section, the resulting switching frequency is 11.9 kHz. The on-time is $t_{ON} = (1 / f_{SW}) - t_{OFF} \cong 70$ µs, which is far from the minimum allowed (1.5 µs), so slow decay can be used. The duty cycle is D ≅ 78%.

The sense resistors' power rating is about $P_R \cong I_{rms}^2 \cdot R_{SENSE} \cdot D \cong 0.25$ W. A 1 Ω - 0.25 W - 1% resistor is used. The charge pump uses recommended components (1N4148 diodes and ceramic capacitors).

R = 18 kΩ, C = 1.2 nF are connected to the RC pins, obtaining $t_{OFF} \cong 16$ µs. On the EN pins 5.6 nF capacitors have been placed, and the pins are driven by the µC through 100 kΩ resistors. With these values, in case of short-circuit between two OUT pins or an OUT pin and GND, the powerDMOS turns off after about 1 µs, and $t_{DISABLE} \cong 240$ µs.

Figure 41. Application example



With wave drive selected, the dissipating power is about 0.8 W. If the ambient temperature is about 50 °C, with 4 cm^2 of copper area on the PCB and a SO24 package, the estimated junction temperature is about 94°C. Using more copper area or a PowerDIP package reduces the junction temperature.

Appendix A Demonstration boards

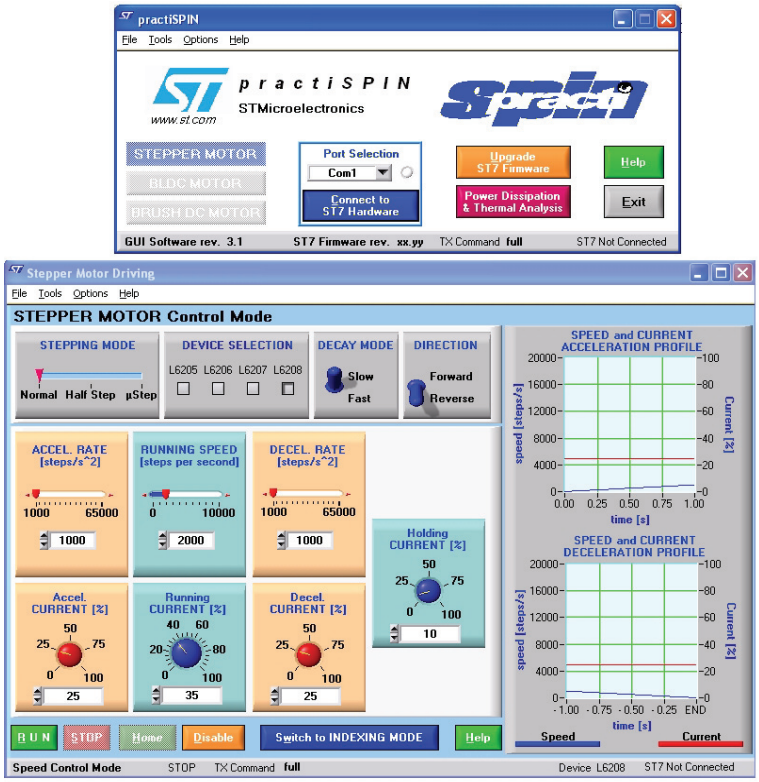
A.1 PractiSPIN™

PractiSPIN™ is an evaluation and demonstration system that can be used with the powerSPIN™ family of devices. A graphical user interface (GUI) program (see *Figure 42*) runs on an IBM-PC under windows and communicates with a common ST7-based interface board (see *Figure 43*) through the RS232 serial port. The ST7 interface board is connected to a device-specific board (target board) via a standard 34-pin ribbon cable interface.

Depending on the target device, the PractiSPIN™ can drive a stepper motor, 1 or 2 DC motors or a brushless DC (BLDC) motor, setting significant parameters such as speed, current, voltage, direction, acceleration and deceleration rates from a user friendly graphic interface, and programming a sequence of movements.

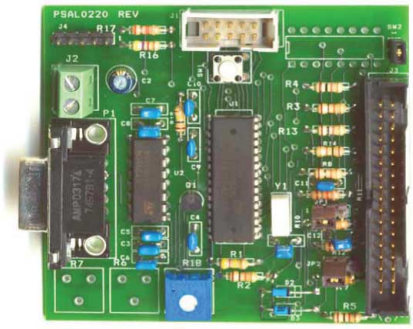
The software also allows evaluating the power dissipated by the selected device and, for a given package and dissipating copper area on the PCB, estimates the junction temperature of the device.

Figure 42. PractiSPIN™ PC software



AM01662v1

Figure 43. PractiSPIN™ ST7 demonstration board



AM01663v1

A.2 EVAL6225PD

A demonstration board has been produced to help the evaluation of the device in a PowerSO package. It implements a typical application with several added components. *Figure 45* shows the electrical schematic of the board. *Table 1* gives the part list.

Table 4. EVAL6225PD part list

Part reference	Value	Description
CN1, CN2, CN3, CN4	2-pole	Connector
CN5	34-pole	Connector
C1	220 nF/100 V	Ceramic or polyester capacitor
C2	220 nF/100 V	Ceramic or polyester capacitor
C3	100 µF/63 V	Capacitor
C4	10 nF/100 V	Ceramic capacitor
C5	10 µF/16 V	Capacitor
C6, C7	5.6 nF	Capacitor
C11	100 nF	Capacitor
C8, C10	470 pF	Capacitor
C9, C12	68 nF	Capacitor
C13	2.2 nF	Capacitor
D1	BAT46SW	Diode
D3	BZX79C5V1 5.1 V	Zener diode
JP1	3-pole	Jumper
R1	0 Ω	Resistor
R2	700 Ω 0.6 Ω	Resistor
R13	10 kΩ	Resistor
R3, R4, R5, R6	100 kΩ	Resistor

Table 4. EVAL6225PD part list (continued)

Part reference	Value	Description
R7, R9, R10, R12	1 Ω 0.4 Ω	Resistor
R18, R14	1 kΩ	Resistor
R15, R19	20 kΩ	Resistor
R16, R20	2.2 kΩ	Resistor
R17, R21	5 kΩ	Trimmer
R22	12 kΩ	Resistor
R23	50 kΩ	Trimmer
U1	L6225PD	L6225PD
U2	L6506D	L6506D
JP2, JP3, JP4, JP5, JP6	2-pole	Jumper

The demonstration board provides external connectors for the supply voltage, an external 5V reference for the logic inputs, four outputs for the motor and a 34-pin connector to control the main functions of the board through an external µC board or the PractiSPIN™ tool. The board also accommodates the L6506 PWM current controller. R23 sets the PWM operating frequency. If the L6506 does not need to be used, simply connect the two V_{REF} inputs to a voltage high enough to keep current control inactive.

The PractiSPIN™ tool is composed of a graphic interface software running on a PC that connects with the hardware based on the ST7 µC, which contains upgradable firmware. This tool allows a fast and easy evaluation of the powerSPIN™ family of devices, allowing to drive DC, BLDC and stepper motors, depending on the target device. The practiSPIN connected to the EVAL6225PD can drive DC motors and inductive loads, allowing output voltage and current settings.

The PC software also provides a power dissipation and thermal analysis section, intended to help give a fast evaluation of the device, package and dissipating copper area required by the user's application, and to be a good starting point for designing an application (from the power dissipation and thermal point of view).

Running the demonstration board in standalone mode, instead, R17 and R21 set the reference voltage separately for the two bridges, while R16, C9 and R20, C12 are low-pass filters which provide an external reference voltage by a PWM output of a µC (see also the microstepping section in the AN2839). Using external V_{REF} inputs, R15, R17, R19, R21 can be disconnected through JP4 and JP5, unless the PractiSPIN™ ST7 demonstration board is used. This board, in fact, is provided with an offset cancellation circuitry trimmable through a potentiometer (see PractiSPIN™ documentation). Closing JP2 and JP3 is recommended for safe overcurrent protection.

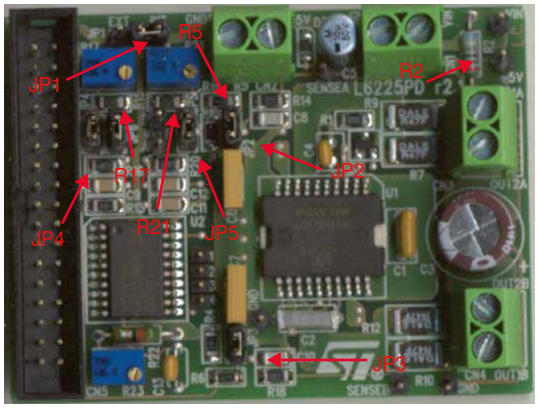
The 5 V voltage for logic inputs and for references (V_{refA} and V_{refB}) is obtained from R2, D3. Depending on the supply voltage, the value of resistor R2 should be changed in order to ensure a correct biasing of D3.

The jumper JP1 allows choosing the 5 V voltage from the internal Zener diode network or pin 11 of CN5 (for example an external µC board can provide 5 V to the demonstration board). Also a CN2 connector can be used to provide an external 5 V voltage to the board (in that case R2, D3 should be disconnected). CN2, or pin 1 of CN5, can also be used to provide a 5 V voltage to external circuits (as, for example, the PractiSPIN™ ST7 board). In

this case the current that can be drawn from the board depends on the supply voltage and on the value of R2.

Figure 46 to *48* show the placement of the components and the two-layer layout of the L6225PD demonstration board. A large GND area has been used, to guarantee minimal noise and good power dissipation for the device.

Figure 44. EVAL6225PD board



A.2.1 Important notes

- JP1: closed in INT position for use with PractiSPIN™ ST7 board
- R17, R21: set the maximum current obtainable through practiSPIN (see PractiSPIN™ documentation)
- R2 : recommended to be changed to adequate value (depending on supply voltage) to obtain 5 V across D3
- JP2, JP3 : closed for safe overcurrent protection
- JP4, JP5 : closed for use with PractiSPIN™ ST7 board
- JP6: open for use with PractiSPIN™ ST7 board.

Figure 45. EVAL6225PD electrical schematic

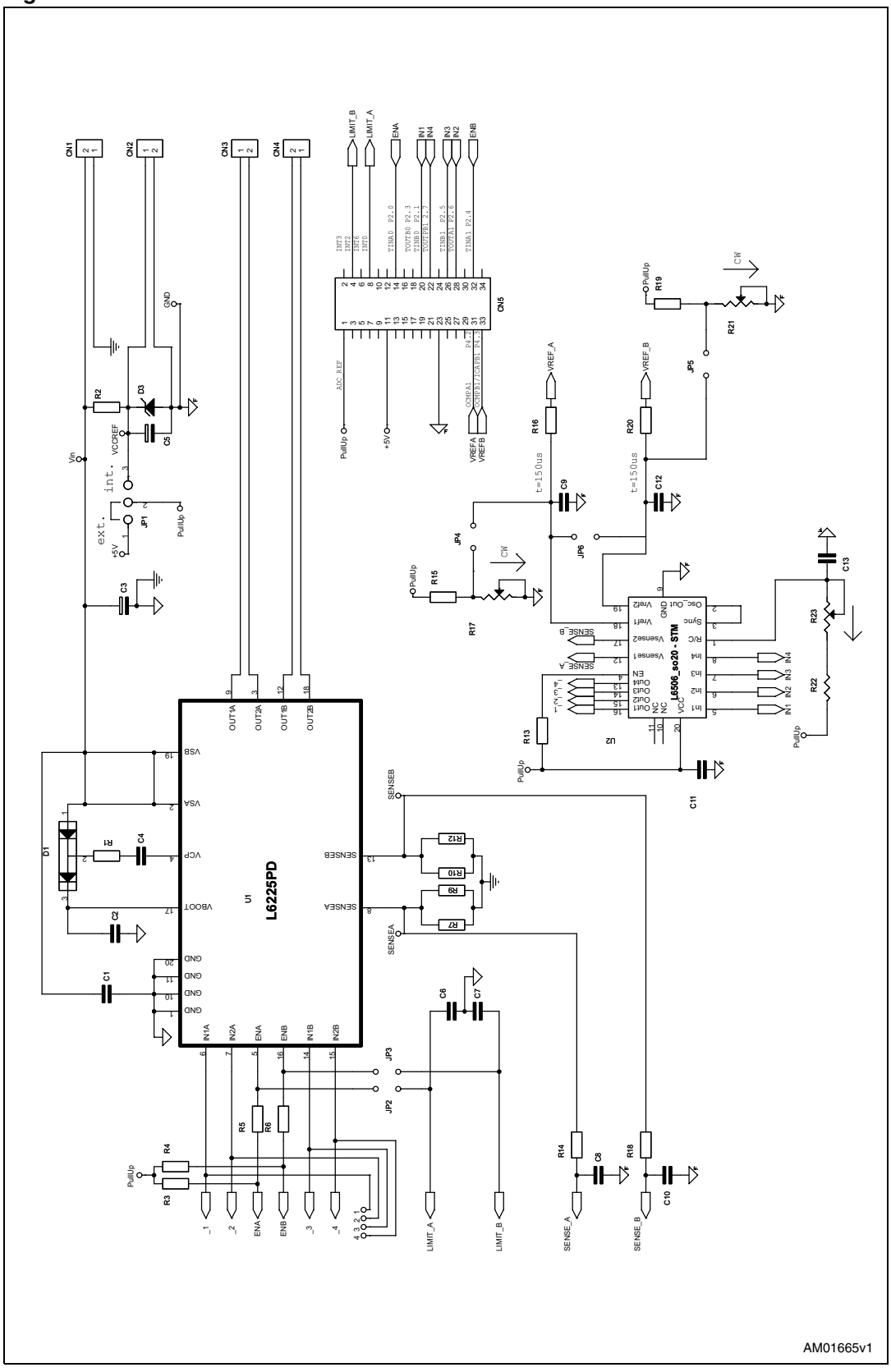
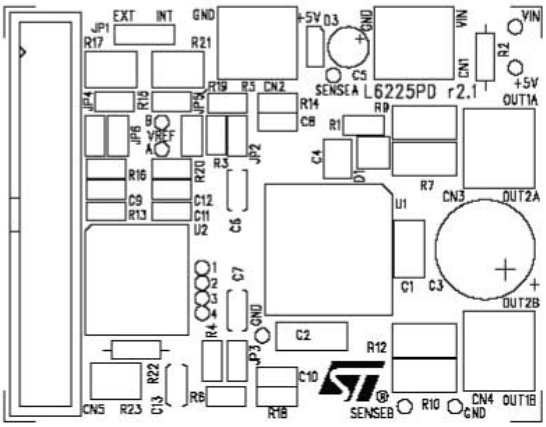
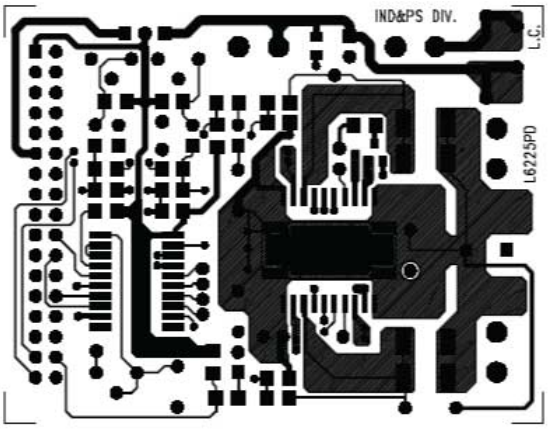


Figure 46. EVAL6225PD component placement



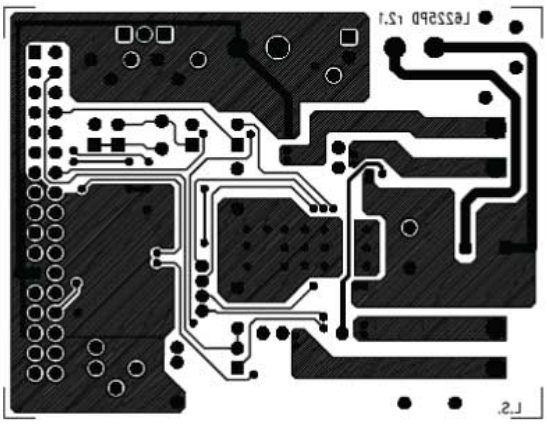
AM01666v1

Figure 47. EVAL6225PD top layer layout



AM01667v1

Figure 48. EVAL6225PD bottom layer layout



AM01668v1

A.3 EVAL6227PD

A demonstration board has been produced to help the evaluation of the device in a PowerSO package. It implements a typical application with several added components. *Figure 50* shows the electrical schematic of the board. *Table 5* gives the part list.

Table 5. EVAL6227PD part list

Part name	Value	Description
CN1, CN2, CN3, CN4	2-pole	Connector
CN5	34-pole	Connector
C1	220 nF/100 V	Ceramic or polyester capacitor
C2	220 nF/100 V	Ceramic or polyester capacitor
C3	100 µF/63 V	Capacitor
C4	10 nF/100 V	Ceramic capacitor
C5	10 µF/16 V	Capacitor
C6, C7	5.6 nF	Capacitor
C8, C9	68 nF	Capacitor
C10, C11	820 pF	Capacitor
D1	BAT46SW	Diode
D3	BZX79C5V1 5.1 V	Zener diode
JP1	3-pole	Jumper
JP2, JP3, JP4, JP5, JP6	2-pole	Jumper
R1	0 Ω	Resistor
R2	3.17 kΩ 0.6 Ω	Resistor
R3, R4	100 kΩ	Resistor
R5, R16	20 kΩ	Resistor
R6, R7	100 kΩ	Trimmer
R8, R17	2.2 kΩ 0.4 Ω	Resistor
R9, R11, R12, R14	0.4 Ω 1 Ω	Resistor
R18, R15	5 kΩ	Trimmer
U1	L6227PD	L6227PD

The demonstration board provides external connectors for the supply voltage, an external 5 V reference for the logic inputs, four outputs for the motor and a 34-pin connector to control the main functions of the board through an external µC board or the PractiSPIN™ tool.

The PractiSPIN™ tool is composed of a graphic interface software running on a PC that connects with the hardware based on the ST7 µC, which contains upgradable firmware. This tool allows a fast and easy evaluation of the powerSPIN™ family of devices, allowing to drive DC, BLDC and stepper motors, depending on the target device. The PractiSPIN™ connected to the EVAL6227PD can drive DC motors and inductive loads, allowing output voltage and current settings.

The PC software also provides a power dissipation and thermal analysis section, intended to help give a fast evaluation of the device, package and dissipating copper area required by the user's application, and to be a good starting point for designing an application (from the power dissipation and thermal point of view).

Running the demonstration board in standalone mode, instead, R15 and R18 set the reference voltage separately for the two bridges, while R8, C8 and R17, C9 are low-pass filters which provide an external reference voltage by a PWM output of a µC (see also the microstepping section in the AN2839). Using external V_{REF} inputs, R5, R15, R16, R18 should be disconnected, unless the practiSPIN ST7 demonstration board is used. This board, in fact, is provided with an offset cancellation circuitry trimmable through a potentiometer (see PractiSPIN™ documentation).

R6, C10 and R7, C11 are used to set the off-time of the two channels of the IC.

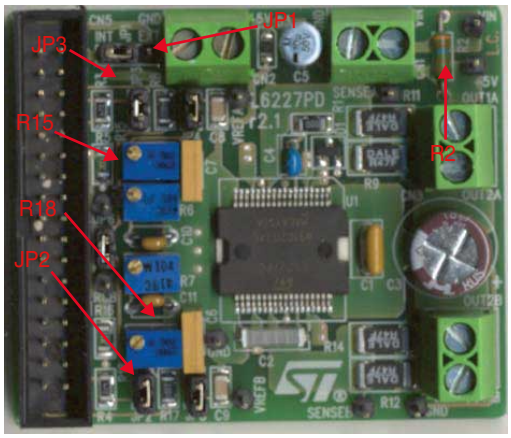
Closing JP2 and JP3 is recommended for safe overcurrent protection.

The 5 V voltage for logic inputs and for references (V_{refA} and V_{refB}) is obtained from R2 and D3. Depending on the supply voltage, the value of resistor R2 should be changed in order to ensure a correct biasing of D3.

The jumper JP1 allows choosing the 5 V voltage from the internal Zener diode network or pin 11 of CN5 (for example an external µC board can provide 5 V to the demonstration board). Also a CN2 connector can be used to provide an external 5 V voltage to the board (in that case R2, D3 should be disconnected). CN2, or pin 1 of CN5, can also be used to provide a 5V voltage to external circuits (as, for example, the PractiSPIN™ ST7 board). In this case the current that can be drawn form the board depends on the supply voltage and on the value of R2.

Figure 51 to *Figure 53* show the placement of the components and the two-layer layout of the L6227PD demonstration board. A large GND area has been used, to guarantee minimal noise and good power dissipation for the device.

Figure 49. EVAL6227PD board



AM01669v1

A.3.1 Important notes

- JP1 : closed in INT position for use with PractiSPIN™ ST7 board
- R15, R18 : set the maximum current obtainable through PractiSPIN™ (see PractiSPIN™ documentation)
- R2 : recommended to be changed to adequate value (depending on supply voltage) to obtain 5 V across D3
- JP2, JP3 : closed for safe overcurrent protection
- JP4, JP5: closed for use with PractiSPIN™ ST7 board
- JP6: open for use with PractiSPIN™ ST7 board

Figure 50. EVAL6227PD electrical schematic

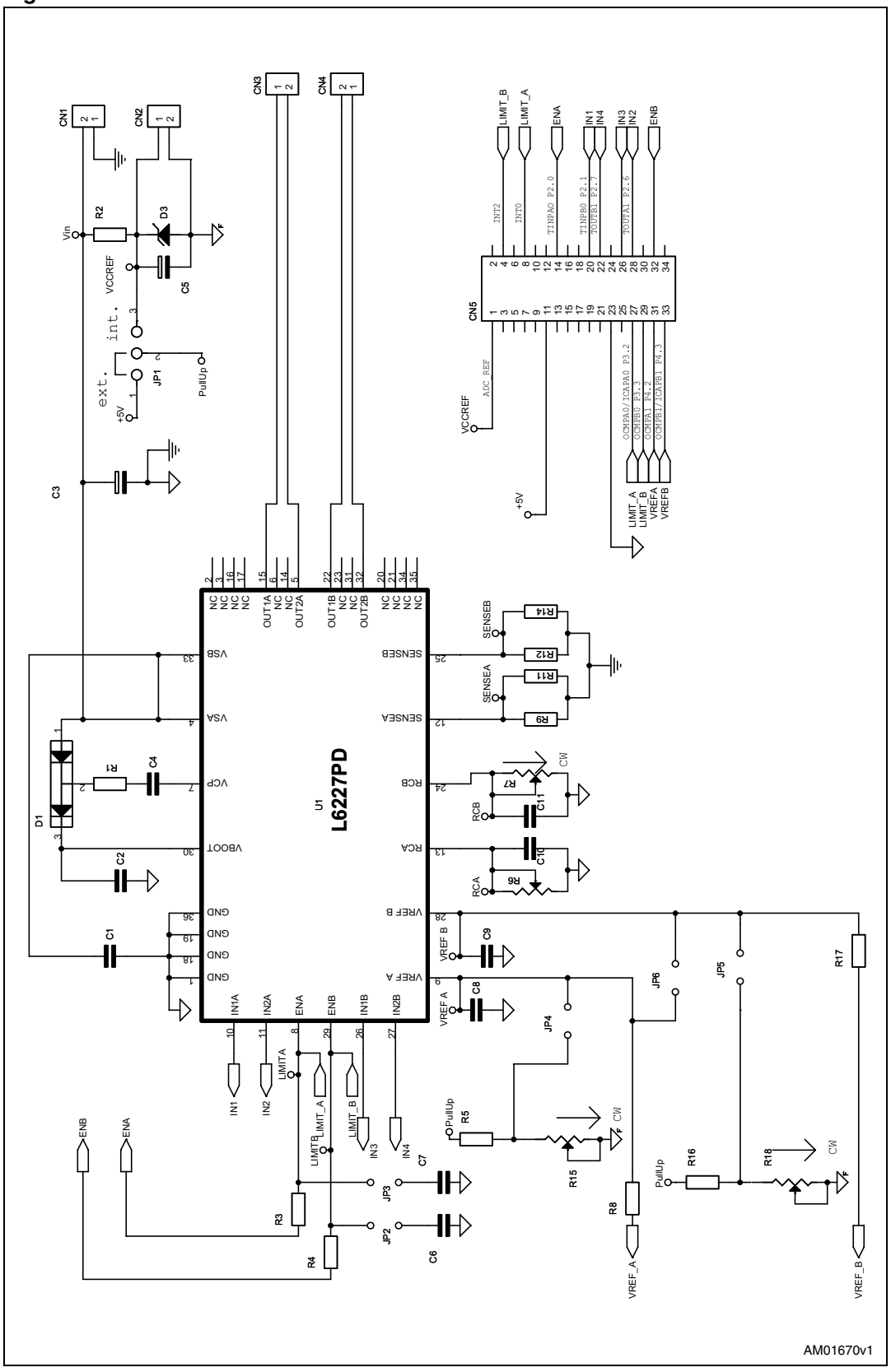


Figure 51. EVAL6227PD component placement

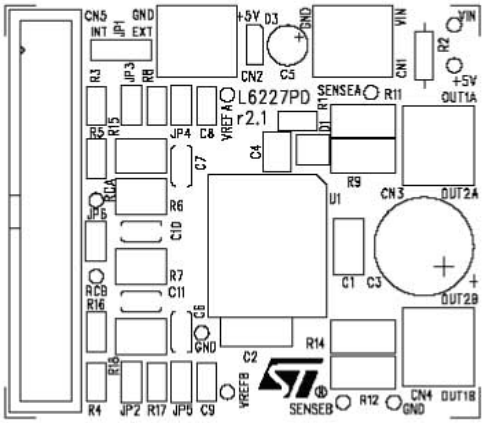


Figure 52. EVAL6227PD top layer layout

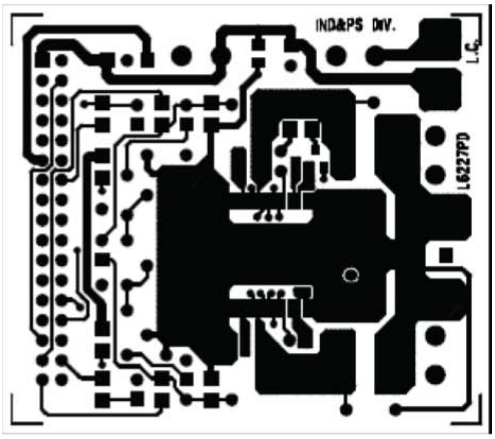
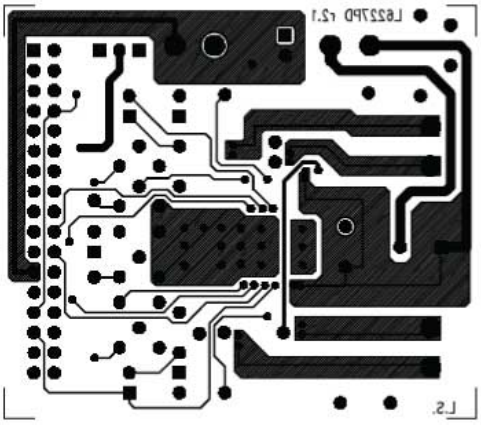


Figure 53. EVAL6227PD bottom layer layout



A.4 EVAL6226QR

A demonstration board has been produced to help the evaluation of the device in the QFN package. The board implemets a typical application that can be used as a reference design to drive a two-phase bipolar stepper motor up to 1 A DC, multiple DC motors and a wide range of inductive loads.

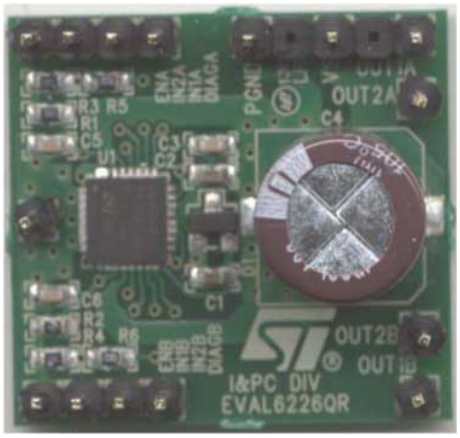
Thanks to the small footprint of L6226Q (QFN 5x5 mm 32 leads), the PCB is very compact (27x24.5 mm).

Figure 58 shows the electrical schematic of the board. *Table 6* gives the part list.

Table 6. EVAL6226QR part list

Part reference	Part value	Part description
C1	220 nF/25 V	Capacitor
C2	220 nF/63 V	Capacitor
C3	10 nF/25 V	Capacitor
C4	100 µF/63 V	Capacitor
C5, C6	5.6 nF	Capacitor
D1	BAT46SW	Diodes
R1, R2, R3, R4	100 kΩ 5% 0.25 W	Resistor
R5, R6	10 kΩ 1% 0.25 W	Resistor
R9, R10	0.4 Ω 1 W	Resistor
U1	L6226Q	Dual full bridge in VFQFPN5x5

Figure 54. EVAL6226QR



AM01674v1

The INx input pins drive the corresponding half bridge. When low logic level is applied, the low-side MOSFET is switched on whereas a high logic level turns on the high-side MOSFET.

Pins ENA and ENB are used to implement overcurrent and thermal protection by connecting them respectively to the outputs DIAGA and DIAGB.

The output current detection threshold is selectable by a resistor connected between the IC dedicated pins and ground.

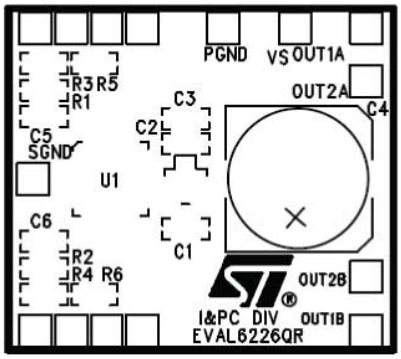
D1, C1 and C3 establish a charge pump circuit, which generates the supply voltage for the high-side integrated MOSFETs. Due to voltage and current switching at relatively high frequency, these components are connected together through short paths in order to minimize induced noise on other circuitries.

R1, R2 and C5, C6 are used by the overcurrent protection integrated circuitry (disable time $t_{DISABLE}$ is about 200 µs and delay time t_{DELAY} about 1 µs with the values in *Table 6*).

R5 and R6 are used to set the output current detection threshold at about 1.1 A typical value.

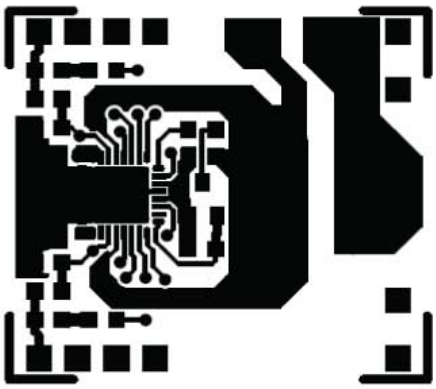
Figure 55 and *57* show the placement of the components and the two-layer layout of the EVAL6226QR reference design board. A GND area has been used to improve the IC power dissipation.

Figure 55. EVAL6226QR component placement



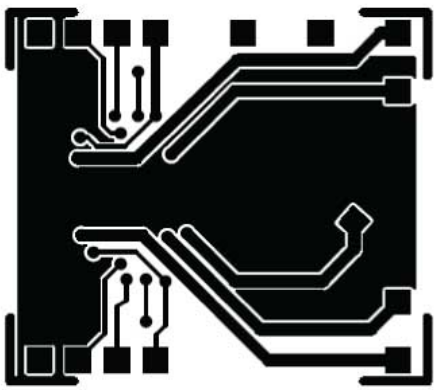
AM01675v1

Figure 56. EVAL6226QR top layer layout



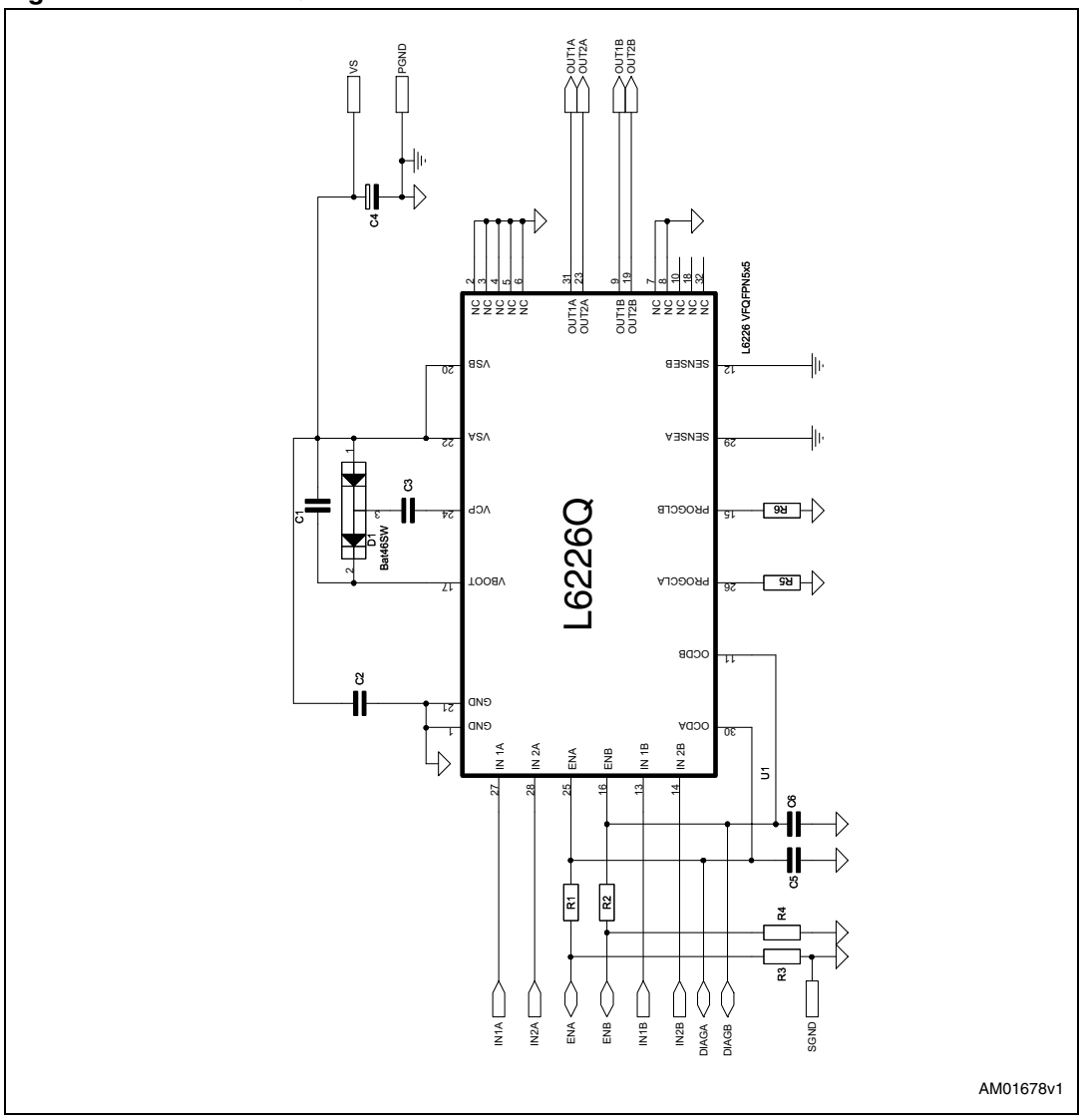
AM01676v1

Figure 57. EVAL6226QR bottom layer layout



AM01677v1

Figure 58. EVAL6226QR electrical schematic



A.5 EVAL6227QR

A demonstration board has been produced to help the evaluation of the device in a QFN package. The board implemets a typical application that can be used as a reference design to drive a two-phase bipolar stepper motor up to 1 A DC, multiple DC motors and a wide range of inductive loads.

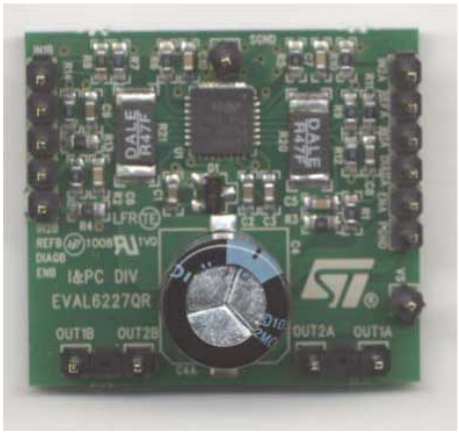
Thanks to the small footprint of L6227Q (QFN 5x5 mm 32 leads), the PCB is very compact (27x32 mm).

Figure 63 show the electrical schematic of the board. *Table 7* gives the part list.

Table 7. EVAL6226QR part list

Part reference	Part value	Part description
C1	220 nF/25 V	Capacitor
C2	220 nF/63 V	Capacitor
C3	10 nF/25 V	Capacitor
C4	100 µF/63 V	Capacitor
C5, C6	5.6 nF	Capacitor
C7, C10	820 pF	Capacitor
C8, C9	220 nF	Capacitor
D1	BAT46SW	Diodes
R1, R2, R3, R4, R7, R8, R9, R10	100 kΩ 5% 0.25 W	Resistor
R5, R6	10 kΩ 1% 0.25 W	Resistor
R11, R13	20 kΩ 5% 0.25 W	Resistor
R12, R14	2 kΩ 1% 0.25 W	Resistor
R20, R21	0.4 Ω 1 W	Resistor
U1	L6227Q	Dual full bridge in VFQFPN5x5

Figure 59. EVAL6226QR



AM01679v1

The INx input pins drive the corresponding half bridge. When low logic level is applied the low-side MOSFET is switched on whereas a high logic level turns on the high-side MOSFET.

To perform the PWM current control an analog reference voltage should be provided to each channel of the driver. A fixed reference voltage can be easily obtained through a resistive divider from an external voltage rail and GND (maybe the one supplying the µC or the rest of the application).

Otherwise a very simple way to obtain a variable voltage without using a DAC is to low-pass filter a PWM output of a µC.

D1, C1 and C3 establish a charge pump circuit, which generates the supply voltage for the high-side integrated MOSFETs. Due to voltage and current switching at relatively high frequency, these components are connected together through short paths in order to minimize induced noise on other circuitries.

R1, R2 and C5, C6 are used by the overcurrent protection integrated circuitry (disable time $t_{DISABLE}$ is about 200 µs and delay time t_{DELAY} about 1 µs with the values in *Table 7*).

R5, C7 and R6, C10 are used to set the off-time t_{OFF} of the two PWM channels at about 50 µs. The off-time should be adjusted according to the motor electrical characteristics and supply voltage, changing R5, C7 and R6, C10 values.

R11, R12, C8 and R13, R14, C9 are low-pass filters which provide an external reference voltage through a PWM output of a µC.

Figure 60 to *62* show the placement of the components and the two-layer layout of the EVAL6227QR reference design board. A GND area has been used to improve the IC power dissipation.

Figure 60. EVAL6227QR component placement

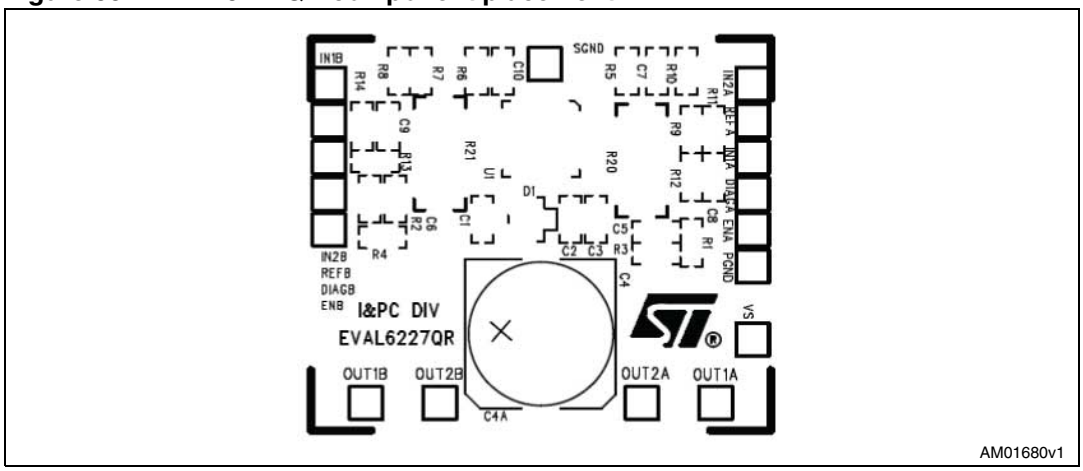


Figure 61. EVAL6227QR top layer layout

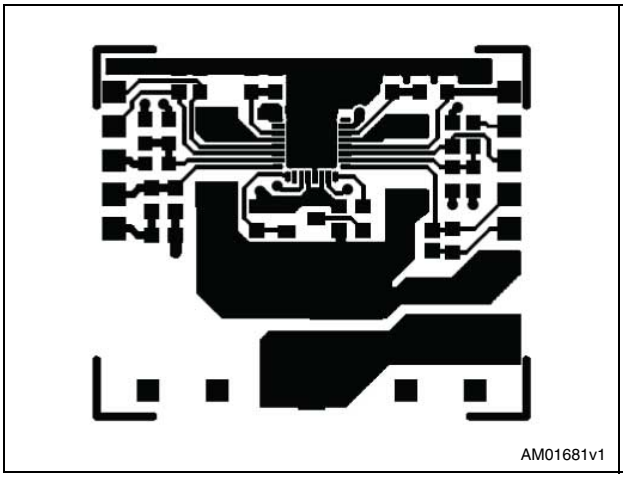


Figure 62. EVAL6227QR bottom layer layout

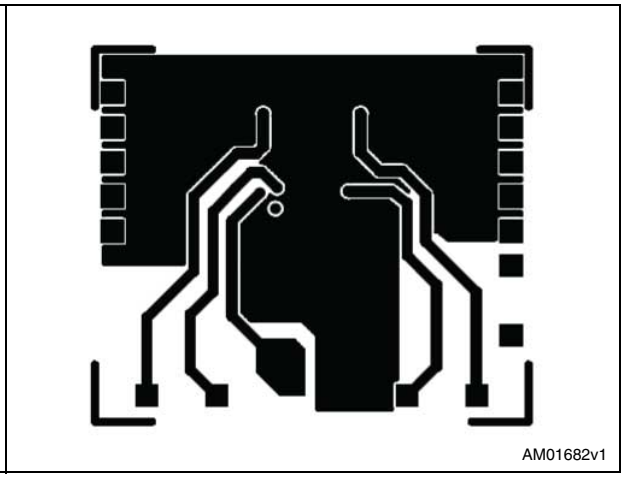
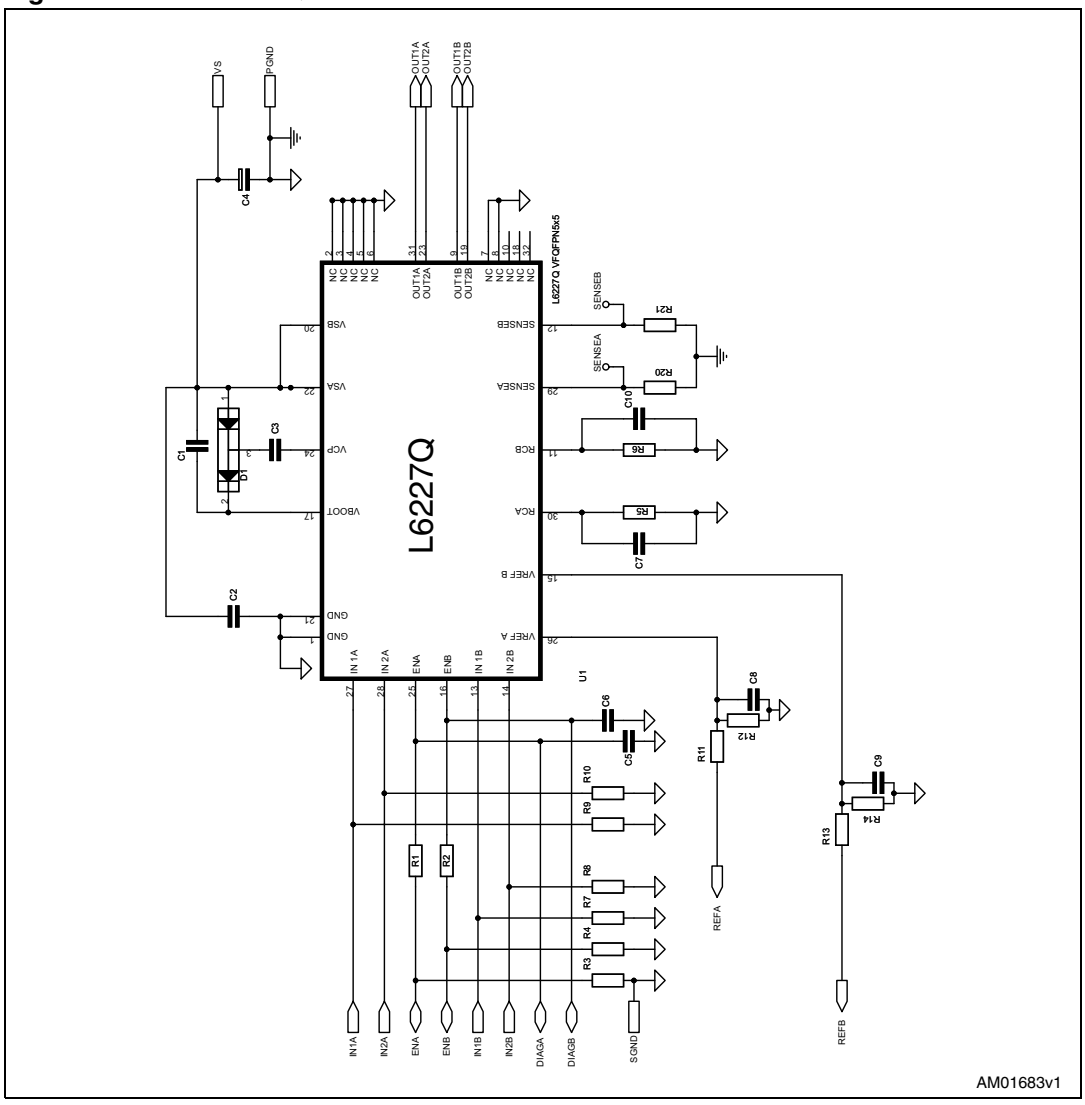


Figure 63. EVAL6227QR electrical schematic



Revision history

Table 8. Document revision history

Date	Revision	Changes
22-Jul-2009	1	Initial release