TEA1732CTS

GreenChip SMPS control IC

Rev. 1 — 18 March 2014 Product data sheet

1. General description

The TEA1732CTS is a low cost Switched Mode Power Supply (SMPS) controller IC intended for flyback topologies. The TEA1732CTS operates in peak current and frequency control mode. Frequency jitter has been implemented to reduce ElectroMagnetic Interference (EMI). Slope compensation is integrated for Continuous Conduction Mode (CCM) operation.

The TEA1732CTS IC features OverPower Protection (OPP). The controller accepts an overpower situation for a limited amount of time.

Mains undervoltage protection (brownout), output OverVoltage Protection (OVP), and OverTemperature Protection (OTP) can be implemented using a minimal number of external components.

At low-power levels, the primary peak current is set to 25 % of the maximum peak current. The switching frequency is reduced to limit the switching losses. The combination of fixed frequency operation at high output power and frequency reduction at low output power provides high efficiency over the total load range.

The TEA1732CTS makes the design of low-cost, highly efficient and reliable supplies for power requirements up to 75 W easier by requiring a minimum number of external components.

2. Features and benefits

- SMPS controller IC enabling low-cost applications
- Large input voltage range (12 V to 30 V)
- Integrated OverVoltage Protection (OVP) on the VCC pin
- Accurate OverVoltage Protection (OVP) via the ISENSE pin
- Very low supply current during start-up and restart (10 μA typical)
- Low supply current during normal operation (0.58 mA typical without load)
- Internal overpower time-out
- Overpower protection or high/low line compensation
- Fixed switching frequency with frequency jitter to reduce EMI
- Frequency reduction with fixed minimum peak current to maintain high efficiency at low output power levels
- Frequency increase at peak power operation
- Slope compensation for CCM operation
- Integrated soft-start

- Low and adjustable OverCurrent Protection (OCP) trip level
- Mains undervoltage protection (brownout)
- External OverTemperature Protection (OTP)
- IC overtemperature protection

3. Applications

- All applications that require an efficient and cost-effective power supply solution up to 75 W.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1732CTS/1	TSOP6	plastic surface-mounted package; 6 leads	SOT457

5. Block diagram

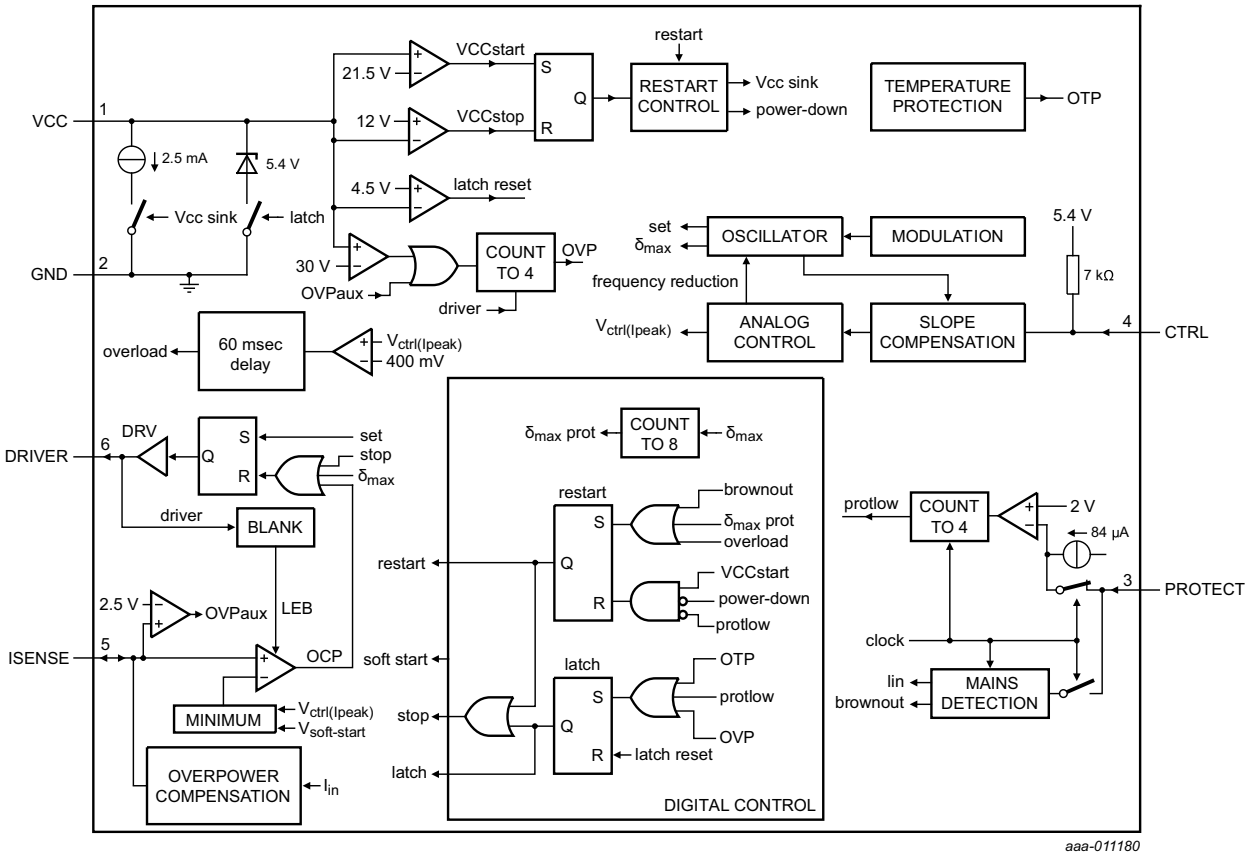


Fig 1. TEA1732CTS block diagram

6. Pinning information

6.1 Pinning

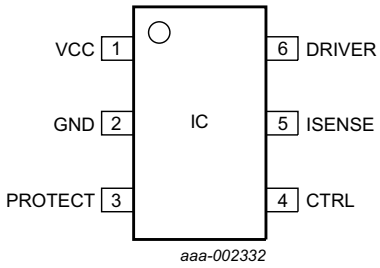


Fig 2. TEA1732CTS pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
VCC	1	supply voltage
GND	2	ground
PROTECT	3	protection and mains detect input
CTRL	4	control input
ISENSE	5	current sense and accurate OVP input
DRIVER	6	gate driver output

7. Functional description

7.1 General control

The TEA1732CTS contains a controller for a flyback circuit. A typical configuration is shown in Figure 3.

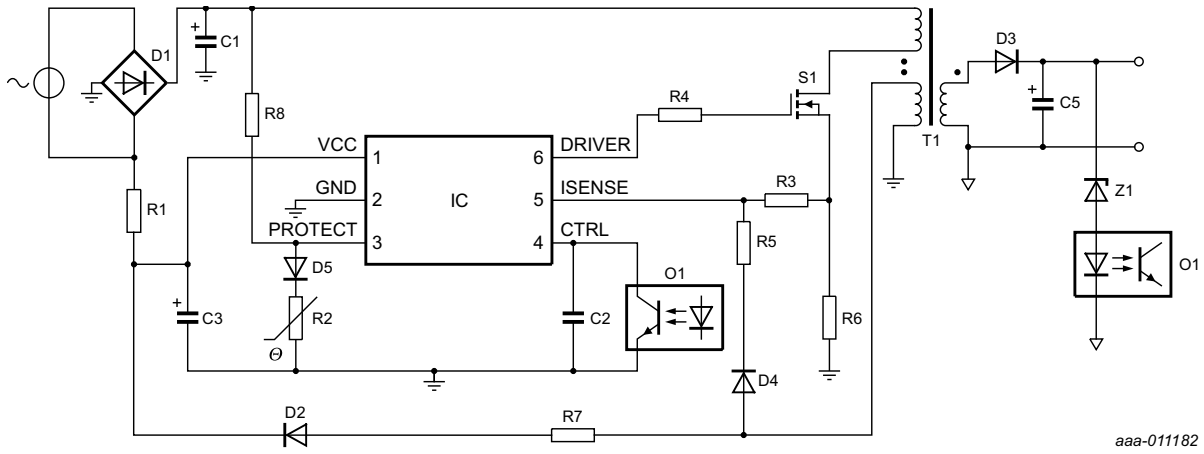


Fig 3. TEA1732CTS typical configuration

7.2 Start-up and UnderVoltage LockOut (UVLO)

Initially, the capacitor on the VCC pin, C3, is charged from the high-voltage mains via resistor R1.

As long as VCC is below $V_{startup}$, the IC current consumption is low (10 μA typical). When VCC reaches $V_{startup}$, the IC first waits for the mains voltage to exceed the brownin level, and the PROTECT pin to reach the $V_{det(PROTECT)(L)}$ voltage. When both conditions are met, the IC starts switching. An internal soft-start time of 3.5 ms allows the ISENSE peak voltage to increase gradually to prevent audible noise. In a typical application, the auxiliary winding of the transformer takes over the supply voltage.

If a protection is triggered, the controller stops switching. Depending on the protection triggered, it either causes a restart or latches the converter to an off-state.

The OPP, UVLO, brownout, maximum duty cycle, OVP, and external OTP protections cause a save restart. The internal OTP protection latches the converter to an off-state.

A restart protection disables the switching of the IC. The supply voltage of the IC drops to the UVLO level. When the UVLO level is reached, the IC switches to Power-down mode, where it consumes a low supply current (10 μA typical). The VCC capacitor is recharged via R1 until the VCC start-up level is reached. A delayed restart is performed to lower the average input power during a fault condition. Depending on the cause of the restart protection, the restart sequence that discharges and recharges the VCC capacitor is performed once or repeated three times, before switching recommences (See Figure 4).

When a latched protection is triggered, the TEA1732CTS immediately enters Power-down mode. The VCC pin is clamped to a voltage just above the latch protection reset voltage ($V_{rst(latch)}$ + 0.9 V).

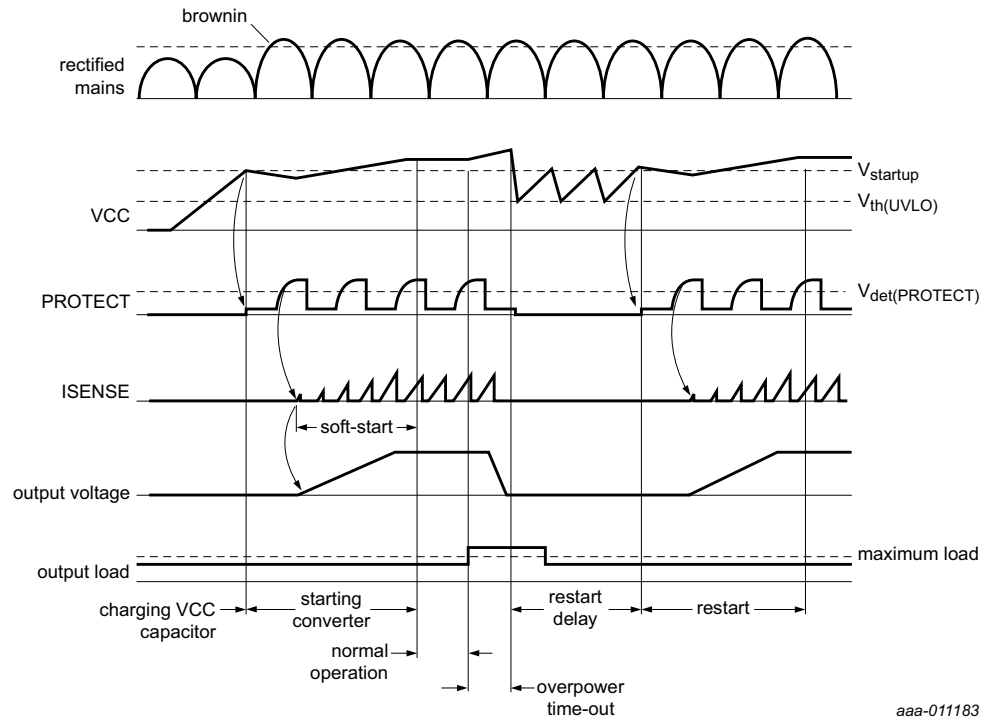


Fig 4. Start-up sequence, normal operation and restart sequence

When the voltage on pin VCC drops below the $V_{th(UVLO)}$ level during normal operation, the controller stops switching. The TEA1732CTS waits for the rectified mains to charge the VCC pin using resistor R1.

7.3 Supply management

All internal reference voltages are derived from a temperature compensated on-chip band gap circuit. Internal reference currents are derived from a trimmed and temperature compensated current reference circuit.

7.4 External overtemperature protection and mains detect input (pin PROTECT)

The PROTECT input combines the functions of the external OverTemperature Protection (OTP) and the mains voltage detection. An internal clock separates the period of measuring the mains voltage and the period of detecting external OverTemperature Protection (OTP). In a typical application, the PROTECT pin is connected to the mains via a resistor. It is connected to ground via a negative temperature coefficient (NTC) thermistor and a diode.

When measuring the mains voltage, the PROTECT pin is regulated to 0.25 V so that the external diode does not conduct any current. The current into the PROTECT pin is measured and stored. Once the measured current is above the brownin level, the system is allowed to start switching. If the mains voltage is continuously below the brownout level for at least 32 ms, a brownout is detected. The system immediately stops switching and performs a restart. The VCC capacitor is discharged to the UVLO level and then charged to $V_{startup}$ once before switching recommences (See Figure 5).

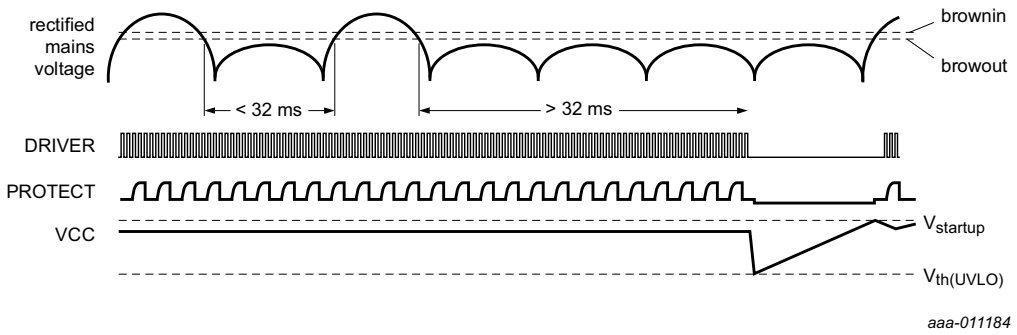


Fig 5. Mains detection

When detecting the external temperature, a current of 84 μA (typical) out of the PROTECT pin flows through the external capacitor and the NTC thermistor. If the PROTECT voltage at the end of the measuring period is below $V_{det(PROTECT)}$ for four consecutive measuring cycles, the IC detects overtemperature and activates a latched protection.

The offset due to the current from the mains is canceled internally by remembering the sinking current I_{in} when measuring the mains voltage (See Figure 6). The remembered current is also used as the input of high/low line compensation.

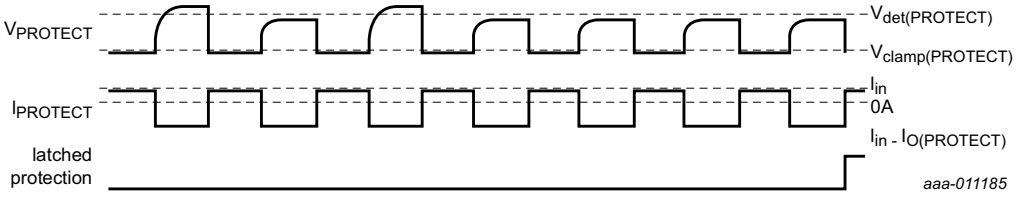


Fig 6. External overtemperature protection

An internal clamp of 4.1 V (typical) protects this pin from excessive voltages.

7.5 Duty cycle control (pin CTRL)

Pin CTRL regulates the output power of the converter. This pin is connected to an internal voltage source of 5.4 V via an internal resistor (typical resistance: 7 kΩ).

The CTRL pin voltage sets the peak current which is measured using the ISENSE pin (see Section 7.8). At low output power, the switching frequency is reduced (see Section 7.11). The maximum duty cycle is limited to 80 % (typical).

After eight consecutive converter strokes at maximum duty cycle the restart protection is activated. In a restart, the VCC capacitor is quickly discharged to the $V_{th(UVLO)}$ level and recharged to the start-up level from the high-voltage mains, before switching recommences. This occurs when the mains input voltage is removed.

7.6 Slope compensation (pin CTRL)

A slope compensation circuit is integrated for CCM. The slope compensation guarantees stable operation for duty cycles exceeding 50 %.

7.7 Overpower timer

A temporary overload situation is allowed. If $V_{ctrl(Ipeak)}$ (see Figure 1) set by pin CTRL exceeds 400 mV, an internal timer is started. If the overload situation continues to exist for more than 60 ms (typical), an OverPower Protection (OPP) is triggered (see Figure 7).

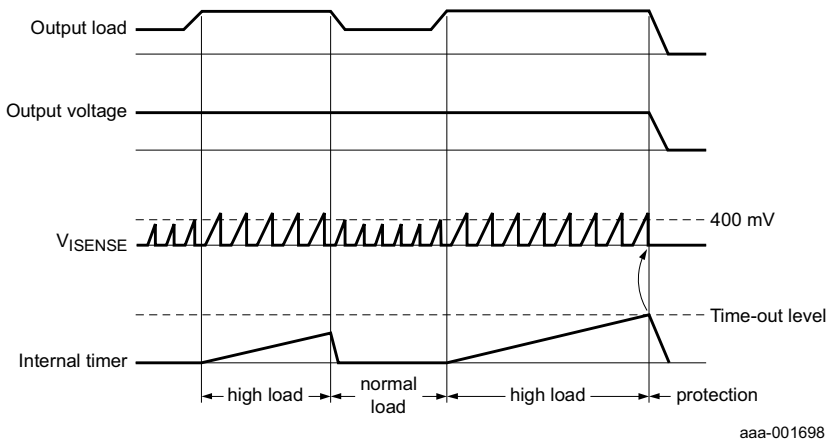


Fig 7. Overpower delay

The TEA1732CTS enters the overpower restart mode when the overload time-out is reached. In overpower restart mode, the VCC capacitor is discharged to UVLO level and then charged to the start-up level three times before the converter switches again.

7.8 Current mode control (pin ISENSE)

Current mode control is used because it ensures a good line regulation.

Pin ISENSE senses the primary current across external resistor R6 and compares it with an internal control voltage. The internal control voltage is proportional to the CTRL pin voltage (see Figure 8).

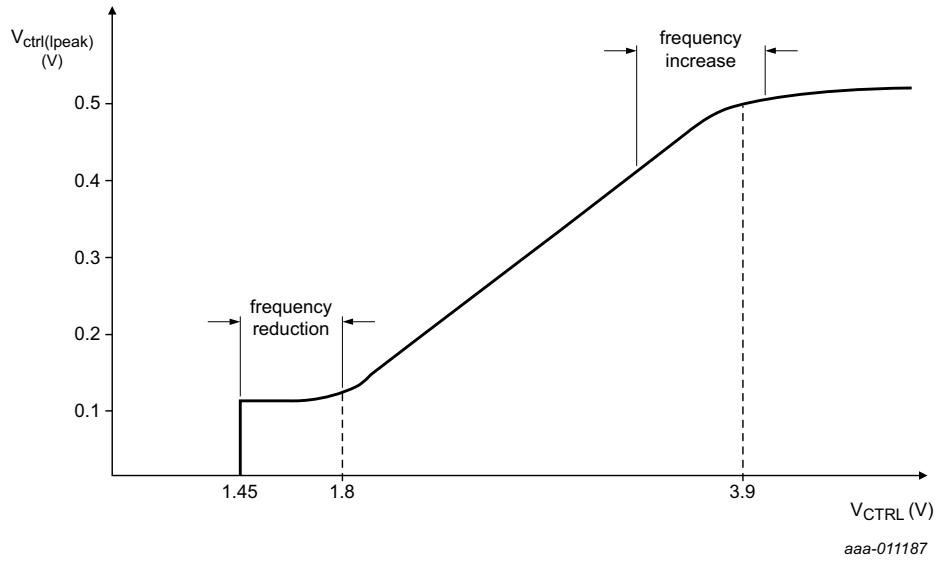


Fig 8. Peak current control

Leading edge blanking prevents false triggering due to capacitive discharge when switching on the external power switch (see Figure 9).

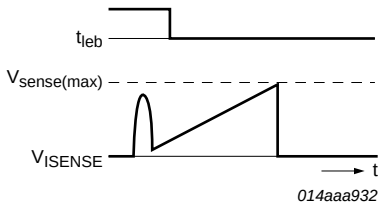


Fig 9. Leading edge blanking

7.9 Overvoltage protection (pin ISENSE)

Accurate overvoltage protection can be realized at the ISENSE pin by sensing the auxiliary voltage. During the primary stroke, diode D4 (see Figure 3) is blocked so that the converter still works under current mode control. During the secondary stroke, the ISENSE voltage represents the output voltage via the resistor divider R5 and R3 (see Figure 3). The ISENSE voltage is sampled 2 μs after the gate signal drops to avoid the ringing of the transformer. If the sampled voltage exceeds $V_{ovp(ISENSE)}$ for four consecutive switching cycles, the IC triggers the latched protection.

7.10 Overvoltage protection (pin VCC)

An OverVoltage Protection (OVP) circuit is connected to the VCC pin. When the V_{CC} exceeds $V_{th(OVP)}$ (30 V typical) for four consecutive switching cycles, the IC triggers the latched protection. When V_{CC} drops below $V_{th(OVP)}$ before count = 4 is reached, the counter is reset to zero.

7.11 Peak power, high-power and low-power operation

During high-power operation, with the converter running at a 65 kHz (typical) fixed frequency, the power is controlled by varying the peak current. A peak power mode is implemented to supply a short overload situation. In peak power mode, both frequency and peak current are increased.

In low-power operation switching losses are reduced by lowering the switching frequency.

The switching frequency of the converter is reduced while the peak current is set to 25 % of the maximum peak current (see Figure 8 and Figure 10).

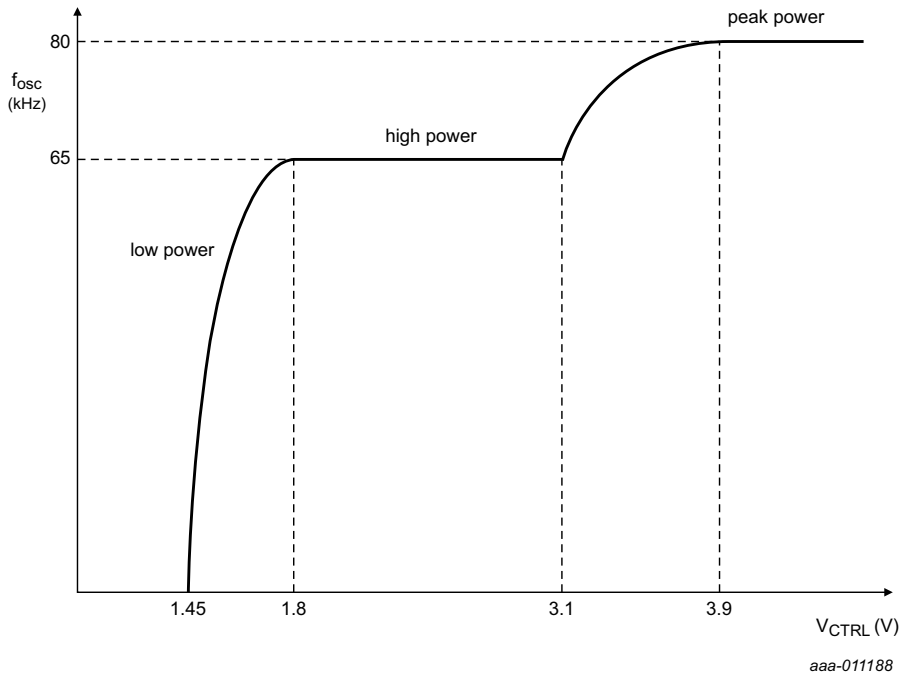


Fig 10. Frequency control

7.12 Overpower or high/low line compensation

The overpower compensation function can be used to realize a maximum output power which is nearly constant over the full input mains. The overpower compensation circuit measures the input current on the PROTECT pin and outputs a proportionally dependent current on the ISENSE pin. The DC voltage across resistor R3 (see Figure 3) limits the maximum peak current on the current sense resistor (see Figure 11).

At low output power levels, the overpower compensation circuit is switched off.

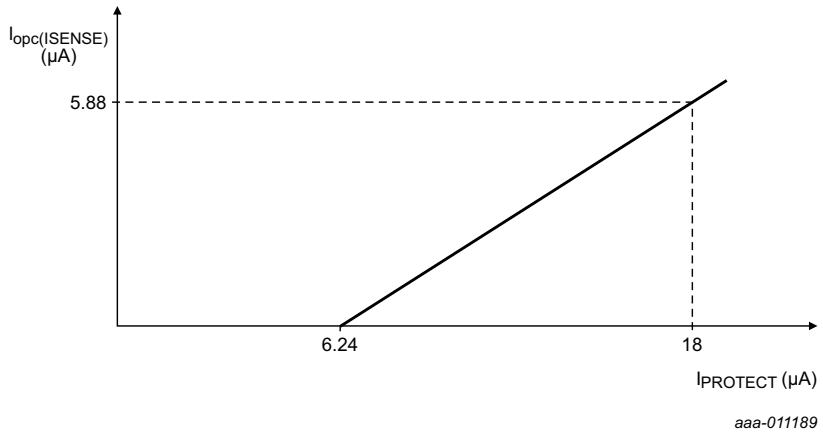


Fig 11. Overpower compensation

7.13 Driver (pin DRIVER)

The driver circuit to the gate of the power MOSFET has a current sourcing capability of typically 300 mA and a current sink capability of typically 750 mA. This enables a fast turn-on and turn-off of the power MOSFET for efficient operation.

7.14 OverTemperature Protection (OTP)

If the junction temperature exceeds the thermal shutdown limit, integrated overtemperature protection ensures that the IC stops switching.

OTP is a latched protection. It can be reset by removing the voltage on pin VCC.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{CC}	supply voltage	continuous	–0.4	+30	V
		t < 100 ms	-	35	V
$V_{PROTECT}$	voltage on pin PROTECT	current limited	–0.4	+5	V
V_{CTRL}	voltage on pin CTRL		–0.4	+5.5	V
V_{ISENSE}	voltage on pin ISENSE	current limited to 2 mA	–0.7	+5	V
Currents					
I_{VCC}	current on pin VCC	δ < 10 %	-	0.4	A
$I_{I(PROTECT)}$	input current on pin PROTECT		–1	+1	mA
I_{CTRL}	current on pin CTRL		–3	0	mA
I_{ISENSE}	current on pin ISENSE		–10	+0.5	mA
I_{DRIVER}	current on pin DRIVER	δ < 10 %	–0.4	+1	A
General					
P_{tot}	total power dissipation	T_{amb} < 75 °C	-	0.29	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–40	+150	°C
ESD					
V_{ESD}	electrostatic discharge voltage	class 1			
		human body model [1]	-	4000	V
		changed device model	-	750	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; single layer JEDEC test board	259	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	in free air; JEDEC test board	152	K/W

10. Characteristics

Table 5. Characteristics

Tamb = 25 °C; VCC = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage management (pin VCC)						
$V_{startup}$	start-up voltage		19.3	21.5	23.8	V
$V_{th(UVLO)}$	undervoltage lockout threshold voltage		11.2	12.5	13.8	V
$V_{clamp(VCC)}$	clamp voltage on pin VCC	activated during latched protection; I_{CC} = 100 μA	-	$V_{rst(latch)}$ + 0.9	-	V
		activated during latched protection, I_{CC} = 1 mA	-	-	$V_{rst(latch)}$ + 3.5	V
$I_{CC(restart)}$	restart supply current		1	2.5	-	mA
V_{hys}	hysteresis voltage	$V_{startup}$ - $V_{th(UVLO)}$	6.6	9.1	11.6	V
$I_{CC(startup)}$	start-up supply current	V_{CC} < $V_{startup}$	5	10	15	μA
$I_{CC(oper)}$	operating supply current	no-load on pin DRIVER; δ = 2 %; excluding optocurrent	-	0.58	-	mA
		no-load on pin DRIVER; δ = 25 %, excluding optocurrent	-	0.62	-	mA
$V_{rst(latch)}$	latched reset voltage		3.5	4.5	5.5	V
Protection input (pin PROTECT)						
$V_{det(PROTECT)}$	detection voltage on pin PROTECT		1.95	2	2.05	V
$I_{O(PROTECT)}$	output current on pin PROTECT	$V_{PROTECT}$ = $V_{det(PROTECT)}$)	–89	–84	–79	μA
$V_{clamp(PROTECT)}$	clamp voltage on pin PROTECT	$I_{I(PROTECT)}$ = 6 μA; mains detect period; $C_{max(PROTECT)}$ = 10 pF	205	260	315	mV
		$I_{I(PROTECT)}$ = 200 μA [1]	3.5	4.1	4.7	V
Mains detect (pin PROTECT)						
$I_{mains(bi)}$	mains brownin current		5.58	6	6.42	μA
$I_{mains(bo)}$	mains brownout current		4.93	5.3	5.67	μA
Peak current control (pin CTRL)						
V_{CTRL}	voltage on pin CTRL	for minimum flyback peak current	1.5	1.8	2.1	V
		for maximum flyback peak current	3.4	3.9	4.3	V
$R_{int(CTRL)}$	internal resistance on pin CTRL		5	7	9	kΩ
$I_{O(CTRL)}$	output current on pin CTRL	V_{CTRL} = 1.4 V	–0.7	–0.5	–0.3	mA
		V_{CTRL} = 3.7 V	–0.28	–0.2	–0.12	mA

Table 5. Characteristics *...continued*

Tamb = 25 °C; VCC = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pulse width modulator						
f_{osc}	oscillator frequency	peak power	73	80	87	kHz
		high power	60.5	65	69.5	kHz
f_{mod}	modulation frequency		195	260	325	Hz
Δf_{mod}	modulation frequency variation	high power	±3	±4	±5	kHz
δ_{max}	maximum duty cycle		77	80	83	%
$N_{cy(dmax)}$	number of switching cycles with maximum duty cycle		7	-	8	
$V_{start(red)f}$	frequency reduction start voltage	pin CTRL dropping to low power	1.5	1.8	2.1	V
$V_{start(incr)f}$	frequency increase start voltage	pin CTRL	2.8	3.1	3.4	V
$V_{M(f)max}$	maximum frequency peak voltage	pin CTRL	3.6	3.9	4.2	V
$V_{\delta(zero)}$	zero duty cycle voltage	pin CTRL	1.15	1.45	1.75	V
Overpower protection						
$t_{to(opp)}$	overpower protection time-out time		45	60	75	ms
Current sense and overpower compensation (pin ISENSE)						
$V_{sense(max)}$	maximum sense voltage	$\Delta V/\Delta t$ = 0 V/s	0.47	0.50	0.53	V
$t_{PD(sense)}$	sense propagation delay		130	155	180	ns
$V_{th(sense)opp}$	overpower protection sense threshold voltage		370	400	430	mV
$\Delta V_{ISENSE}/\Delta t$	slope compensation voltage on pin ISENSE	high-power mode	-	20	-	mV/µs
t_{leb}	leading edge blanking time		275	325	375	ns
$I_{opc(ISENSE)}$	overpower compensation current on pin ISENSE	$I_{PROTECT}$ = 10 µA; $V_{sense(max)}$ > 400 mV	–1	–1.88	–3	µA
		$I_{PROTECT}$ = 18 µA; $V_{sense(max)}$ > 400 mV	–5	–5.88	–7	µA
Soft start (pin ISENSE)						
$t_{start(soft)}$	soft start time		2.7	3.5	4.2	ms
Driver (pin DRIVER)						
$I_{source(DRIVER)}$	source current on pin DRIVER	V_{DRIVER} = 2 V	-	–0.3	–0.25	A

Table 5. Characteristics *…continued*

Tamb = 25 °C; VCC = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{sink(DRIVER)}$	sink current on pin DRIVER	V_{DRIVER} = 2 V	0.25	0.3	-	A
		V_{DRIVER} = 10 V	0.6	0.75	-	A
$V_{O(DRIVER)max}$	maximum output voltage on pin DRIVER		9	10.5	12	V
Overvoltage protection (pins VCC and ISENSE)						
$V_{ovp(VCC)}$	overvoltage protection voltage on pin VCC		29	30	31	V
$V_{ovp(ISENSE)}$	overvoltage protection voltage on pin ISENSE		2.4	2.5	2.6	V
$t_{blank(ovp)ISENSE}$	overvoltage protection blanking time on pin ISENSE		1.7	2.1	2.5	µs
$N_{cy(ovp)}$	number of overvoltage protection cycles		4	4	4	
Temperature protection						
$T_{pl(IC)}$	IC protection level temperature		130	140	150	°C

[1] The clamp voltage on the PROTECT pin is lowered when the IC is in Power-down mode. (latched or restart protection)

11. Application information

A power supply with the TEA1732CTS is a flyback converter operating in continuous conduction mode (see Figure 12).

Capacitor C3 buffers the IC supply voltage, which is powered via resistor R1 for start-up and via the auxiliary winding during normal operation. Sense resistor R6 converts the current through MOSFET S1 into a voltage on pin ISENSE. The value of resistor R6 defines the maximum primary peak current through MOSFET S1.

Capacitor C2 is added to reduce noise on the CTRL pin.

Resistor R4 is required to limit the current spikes to pin DRIVER because of parasitic inductance of current sense resistor R6. Resistor R4 also dampens possible oscillations of MOSFET S1. Adding a bead on the gate pin of MOSFET S1 can be required to prevent local oscillations of the MOSFET.

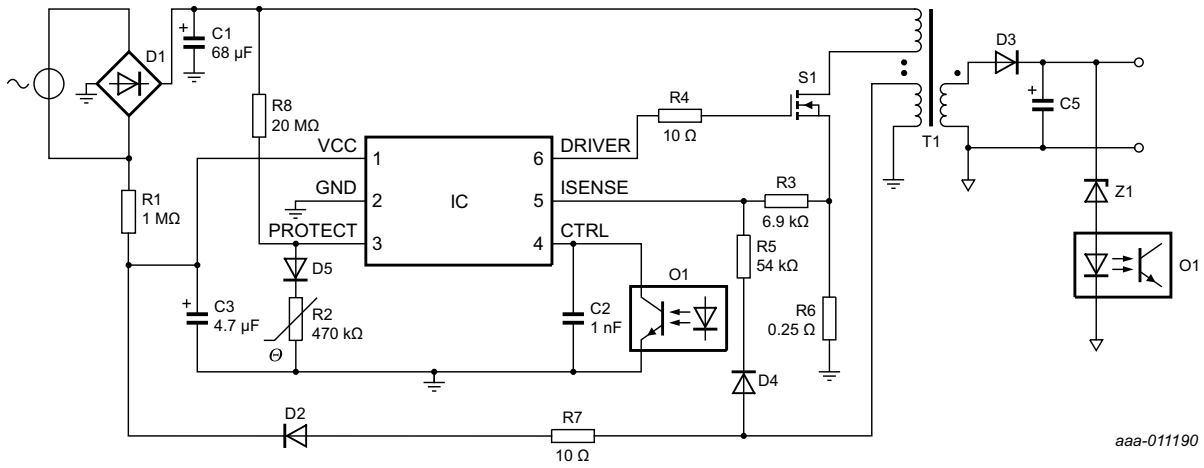
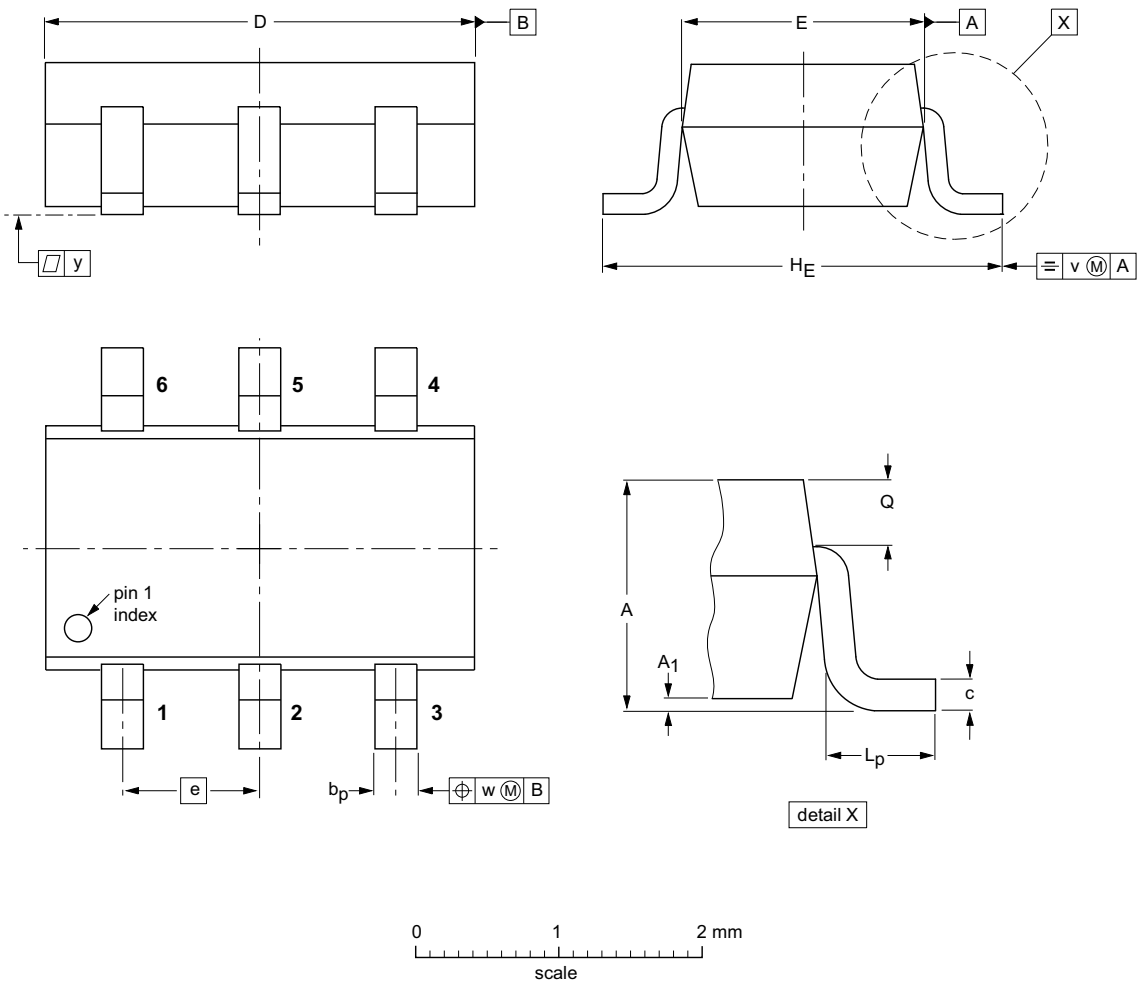


Fig 12. TEA1732CTS application diagram

12. Package outline

Plastic surface-mounted package (TSOP6); 6 leads **SOT457**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT457			SC-74			~~05-11-07~~ 06-03-16

Fig 13. Package outline SOT457 (TSOP6)

13. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1732CTS v.1	20140318	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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15. Contact information

For more information, please visit: **http://www.nxp.com**

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16. Contents

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