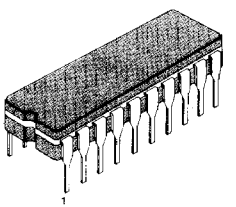
COMBO CODEC

The KT3064 (μ-law), is monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion, a serial PCM interface. The devices are fabricated using double-poly CMOS process. The device feature an additional receive power amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to $\pm 6.6V$ across a balanced 600Ω load. The Analog Loopback switch and $\overline{TS_X}$ output is also included.

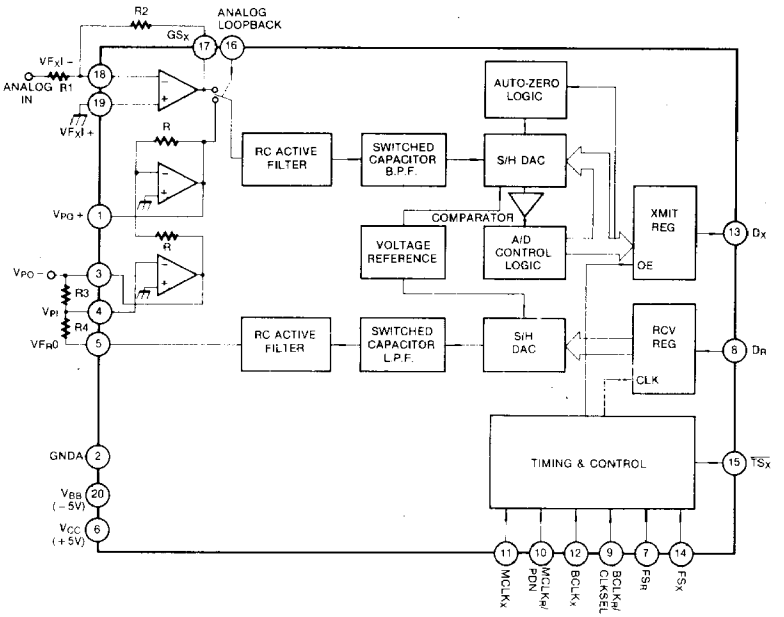
20 CERDIP



FEATURES

- **μ-law compatible**
- **Meets or exceeds all D3/D4 and CCITT specifications**
- **$\pm 5V$ operation**
- **Low operating power: typically 70mW**
- **Active RC noise filters**
- **Power-down standby mode: typically 3mW**
- **Automatic power-down**
- **Transmit high-pass and low-pass filtering**
- **Internal precision voltage reference**
- **Serial I/O interface**
- **Internal auto-zero circuitry**
- **TTL or CMOS compatible digital interface**
- **Maximizes line interface card circuit density**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
V_{CC} to GNDA	V_{CC}	7	V
V_{BB} to GNDA	V_{BB}	−7	V
Voltage at Any Analog Input or Output	Analoge I/O	$V_{CC}+0.3$ to $V_{BB}-0.3$	V
Voltage at Any Digital Input or Output	Digital I/O	$V_{CC}+0.3$ to GNDA − 0.3	V
Operating Temperature Range	T_a	−25 ~ +125	°C
Storage Temperature Range	T_s	−65 ~ +150	°C
Lead Temperature Soldering, 10 secs)	T_L	300	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted: $V_{CC}=5.0V\pm5\%$, $V_{BB}=-5V\pm5\%$, GNDA = 0V, Ta = 0°C to 70°C; typical characteristics specified at $V_{CC}=5.0V$, Ta = 25°C; all signals are referenced to GNDA)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Power Dissipation						
Active Current	$I_{CC}1$	Power amplifiers active, VPI = 0V		7.0	10.0	mA
Active Current	$I_{BB}1$	Power amplifiers active, VPI = 0V		7.0	10.0	mA
Power-Down Current	I_{CCO}			0.5	1.5	mA
Power-Down Current	I_{BBO}			0.05	0.3	mA
Digital Interface						
Input Low Current	I_{IL}	$GNDA\le V_{IN}\le V_{IL}$, All digital inputs	−10		10	μA
Input High Current	I_{IH}	$V_{IH}\le V_{IN}\le V_{CC}$	−10		10	μA
Output Current in High Impedance State (TRI-STATE)	I_{OZ}	D_X, $GNDA\le V_O\le V_{CC}$	−10		10	μA
Input Low Voltage	V_{IL}				0.6	V
Input High Voltage	V_{IH}		2.2			V
Output Low Voltage	V_{OL}	D_X, $I_L=3.2mA$ SIG_R, $I_L=1.0mA$ $\overline{T_{SX}}$, $I_L=3.2mA$, Open Drain			0.4 0.4 0.4	V
Output High Voltage	V_{OH}	D_X, $I_H=-3.2mA$ SIG_R, $I_H=-1.0mA$	2.4 2.4			V
Analog Interface with Transmit Input Amplifier						
Input Leakage Current	I_IXA	$-2.5V\le V\le+2.5V$, VFxI+ or VFxI−	−200		200	nA
Input Resistance	R_IXA	$-2.5V\le V\le+2.5V$, VFxI+ or VFxI−	10			MΩ
Output Resistance	R_OXA	Closed loop, unity gain		1	3	MΩ
Load Resistance	R_LXA	GS_X	10			KΩ
Load Capacitance	C_LXA	GS_X			50	pF
Output Dynamic Range	V_OXA	GS_X, $R_L\ge10K\Omega$	±2.8			V

ELECTRICAL CHARACTERISTICS (Continued)

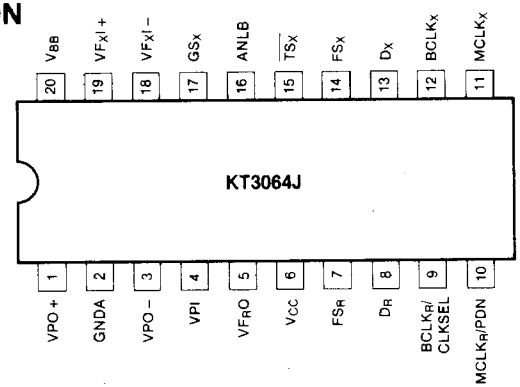
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Voltage Gain	A_VXA	VF_XI+ to GS_X	5000			V/V
Unit-Gain Bandwidth	F_UXA		1	2		MHz
Offset Voltage	$V_{OS}XA$		−20		20	mV
Common-Mode Voltage	$V_{CM}XA$	CMRRXA>60dB	−2.5		2.5	V
Common-Mode Rejection Ratio	CMRRXA	DC Test	60			dB
Power Supply Rejection Ratio	PSRRXA	DC Test	60			dB
Analog Interface with Receive Filter (All Devices)						
Output Resistance	R_ORF	Pin VF_RO		1	3	Ω
Output DC Offset Voltage	VOS_RO	Measure from VF_RO to GND A	−200		200	mV
Load Resistance	R_LRF	$VF_RO = \pm 2.5V$	10			KΩ
Load Capacitance	C_LRF	Connect from VF_RO to GND A			25	pF
Analog Interface with Power Amplifiers (All Devices)						
Input Leakage Current	IPI	$-1.0V \leq VPI \leq 1.0V \leq VPI \leq 1.0V$	−100		100	nA
Input Resistance	RIPI	$-1.0V \leq VPI \leq 1.0V$	10			MΩ
Input Offset Voltage	VI_{OS}		−25		25	mV
Output Resistance	ROP	Inverting unity gain at VPO+ or VPO−		1		Ω
Unit-Gain Bandwidth	F_C	Open loop (VPO−)		400		KHz
Load Capacitance	C_{LP}	$R_L \geq 1500\Omega$ VPO+ or $R_L = 600\Omega$ VPO− to $R_L = 300\Omega$ GNDA			100 500 1000	pF pF pF
Gain from VPO− to VPO+	GA_P+	$R_L = 300\Omega$ VPO+ to GNDA level at VPO− = −1.77Vrms (+3dBmo)		−1		V/V
Power Supply Rejection of V_{CC} or V_{BB}	$PSRR_P$	VPO− connected to VPI 0KHz−4KHz 0KHz−50KHz	 60 36			 dB dB
Frequency of Master Clock	I/t_{PM}	Depends on the device used and the $BCLK_R$/CLKSEL Pin $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
Width of Master Clock High	t_{WMH}	$MCLK_X$ and $MCLK_R$	160			ns
Width of Master Clock Low	t_{WML}	$MCLK_X$ and $MCLK_R$	160			ns
Rise Time of Master Clock	t_{RM}	$MCLK_X$ and $MCLK_R$			50	ns
Fall Time of Master Clock	t_{FM}	$MCLK_X$ and $MCLK_R$			50	ns
Set-Up Time from $BCLK_X$ High (and FS_X in Long Frame Sync Mode) to $MCLK_X$ Falling Edge	t_{SBFM}	First bit clock after the leading edge of FS_X	100			ns
Period of Bit Clock	t_{PB}		485	488	15,725	ns
Width of Bit Clock High	t_{WBH}	$V_{IH} = 2.2V$	160			ns
Width of Bit Clock Low	t_{WBL}	$V_{IL} = 0.6V$	160			ns
Rise Time of Bit Clock	t_{RB}	$t_{PB} = 480ns$			50	ns
Fall Time of Bit Clock	t_{FB}	$t_{PB} = 488ns$			50	ns

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Holding Time from Bit Clock Low to Frame Sync	t_{HBF}	Long frame only	0			ns
Holding Time from Bit Clock High to Frame Sync	t_{HOLD}	Short frame only	0			ns
Set-Up Time for Frame Sync to Bit Clock Low	t_{SFB}	Long Frame Only	80			ns
Delay Time from $BCLK_X$ High to Data Valid	t_{DBD}	Load = 150pF plus 2 LSTTL loads	0		180	ns
Delay Time to TS_X Low	t_{XDP}	Load = 150pF plus 2 LSTTL loads			140	ns
Delay Time from $BCLK_X$ Low to Data Output Disabled	t_{DEC}		50		165	ns
Delay Time to Valid Data from FS_X or $BCLK_X$, whichever Comes Later	t_{DZF}	C_L = 0pF to 150pF	20		165	ns
Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low	t_{SDB}		50			ns
Hold Time from $BCLK_{R/X}$ Low to D_R Invalid	t_{HBD}		50			ns
Delay Time from $BCLK_{R/X}$ Low to SIG_R Valid	t_{DFSSF}	Load = 50pF plus 2 LSTTL loads			300	ns
Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	t_{SF}	Short frame sync pulse (1 or 2 bit clock periods long)(Note 1)	50			ns
Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	t_{HF}	Short frame sync pulse (1 or 2 bit clock periods long)(Note 1)	100			ns
Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X of FS_R)	t_{HBFI}	Long frame sync pulse (from 3 to 8 bit clock periods long)	100			ns
Minimum Width of the Frame Sync Pulse (Low Level)	t_{WFL}	64K bit/s operating mode	160			ns

Note 1: For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

PIN CONFIGURATION



TIMING DIAGRAM

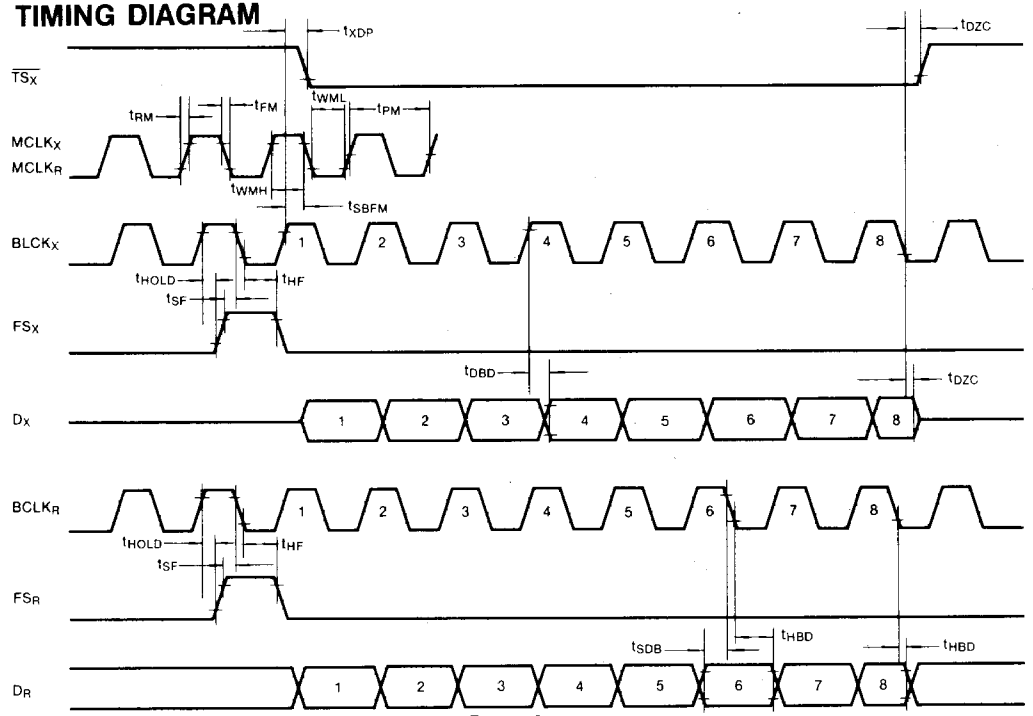


Fig. 2. Short Frame Sync Timing

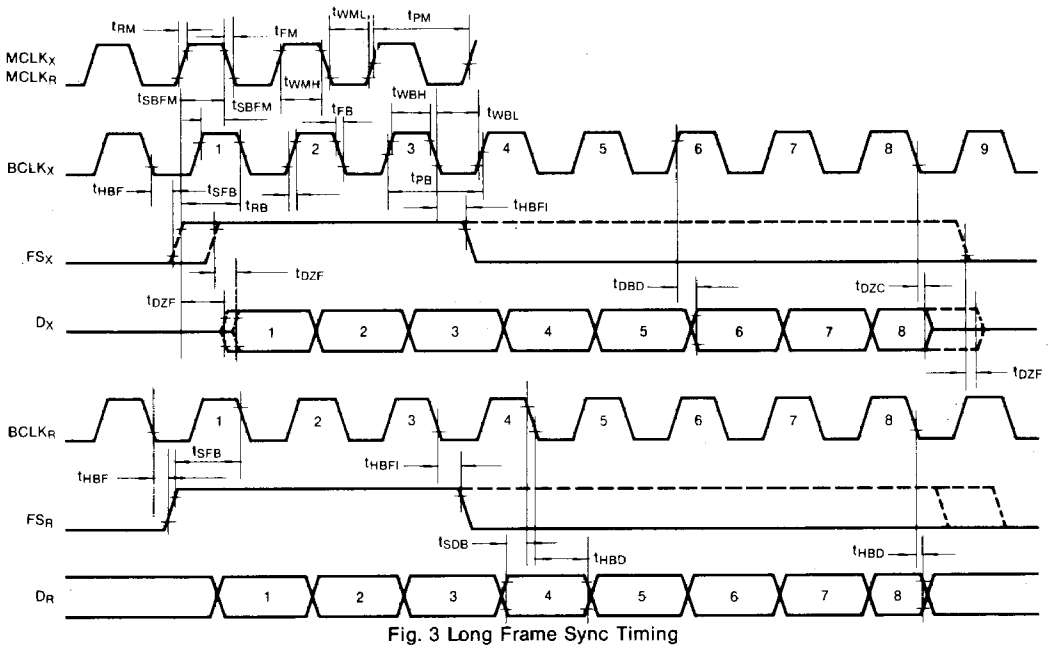


Fig. 3 Long Frame Sync Timing

PIN DESCRIPTION

Pin	Name	Function
1	VPO^+	The non-inverted output of the receive power amplifier.
2	GNDA	Analog ground. All signals are referenced to this pin.
3	VPO^-	The inverted output of the receive power amplifier.
4	VPI	Inverting input to the receive power amplifier. Also powers down both amplifiers when connected to V_{BB}.
5	VF_RO	Analog output of the receive filter.
6	V_{CC}	Positive power supply pin $V_{CC} = +5V \pm 5\%$.
7	FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R, FS_R is an 8KHz pulse train. (refer to Fig 2 and 3 for timing details)
8	D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
9	$BCLK_R$/ CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64KHz to 2.048MHz. Alternatively, may be a logic input which selects either 1.536MHz/1.544MHz or 2.048MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions. (see Table 1)
10	$MCLK_R$/ PDN	Receive master clock. Must be 1.536MHz or 2.048MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
11	$MCLK_X$	Transmit master clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_R$.
12	$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64KHz to 2.048MHz, but must be synchronous with $MCLK_X$.
13	D_X	The TRI-STATE PCM data output which is enabled by FS_X.
14	FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data a on D_X, FS_X is an 8KHz pulse train. (refer to Fig 2, 3)
15	$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
16	ANLB	Analog loopback control input. Must be set to logic '0' for normal operation. When pulled to logic '1', the transmit filter input is dis connected from the output of the preamplifier and connected to the VPO^+ output of the receive power, amplifier.
17	GS_X	Analog output of the transmit input amplifier. Used to externally set again.
18	VF_XI^-	Inverting input of the transmit input amplifier.
19	VF_XI^+	Non-inverting input of the transmit input amplifier.
20	V_{BB}	Negative power supply pin $V_{BB} = -5V \pm 5\%$.

FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_X, VF_RO, VPO – and VPO + outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin and FS_X and/or FS_R pulses must be present. Thus, 2-power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both FS_X and FS_R inputs continuously low-the device will power-down approximately 2ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536MHz, 1.544MHz or 2.048MHz. For 1.544MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. In synchronous mode, the bit clock, $BCLK_X$, may be from 64KHz to 2.048MHz, but must be synchronous with $MCLK_X$. Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

TABLE 1. Selection of Master Clock Frequencies

$BCLK_R$/CLKSEL	Master Clock Frequency Selected
Clocked	1.536MHz or 1.544MHz
0	2.048MHz
1 (or Open Circuit)	1.544MHz

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks maybe applied. $MCLK_X$ and $MCLK_R$ must be 1.536MHz, 1.544MHz for the KT3064, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (refer to pin description). For 1.544MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$, $BCLK_R$ must be a clock. $BCLK_X$ and $BCLK_R$ many operate from 64KHz to 2.048MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long (refer to Fig. 2). With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long (KT5116-type) frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long (refer to Fig. 3). Based on the transmit frame sync, FS_X, the COMBO will sense whether short or long frame sync pulses are being used. For 64KHz operation, the frame sync pulse must be kept low for a minimum of 160ns. The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors. The low noise and wide bandwidth allow gains in excess of 20dB across the audio passband to be realized. The OP amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256KHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-law (KT3064) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{max}) of nominally 2.5V peak. The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165μs (due to the transmit filter) plus 125μs (due to encoding delay), which totals 290μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256KHz. The decoder is μ-law (KT3064) and 5th order low pass filter corrects for the sin x/x attenuation due to the 8KHz sample/hold. The filter is then followed by a 2nd order RC active post-filter with its output at VF_RO. The receive section is unity-gain, but gain can be added by using the power amplifiers. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10μs later the decoder DAC output is updated. The total decoder delay is 210μs (decoder update) plus 110μs (filter delay) plus 62.5μs (1/2 frame), which gives approximately 180μs.

RECEIVE POWER AMPLIFIERS

Two inverting mode power amplifiers are provided for directly driving a matched line interface transformer. The gain of the first power amplifier can be adjusted to boost the $\pm$2.5V peak output signal from the receive filter upto $\pm$3.3V peak into an unbalanced 300Ω load, or $\pm$4.0V into an unbalanced 15KΩ load. The second power amplifier is internally connected in unity-gain inverting mode to give 6dB of signal gain for balanced loads.

Maximum power transfer to a 600Ω subscriber line termination is obtained by differently driving a balanced transformer with a $\sqrt{2}$:1 turns ratio, as shown in Fig. 2. A total peak power of 15.6dBm can be delivered to the load plus termination. Both power amplifiers can be powered down independently from the PDN input by connecting the VPI input to V_{BB}, saving approximately 12mW of power.

ENCODING FORMAT AT Dx OUTPUT

V_{IN} = + Full – Scale	1 0 0 0 0 0 0 0
V_{IN} = 0V	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
V_{IN} = – Full – Scale	0 0 0 0 0 0 0 0

TRANSMISSION CHARACTERISTICS

(Unless otherwise specified: Ta = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{BB} = − 5V ± 5%, GNDA = 0V, f = 1.02KHz, V_{IN} = 0dBm0 transmit input amplifier connected for unity-gain non-inverting.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Amplitude Response						
Absolute Levels		Nominal 0dBm0 level is 4dBm (600Ω) 0dBm0		1.2276		Vrms
Max Transmit Overload Level	t_{MAX}	Max transmit overload level (3.17dBm0)		2.501		V_{PK}
Transmit Gain, Absolute	G_{XA}	Ta = 25°C, V_{CC} = 5V, V_{BB} = − 5V Input at GS_X = 0dBm0 at 1020Hz	− 0.15		0.15	dB
Transmit Gain, Relative to G_{XA}	G_{XR}	f = 16Hz f = 50Hz f = 60Hz f = 200Hz f = 300Hz − 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz f = 4600Hz and up, measure Response from 0Hz to 4000Hz	 − 1.8 − 0.15 − 0.35 − 0.7 	 	− 40 − 30 − 26 − 0.1 0.15 0.05 0 − 14 − 32	dB dB dB dB dB dB dB dB dB
Absolute Transmit Gain Variation with Temperature	G_{XAT}	Ta = 0°C to 70°C			± 0.1	dB
Absolute Transmit Gain Variation with Supply Voltage	G_{XAV}	V_{CC} = 5V ± 5%, V_{BB} = − 5V ± 5%			± 0.05	dB
Transmit Gain Variations with Level	G_{XRL}	Sinusoidal test method Reference level = − 10dBm0 VF_XI+ = − 40dBm0 to + 3dBm0 VF_XI+ = − 50dBm0 to − 40 dBm0 VF_XI+ = − 55dBm0 to − 50dBm0	 − 0.2 − 0.4 − 1.2	 	 0.2 0.4 1.2	 dB dB dB
Receive Gain, Absolute	G_{RA}	Ta = 25°C, V_{CC} = 5V, V_{BB} = − 5V Input = Digital code sequence for 0dBm0 signal at 1020Hz	− 0.15		0.15	dB
Receive Gain, Relative to G_{RA}	G_{RR}	f = 0Hz to 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz	− 0.15 − 0.35 − 0.7 	 	0.15 0.05 0 − 14	dB dB dB dB
Absolute Receive Gain Variation with Temperature	G_{RAT}	Ta = 0°C to 70°C			± 0.1	dB
Absolute Receive Gain Variation with Supply Voltage	G_{RAV}	V_{CC} = 5V ± 5%, V_{BB} = − 5V ± 5%			± 0.05	dB
Receive Gain Variations with Level	G_{RRL}	Sinusoidal test method; reference input PCM code corresponds to an ideally encoded—10dBm0 signal PCM level = − 40dBm0 to + 3 dBm0 PCM level = − 50dBm0 to − 40dBm0 PCM level = − 55dBm0 to − 50dBm0	 − 0.2 − 0.4 − 1.2	 	 0.2 0.4 1.2	 dB dB dB
Receive Filter Output at VF_RO	V_{RO}	R_L = 10KΩ	− 2.5		2.5	V

TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Envelope Delay Distortion with Frequency						
Transmit Delay, Absolute	D_{XA}	f = 1600Hz		290	315	μs
Transmit Delay, Relative to D_{XA}	D_{XR}	f = 500Hz – 600Hz		195	220	μs
		f = 600Hz – 800Hz		120	145	μs
		f = 800Hz – 1000Hz		50	75	μs
		f = 1000Hz – 1600Hz		20	40	μs
		f = 1600Hz – 2600Hz		55	75	μs
		f = 2600Hz – 2800Hz		80	105	μs
		f = 2800Hz – 3000Hz		130	155	μs
Receive Delay, Absolute	D_{RA}	f = 1600Hz		180	200	μs
Receive Delay, Relative to D_{RA}	D_{RR}	f = 500Hz – 1000Hz	– 40	– 25		μs
		f = 1000Hz – 1600Hz	– 30	– 20		μs
		f = 1600Hz – 2600Hz		70	90	μs
		f = 2600Hz – 2800Hz		100	125	μs
		f = 2800Hz – 3000Hz		145	175	μs
Noise						
Transmit Noise, C Message Weighted	N_{XC}	$VF_XI+ = 0V$		12	15	dBmC0
Receive Noise, C Message Weighted	N_{RC}	PCM code equals alternating positive and negative zero		8	11	dBmC0
Noise, Single Frequency	N_{RS}	f = 0KHz to 100KHz, loop around measurement, $VF_XI+ = 0$Vrms			– 53	dBm0
Positive Power Supply Rejection, Transmit	$PPSR_X$	$VF_XI+ = 0$Vrms, $V_{CC} = 5.0V_{DC} + 100$mVrms f = 0KHz – 50KHz	40			dBC
Negative Power Supply Rejection, Transmit	$NPSR_X$	$VF_XI+ = 0$Vrms, $V_{BB} = -5.0V_{DC} + 100$mVrms f = 0KHz – 50KHz	40			dBC
Positive Power Supply Rejection, Receive	$PPSR_R$	PCM code equals positive zero $V_{CC} = 5.0V_{DC} + 100$mVrms				
		f = 0Hz – 4000Hz	40			dBC
		f = 4KHz – 25KHz	40			dB
		f = 25KHz – 50KHz	36			dB
Negative Power Supply Rejection, Receive	$NPSR_R$	PCM code equals positive zero $V_{BB} = -5.0V_{DC} + 100$mVrms				
		f = 0Hz – 4000Hz	40			dBC
		f = 4KHz – 25KHz	40			dB
		f = 25KHz – 50KHz	36			dB

TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious Out-of-Band Signals at the Channel Output	SOS	Loop around measurement, 0dBm0, 300Hz – 3400Hz input applied to VF_XI+, measure individual image signals at VF_RO				
		4600Hz – 7600Hz			– 32	dB
		7600Hz – 8400Hz			– 40	dB
		8400Hz – 100,000Hz			– 32	dB
Distortion						
Signal to Total Distortion	STD_X	Sinusoidal test method				
Transmit or Receive Half-Channel	STD_R	Level = 3.0dBm0	33			dBC
		= 0dBm0 to 130dBm0	36			dBC
		= – 40dBm0 XMT	29			dBC
		RCV	30			dBC
		= – 55dBm0 XMT	14			dBC
		RCV	15			dBC
Single Frequency Distortion, Transmit	SFD_X				– 46	dB
Single Frequency Distortion, Receive	SFD_R				– 46	dB
Intermodulation Distortion	IMD	Loop around measurement, VF_X+ = – 4dBm0 to – 21dBm0, two frequencies in the range 300Hz – 3400Hz			– 41	dB
Crosstalk						
Transmit to Receive Crosstalk	CT_{X-R}	f = 300Hz – 3400Hz, D_R = Steady PCM code		– 90	– 75	dB
Receive to Transmit Crosstalk	CT_{R-X}	f = 300Hz – 3000Hz, VF_XI = 0V		– 90	– 70 (Note 1)	dB
Power Amplifiers						
Maximum 0dBm0 Level for Better than ±0.1dB Linearity Over the Range – 10dBm0 to + 3dBm0	V_{OL}	Balanced load, R_L connected between VPO+ and VPO–				
		R_L = 600Ω	3.3			Vrms
		R_L = 1200Ω	3.5			Vrms
		R_L = 30KΩ	4.0			Vrms
Signal/Distortion	S/Dp	R_L = 600Ω, 0dBm0	50			dB

Note 1. CT_{R-X} is measured with a – 40dBm0 activating signal applied at VF_XI+.

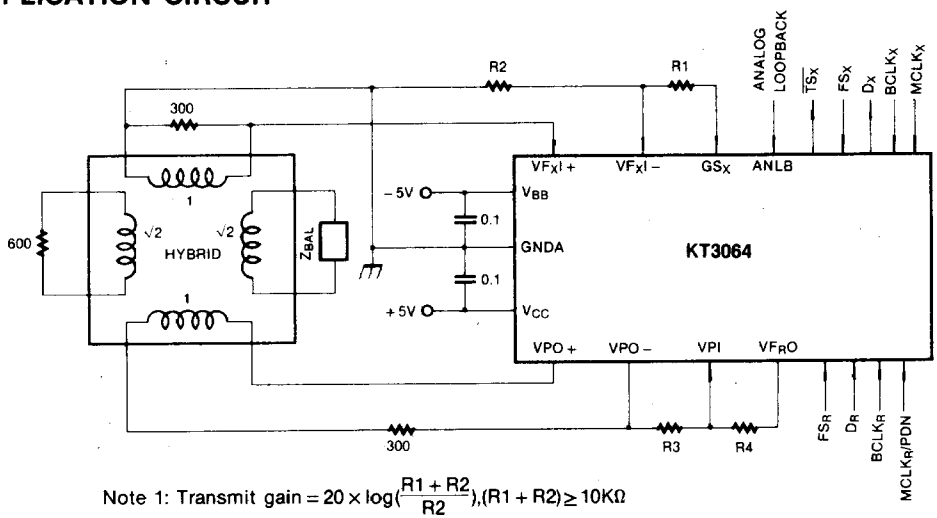
APPLICATION INFORMATION

POWER SUPPLY

While the pins of the KT3064 are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}. For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in start formation, rather tha via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10μF capacitors.

APPLICATION CIRCUIT



Note 1: Transmit gain $= 20 \times \log(\frac{R1+R2}{R2}), (R1+R2) \geq 10K\Omega$

Note 2: Receive gain $= 20 \times \log(\frac{2 \times R3}{R4}), R4 \geq 10K\Omega$