AN4217
Application note

Designing the SPV1020 with serial and parallel output configurations

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Introduction

The STEVAL-ISV008V1 and STEVAL-ISV018V1 demonstration boards are based on STMicroelectronics' photovoltaic products SPV1020, SPV1001N30 and SPV1001N40.

These boards are designed for innovative distributed PV panels and their size is suitable for most junction boxes available on the market. Each PCB uses three of the SPV1020 solar boost MPPT regulators, whose outputs can be connected in parallel (STEVAL-ISV008V1) or in series (STEVAL-ISV018V1).

Details on the SPV1020 device can be found in the product's datasheet, and in application note AN3392, both available at www.st.com.

The SPV1001N30 is used as a high efficiency bypass device between the input and output. It automatically turns ON when the SPV1020 is OFF due to an input voltage lower than its UVLO.

The SPV1001N40 is used as a high efficiency bypass device at the output stage of each SPV1020. It automatically turns ON when the SPV1020 is OFF, offering a low impedance path from V_{OUT-} to the output rail V_{OUT+}, as shown in *Figure 5.*

1 Output parallel and series (bottom and top view) connections

Figure 1. STEVAL-ISV008V1 (output parallel connection) bottom view

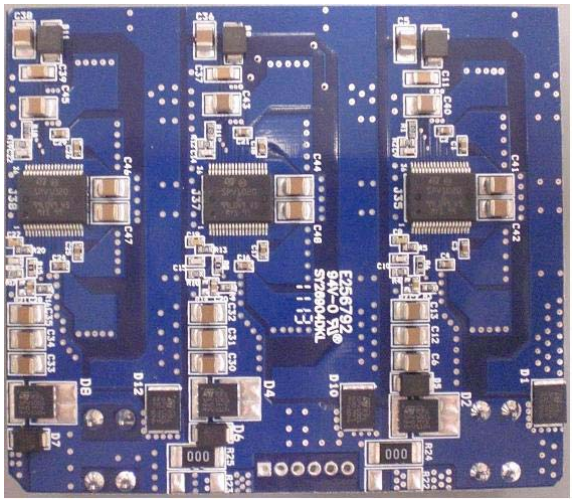


Figure 2. STEVAL-ISV008V1 (output parallel connection) top view

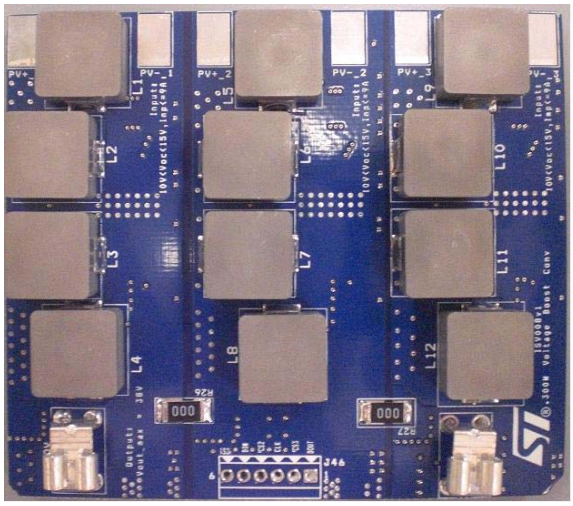


Figure 3. STEVAL-ISV018V1 (output series connection) bottom view

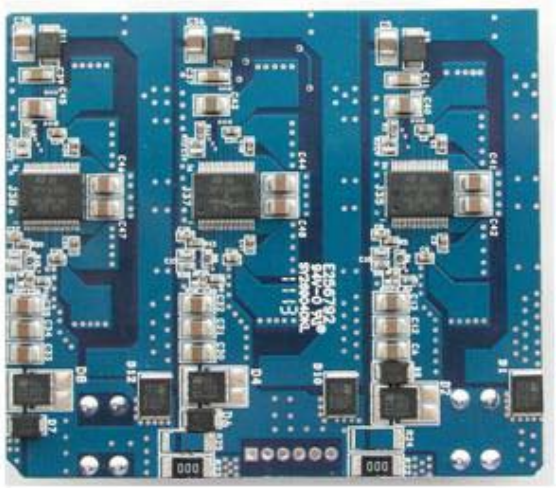
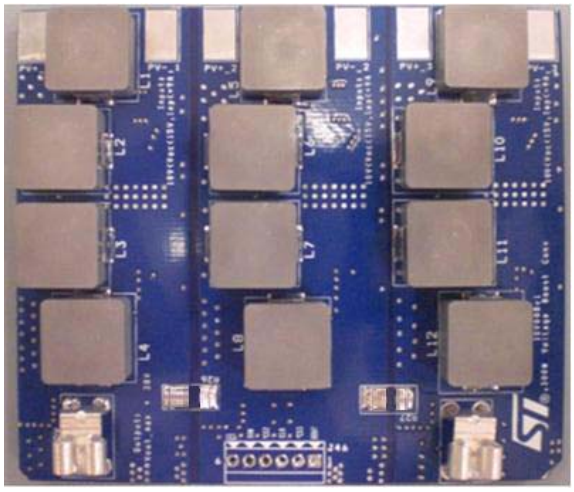


Figure 4. STEVAL-ISV018V1 (output series connection) top view



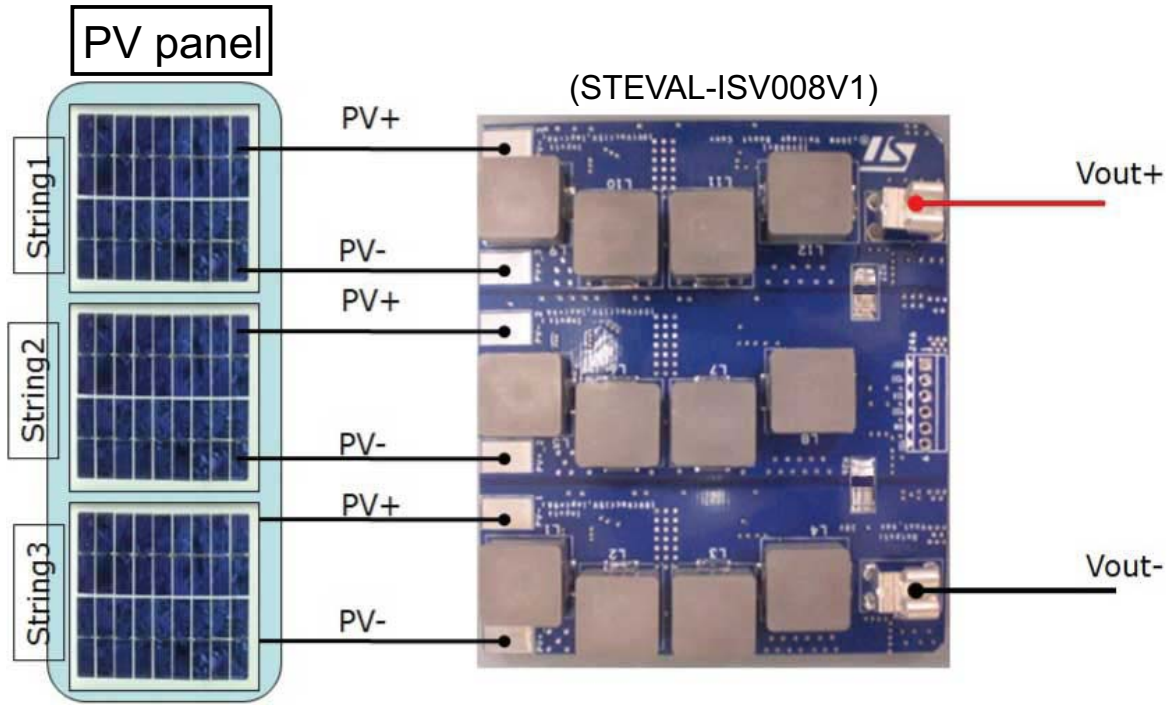
2 Connections

2.1 Input and output connection example

The following figure shows how to connect STEVAL-ISV0x8V1 to a distributed photovoltaic panel and load.

Please note that although the illustration below refers to the STEVAL-ISV008V1, the input and output connections are the same for the STEVAL-ISV018V1.

Figure 5. STEVAL-ISV008V1 input and output connection example



SPV1020 and SPV1001N30/N40 at thr bottom side

3 STEVAL-ISV0x8V1 parallel and series connection

The output pins of different SPV1020 devices can be connected both in parallel and in series. In both cases, the output power (P_{OUT}) will depend on light irradiation of each panel (P_{IN}), application efficiency and by the specific constraints of the selected topology.

The objective of this section is to show how the output power is impacted by the selected topology.

Examples with three PV panels are presented and the results can be extended to a larger number of PV panels.

When the SPV1020 is on (light irradiation generating $V_{in} \geq 6.5$ V)

Equation 1

$$P_{outx} = \eta P_{inx} [x = 1..3]$$

When the SPV1020 is off, system efficiency will depend upon the drop of the bypass diodes (D1, D10, D12, as shown in the STEVAL-ISV0x8V1 schematics see *Figure 17* and *Figure 18*):

Equation 2

$$P_{outx} = \eta_{bp} P_{inx} [x = 1..3]$$

In the case of panel completely shaded:

Equation 3

$$P_{outx} = 0$$

3.0.1 STEVAL-ISV008V1 parallel connection

This topology guarantees the desired output voltage even if only one of the panels is irradiated. Output voltage of the STEVAL-ISV008V1 is limited to the SPV1020 maximum output voltage, which is 40 V.

Figure 5 and *6* show details of the parallel connection topology:

Figure 6. STEVAL-ISV008V1, panel connections for output parallel connection

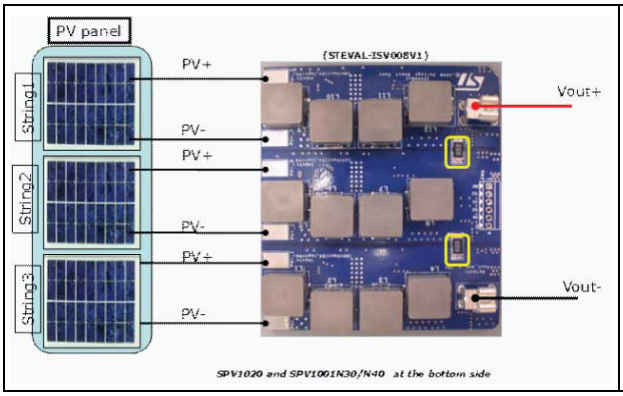
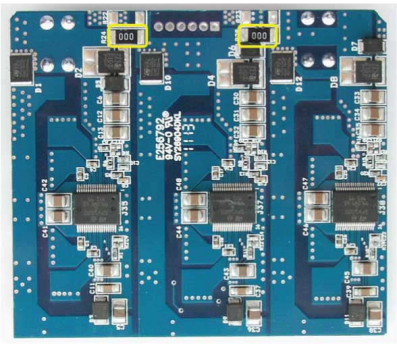


Figure 7. STEVAL-ISV008V1, component configuration for output parallel connection



The output partitioning (R3/R4, R9/R10, R16/R17 in the STEVAL-ISV0x8V1 schematic) of each of the three SPV1020 devices must be in accordance with the desired V_{OUT}.

According to the topology:

Equation 4

$$V_{out} = V_{out1} = V_{out2} = V_{out3}$$

$$I_{out} = I_{out1} + I_{out2} + I_{out3}$$

According to the light irradiation on each panel (P_{IN}) and to the system efficiency (η), output power is:

Equation 5

$$P_{out} = P_{out1} + P_{out2} + P_{out3}$$

$$P_{outx} = V_{outx} * I_{outx} [x = 1..3]$$

$$P_{inx} = V_{inx} * I_{inx} [x = 1..3]$$

Therefore:

Equation 6

$$P_{out} = V_{out}(I_{out1} + I_{out2} + I_{out3}) = \eta P_{in1} + \eta P_{in2} + \eta P_{in3}$$

Each SPV1020 contributes to the output power providing I_{OUTX} according to the irradiation of its panel.

Moreover, the desired V_{OUT} is guaranteed if at least one of the three PV panels provides enough voltage to turn on the related SPV1020.

Figure 8 shows the power conversion efficiency when V_{MPP} = 12 V and I_{MPP} ranges from 1 A to 8 A (in steps of 1 A). Power ranges between 36 W and 288 W.

Figure 8. Power efficiency versus output voltage

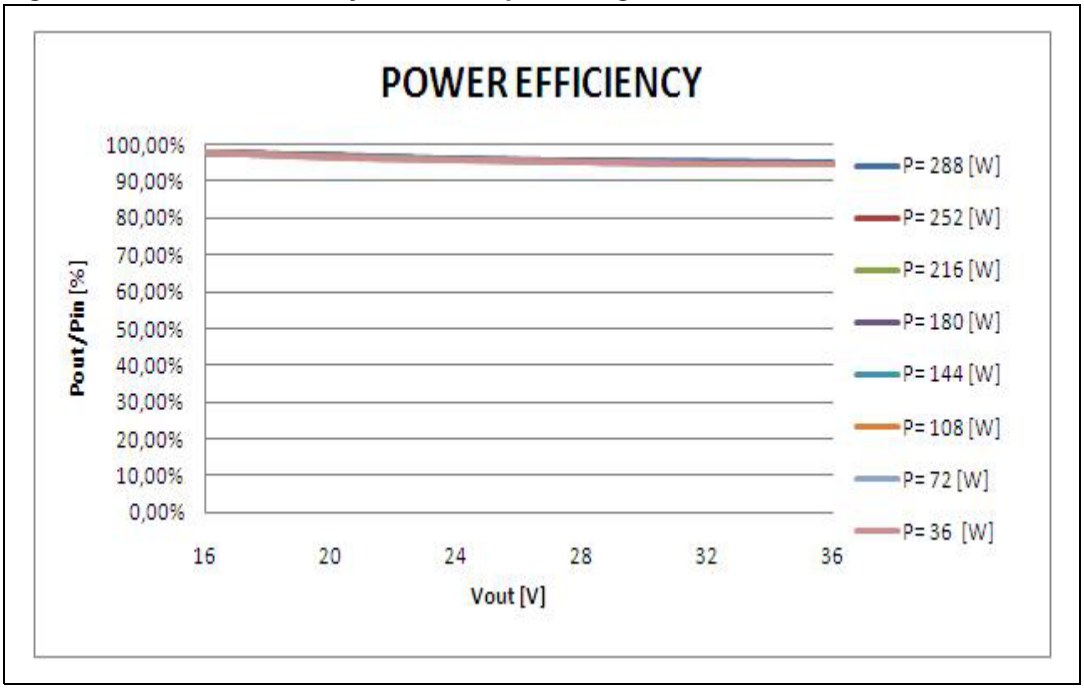
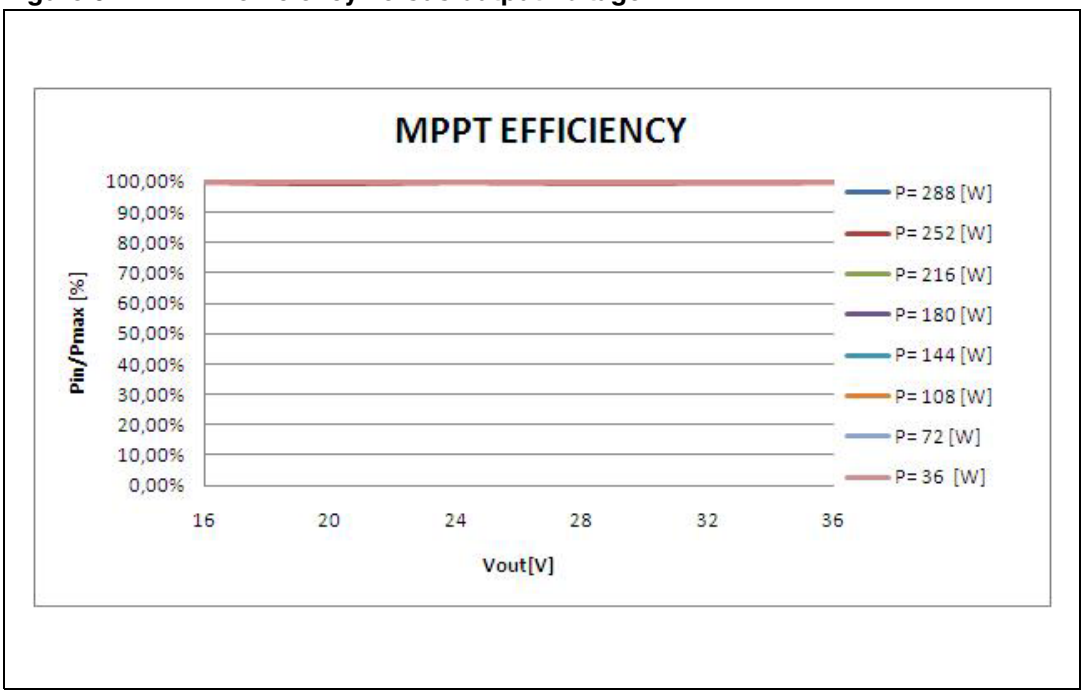


Figure 9 shows the MPPT efficiency (*) when V_{MPP} = 12 V and I_{MPP} ranges from 1 A to 8 A (in steps of 1A). Power ranges between 36 W and 288 W.

(*) MPPT Efficiency = P_{IN}/P_{MAX};

P_{IN} is the power measured at the input stage of the PCB; P_{MAX} is the maximum power the PV panel can provide.

Figure 9. MPPT efficiency versus output voltage



3.0.2 STEVAL-ISV018V1 series connection

This topology provides an output voltage that is the sum of the output voltages of each SPV1020 connected in series. The following information shows how the output power is determined by the output series connection.

Figure 10 shows a detail of the series connection topology:

Figure 10. STEVAL-ISV018V1, panel connections for output series connection

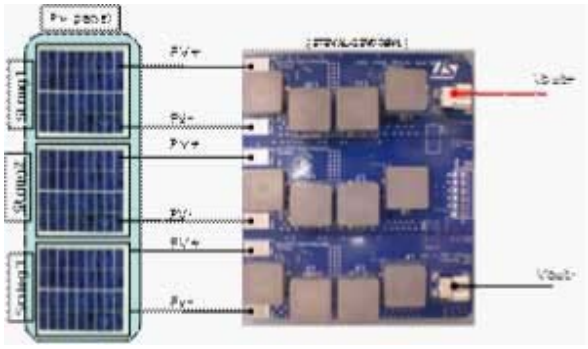
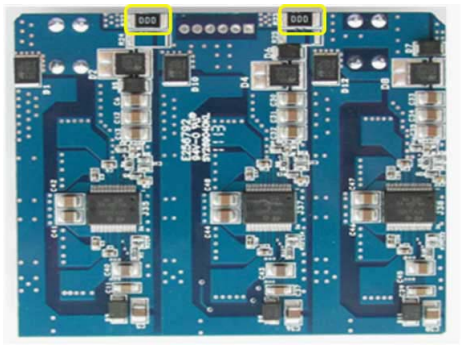


Figure 11. STEVAL-ISV018V1, components configuration for output series connection



In this case, the topology constraint implies:

Equation 7

$$I_{out} = I_{out1} = I_{out2} = I_{out3}$$

$$V_{out} = V_{out1} + V_{out2} + V_{out3}$$

In the case where the irradiation is the same for each panel:

Equation 8

$$P_{in1} = P_{in2} = P_{in3}$$

$$P_{out} = 3 * P_{outx}\ [x = 1..3]$$

$$P_{outx} = \frac{1}{3} P_{out}$$

$$P_{outx} = V_{outx} * I_{outx} = V_{out1} * I_{out}$$

So

Equation 9

$$V_{outx} = \frac{1}{3} V_{out}$$

For example, assuming, P_{OUT} = 90 W and, if desired V_{OUT} = 90 V then

V_{OUTX} = 30 V

Lower irradiation for one panel, for example on panel 2, causes lower output power, so lower V_{OUT2} due to the I_{OUT} constraint:

Equation 10

$$V_{out\,x} = \frac{P_{out\,x}}{I_{out}}$$

The output voltage (V_{OUT}) required by the load can be supplied by the first and third SPV1020 but only up to the limit imposed by their output voltage resistor partitioning (R3/R4, R9/R10, R16/R17 in the STEVAL-ISV0x8V1 schematics).

These examples show various scenarios as shown in the STEVAL-ISV0x8V1 schematics.

Assuming the following conditions: R3/R4 limits V_{OUTX} to 40 V and the desired V_{OUT} = 90 V.

Example 1:

Panel 2 has 75% of the irradiation of panels 1 and 3:

Equation 11

$$V_{out\,2} = \frac{3}{4} * V_{out\,1} = \frac{3}{4} * V_{out\,3}$$

$$P_{out1} = P_{out\,2} = 30\,W$$

$$P_{out\,2} = \frac{3}{4} P_{in\,1} = 22.5W$$

$$P_{out} = P_{out\,1} + P_{out\,2} + P_{out\,3} = 82.5W$$

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{82.5}{90} = 0.92\,A$$

$$V_{out\,1} = V_{out\,3} = \frac{30}{0.92} = 32.6V$$

Two of the SPV1020 devices (first and third) supply most of the voltage output due to lower irradiation on panel 2.

Note: SPV1020 is a boost controller, so V_{OUTX} must be higher than V_{INX}, otherwise the SPV1020 turns off and the input power is transferred to the output stage trough bypass diodes (D1, D10 or D12).

Example 2:

Panel 2 has 25% of the irradiation of panels 1 and 3:

Equation 12

$$V_{out\,2} = \frac{1}{4} * V_{out\,1} = \frac{1}{4} * V_{out\,3}$$

$$P_{out1} = P_{out\,2} = 30W$$

$$P_{out\,2} = \frac{1}{4} P_{in1} = 7.5W$$

$$P_{out} = P_{out\,1} + P_{out\,2} + P_{out\,3} = 67.5W$$

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{67.5}{90} = 0.75\ A$$

$$V_{out1} = V_{out3} = \frac{30}{0.75} = 40\,V$$

$$V_{out\,2} = \frac{7.5}{0.75} = 10V$$

In this case the system is at its limit. A lower irradiation will impact V_{OUT1} and/or V_{OUT3} which are already at the limit (40 V) imposed by R3/R4 partitioning.

Example 3:

Panel 2 is completely shaded.

In this case, the maximum V_{OUT} available is 80 V (V_{OUT1}+V_{OUT3}).

On the STEVAL-ISV018V1 application board, bypass diode (D4) around the second SPV1020 allows I_{OUT} to flow.

Figure 12 shows power conversion efficiency when V_{MPP} = 12 V and I_{MPP} ranges from 1 A to 8 A (in steps of 1 A). Power ranges between 36 W and 288 W.

Figure 12. Power efficiency versus output voltage

Figure 13. MPPT efficiency versus output voltage

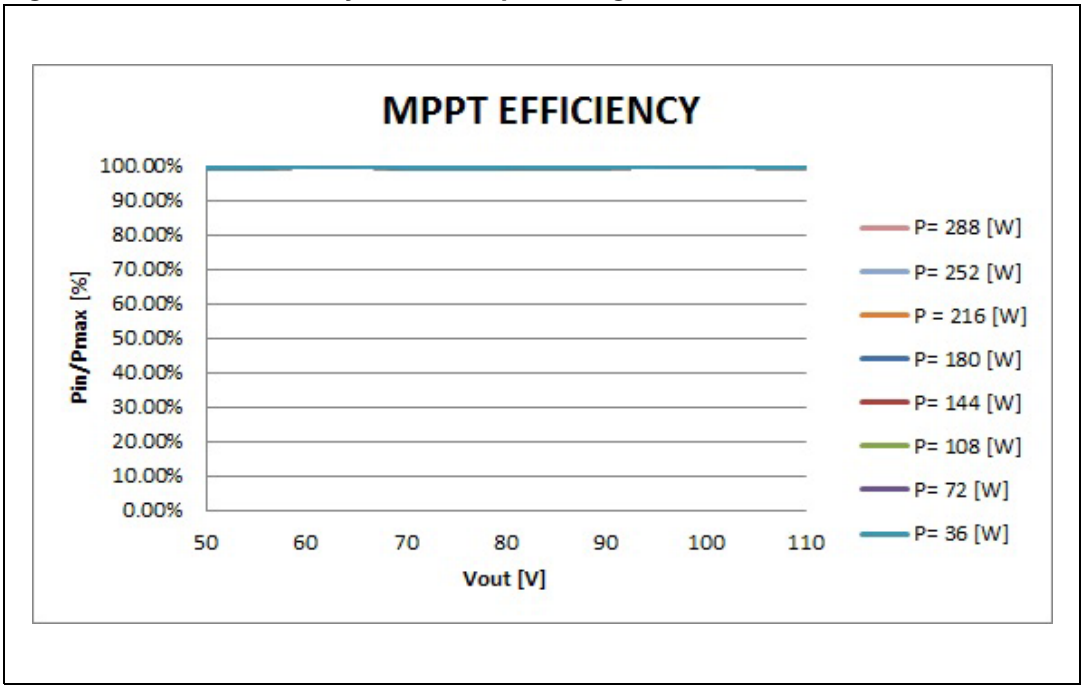


Figure 12 shows MPPT efficiency when V_{MPP} = 12 V and I_{MPP} ranges from 1 A to 8 A (in steps of 1 A). Power ranges between 36 W and 288 W. In both cases all the three strings have the same input power.

Figure 14 shows the output current versus input current when the input power to each string is different. The configurations are:

Table 1. V_{in} = 12 V, V_{out} = 80 V

Istring1	Istring2	Istring3
4	4	4
6	6	4
8	8	4

Figure 14. Output current vs input current

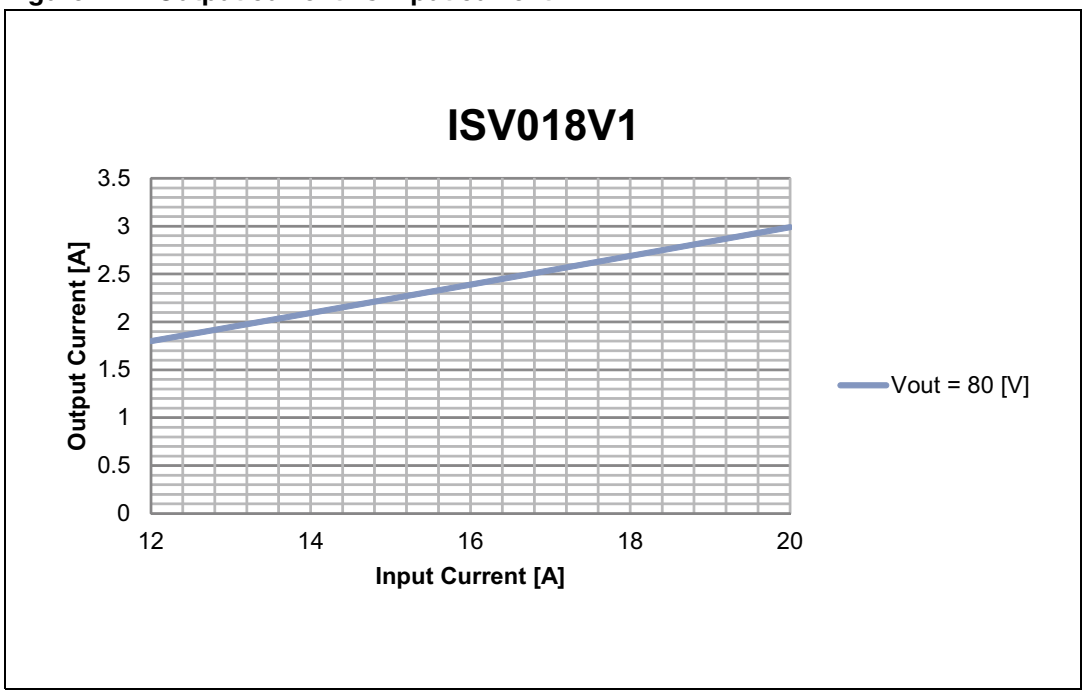


Figure 15. STEVAL-ISV008V1 SPI connection

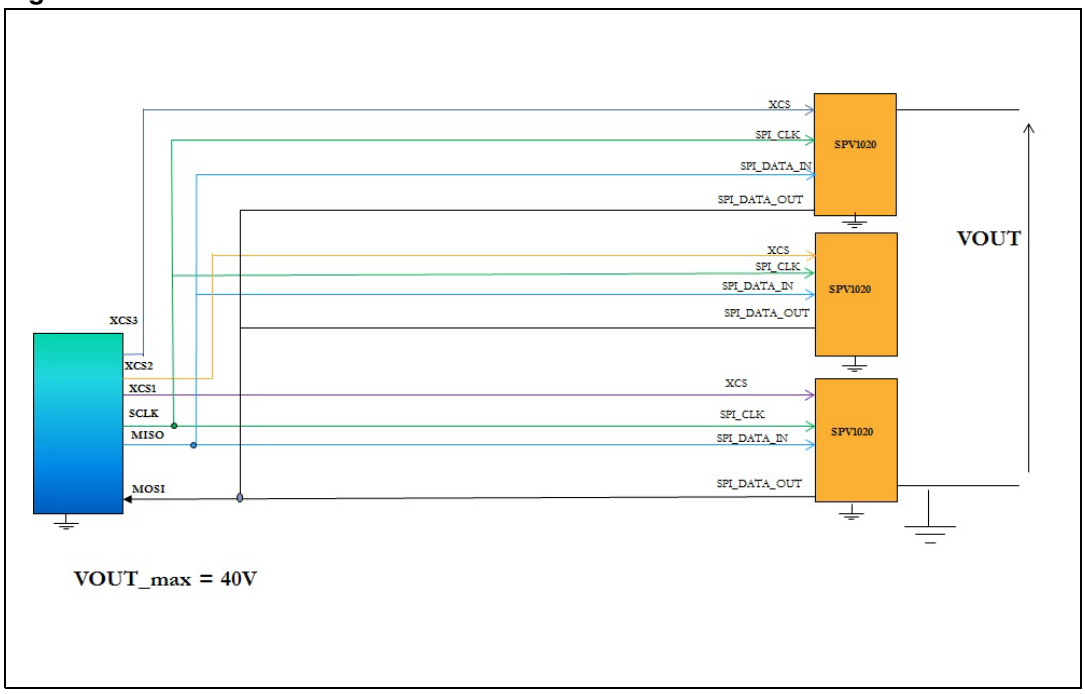
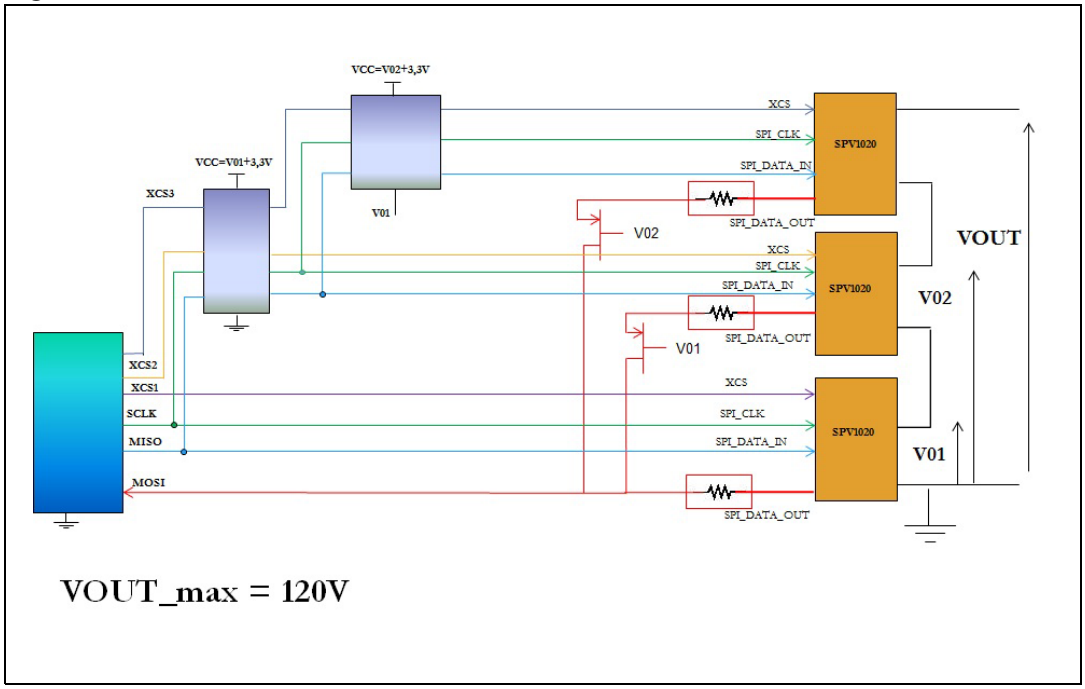


Figure 16. STEVAL-ISV018V1 SPI connection



In the STEVAL-ISV008V1 the SPI connection is accomplished by means of the J46 connector. Instead in STEVAL-ISV008V1 the SPI connection requires additional external components not present in the STEVAL-ISV008V1. These additional components are shown in *Figure 16*.

4 BOM

The STEVAL-ISV008V1 and STEVAL-ISV018V1 differ mainly in their output configurations (defined by R22 and R23 for STEVAL-ISV008V1 and by R24, R25, R26 and R27 for STEVAL-ISV018V1). The SPI connector J46 is available only on STEVAL-ISV008V1.

The following table shows the list of external components configuring the STEVAL-ISV0x8V1; last column highlights the difference between STEVAL-ISV008V1 and STEVAL-ISV018V1.

The application boards have been designed for PV strings providing V_{OC} = 15 V, I_{SC} =9 A, output voltage of each SPV1020 V_{OUT_MAX} = 36 V and F_{SW} = 100 KHz.

Table 2. STEVAL-ISV008V1 and STEVAL-ISV018V1 component list

Component	Name	Value	Supplier	Part number	Notes: [STEVAL-ISV008V1 vs. STEVAL-ISV018V1]
C1, C2,C3,C4, C16, C17, C18, C21, C24, C25,C26, C29	Bootstrap capacitors	100 nF	MURATA EPCOS	GRM188R71C104KA01 C1608X7R1H104K	
C11, C37, C39	Input supply pin capacitor	1 µF	MURATA EPCOS	GRM31MR71H105KA88 C3216X7R1H105K\	
C5, C36, C38	Input capacitor	4.7 uF	MURATA EPCOS	GRM32ER71H475KA88K C3225X7R1H475K	
C9, C14, C22	Voltage sensing capacitor	220 pF	MURATA EPCOS	GRM188R71E221KA01 C1608C0G1H221J	
C8, C19, C27	Compensation capacitor	22 nF	MURATA EPCOS	GRM188R71C223KA01 C1608X7R1H223K	
C10, C15, C23	Voltage sensing capacitor	220 pF	MURATA EPCOS	GRM188R71E221KA01 C1608C0G1H221J	
C7, C20, C28	Internal reference voltage capacitor	470 nF	MURATA EPCOS	GRM188R71A474KA61 C1608X7R1C474K	
C6, C12, C13, C40, C41, C42 C30, C31, C32, C43, C44, C48 C33, C34, C35, C45, C46, C47	Output capacitor	4.7 uF	MURATA EPCOS	GRM32ER71H475KA88K C3225X7R1H475K	
D3, D9, D11	Noise filter on supply pin	STPS160U	ST	STPS160U	

Table 2. STEVAL-ISV008V1 and STEVAL-ISV018V1 component list (continued)

R1,R11,R18	Input voltage partitioning resistor	1.2 MΩ	VISHAY	D11/CRCW0603 1.2M	
R2,R12,R19	Input voltage partitioning resistor	110 kΩ	CYNTEC	RR0816R-114-DN-11	
R3,R9,R16	Output voltage partitioning resistor	3.9 MΩ	VISHAY	D11/CRCW0603 4.3M 1%	
R4,R10,R17	Output voltage partitioning resistor	110 kΩ	CYNTEC	RR0816R-114-DN-11	
R5,R13,R20	Compensation resistor	1 kΩ	CYNTEC	RR0816R-102-DN-11	
R6, R8,R15	Pull up resistor (Note: R6 must be removed if R7 is soldered)	0 Ω			
R7 (optional) R14 (optional) R21 (optional)	Oscillator resistor (Note: R6 must be removed if R7 is soldered)	Depending on desired Fsw			
L1, L2, L3, L4 L5, L6, L7, L8 L9, L10, L11, L12	Phase x (x=1..4) inductors	47 uH	EPCOS COILCRAFT CYNTEC MURATA B82477G4473M003 MSS1278T-473ML PIMB136T-470MS-11 49470SC		
D1,D10,D12	Bypass diodes	SPV1001N30	ST	SV1001N30	
D2,D4,D8	Bypass diodes	STPS15L60CB-TR	ST	STPS15L60CB-TR	
J35,J37,J38	ST SUPPLY	SPV1020	ST	SPV1020	
J46	SPI connector	6-pin Connector	Phoenix Contact	MPT 0.5/ 6-2.54	Disconnected on STEVAL-ISV018V1.
D5,D6,D7	600W, 40V unidirectional protection transil	SMBJ36CA	ST	SMBJ36A-TR	

Table 2. STEVAL-ISV008V1 and STEVAL-ISV018V1 component list (continued)

R22, R23	Output series connection switch	0 Ω	VISHAY	CRCW25120000Z0EGHP	Mounted on STEVAL-ISV008V1; Not Mounted on STEVAL-ISV018V1
R24, R25, R26, R27	Output parallel connection switch	0 Ω	VISHAY	CRCW25120000Z0EGHP	Mounted on STEVAL-ISV018V1; Not Mounted on STEVAL-ISV008V1
J47, J48	Output connector	FASTON CONNECTOR			

5 Schematic diagrams

Figure 17. STEVAL-ISV008V1 schematic

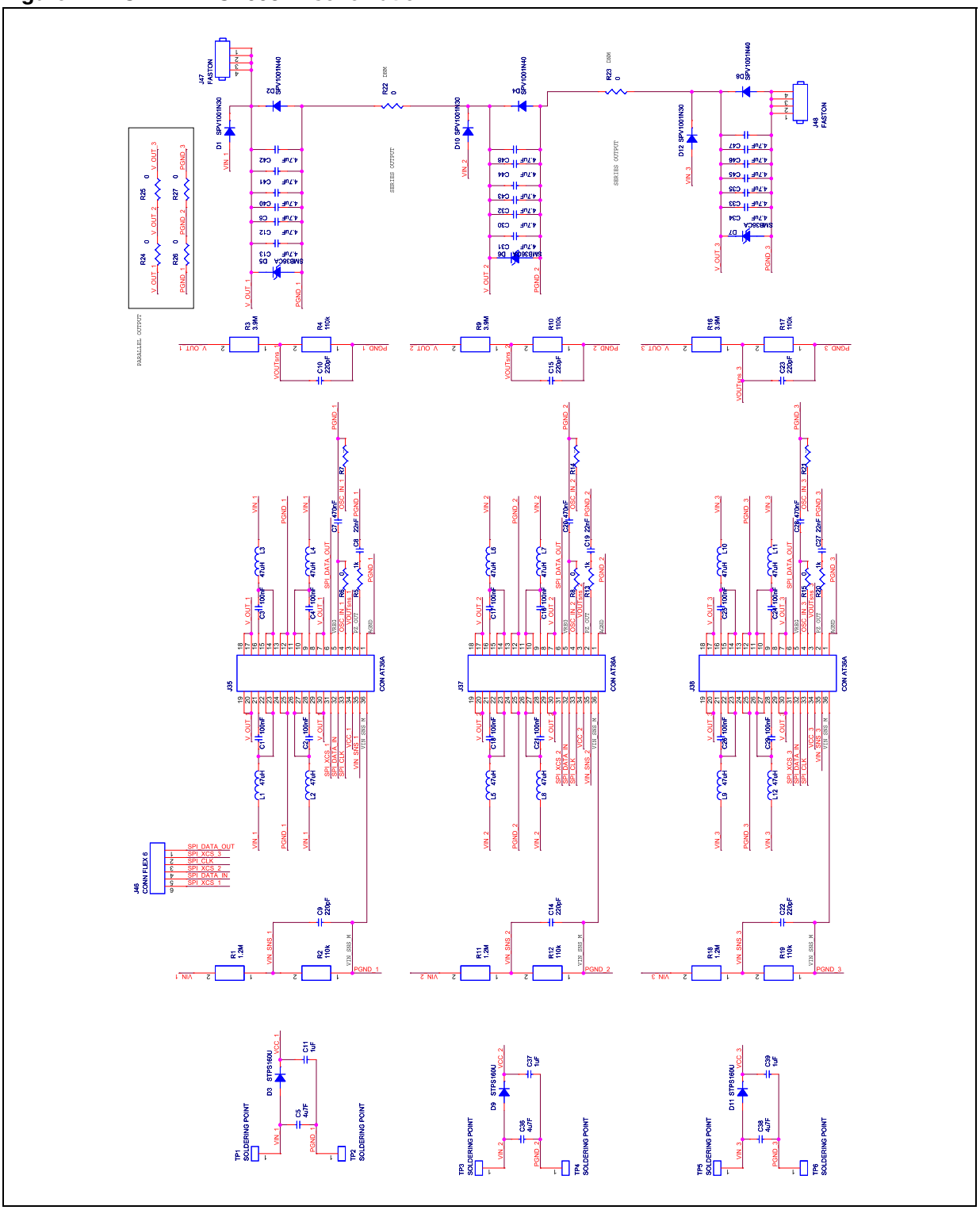
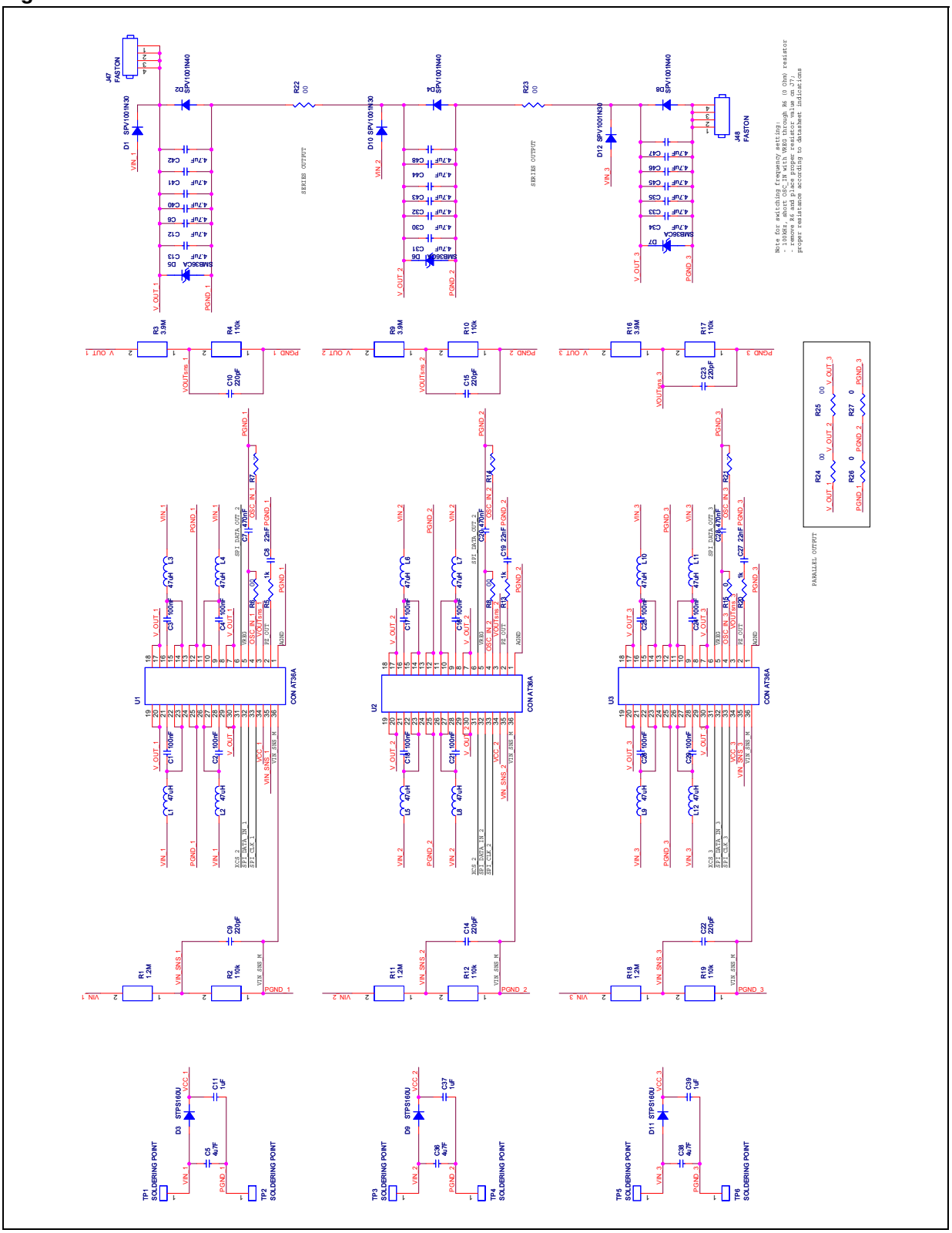


Figure 18. STEVAL- ISV018V1 schematic



6 Layout guidelines

PCB layout is very important in order to minimize noise, high frequency resonance problems and electromagnetic interference.

Paths between each inductor and its relative pin must be designed with the same resistance. Different resistances among the four branches can be the cause of unbalanced current flow among the four branches. Unbalanced currents could damage the chip or cause poor MPPT tracking.

To reduce radiation and resonance problems it is essential to keep high current paths as small as possible.

Large traces for high current paths and an extended ground plane under the metal slug of the package help reduce noise and improve heat dissipation, as well as increase the efficiency.

High current paths are highlighted by thicker lines in the *Figure 17* and *Figure 18*.

Input and output capacitors must be close as possible to the device. Output capacitance must be equally distributed among the V_{OUT} pins of the device. For example, refer to the placement of C6, C12, C13, C40, C41 and C42 in *Figure 19: STEVAL-ISV008V1 PCB layout example (top view)*

Boostrap capacitors (connected between Lx and CBx pins) must be connected as close as possible to the related pins.

External resistor dividers should be as close as possible to the V_{IN_SNS} and V_{OUT_SNS} pins of the device, and as far as possible from the high current circulating paths, to avoid noise pickup.

For an example of a recommended layout, see the following demonstration board (dimensions expressed in mm):

Figure 19. STEVAL-ISV008V1 PCB layout example (top view)

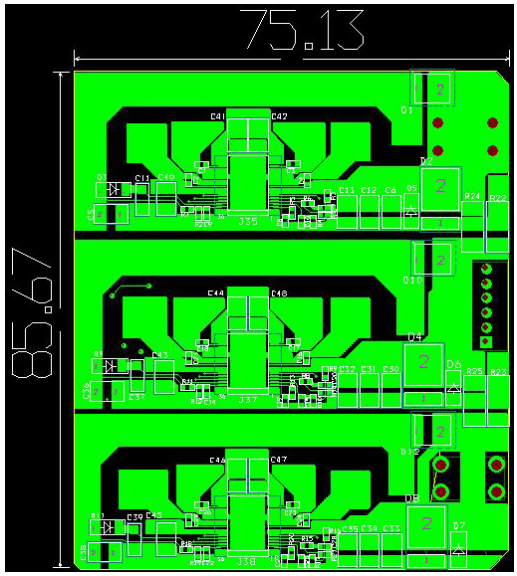


Figure 20. STEVAL- ISV008V1 PCB layout example (bottom view)

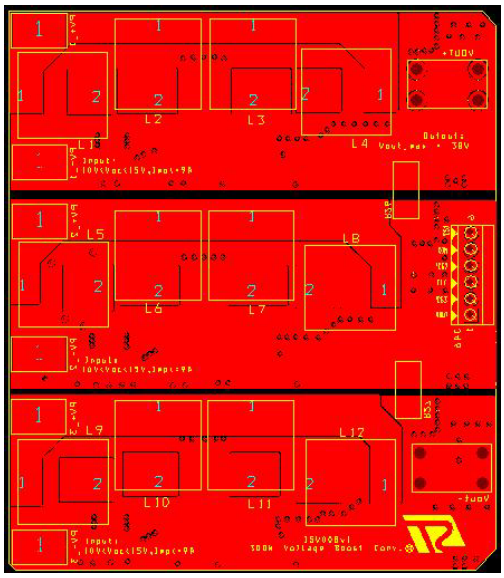


Figure 21. STEVAL-ISV018V1 PCB layout example (bottom view)

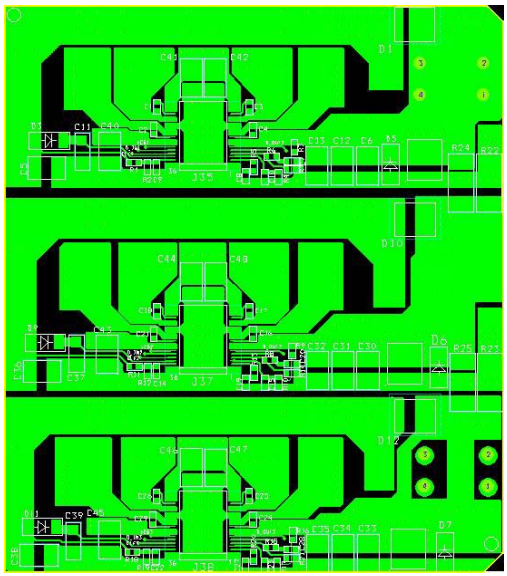
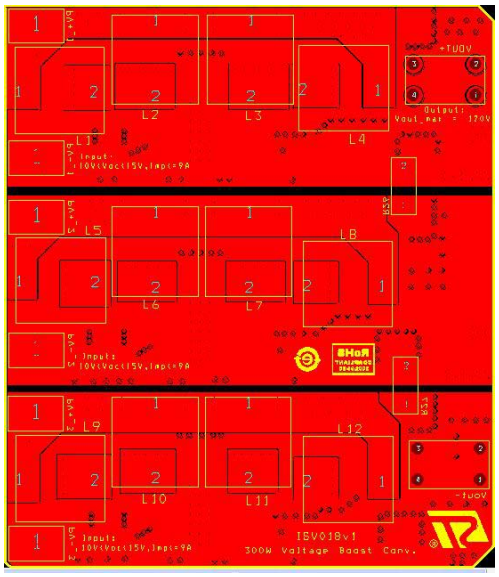


Figure 22. STEVAL- ISV018V1 PCB layout example (bottom view)



7 Revision history

Table 3. Document revision history

Date	Revision	Changes
22-Jan-2013	1	Initial release.

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