81 COMMON x 132 SEGMENT STN LCD DRIVER / CONTROLLER

SL20T0081

DEVICE SPECIFICATION

OVERVIEW

INTRODUCTION

The SL20T0081 is a single-chip graphic dot-matrix liquid crystal display driver & controller that can be connected directly to a microprocessor bus. 8-bit parallel or serial display data sent from the microprocessor is stored in the internal display data RAM and the chip generates a liquid crystal drive signal independent of the micro-processor. The SL20T0081 contains 81x132 bits of display data RAM and there is a 1-to-1 correspondence between the liquid crystal panel pixels and the internal RAM bits, and the device contains 81 common output circuits and 132 segment output circuits, so that a single chip can drive a 81x132 dot display (capable of displaying 8 columns x 5 rows of a 16 x 16 dot font). Moreover, the capacity of the display can be extended through the use of master/ slave structures between chips. The chips are able to minimize power consumption because no external operating clock is necessary for the display data RAM read/write operation. Furthermore, because each chip is equipped internally with a low-power liquid crystal driver power supply, resistors for liquid crystal driver power voltage adjustment and a display clock RC oscillator circuit, the SL20T0081 Series chips can be used to create the lowest power display system with the fewest components for high performance portable systems.

FEATURES

Direct display of RAM data through the display data RAM.
RAM capacity : 81x132 = 8580 bits

Table 1. Duty and Bias selection

Duty	LCD Driver Bias	Maximum display matrix
1/81	1/10 or 1/8	81 x 132
1/65	1/9 or 1/7	65 x 132
1/55	1/8 or 1/6	55 x 132
1/49	1/8 or 1/6	49 x 132
1/33	1/6 or 1/5	33 x 132

RAM bit data : "1" Non-illuminated
"0" illuminated
(during normal display)

High-speed 8-bit MPU interface
The chip can be connected directly to the both the 80x86 series MPUs and the 68000 series MPUs.
Serial interface available (supports write operation only).

Abundant command functions
Display data Read/Write,display ON/OFF, Normal/Reverse display mode, page address set, display start line set, column address set, status read, display all point ON/OFF, LCD bias set, electronic volume, read/modify/write, segment driver direction select, power saver, static indicator, common output status select, V5 voltage regulation internal resistor ratio set.

Static drive circuit equipped internally for indicators
1 driver, with 4 kinds of flashing mode

Built-in Power Supply Circuit

Low-power liquid crystal display power supply circuit equipped internally.
Booster circuit (with Boost ratios of x2 / x3 / x4 / x5, where the step-up voltage reference power supply can be input externally).
High-accuracy voltage adjustment circuit (Thermal gradient -0.05%/^{o}C or external input).
LCD driver voltage regulator resistors and voltage followers equipped internally.
RC oscillator circuit equipped internally (external clock can also be selected).

Operating Voltage Range

Supply Voltage (VDD) : 2.4V ~ 3.6V
LCD driver Voltage (VLCD) : 4.5V ~ 16.0V

Low Power Consumption

Operating power : 40uA typical (conditions:V_{DD} =3V, x 4 boosting (VCI = V_{DD}), V0 =11V, Internal power supply ON,display OFF and normal mode is selected)
Standby power : 10uA maximum (during power save [standby] mode)

Operating Temperatures

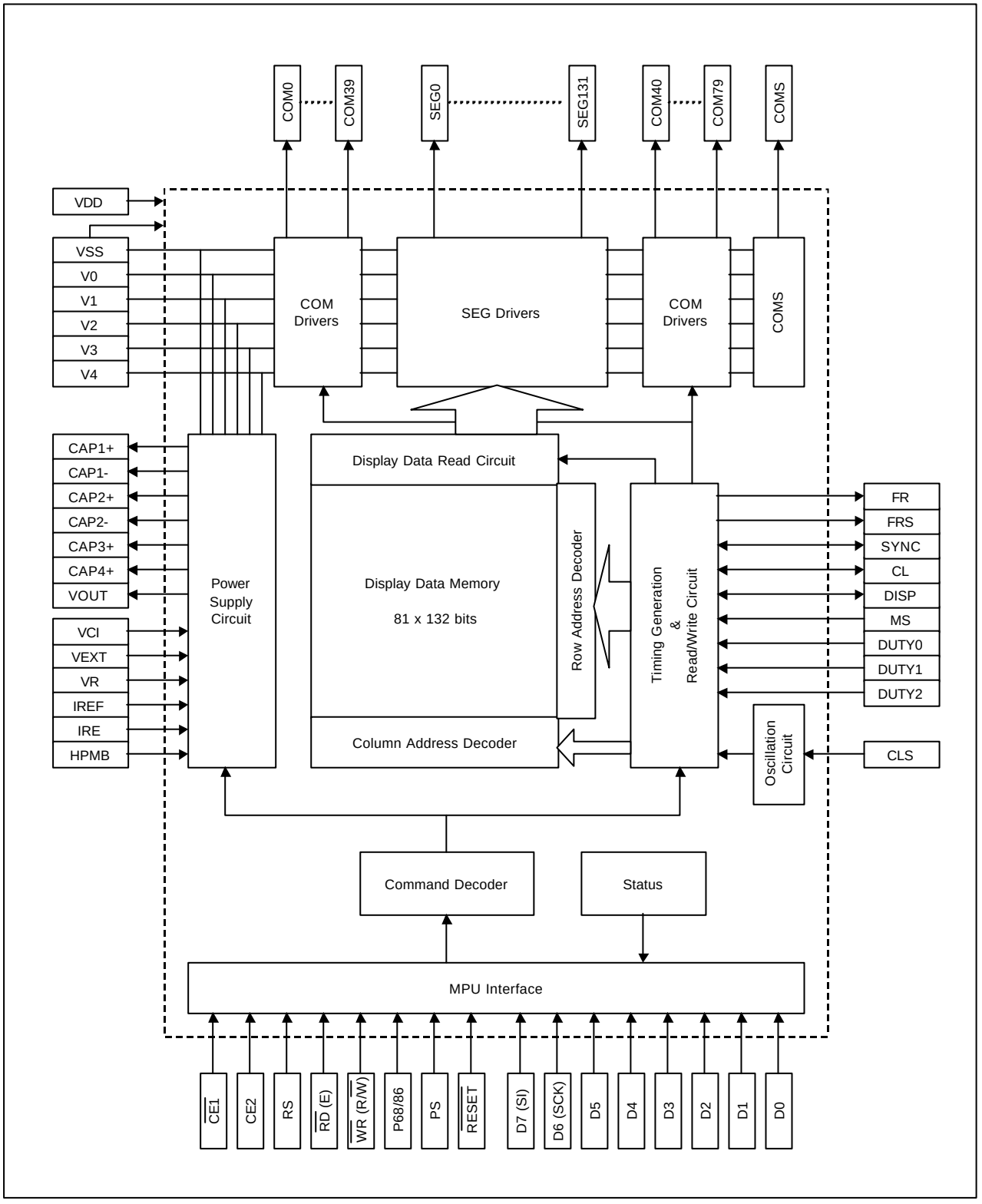
Wide range of operating temperatures : -40 to 85^{o}C

CMOS Process

Package Type

TCP

BLOCKDIAGRAM



PAD CONFIGURATION

PAD Layout

Figure 1. SL20T0081 PAD Layout

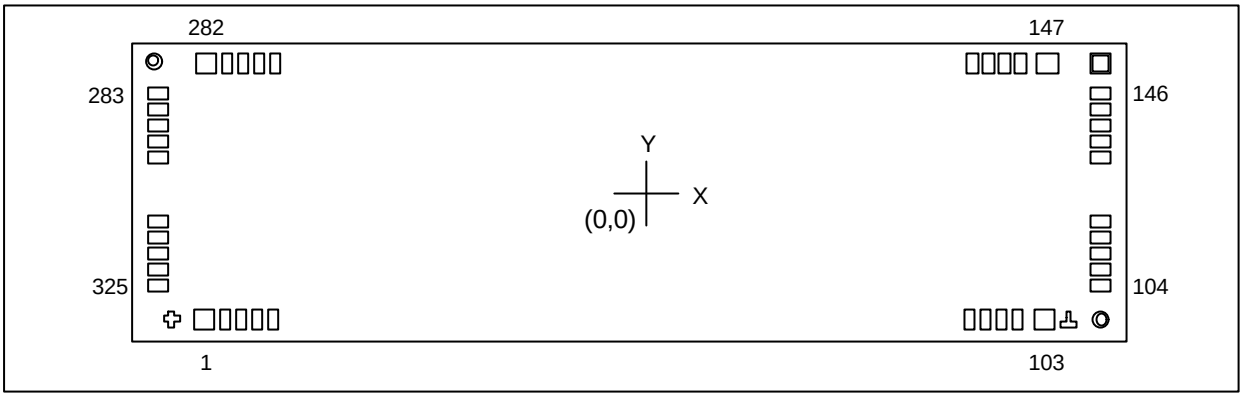
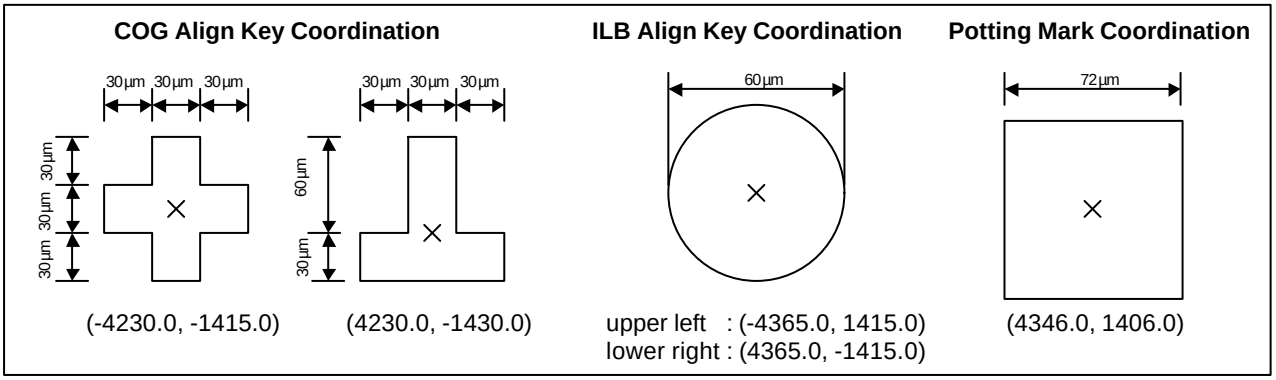


Table 2. SL20T0081 PAD Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip Size	-	8900	3000	μm
Pad pitch	2 to10, 94 to 102, 104 to 146, 148 to 281, 283 to 325	60		
	11 to 41, 45-46, 50 to 93	80		
	41-42, 44-45, 46-47, 49-50	110		
	42 to 44, 47 to 49	120		
	1-2, 102-103, 147-148, 281-282	131		
	10-11, 93-94	90		
Bumped PAD size (Bottom)	2 to 10, 94 to 102, 148 to 281	37	92	
	104 to 146, 283 to 325	92	37	
	11 to 41, 45, 46, 50 to 93	57	92	
	42 to 44, 47 to 49	67	92	
	1, 103, 147, 282	72	97	
Bumped PAD height	All PAD	18		

Figure 2. Align Key Coordination



PAD CENTER COORDINATES

PAD No.	PAD name	X	Y	PAD No.	PAD name	X	Y
1	DUMMY5	-4121	-1411	57	CAP1-	540	-1411
2	DUMMY6	-3990	-1411	58	CAP1+	620	-1411
3	DUMMY7	-3930	-1411	59	CAP1+	700	-1411
4	DUMMY8	-3870	-1411	60	CAP2+	780	-1411
5	DUMMY9	-3810	-1411	61	CAP2+	860	-1411
6	DUMMY10	-3750	-1411	62	CAP2-	940	-1411
7	DUMMY11	-3690	-1411	63	CAP2-	1020	-1411
8	DUMMY12	-3630	-1411	64	VDD	1100	-1411
9	DUMMY13	-3570	-1411	65	VEXT	1180	-1411
10	DUMMY14	-3510	-1411	66	IREF	1260	-1411
11	FRS	-3420	-1411	67	TEST_VREF	1340	-1411
12	FR	-3340	-1411	68	VSS	1420	-1411
13	SYNC	-3260	-1411	69	V1	1500	-1411
14	CL	-3180	-1411	70	V1	1580	-1411
15	DISP	-3100	-1411	71	V2	1660	-1411
16	VDD	-3020	-1411	72	V2	1740	-1411
17	VSS	-2940	-1411	73	V3	1820	-1411
18	$\overline{CE1}$	-2860	-1411	74	V3	1900	-1411
19	CE2	-2780	-1411	75	V4	1980	-1411
20	VDD	-2700	-1411	76	V4	2060	-1411
21	RESETB	-2620	-1411	77	V0	2140	-1411
22	RS	-2540	-1411	78	V0	2220	-1411
23	VSS	-2460	-1411	79	VR	2300	-1411
24	$\overline{WR}$(R/$\overline{W}$)	-2380	-1411	80	VR	2380	-1411
25	$\overline{RD}$(E)	-2300	-1411	81	VSS	2460	-1411
26	VDD	-2220	-1411	82	VSS	2540	-1411
27	D<0>	-2140	-1411	83	VDD	2620	-1411
28	D<1>	-2060	-1411	84	MS	2700	-1411
29	D<2>	-1980	-1411	85	CLS	2780	-1411
30	D<3>	-1900	-1411	86	VSS	2860	-1411
31	D<4>	-1820	-1411	87	P68/80	2940	-1411
32	D<5>	-1740	-1411	88	PS	3020	-1411
33	D<6>	-1660	-1411	89	VDD	3100	-1411
34	D<7>	-1580	-1411	90	HPMB	3180	-1411
35	VSS	-1500	-1411	91	VSS	3260	-1411
36	VDD	-1420	-1411	92	IRE	3340	-1411
37	DUTY0	-1340	-1411	93	VDD	3420	-1411
38	DUTY1	-1260	-1411	94	TRCON	3510	-1411
39	VDD	-1180	-1411	95	VSS	3570	-1411
40	VSS	-1100	-1411	96	TRIM<4>	3630	-1411
41	DUTY2	-1020	-1411	97	TRIM<3>	3690	-1411
42	VDD	-910	-1411	98	VSS	3750	-1411
43	VDD	-790	-1411	99	TRIM<2>	3810	-1411
44	VDD	-670	-1411	100	TRIM<1>	3870	-1411
45	VCI	-560	-1411	101	VSS	3930	-1411
46	VCI	-480	-1411	102	TRIM<0>	3990	-1411
47	VSS	-370	-1411	103	DUMMY15	4121	-1411
48	VSS	-250	-1411	104	DUMMY16	4361	-1250
49	VSS	-130	-1411	105	COM<39>	4361	-1190
50	VOUT	-20	-1411	106	COM<38>	4361	-1130
51	VOUT	60	-1411	107	COM<37>	4361	-1070
52	CAP4+	140	-1411	108	COM<36>	4361	-1010
53	CAP4+	220	-1411	109	COM<35>	4361	-950
54	CAP3+	300	-1411	110	COM<34>	4361	-890
55	CAP3+	380	-1411	111	COM<33>	4361	-830
56	CAP1-	460	-1411	112	COM<32>	4361	-770

PAD CENTER COODINATES (continued)

PAD No.	PAD name	X	Y	PAD No.	PAD name	X	Y
113	COM<31>	4361	-710	169	SEG<20>	2730	1411
114	COM<30>	4361	-650	170	SEG<21>	2670	1411
115	COM<29>	4361	-590	171	SEG<22>	2610	1411
116	COM<28>	4361	-530	172	SEG<23>	2550	1411
117	COM<27>	4361	-470	173	SEG<24>	2490	1411
118	COM<26>	4361	-410	174	SEG<25>	2430	1411
119	COM<25>	4361	-350	175	SEG<26>	2370	1411
120	COM<24>	4361	-290	176	SEG<27>	2310	1411
121	COM<23>	4361	-230	177	SEG<28>	2250	1411
122	COM<22>	4361	-170	178	SEG<29>	2190	1411
123	COM<21>	4361	-110	179	SEG<30>	2130	1411
124	COM<20>	4361	-50	180	SEG<31>	2070	1411
125	COM<19>	4361	10	181	SEG<32>	2010	1411
126	COM<18>	4361	70	182	SEG<33>	1950	1411
127	COM<17>	4361	130	183	SEG<34>	1890	1411
128	COM<16>	4361	190	184	SEG<35>	1830	1411
129	COM<15>	4361	250	185	SEG<36>	1770	1411
130	COM<14>	4361	310	186	SEG<37>	1710	1411
131	COM<13>	4361	370	187	SEG<38>	1650	1411
132	COM<12>	4361	430	188	SEG<39>	1590	1411
133	COM<11>	4361	490	189	SEG<40>	1530	1411
134	COM<10>	4361	550	190	SEG<41>	1470	1411
135	COM<9>	4361	610	191	SEG<42>	1410	1411
136	COM<8>	4361	670	192	SEG<43>	1350	1411
137	COM<7>	4361	730	193	SEG<44>	1290	1411
138	COM<6>	4361	790	194	SEG<45>	1230	1411
139	COM<5>	4361	850	195	SEG<46>	1170	1411
140	COM<4>	4361	910	196	SEG<47>	1110	1411
141	COM<3>	4361	970	197	SEG<48>	1050	1411
142	COM<2>	4361	1030	198	SEG<49>	990	1411
143	COM<1>	4361	1090	199	SEG<50>	930	1411
144	COM<0>	4361	1150	200	SEG<51>	870	1411
145	COMSR	4361	1210	201	SEG<52>	810	1411
146	DUMMY17	4361	1270	202	SEG<53>	750	1411
147	DUMMY18	4121	1411	203	SEG<54>	690	1411
148	DUMMY19	3990	1411	204	SEG<55>	630	1411
149	SEG<0>	3930	1411	205	SEG<56>	570	1411
150	SEG<1>	3870	1411	206	SEG<57>	510	1411
151	SEG<2>	3810	1411	207	SEG<58>	450	1411
152	SEG<3>	3750	1411	208	SEG<59>	390	1411
153	SEG<4>	3690	1411	209	SEG<60>	330	1411
154	SEG<5>	3630	1411	210	SEG<61>	270	1411
155	SEG<6>	3570	1411	211	SEG<62>	210	1411
156	SEG<7>	3510	1411	212	SEG<63>	150	1411
157	SEG<8>	3450	1411	213	SEG<64>	90	1411
158	SEG<9>	3390	1411	214	SEG<65>	30	1411
159	SEG<10>	3330	1411	215	SEG<66>	-30	1411
160	SEG<11>	3270	1411	216	SEG<67>	-90	1411
161	SEG<12>	3210	1411	217	SEG<68>	-150	1411
162	SEG<13>	3150	1411	218	SEG<69>	-210	1411
163	SEG<14>	3090	1411	219	SEG<70>	-270	1411
164	SEG<15>	3030	1411	220	SEG<71>	-330	1411
165	SEG<16>	2970	1411	221	SEG<72>	-390	1411
166	SEG<17>	2910	1411	222	SEG<73>	-450	1411
167	SEG<18>	2850	1411	223	SEG<74>	-510	1411
168	SEG<19>	2790	1411	224	SEG<75>	-570	1411

PAD CENTER COODINATES (continued)

PAD No.	PAD name	X	Y	PAD No.	PAD name	X	Y
225	SEG<76>	-630	1411	281	DUMMY1	-3990	1411
226	SEG<77>	-690	1411	282	DUMMY2	-4121	1411
227	SEG<78>	-750	1411	283	DUMMY3	-4361	1270
228	SEG<79>	-810	1411	284	COM<40>	-4361	1210
229	SEG<80>	-870	1411	285	COM<41>	-4361	1150
230	SEG<81>	-930	1411	286	COM<42>	-4361	1090
231	SEG<82>	-990	1411	287	COM<43>	-4361	1030
232	SEG<83>	-1050	1411	288	COM<44>	-4361	970
233	SEG<84>	-1110	1411	289	COM<45>	-4361	910
234	SEG<85>	-1170	1411	290	COM<46>	-4361	850
235	SEG<86>	-1230	1411	291	COM<47>	-4361	790
236	SEG<87>	-1290	1411	292	COM<48>	-4361	730
237	SEG<88>	-1350	1411	293	COM<49>	-4361	670
238	SEG<89>	-1410	1411	294	COM<50>	-4361	610
239	SEG<90>	-1470	1411	295	COM<51>	-4361	550
240	SEG<91>	-1530	1411	296	COM<52>	-4361	490
241	SEG<92>	-1590	1411	297	COM<53>	-4361	430
242	SEG<93>	-1650	1411	298	COM<54>	-4361	370
243	SEG<94>	-1710	1411	299	COM<55>	-4361	310
244	SEG<95>	-1770	1411	300	COM<56>	-4361	250
245	SEG<96>	-1830	1411	301	COM<57>	-4361	190
246	SEG<97>	-1890	1411	302	COM<58>	-4361	130
247	SEG<98>	-1950	1411	303	COM<59>	-4361	70
248	SEG<99>	-2010	1411	304	COM<60>	-4361	10
249	SEG<100>	-2070	1411	305	COM<61>	-4361	-50
250	SEG<101>	-2130	1411	306	COM<62>	-4361	-110
251	SEG<102>	-2190	1411	307	COM<63>	-4361	-170
252	SEG<103>	-2250	1411	308	COM<64>	-4361	-230
253	SEG<104>	-2310	1411	309	COM<65>	-4361	-290
254	SEG<105>	-2370	1411	310	COM<66>	-4361	-350
255	SEG<106>	-2430	1411	311	COM<67>	-4361	-410
256	SEG<107>	-2490	1411	312	COM<68>	-4361	-470
257	SEG<108>	-2550	1411	313	COM<69>	-4361	-530
258	SEG<109>	-2610	1411	314	COM<70>	-4361	-590
259	SEG<110>	-2670	1411	315	COM<71>	-4361	-650
260	SEG<111>	-2730	1411	316	COM<72>	-4361	-710
261	SEG<112>	-2790	1411	317	COM<73>	-4361	-770
262	SEG<113>	-2850	1411	318	COM<74>	-4361	-830
263	SEG<114>	-2910	1411	319	COM<75>	-4361	-890
264	SEG<115>	-2970	1411	320	COM<76>	-4361	-950
265	SEG<116>	-3030	1411	321	COM<77>	-4361	-1010
266	SEG<117>	-3090	1411	322	COM<78>	-4361	-1070
267	SEG<118>	-3150	1411	323	COM<79>	-4361	-1130
268	SEG<119>	-3210	1411	324	COMSL	-4361	-1190
269	SEG<120>	-3270	1411	325	DUMMY4	-4361	-1250
270	SEG<121>	-3330	1411				
271	SEG<122>	-3390	1411				
272	SEG<123>	-3450	1411				
273	SEG<124>	-3510	1411				
274	SEG<125>	-3570	1411				
275	SEG<126>	-3630	1411				
276	SEG<127>	-3690	1411				
277	SEG<128>	-3750	1411				
278	SEG<129>	-3810	1411				
279	SEG<130>	-3870	1411				
280	SEG<131>	-3930	1411				

PIN DESCRIPTION

Power Supply Pins

Pin Name	I/O	Function
VDD	Power Supply	Positive Power Supply.
VSS	Power Supply	System Ground.
VCI	Power Supply	Voltage Booster input pin. The power supply for the voltage booster. VCI input voltage is the reference of boosted output voltage (VOUT) of voltage booster.
V0 V1 V2 V3 V4	Power Supply	LCD driver supply voltage pins. When the internal LCD power supply circuit is enabled, these voltages are generated by it. When the internal LCD power supply circuit is disabled, these voltages must be supplied externally, and they should have the following relationship. VSS ≤ V4 ≤ V3 ≤ V2 ≤ V1 ≤ V0

LCD Power Supply Circuit Pins

Pin Name	I/O	Function
CAP1+	O	Voltage booster pin. Connect a capacitor between this pin and the CAP1- pin
CAP1-	O	Voltage booster pin. Connect a capacitor between this pin and the CAP1+ pin
CAP2+	O	Voltage booster pin. Connect a capacitor between this pin and the CAP2- pin
CAP2-	O	Voltage booster pin. Connect a capacitor between this pin and the CAP2+ pin
CAP3+	O	Voltage booster pin. (refer the application example to connecting a capacitor)
CAP4+	O	Voltage booster pin. (refer the application example to connecting a capacitor)
VOUT	O	Voltage booster pin. Connect a capacitor between this pin and VSS.
VEXT	I	This is the external reference voltage input pin of the LCD power supply circuit. This pin is valid only when internal reference voltage circuit is disabled (IREF=0).
IREF	I	Internal reference voltage circuit enable pin. IREF = 0 : Internal reference voltage circuit is disabled. External reference voltage is inputted via VEXT pin. IREF = 1 : Internal reference voltage circuit is enabled.
VR	I	External V0 voltage adjustment pin. VR pin is valid only when the internal voltage regulator resistors are not used (IRE=0)
IRE	I	Internal voltage regulator resistor enable pin. This pin selects the resistors for the V0 voltage level adjustment. IRE = 1 : Use the internal resistors IRE = 0 : Do not use the internal resistors. The V0 voltage level is controlled by the external resisters that connected among V0 pin and VR pin and VSS.

System Control pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>MS</td><td>I</td><td>This pin selects the master/slave operation for the SL20T0081 chip. Master operation outputs the timing signals that are required for the LCD display, while slave operation inputs the timing signals required for the liquid crystal display.
MS = 1 : Master operation
MS = 0 : Slave operation
Following table shows difference of the master operation and the slave operation.
<table>
<tr><th>MS</th><th>CLS</th><th>Internal Oscillator Circuit</th><th>Internal Power Supply Circuit</th><th>CL</th><th>SYNC</th><th>DISP</th></tr>
<tr><td rowspan="2">1</td><td>1</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>0</td><td>Disabled</td><td>Enabled</td><td>Input</td><td>Output</td><td>Output</td></tr>
<tr><td>0</td><td>-</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Input</td></tr>
</table></td></tr>
<tr><td>CL</td><td>I/O</td><td>This is the display clock input/output pin.
When multiple SL20T0081 chips are used in master/slave mode, all of CL pins must be connected each other.</td></tr>
<tr><td>CLS</td><td>I</td><td>Internal RC oscillator enable pin.
CLS = 1 : Internal oscillator circuit is enabled.
CLS = 0 : Internal oscillator circuit is disabled.
When CLS=0, the display clock must be inputted through the CL pin.
This pin is valid only when SL20T0081 operating in master operation.</td></tr>
<tr><td>SYNC</td><td>I/O</td><td>LCD synchronization signal input/output pin.
When multiple SL20T0081 chips are used in master/slave mode, all of SYNC pins must be connected each other.</td></tr>
<tr><td>DISP</td><td>I/O</td><td>This is the liquid crystal display blanking control pin.
When multiple SL20T0081 chips are used in master/slave mode, all of DISP pins must be connected each other.</td></tr>
<tr><td>DUTY0
DUTY1
DUTY2</td><td>I</td><td>The LCD driver duty ratio selection pins.
<table>
<tr><th>DUTY2</th><th>DUTY1</th><th>DUTY0</th><th>Duty ratio</th><th>Common Output</th></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1/81</td><td>Even, Odd</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1/81</td><td>normal</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1/65</td><td>“</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1/55</td><td>“</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1/49</td><td>“</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1/33</td><td>“</td></tr>
</table>
When Duty = (1, 1, 1), 1/81 duty ratio is selected, and common output pin configuration is changed. At this mode, all even numbered common output pins are outputting right side of the device and all odd numbered common output pins are outputting left side of the device.</td></tr>
<tr><td>HPMB</td><td>I</td><td>This is the power control pin for the power supply circuit for liquid crystal drive.
HPMB = 1 : Normal mode
HPMB = 0 : High power mode
This pin is enabled only when the master operation mode is selected.
It is fixed to either 0 or 1 when the slave operation mode is selected.</td></tr>
</table>

System Interface pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>$\overline{\text{RESET}}$</td><td>I</td><td>Device Reset pin.
When $\overline{\text{RESET}}$ = 0, device initialization operation is executed.</td></tr>
<tr><td>D7 ~ D0

(SI)
(SCK)</td><td>I/O</td><td>8bit bi-directional data bus that should be connected to the standard MPU data bus.
When PS=0 the serial interface is enabled and pins are set as following.
D7 : Serial data input (SI)
D6 : Serial interface clock input (SCK)
D5 ~ D0 : high impedance state
When the chip does not be selected, D7 ~ D0 are set to high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Display data / Control data selection signal input pin
RS = 1 : D7 ~ D0 input are display data
RS = 0 : D7 ~ D0 input are control data</td></tr>
<tr><td>$\overline{\text{CE1}}$
CE2</td><td>I</td><td>Chip Select signal input pins
When $\overline{\text{CE1}}$ = 0 and CE2 = 1, then the chip select becomes active,
and data/command I/O is enabled.</td></tr>
<tr><td>$\overline{\text{RD}}$
(E)</td><td>I</td><td>• When the device connected to an 8080 MPU bus, this pin acts as “active LOW” read signal input pin. If the device is selected and $\overline{\text{RD}}$ = 0, then SL20T0081 outputs the data to data bus pins.
• When the device connected to a 6800 MPU bus, this pin acts as “active HIGH” R/$\overline{\text{W}}$ enable signal input pin. If the device is selected and $\overline{\text{RD}}$ = 1, then SL20T0081 executes read or write operation that controlled by $\overline{\text{WR}}$ signal.</td></tr>
<tr><td>$\overline{\text{WR}}$
(R/$\overline{\text{W}}$)</td><td>I</td><td>• When the device connected to an 8080 MPU bus, this pin acts as “active LOW” write signal input pin. If the device is selected and $\overline{\text{WR}}$ = 0, then SL20T0081 accepts the data via data bus pins.
• When the device connected to a 6800 MPU bus, this pin acts as read/write control signal input pin.
$\overline{\text{WR}}$(R/$\overline{\text{W}}$) = 1 : Read
$\overline{\text{WR}}$(R/$\overline{\text{W}}$) = 0 : Write</td></tr>
<tr><td>P68/80</td><td>I</td><td>Bus type selection pin.
P68/80 = 1 : 6800 MPU bus type interface.
P68/80 = 0 : 8080 MPU bus type interface</td></tr>
<tr><td>PS</td><td>I</td><td>Parallel data transfer / Serial data transfer mode selection pin.
PS = 1 : Parallel data transfer mode.
PS = 0 : Serial data transfer mode.
<table>
<tr><th>PS</th><th>Data transfer mode</th><th>Read</th><th>Write</th><th>Data bus</th><th>SCK pin</th></tr>
<tr><td>1</td><td>Parallel data transfer</td><td>enabled</td><td>enabled</td><td>D7 ~D0</td><td>-</td></tr>
<tr><td>0</td><td>Serial data transfer</td><td>disabled</td><td>enabled</td><td>D7 (SI)</td><td>D6 (SCK)</td></tr>
</table>
When PS = 0, $\overline{\text{RD}}$(E) and $\overline{\text{WR}}$(R/$\overline{\text{W}}$) pins are fixed to either 0 or 1.</td></tr>
</table>

Liquid Crystal Drive Pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>SEG0
~
SEG131</td><td>O</td><td>LCD segment driver output pins.
Segment driver output voltage is controlled by display data and FR signal.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">FR</th><th colspan="2">Segment driver output voltage</th></tr>
<tr><th>Normal Display</th><th>Reverse Display</th></tr>
<tr><td>1</td><td>1</td><td>V0</td><td>V2</td></tr>
<tr><td>1</td><td>0</td><td>VSS</td><td>V3</td></tr>
<tr><td>0</td><td>1</td><td>V2</td><td>V0</td></tr>
<tr><td>0</td><td>0</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Power save</td><td colspan="2">VSS</td></tr>
</table></td></tr>
<tr><td>COM0
~
COM79</td><td>O</td><td>LCD common driver output pins.
Common driver output voltage is controlled by internal scanning data and FR signal.
<table>
<tr><th>Scan Data</th><th>FR</th><th>Common driver output voltage</th></tr>
<tr><td>1</td><td>1</td><td>VSS</td></tr>
<tr><td>1</td><td>0</td><td>V0</td></tr>
<tr><td>0</td><td>1</td><td>V1</td></tr>
<tr><td>0</td><td>0</td><td>V4</td></tr>
<tr><td colspan="2">Power save mode</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COMS(R)
COMS(L)</td><td>O</td><td>Common drive output for the icons. There are two COMS pin, COMS(R), COMS(L). They output same signal. When in master/slave mode, the same signal is output by both master and slave.</td></tr>
<tr><td>FR</td><td>O</td><td>Static segment driver output pin. This pin is paired with FRS pin.</td></tr>
<tr><td>FRS</td><td>O</td><td>Static segment driver output pin. This pin is paired with FR pin.</td></tr>
</table>

FUNCTION DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There are CE1 and CE2 pins for chip selection. The SL20T0081 can interface with an MPU only when CE1 is "L" and CE2 is "H". When these pins are set to any other combination, RS, RDB(E) and_WRB(RW) inputs are disabled and D0to D7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

SL20T0081 has three types of interface with an MPU, which are one serial and two parallel interfaces. This parallel or serial inter face is determined by PS pin.

Table 3. Parallel / Serial Interface Mode

PS	Type	$\overline{CE1}$	CE2	P68/80	Interface mode
H	Parallel	$\overline{CE1}$	CE2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	$\overline{CE1}$	CE2	*x	Serial-mode

*x :Don' t care

Parallel Interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by P68/80 as shown in table 4. The type of data transfer is determined by signals at RS, $\overline{RD}$(E) and $\overline{WR}$(R/$\overline{W}$) as shown in table 5.

Table 4. Microprocessor Selection for Parallel Interface

P68/80	$\overline{CE1}$	CE2	RS	$\overline{RD}$(E)	$\overline{WR}$(R/$\overline{W}$)	D0 to D7	MPU bus
H	$\overline{CE1}$	CE2	RS	E	R/$\overline{W}$	D0 to D7	6800-series
L	$\overline{CE1}$	CE2	RS	$\overline{RD}$	$\overline{WR}$	D0 to D7	8080-series

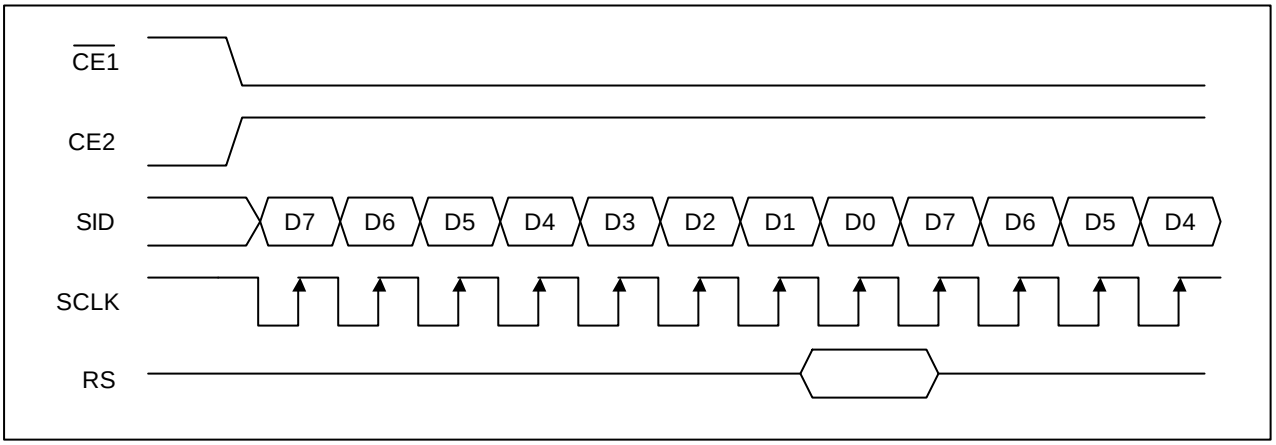
Table 5. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	$\overline{RD}$	$\overline{WR}$	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

Serial Interface (PS = "L")

When the SL20T0081 is active, serial data (D7) and serial clock (D6) input are enabled. And not active,the internal 8-bit shift register and the 3-bit counter are reset. Serial data can be read on the rising edge of serial clock going into D6 and processed as 8-bit parallel data on the eighth serial clock. Serial data input is display data when RS is high and caused by the line length, the operation check on the actual machine is recommended.

Figure 3. Serial Interface Timing



Busy Flag

The Busy Flag indicates whether the SL20T0081 is operating or not. When D7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The SL20T0081 used bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to internal RAM, data is automatically transferred the bus holder to the RAM as shown in figure 4. And when reading data from internal RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 5. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

Figure 4. Write Timing

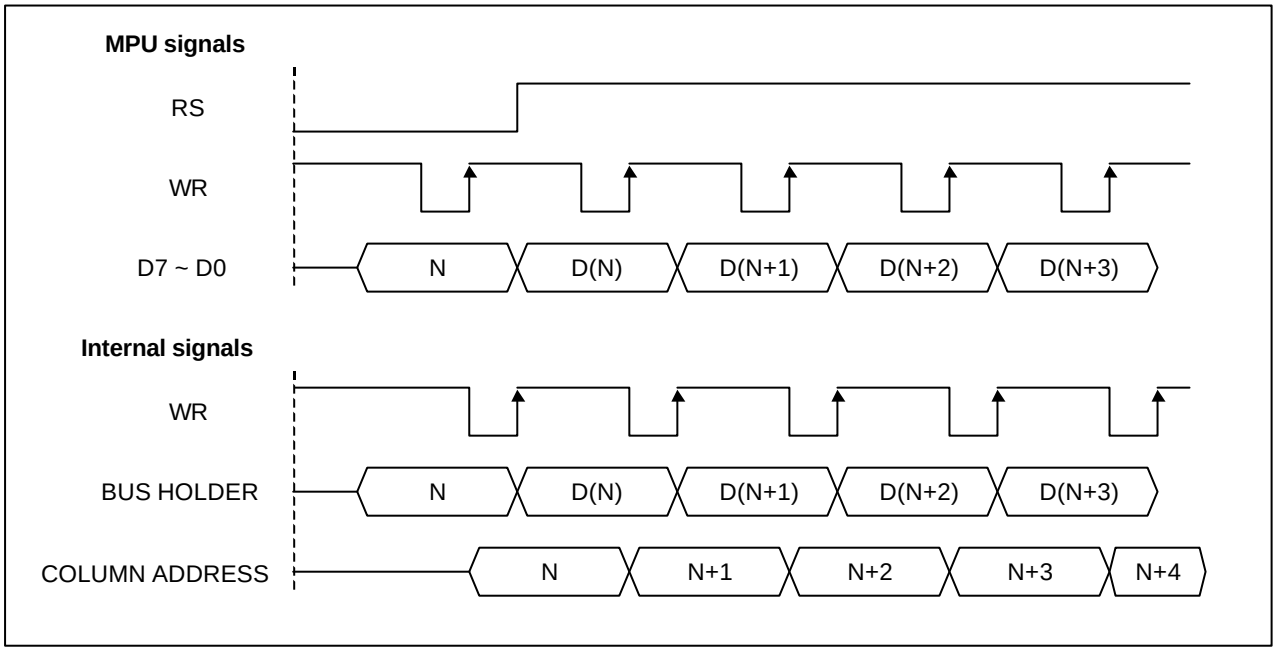
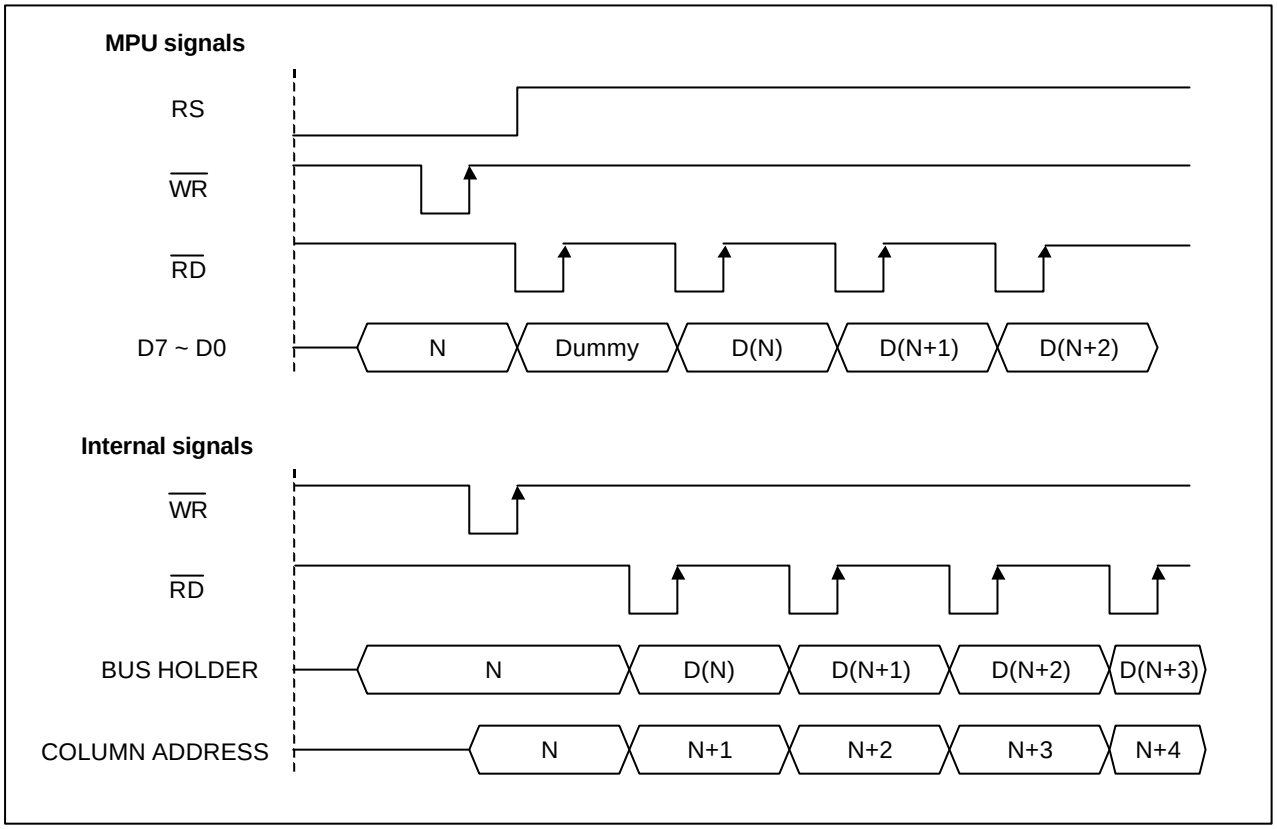


Figure 5. Read Timing

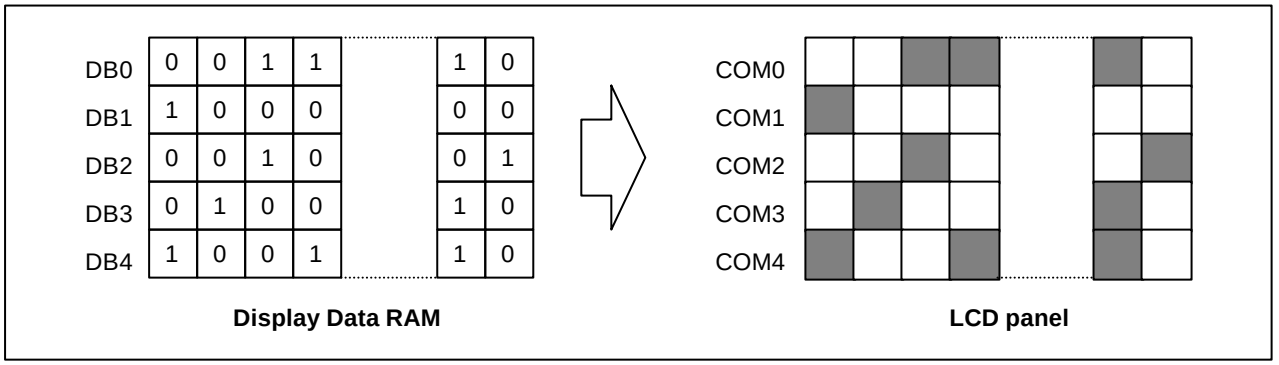


LCD DISPLAY CIRCUIT

Display Data RAM

The Display Data RAM stores pixel data for the LCD. It is 81-row by 132-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 81 row are divided into 10 pages of 8 lines and the 11th page with a single line (D0 only). Data is read from or written to the 8 lines of each page directly through D7 to D0. The display data of D7 to D0 from the microprocessor correspond to the LCD common lines as shown in figure 6. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Figure 6. Display Data RAM to LCD panel Data Transfer



Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM show in figure 6. It incorporates 4-bit Page Address register changed by only the "Set Page" instruction. Page Address 11 is a special RAM area for the icons and display dataD0 is only valid. When Page Address is above 8, it is impossible to access to Display Data RAM.

Line Address Circuit

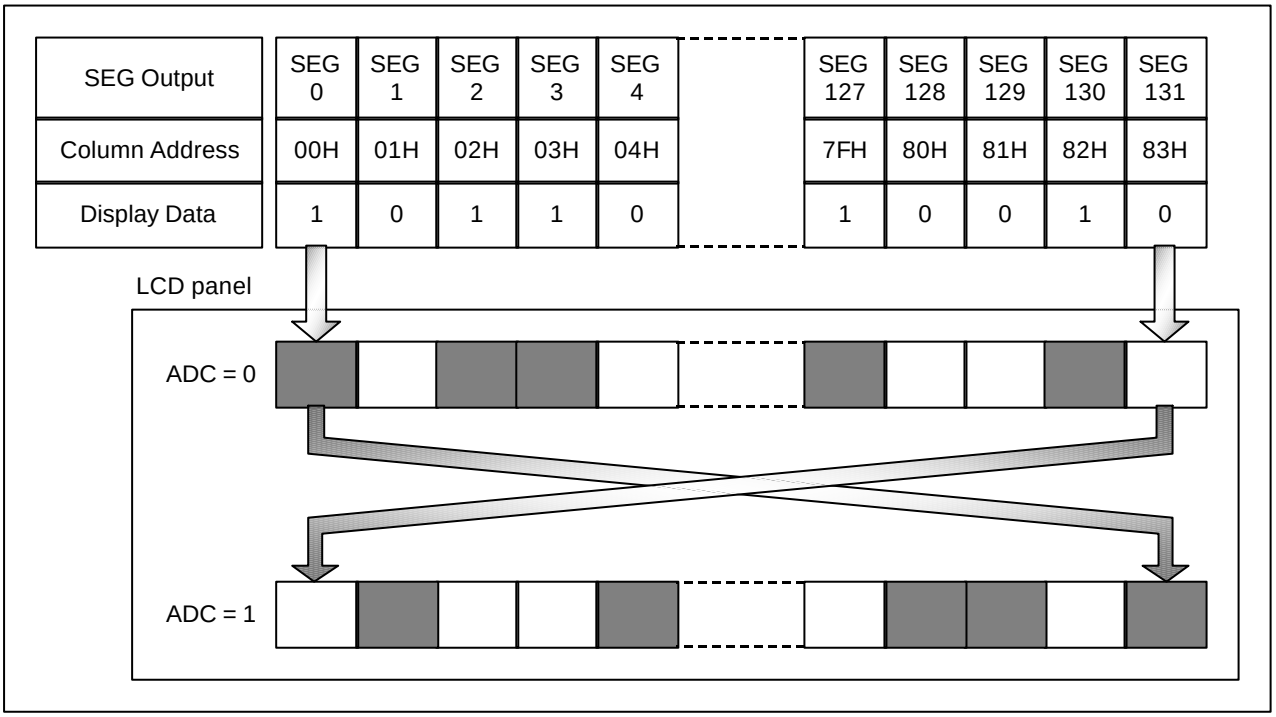
This circuit assigns Display Data RAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of Display Data RAM as shown in figure 6. It incorporates 7-bit line address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the Line Address for transferring the 132-bit RAM data to the display data latch circuit. However, display data of icons are not scrolled because the MPU can not access Line Address of icons.

Column Address Circuit

Column Address circuit has an 8-bit preset counter that provides column address to the Display Data RAM as show in figure 7. When Set Column Address MSB/LSB instruction is issued, 8-bit [Y7:Y0] is updated. And, since this address is increased by 1 each or write data instruction, microprocessor can access the display data continuously. However, the counter is not increased and locked if a non-existing address above 84H. It is unlocked if a column address is set again by set Column Address MSB/LSB instruction. And the Column Address counter is independent of page address register.

ADC Select instruction makes it possible to invert the relationship between the Column Address and the segment outputs.It is necessary to rewrite the display data on built-in RAM after issuing ADC select instruction. Refer to the following figure 7.

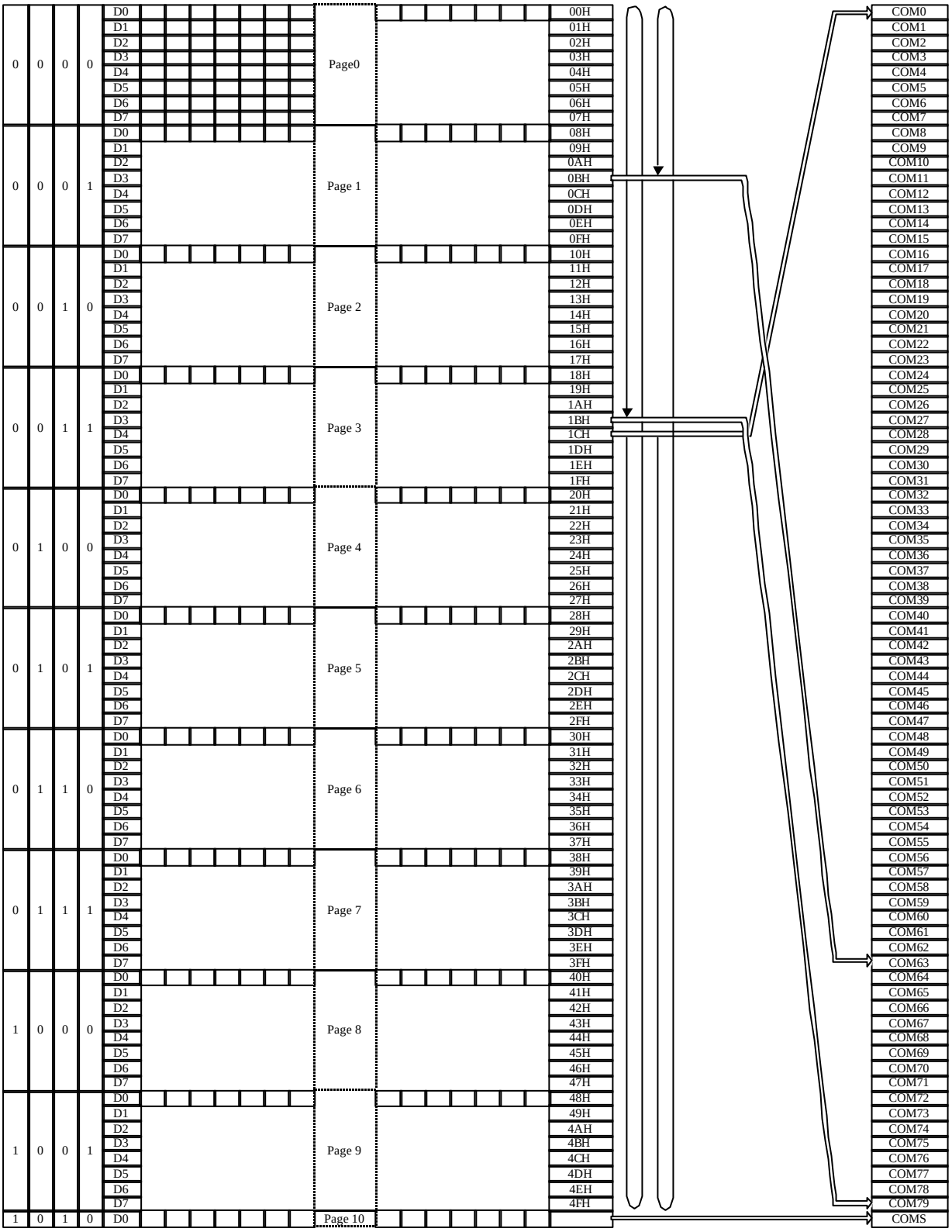
Figure 7. The Relationship between Column Address and Segment output



Segment Control Circuit

This circuit controls the display data by the display ON/OFF, reverse display ON/OFF and entire display ON/OFF instructions without changing the data in display data RAM.

Figure 8. Display Data RAM Map (1/81, 1/65 duty mode)



Column Address	ADC=0	00	01	02	03	04	05	06	----	7D	7E	7F	80	81	82	83
	ADC=1	83	82	81	80	7F	7E	7D	----	06	05	04	03	02	01	00
LCD Output		SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	----	SEG125	SEG126	SEG127	SEG128	SEG129	SEG130	SEG131

Example of when initial display start line address is 1CH.

Oscillator

This is completely on-chip oscillator and its frequency is nearly independent of VDD. This oscillator signal is used in the voltage converter and display timing generation circuit. The oscillator circuit is only enabled when MS="H" and CLS="H". When on-chip oscillator is not used, CLS pin must be "L" condition. In this time, external clock must be input from CL pin.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL generated by oscillation clock, generates a clock to the line counter and a latch signal to the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock (CL) and the 132-bit display data is latched by the display data latch circuit in synchronization with display clock. The display data which is read to the LCD driver is completely independent of the access to the display data RAM from the microprocessor. The LCD AC signal, SYNC is generated from the display clock. 2-frame AC driver waveforms with internal timing signal are shown in figure 8.

In a multiple chip configuration, the slave chip requires the SYNC, CL and DISP signals from the master. Table 6 shows the SYNC, CL, and DISP status.

Table 6. Master and Slave Timing Signal Status

Operation mode	Oscillator	SYNC	CL	DISP
Master	ON(internal clock used)	Output	Output	Output
	OFF(external clock used)	Output	Input	Output
Slave	-	Input	Input	Input

Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio. SHL select instruction specifies the scanning direction of the common output pins.

Table 7. The Relationship between Duty Ratio and Common Output

Duty	SHL	Common output pins										
		COM 0 ~ 15	**COM 16 ~ 23**	**COM 24 ~ 26**	**COM 27 ~ 31**	**COM 32 ~ 39**	**COM 40 ~ 47**	**COM 48 ~ 52**	**COM 53 ~ 55**	**COM 56 ~ 63**	**COM 64 ~ 79**	**COMS**
1/33	**0**	COM 0 ~ 15	NC*1								COM 16 ~ 31	COMS
	1	COM 31 ~ 16	NC*1								COM 15 ~ 0	
1/49	**0**	COM0 ~ COM23			NC*1					COM24 ~ COM47		
	1	COM47 ~ COM24			NC*1					COM23 ~ COM0		
1/55	**0**	COM0 ~ COM26			NC*1				COM27 ~ COM53			
	1	COM53 ~ COM27			NC*1				COM26 ~ COM0			
1/65	**0**	COM0 ~ COM31				NC*1		COM32 ~ COM63				
	1	COM63 ~ COM32				NC*1		COM31 ~ COM0				
1/81	**0**	COM 0 ~ COM79										
	1	COM 79 ~ COM0										

NC*1 : NO Connection

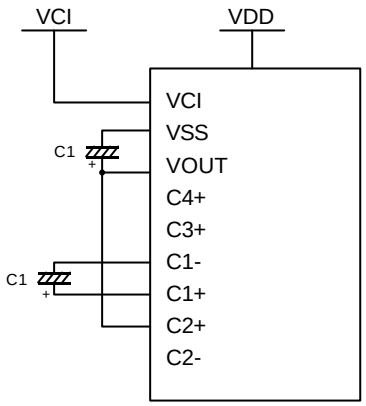
POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to driver liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by power control instruction . For details, refers to " Instruction Description". Table 8 shows the referenced combinations in using Power Supply circuits.

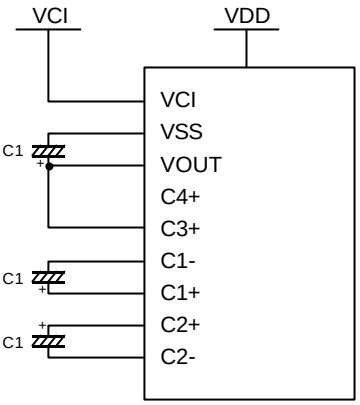
Table 8. Recommended Power Supply Combinations

User Setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	Open	External input	Open
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

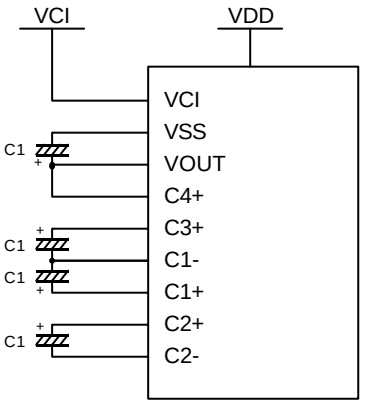
Figure 9. Power supply circuits for various voltage boosting



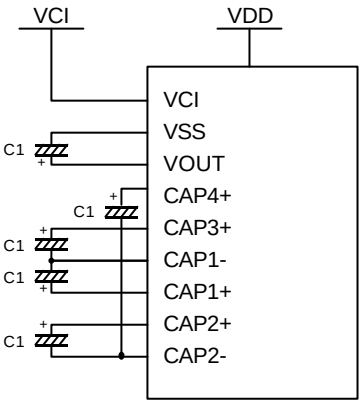
(a) 2-times voltage boosting configuration
(VOUT = 2VCI)



(b) 3-times voltage boosting configuration
(VOUT = 3VCI)



(c) 4-times voltage boosting configuration
(VOUT = 3VCI)



(d) 5-times voltage boosting configuration
(VOUT = 5VCI)

Voltage Regulator Circuits

The function of the internal voltage regulator circuits is to determine liquid crystal operating voltage, V0,by adjusting resistors, Ra and Rb, within the range of [V0]< [VOUT]. Because VOUT is the operating voltage of operational amplifier circuits showing Figure 10, it is necessary to be applied internally or externally.

For the Eq. 1, we determine V0 by Ra, Rb and VEV. The Ra are connected internally or externally by INTRS pin. And VEV called the voltage of electronic volume is determined by Eq. 2,, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. VREF voltage at Ta = 25°C is shown in table 9.

$$V0 = \left(1 + \frac{Rb}{Ra} \right) \times V_{EV} \quad [V] \qquad \cdots\cdots (Eq.1)$$

$$V_{EV} = \left(1 - \frac{(63 - \alpha)}{162} \right) \times V_{REF} \quad [V] \qquad \cdots\cdots (Eq.2)$$

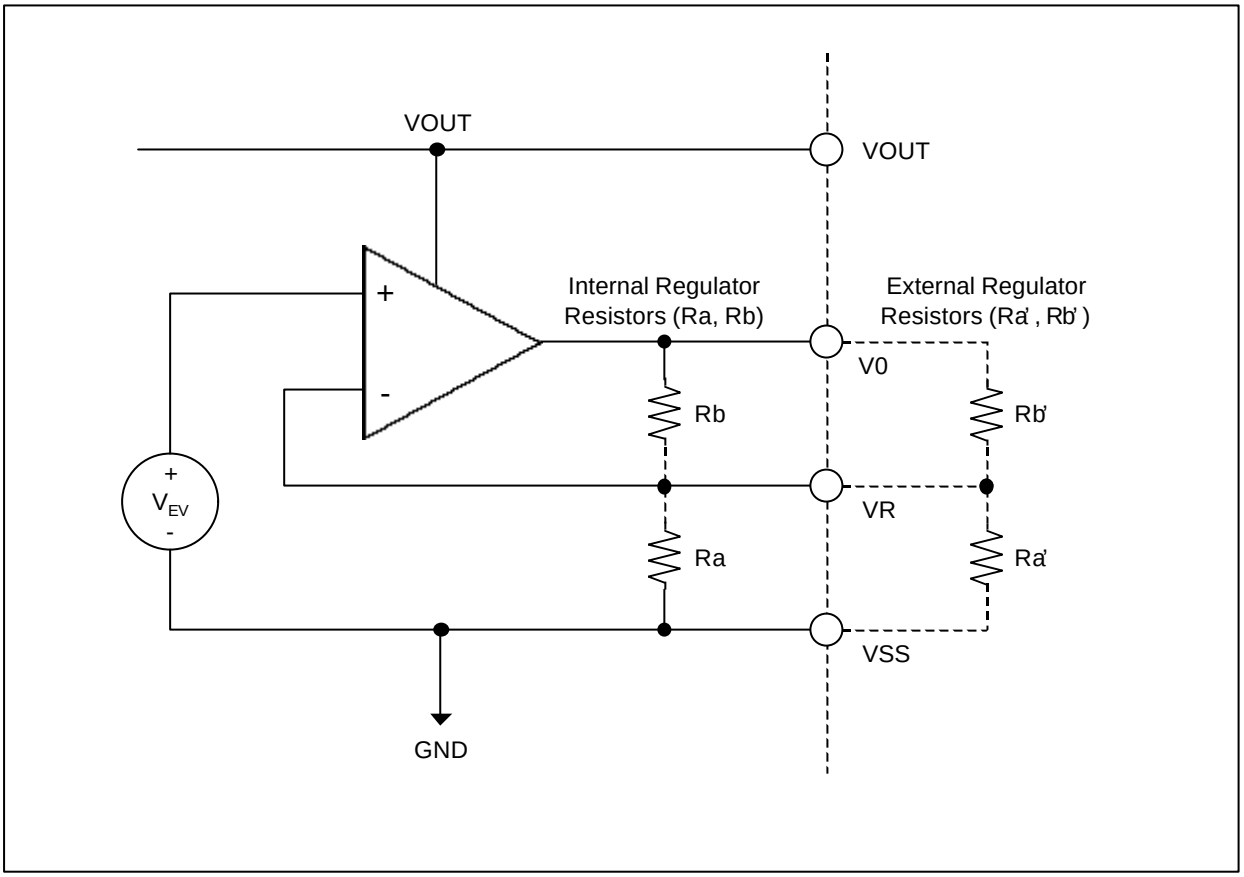
Table 9. VREF Voltage at Ta = 25°C

REF	Temp. coefficient	VREF [V]
H	-0.05% / °C	2.1
L	External input	VEXT

Table 10. Electronic Contrast Control Register (64 Steps)

VR5	VR4	VR3	VR2	VR1	VR0	Reference voltage parameter	V0	Contrast
0	0	0	0	0	0	0	Minimum	Low
0	0	0	0	0	1	1		
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	32(default)		
:	:	:	:	:	:	:		
1	1	1	1	1	0	62	Maximum	High
1	1	1	1	1	1	63		

Figure 10. Internal Voltage Regulator Circuit



In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")

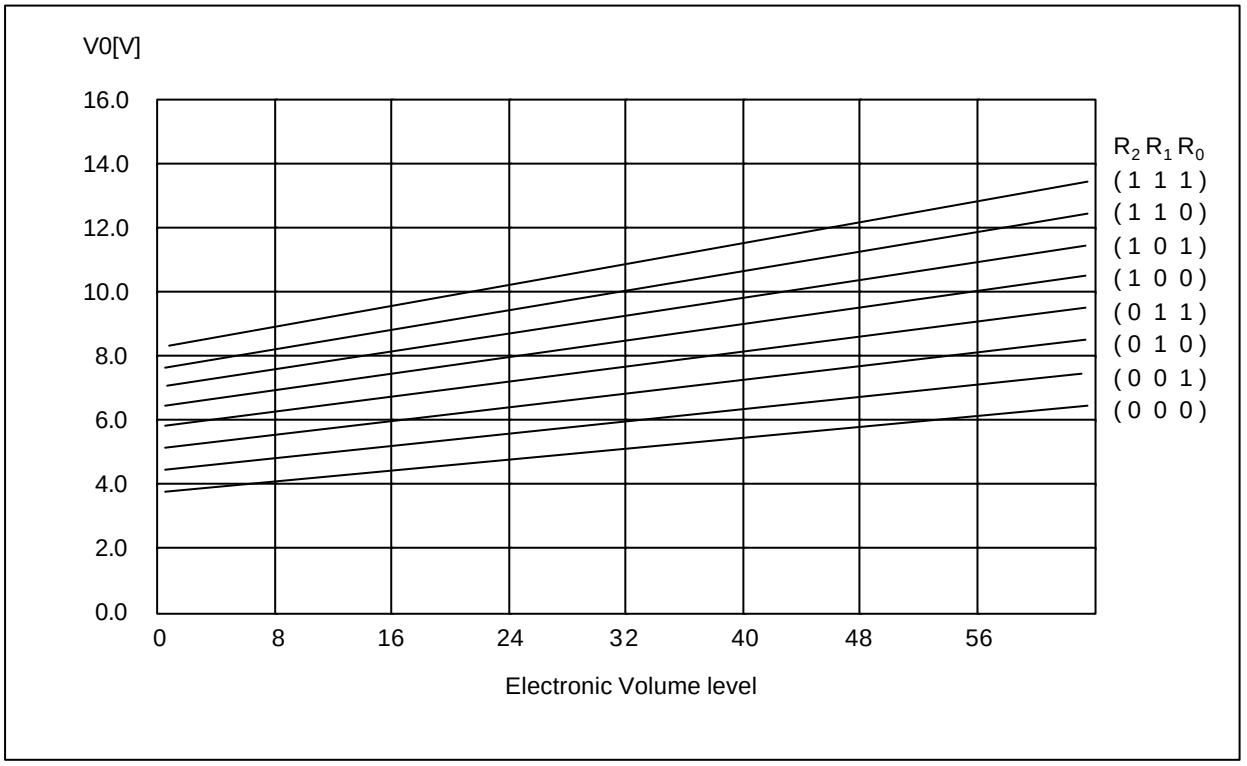
When INTRS pin is "H", resistor Ra is connected internally between VR pin and VSS, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 11. Internal Rb/Ra ratio depending on 3-bit data (R2 R1 R0)

R2 R1 R0	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
1 + (Rb/Ra)	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.4

The following figure shows V0 voltage measured by adjusting internal regulator resistor ratio (Rb/Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25°C.

Figure 11. Electronic Volume Level



In Case of Using External Resistors, Ra and Rb (INTRS ="L")

When INTRS pin is "L", it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example : For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1uA

From Eq.1 and Eq.2

$$10 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \qquad \cdots\cdots \text{(Eq.3)}$$

$$V_{EV} = \left(1 - \frac{(63 - 32)}{162}\right) \times 2.1 \cong 1.698 \ [V] \qquad \cdots\cdots \text{(Eq.4)}$$

From requirement 3

$$\frac{10}{Ra + Rb} = 1 \ [uA] \qquad \cdots\cdots \text{(Eq.5)}$$

From equations Eq.3, 4 and 5

$Ra \cong 1.69$ [MΩ]

$Rb \cong 8.31$ [MΩ]

The following table shows the range of V0 depending on the above requirements.

Table 12. V0 Depending on Electronic Volume Level

	Electronic volume level				
	0	**…..**	**32**	**…..**	**63**
V0	7.57	…..	10.00	…..	12.43

Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3, V4), and those output impedance are converted by the Voltage Follower for increasing drive capability. The following table shows the relationship between V1 to V level and each duty ratio.

Table 13. The Relationship between V1 to V4 Level and Duty Ratio

Duty ratio	DUTY2	DUTY1	DUTY0	LCD bias	V1	V2	V3	V4
1 / 81	H H	L H	L H	1/8	(7/8) x V0	(6/8) x V0	(2/8) x V0	(1/8) x V0
				1/10	(9/10) x V0	(8/10) x V0	(2/10) x V0	(1/10) x V0
1 / 65	L	L	H	1/7	(6/7) x V0	(5/7) x V0	(2/7) x V0	(1/7) x V0
				1/9	(8/9) x V0	(7/9) x V0	(2/9) x V0	(1/9) x V0
1 / 55	L	L	H	1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
				1/8	(7/8) xV0	(6/8) x V0	(2/8) x V0	(1/8) x V0
1 / 49	L	L	H	1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
				1/8	(7/8) xV0	(6/8) x V0	(2/8) x V0	(1/8) x V0
1 / 33	L	L	H	1/5	(4/5) x V0	(3/5) x V0	(2/5) x V0	(1/5) x V0
				1/6	(5/6) xV0	(5/6) x V0	(2/6) x V0	(1/6) x V0

High Power Mode

The power supply circuit equipped in the SL20T0081 for LCD drive has very low power consumption (in normal mode: HPMB = “H”). If use for LCD panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the HPMB pin to “L” (high power mode) can improve the quality of the display. Moreover, if the quality of display is inadequate even after high power mode has been set, then it is necessary to add a liquid crystal drive power supply externally (VOUT or V0 or V1, V2, V3, V4).

RESET CIRCUIT

Setting $\overline{\text{RESET}}$ to "L" or Reset instruction con internal function.
When $\overline{\text{RESET}}$ becomes "L", following procedure is occurred.

Display ON/OFF: OFF
All segments ON/OFF: OFF(normal)
ADC select: OFF(normal)
Reverse display ON/OFF: OFF(normal)
Power control register (VC, VR, VF) = (0,0,0)
Serial interface internal register data clear
LCD bias ratio: 1/9 (1/65 duty), 1/8 (1/55 duty), 1/6 (1/33 duty)
On-chip oscillator OFF
Power save release
Read-modify-write: OFF
SHL select: OFF(normal)
Static indicator mode: OFF
Static indicator register: (S1, S0) = (0, 0)
Display start line: 0 (first)
Column address: 0
Page address: 0
Regulator resistor select register: (R2, R1, R0) = (1, 0, 0)
Reference voltage set: OFF
Reference voltage control register: (VR5, VR4, VR3, VR2, VR1, VR0) = (1, 0, 0, 0, 0, 0)
Test mode release

When $\overline{\text{RESET}}$ instruction is issued, following procedure is occurred.

Read-modify-write: OFF
Static indicator mode: OFF
Static indicator register:(S1, S0) = (0, 0)
SHL select: 0
Display start line: 0 (first)
Column address: 0
Page address: 0
Regulator resistor select register: (R2, R1, R0) = (1, 0, 0)
Reference voltage control register: (VR5, VR4, VR3, VR2, VR1, VR0) = (1, 0, 0, 0, 0, 0)
Test mode release

While $\overline{\text{RESET}}$ is "L" or Reset instruction is executed,no instruction except read status could be accepted. Reset status appears at D4. After D4 becomes "L", any instruction can be accepted. $\overline{\text{RESET}}$ must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by $\overline{\text{RESET}}$ is essential before used.

INSTRUCTION DESCRIPTION

Table 14. Instruction Table

Instruction	Instruction Code											Function
	RS	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	DON	DON = 1 : LCD display ON DON = 0 : LCD display OFF
Display start line set	0	1	0	0	1	SL5	SL4	SL3	SL2	SL1	SL0	Set the Display Data RAM address that corresponds COM0 output
Display start line set (double byte instruction)	0 0	1 1	0 0	1 x	0 SL6	1 SL5	0 SL4	1 SL3	0 SL2	0 SL1	1 SL0	Set the Display Data RAM address that corresponds COM0 output for 1/81 duty (7bits).
Display start line reset	0	1	0	1	0	1	0	1	0	0	0	Reset the Display Start line.
N-line inversion (double byte instruction)	0 0	1 1	0 0	1 x	0 x	1 x	0 NL4	1 NL3	0 NL2	1 NL1	1 NL0	Set the Display Data RAM address that corresponds COM0 output for 1/81 duty (7bits).
N-line inversion reset	0	1	0	1	0	1	0	1	0	1	0	Reset the N-line inversion. (N-line inversion disable)
Set page address	0	1	0	1	0	1	1	P3	P2	P1	P0	Set the page address
Set column address MSB	0	1	0	0	0	0	1	A7	A6	A5	A4	Set the column address MSB
Set column address LSB	0	1	0	0	0	0	0	A3	A2	A1	A0	Set the column address LSB
Read status	0	0	1	BUSY		ONOFF		0	0	0	0	Read device internal status
					ADC		$\overline{RESET}$					
Write display data	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into display RAM
Read display data	1	0	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from display RAM
ADC set	0	1	0	1	0	1	0	0	0	0	ADC	Set SEG output direction ADC = 0 : SEG0→ SEG131 ADC = 1 : SEG131→ SEG0
Reverse display ON/OFF	0	1	0	1	0	1	0	0	1	1	REV	Set display mode REV = 0 : normal display REV = 1 : reverse display
All segments ON/OFF	0	1	0	1	0	1	0	0	1	0	AON	Set display mode AON = 0 : normal display AON = 1 : display all segments ON
LCD bias select	0	1	0	1	0	1	0	0	0	1	BIAS	Select LCD bias
Set read-modify-write (RMW) mode	0	1	0	1	1	1	0	0	0	0	0	Read-modify-write mode enable
Clear read-modify-write (RMW) mode	0	1	0	1	1	1	0	1	1	1	0	Read-modify-write mode disable
Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the device
Common output direction (COD) set	0	1	0	1	1	0	0	COD	x	x	x	Set COM output direction COD = 0 : COM0→ COM63 COD = 1 : COM63→ COM0
LCD power setup	0	1	0	0	0	1	0	1	BE	RE	FE	BE : voltage booster enable RE : voltage regulator enable FE : voltage follower enable

X:Don't care

Table 15. Instruction Table (continued)

Instruction	Instruction Code											Function
	RS	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
Voltage regulator resistor ratio set	0	1	0	0	0	1	0	0	R2	R1	R0	Select internal resistor ratio of the voltage regulator (Rb/Ra)
Reference voltage register set (double byte instruction)	0	1	0	1	0	0	0	0	0	0	1	Select reference voltage to control display contrast.
	0	1	0	x	x	VR5	VR4	VR3	VR2	VR1	VR0	
Static segment driver ON (double byte instruction)	0	1	0	1	0	1	0	1	1	0	1	The static segment driver (FR-FRS) is enabled and display mode is controlled by 2 nd byte.
	0	1	0	x	x	x	x	x	x	S1	S0	
Static segment driver OFF	0	1	0	1	0	1	0	1	1	0	0	The static segment driver is disabled
Power save control (compound instruction)												The device is entered power saving state when instructions set display off and all segments on.
NOP	0	1	0	1	1	1	0	0	0	0	1	*Non-Operation command*
TEST	0	1	0	1	1	1	1	X	X	X	X	*Don' t use this instruction*
TEST	0	1	0	1	0	0	1	X	X	X	X	*Don' t use this instruction*

X:Don' t care

Display ON/OFF

Turns the Display ON/OFF

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	1	1	DON

DON =1 : display ON

DON =0 : display OFF

Display Start Line Set

Sets the line address of display RAM to determine the Initial Display Line. The RAM display data is displayed at the top row (COM0 when SHL = L, COM63 when SHL = H) of LCD panel.

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

ST5	ST4	ST3	ST2	ST1	ST0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the Page Address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the page address doesn't effect to display status.

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	P3	P2	P1	P1

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10

Set Column Address

Sets the Column Address of display RAM from the microprocessor into Column Address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically increased.

Set Column Address MSB

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	A7	A6	A5	A4

Set Column Address LSB

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

Read Status

Read the internal status of the SL20T0081.

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	BUSY	ADC	ON/OFF	$\overline{\text{RESET}}$	0	0	0	0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy
ADC	Indicates the relationship between RAM column address and segment driver. 0: reverse direction (SEG131→SEGO), 1: normal direction (SEGO→ SEG131)
ON/OFF	Indicates display ON / OFF status. 0: display ON, 1: display OFF
$\overline{\text{RESET}}$	Indicates the initialization is progress by $\overline{\text{RESET}}$ signal. 0: chip is active, 1: chip is being reset

Write Display Data

8-bit data of display data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Write data							

Figure 12. Sequence for Writing Display Data

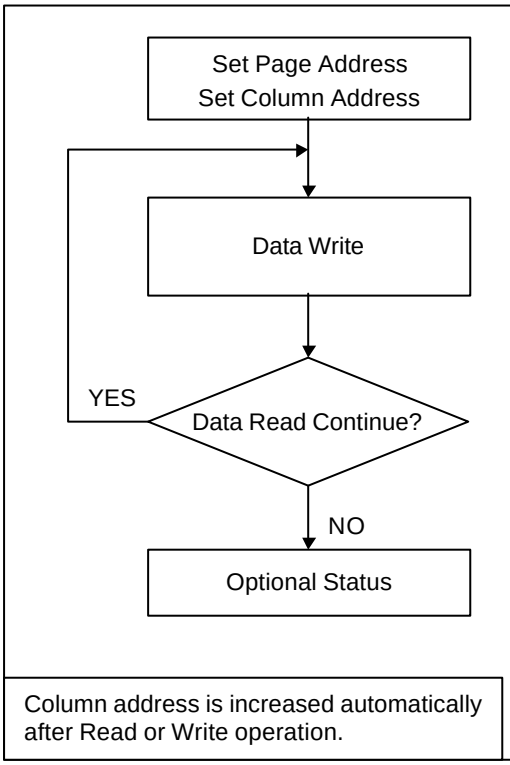
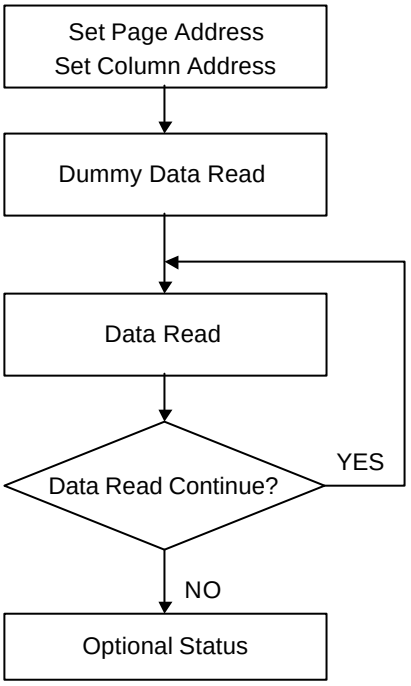


Figure 13. Sequence for Reading Display Data



Read Display Data

8-bit data from display data RAM specified by the column address and page address can be read by this Instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display data cannot be read through the serial interface.

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	1	Read data							

ADC Select (Segment Driver Direction Select)

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins can be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 ➔ SEG131)

ADC = 1: reverse direction (SEG131 ➔ SEG0)

Reverse Display ON / OFF

Reverses the display status in LCD panel without rewriting the contents of the display data RAM.

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	1	REV

REV	RAM bit data = "1"	RAM bit data = "0"
0 (normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (reverse)	LCD pixel is not illuminated	LCD pixel is illuminated

All segments ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM.At this time, the contents of the display data RAM are held. This instruction has priority over the Reverse Display ON / OFF instruction.

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	0	EON

EON = 0: normal display
EON = 1: entire display ON

Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	1	Bias

Duty ratio	DUTY2	DUTY1	DUTY0	LCD bias	
				Bias = 0	Bias = 1
1/33	0	0	0	1/6	1/5
1/49	0	0	1	1/8	1/6
1/55	0	1	0	1/8	1/6
1/65	0	1	1	1/9	1/7
1/81	1	0	0	1/10	1/8

Set Read-Modify-Write

This instruction stops the automatic increment of the column address by the read display data instruction,but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-read instruction.

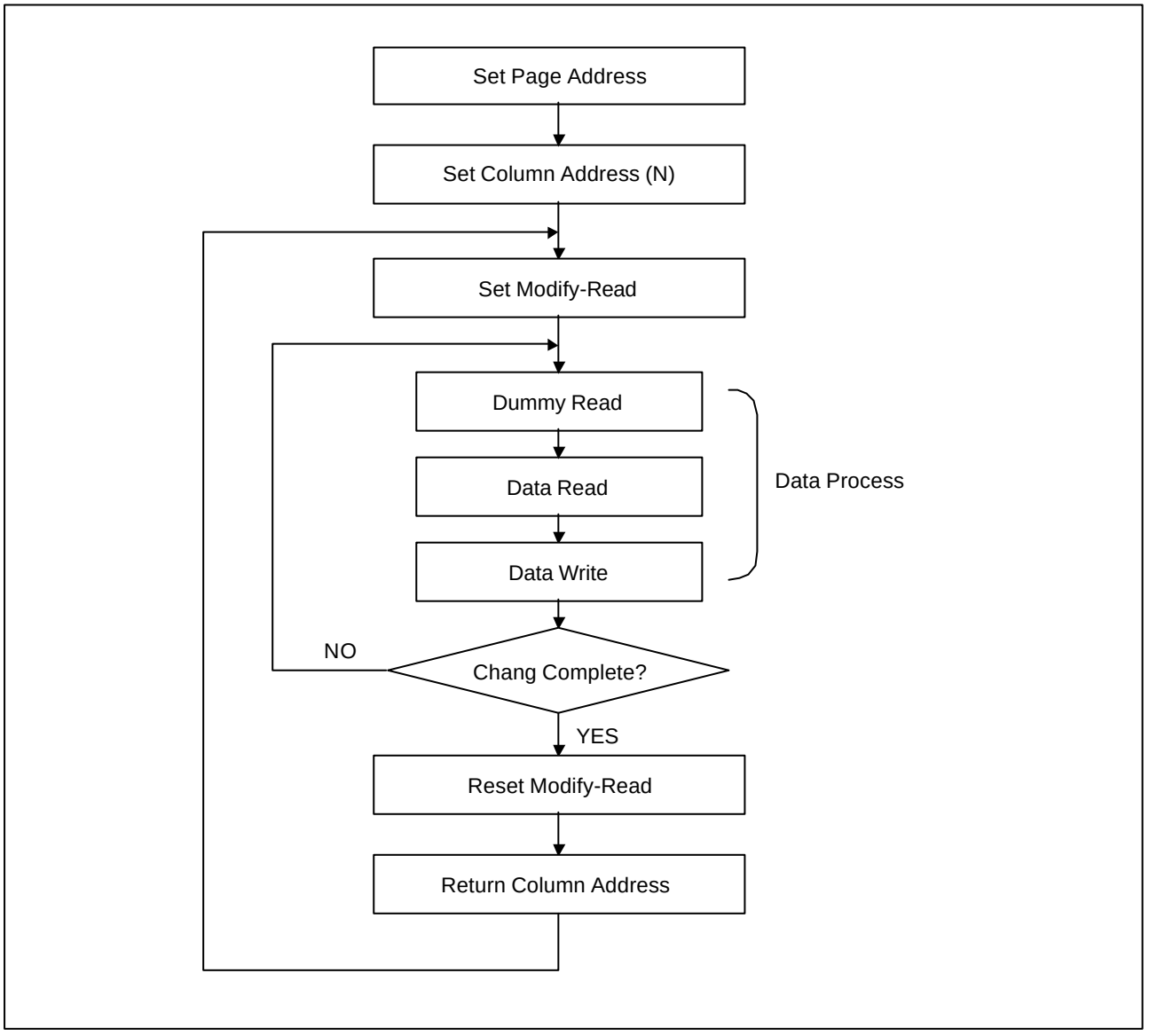
RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	0	0

Reset Read-Modify-Write

This instruction cancels the Read-Modify-Write mode, and makes the column address return to its initial value just before the set Read-Modify-Write instruction is started.

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	1	1	1	0

Figure 14. Sequence for Cursor Display



Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but does not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the $\overline{\text{RESET}}$ pin.

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	0

Common Output Direction (COD) set

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	SHL	x	x	x

COD = 0: normal direction (COM0→COM79) X: Don' t care

COD = 1: reverse direction (COM79→COM0)

Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0 1			Internal voltage converter circuit is OFF Internal voltage converter circuit is ON
	0 1		Internal voltage converter circuit is OFF Internal voltage converter circuit is ON
		0 1	Internal voltage converter circuit is OFF Internal voltage converter circuit is ON

Regulator Resistor Select

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the table 15.

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	(1+ Rb / Ra) ratio
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0 (default)
1	0	1	5.5
1	1	0	6.0
1	1	1	6.4

Reference Voltage Select

Consists of 2- byte instruction. The 1st instruction set reference voltage mode, the 2nd one updates the contents of reference voltage register. After second instruction, reference voltage mode is released.

The 1st Instruction : Set Reference Voltage Select Mode

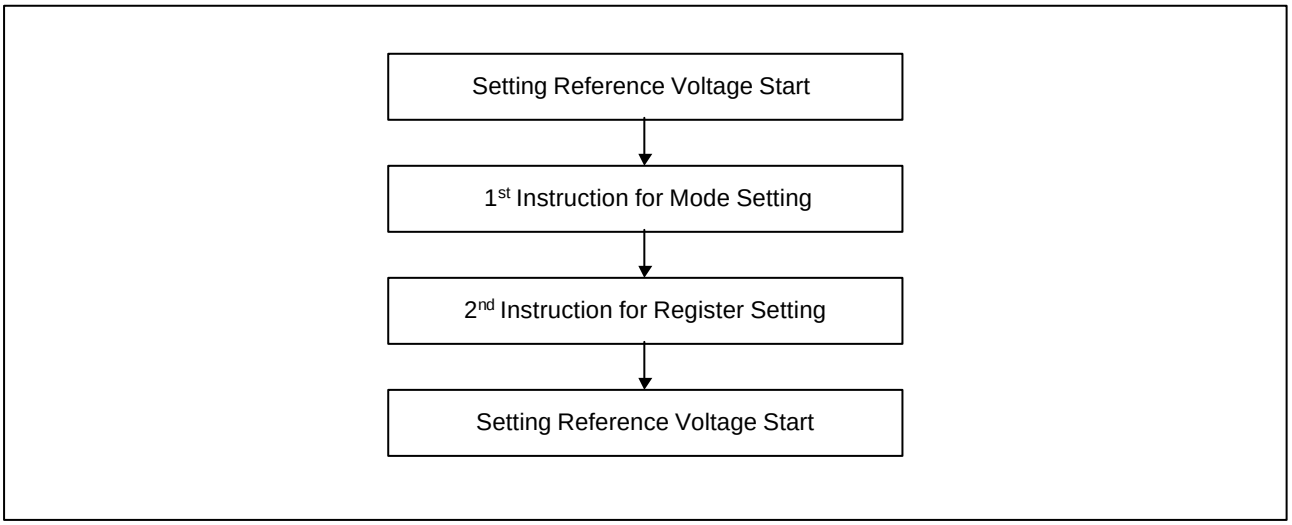
RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction : Set Reference Voltage Register

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	x	x	VR5	VR4	VR3	VR2	VR1	VR0

VR5	VR4	VR3	VR2	VR1	VR0	Reference voltage parameter(a)	V0	Contrast
0	0	0	0	0	0	0	Minimum	Low
0	0	0	0	0	1	1		
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	32 (default)		
:	:	:	:	:	:	:	:	:
1	1	1	1	1	0	62	Maximum	High
1	1	1	1	1	1	63		

Figure 15. Sequence for Setting the Reference Voltage



Set Static Indicator State

Consists of two bytes instruction. The first byte instruction (set Static Indicator Mode) enables the second byte instruction (set Static Indicator Register) to be valid. The first byte sets the static indicator ON /OFF. When it is on, the second byte updates the contents of static indicator register without issuing any other instruction and this Static Indicator state is released after setting the data of indicator register.

The 1st Instruction : Set Static Indicator Mode (ON/OFF)

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	1	0	SM

SM = 0: static instruction OFF
SM = 1: static instruction ON

The 2nd Instruction : Set Static Indicator Register

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	x	x	x	x	x	x	S1	S0

S1	S0	Status of static indicator output
0	0	OFF
0	1	ON (about 1 second blinking)
1	0	ON (about 0.5 second blinking)
1	1	ON (always ON)

NOP

Non Operation Instruction

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	1

Test Instruction (Test Instruction_1 &Test Instruction_2)

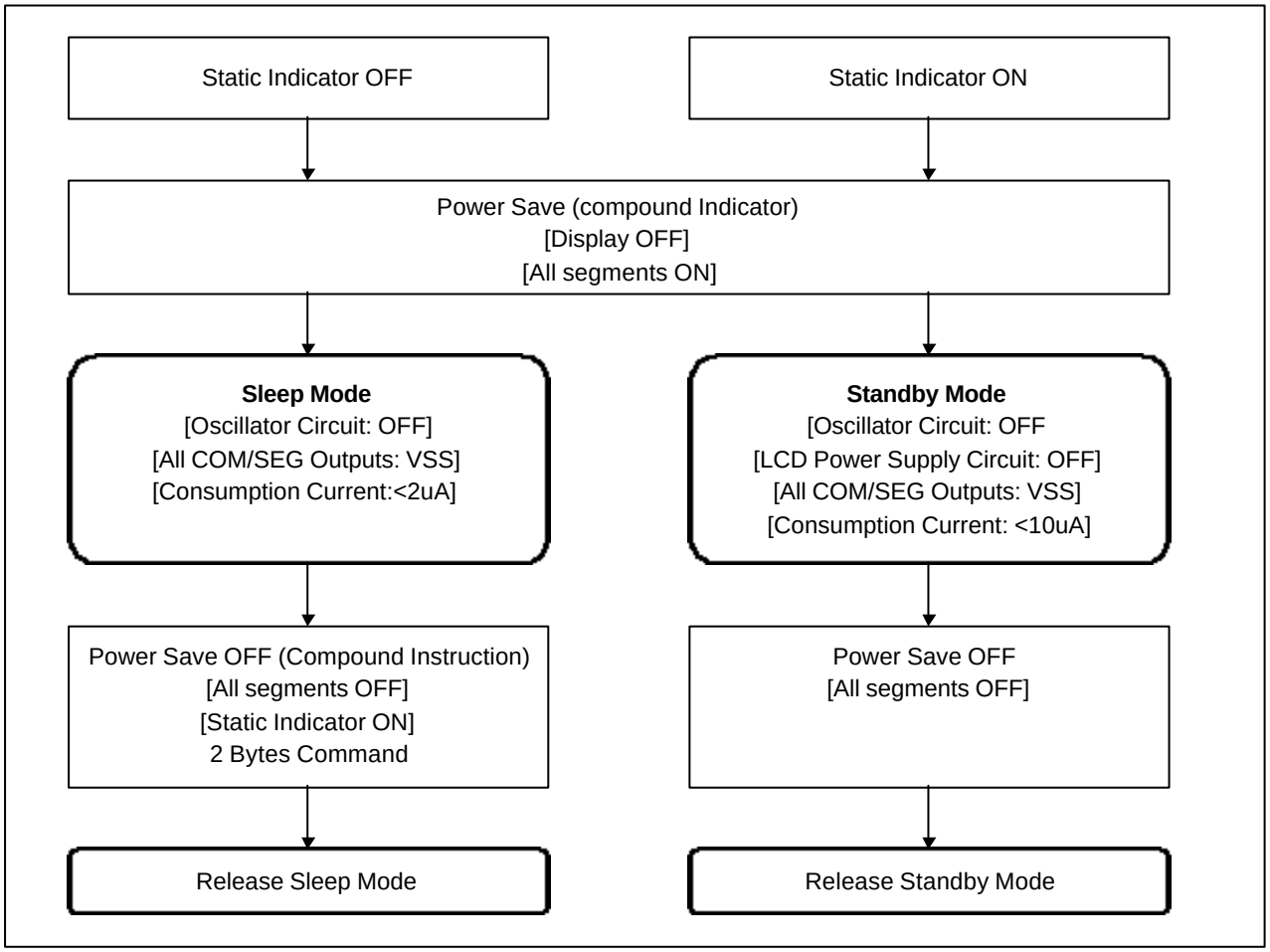
Thee are the instruction for IC chip testing. Please do not use it. If the test instruction is used by accident,it can be cleared by applying "0" signal to the $\overline{\text{RESET}}$ input pin or the reset instruction.

RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	x	x	x	x
0	0	1	0	0	1	x	x	x	x

Power Save (Compound Instruction)

If the entire display ON/OFF instruction is issued during the display OFF state, SL20T0081 enters the Power Save status to reduce the power consumption to the static power consumption value. According to the status of static indicator mode, power save is entered to one mode of sleep and standby mode. When Static Indicator mode is ON, standby mode is issued. When OFF, sleep mode is issued. Power save mode is released by the entire display OFF instruction.

Figure 16. Power Save (Compound Instruction)



- Sleep Mode

  This stops all operations in the LCD display system, and as long as there are no access from the MPU, the consumption current is reduced to a value near the static current. The internal modes are as follows :

a. The oscillator circuit and LCD power supply circuit are halted.
b. All liquid crystal drive circuit are halted, and the segment in common drive outputs a VSS level.

- Standby Mode

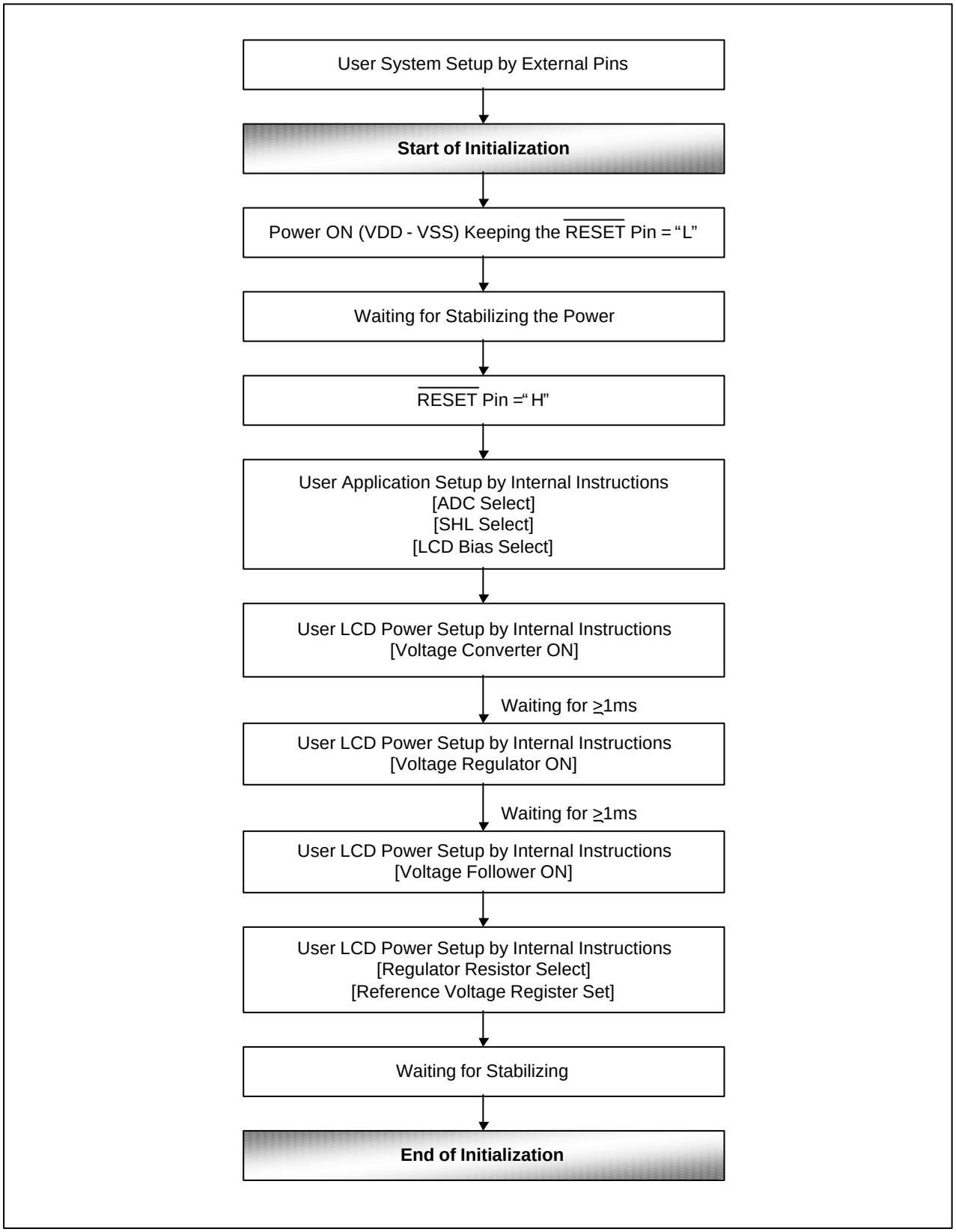
  The duty LCD display system operation are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive.

a. The LCD power supply circuits are halted. The oscillator circuit continues to operate.
b. The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs a VSS level.

The static drive system does not operate. When a reset command is performed while in standby mode, the system enter sleep mode.

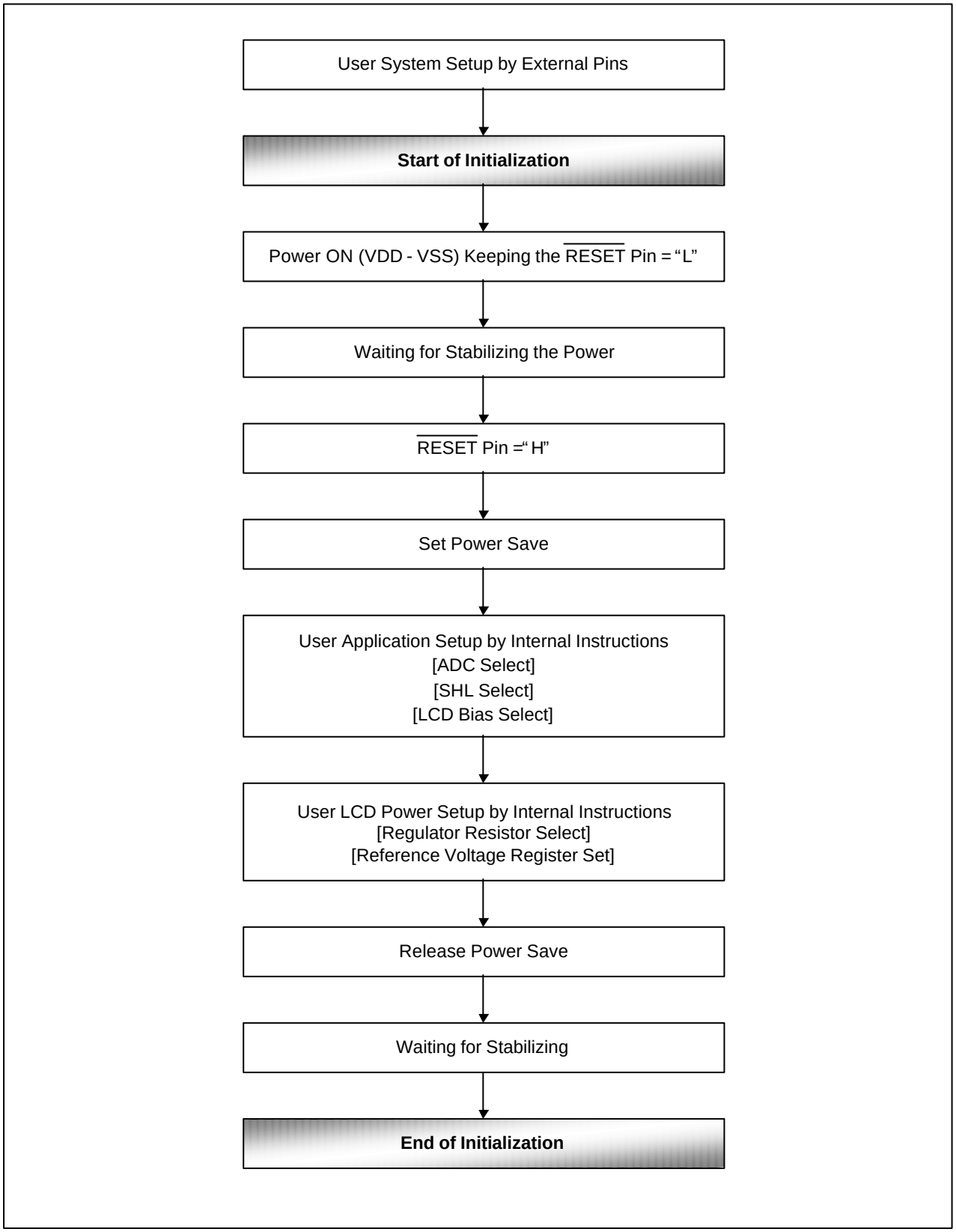
Referential Instruction Setup Flow (1)

Figure 17. Initializing with the Built-in Power Supply Circuits



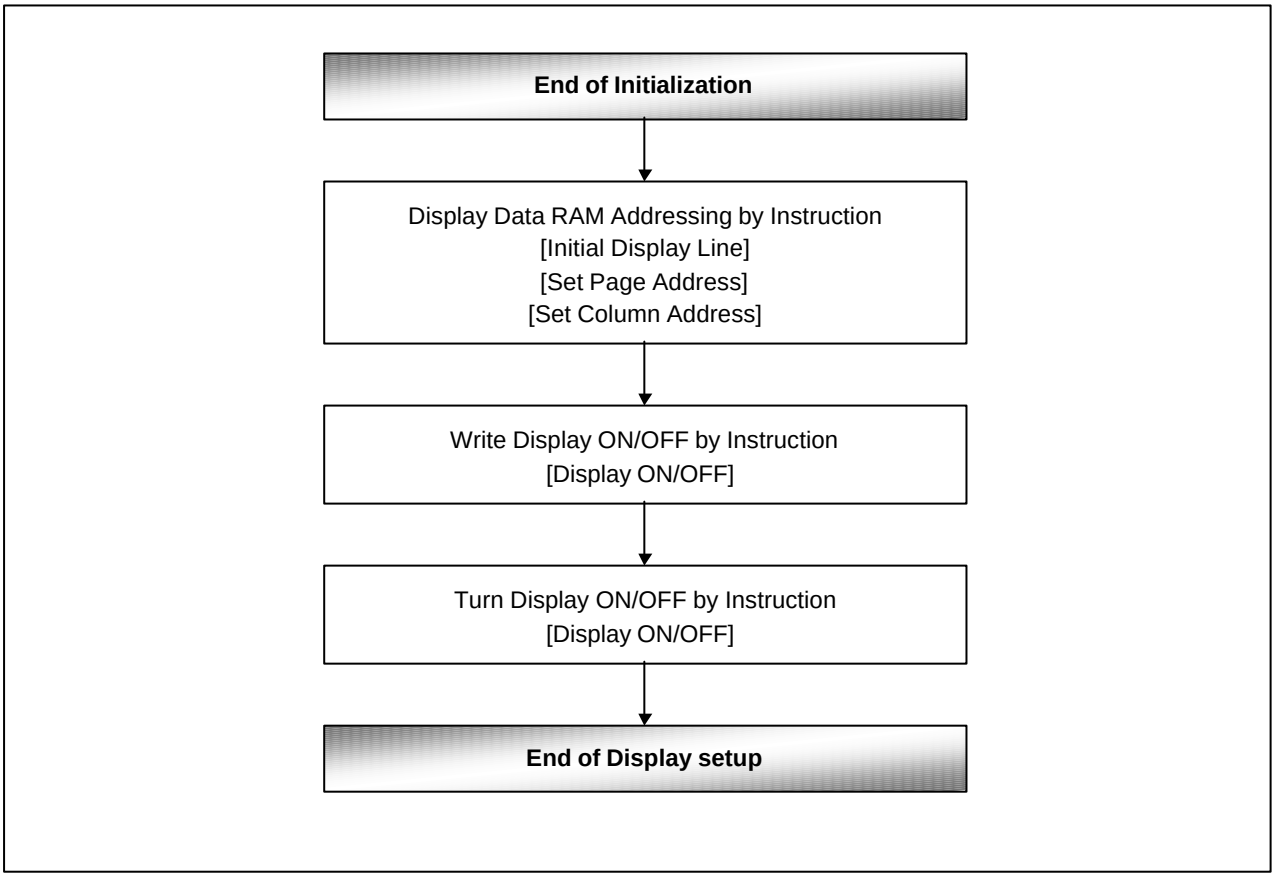
Referential Instruction Setup Flow (2)

Figure 18. Initializing without the Built-in Power Supply Circuits



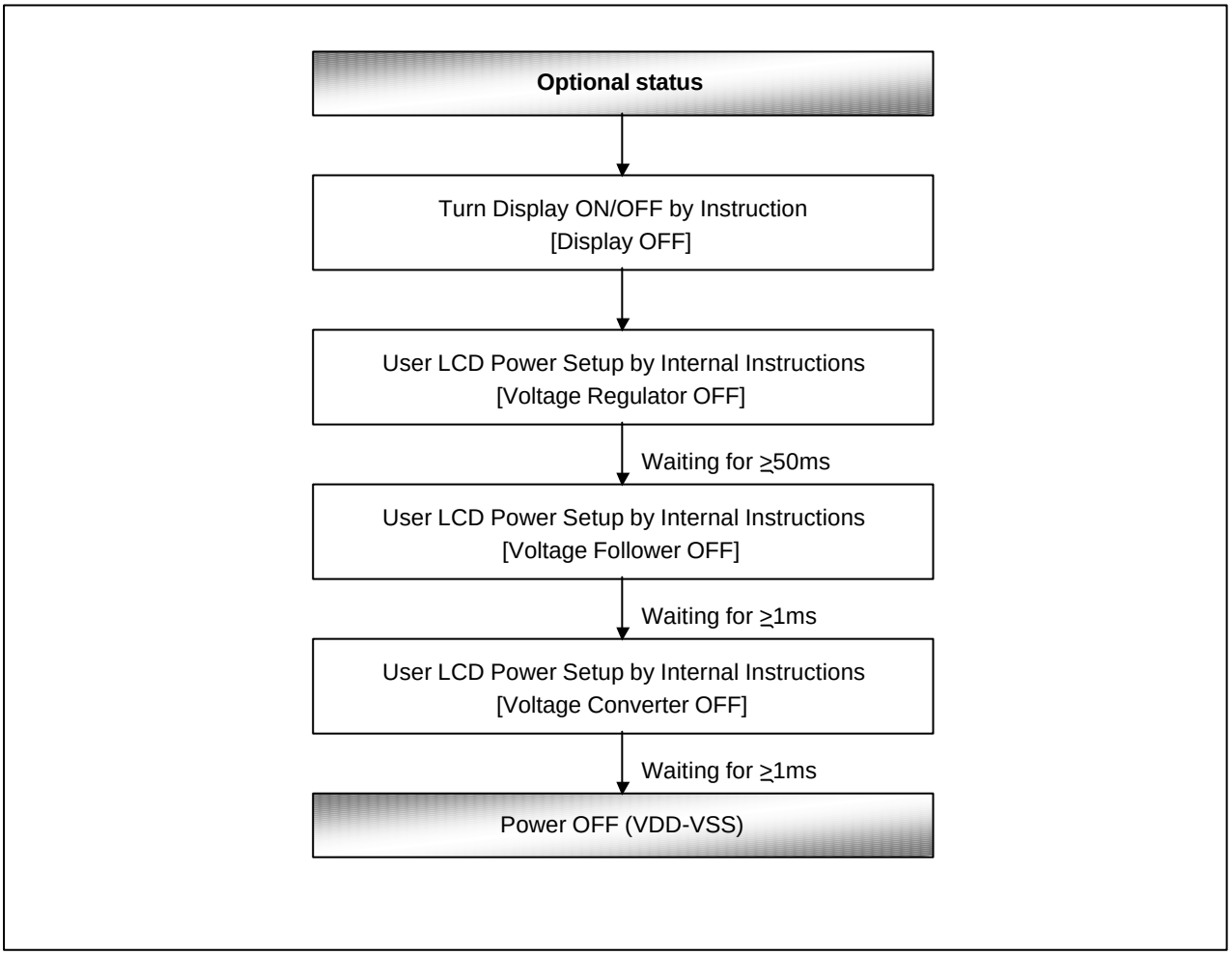
Referential Instruction Setup Flow (3)

Figure 19. Data Display setup



Referential Instruction Setup Flow (4)

Figure 20. Power OFF



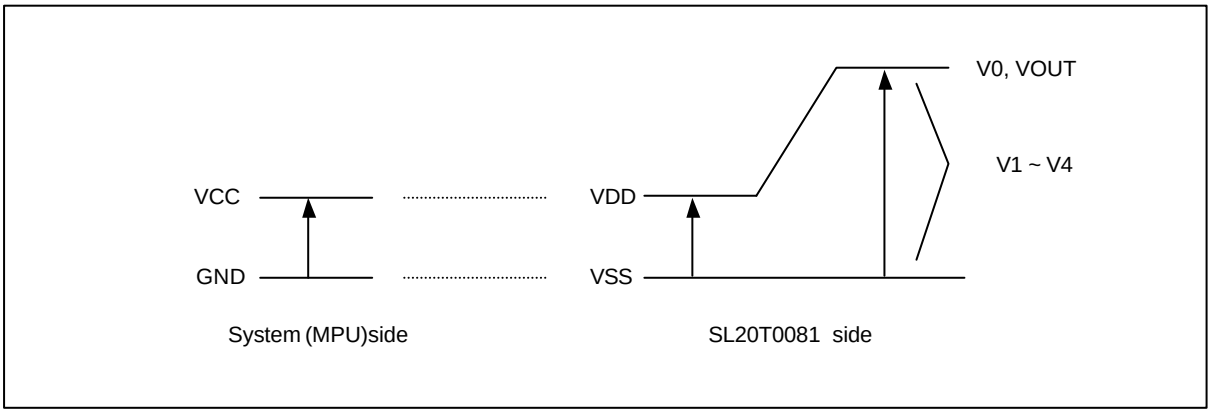
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 16. Absolute Maximum Ratings Unless otherwise noted, VSS = 0V

Parameter		Symbol	Conditions	Unit
Power supply voltage		VDD	-0.3 ~ +7.0	V
Power supply voltage	With Triple step-up With Quad step-up		-0.3 ~ +7.0 -0.3 ~ +6.0 -0.3 ~ +4.5	V
Power supply voltage(3)		V0, VOUT	-0.3 ~ +18.0	V
Power supply voltage(4)		V1, V2, V3, V4	-0.3 ~ V0	V
Input voltage		VIN	-0.3 ~ VDD + 0.3	V
Output voltage		VO	-0.3 ~ VDD + 0.3	V
Operating temperature		TOP	-40 ~ + 85	°C
Storage temperature	TCP Bare chip	TST	-55 ~ + 100 -55 ~ + 125	°C

Figure 21. Relations between powers and V voltages



NOTES :

1. VDD and VLCD are based on VSS = 0V.
2. Voltages V0 ≥ V1≥ V2 ≥ V3 ≥ V4 ≥ VSS must always be satisfied. (VLCD = V0 - VSS)
3. If supply voltage exceeds its absolute maximum range,this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 17. DC Characteristics Unless otherwise specified, VSS = 0V, VDD = 3.0 V± 10%, Ta = -40 to 85ºC

Item		Symbol	Condition	Condition			Units	Pin
				Min.	Typ.	Max.		
Operating Voltage		VDD		2.4	-	5.5	V	VDD
Operating Voltage(2)		V0		4.5	-	15.0	V	V0
High-level Input Voltage		VIH		0.8 × VDD	-	VDD	V	
Low-level Input Voltage		VIL		0	-	0.2 x VDD	V	
High-level Output Voltage		VOH	IOH = - 0.5mA	0.8 × VDD	-	VDD	V	
Low-level Output Voltage		VOL	IOL = 0.5mA	0	-	0.2 x VDD	V	
Input leakage current		IIL	VIN = VDD or VSS	-1.0	-	1.0	uA	
Output leakage current		IOL		-3.0	-	3.0	uA	
LCD driver output ON Resistance		RON	Ta = 25 ºC V0 = 8V	-	2.0	3.0	KΩ	LCD drive pins
Oscillator Frequency	Internal Oscillator	fOSC	1/81 Duty, Ta = 25 ºC	6.3	12.6	18.9	kHz	
	External Input	fCL		-	12.6	-	kHz	CL
	Internal Oscillator	fOSC	1/65 Duty, Ta = 25 ºC	5.5	10.9	16.4	kHz	
	External Input	fCL		-	10.9	-	kHz	CL
	Internal Oscillator	fOSC	1/55 Duty, Ta = 25 ºC	5	10.0	15.0	kHz	
	External Input	fCL		-	10.0	-	kHz	CL
	Internal Oscillator	fOSC	1/49 Duty, Ta = 25 ºC	4.3	8.7	13.0	kHz	
	External Input	fCL		-	8.7	-	kHz	CL
	Internal Oscillator	fOSC	1/33 Duty, Ta = 25 ºC	2.9	5.8	8.7	kHz	
	External Input	fCL		-	5.8	-	kHz	CL

Table 18. DC Characteristics (continued) (VSS = 0V, VDD =2.4 to 3.6V, Ta =-40 to 85°C)

Item	Symbol	Condition	Condition			Units	Pin
			Min.	Typ.	Max.		
Voltage converter input voltage	V	x2	2.4	-	3.6	V	V
		x3	2.4	-	3.6		
		x4	2.4	-	3.6		
		x5	2.4	-	3.2		
Voltage converter output voltage	VOUT	X2 /x3 /x4 /x5 voltage conversion (no-load)	95	99	-	%	VOUT
Voltage regulator operating voltage	VOUT		6.0	-	16.0	V	VOUT
Voltage regulator operating voltage	V0		4.5	-	15.0	V	V0 *9
Reference voltage	VREF	Ta=25°C (-0.05%/°C)	2.04	2.1	2.16	V	

Table 19. Dynamic Current Consumption (1) when the Built - in Power Circuit is OFF (At Operate Mode) (Ta =25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption(1)	I_{DD1}	VDD =3.0V V0-VSS =11.0V 1/65 duty ratio Display pattern OFF	-	15	23	µA	*11

Table 20. Dynamic Current Consumption (2) when the Built - in Power Circuit is ON (At Operate Mode) (Ta =25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption(2)	I_{DD2}	V_{DD} =3.0V (V =V_{DD},4 time boosting) V0-V_{SS} =11.0V, 1/65 duty ratio, Display pattern OFF, Normal power mode	-	40	60	µA	*12
		V_{DD} =3.0V (V =V_{DD},4 time boosting) V0-V_{SS} =11.0V, 1/65 duty ratio, Display pattern checker, Normal power mode	-	150	200	µA	*12

Table 21. Current Consumption during Power Save Mode (Ta =25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Sleep mode current	I_{DD1}	During sleep	-	-	2.0	µA	
Standby mode current	I_{DD2}	During standby	-	-	10.0	µA	

Table 22. The Relationship between Oscillation Frequency and Frame Frequency

Duty ratio	Item	f_{CL}	f_{FR}
1/81	On-chip oscillator circuit is used	f_{OSC} = 12.57 kHz	$\frac{f_{OSC}}{2 \times 2 \times 81}$
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{2 \times 2 \times 81}$
1/65	On-chip oscillator circuit is used	f_{OSC} = 10.90 kHz	$\frac{f_{OSC}}{2 \times 2 \times 65}$
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{2 \times 2 \times 65}$
1/55	On-chip oscillator circuit is used	f_{OSC} = 9.96 kHz	$\frac{f_{OSC}}{2 \times 2 \times 55}$
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{2 \times 2 \times 55}$
1/49	On-chip oscillator circuit is used	f_{OSC} = 8.72 kHz	$\frac{f_{OSC}}{2 \times 2 \times 49}$
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{2 \times 2 \times 49}$
1/33	On-chip oscillator circuit is used	f_{OSC} = 5.82 kHz	$\frac{f_{OSC}}{2 \times 2 \times 33}$
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{2 \times 2 \times 33}$

(fosc:oscillation frequency, f_{CL}: display clock frequency, f_{FR} : LCD AC signal frequency)

[*Remark Solves]

*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.

*2. In case of external power supply is applied.

*3. CE1, CE2, RS, D7, to D0, RD(E), WR(R/W), RESET, MS, P68/80, PS, INTRS, HPMB, CLS, CL, SYNC, FR, DISP pins.

*4. D0 to D7, SYNC, FR, DISP, CL pins.

*5. CE1, CE2, RS, D7 to D0, RD(E), WR(R/W), RESET, MS, P68/80, PS, INTRS, HPMB,CLS, CL, SYNC, FR, DISP pins.

*6. Applies when the DB[7:0], SYNC, FR, DISP, and CL pins are in high impedance.

*7. Resistance value when ≒0.1[mA] is applied during the ON status of the output pin SEGn or COMn. RON = △V / 0.1 [kΩ] (△V : voltage change when ≒0.1[mA] is applied in the IN status.)

*8. See table 22 for the relationship between oscillation frequency and frame frame frequency.

*9. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range

*10. On-chip reference voltage source of the voltage regulator circuit to adjust V0.

*11,*12. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU. The current consumption, when the built-in power supply circuit is ON or OFF. The current flowing through voltage regulation resistors (Ra and Rb) is not included. It does not include the current of the LCD panel capacity, wiring capacity, etc.

AC CHARACTERISTICS

Figure 22. Read/Write Characteristics (8080-series Microprocessor)

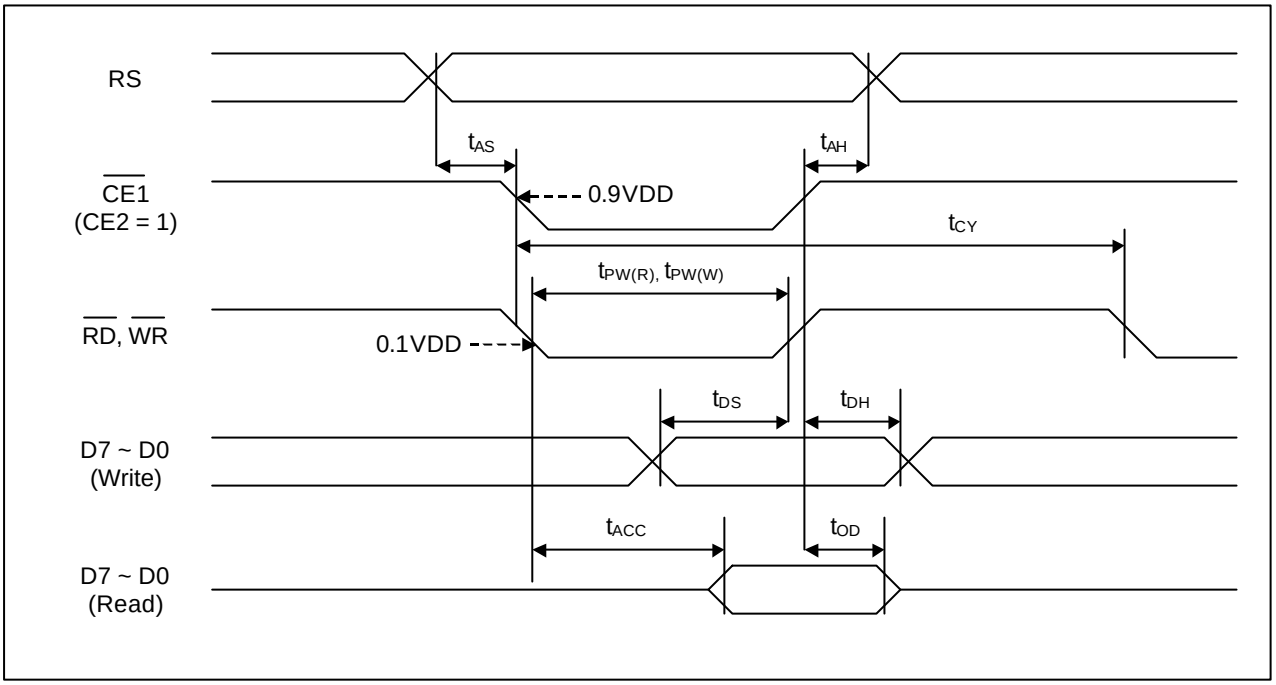


Table 23. Read/Write Characteristics (8080-series Microprocessor) (VDD = 2.4 to 3.6V, ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS} t_{AH}	0 0	-	-	ns	
System cycle time	RS	t_{CY}	300	-	-	ns	
Pulse width (R)	E(RDB)	t_{RD}	60	-	-	ns	
Pulse width (W)	E(RDB)	t_{WR}	60	-	-	ns	
Data setup time Data hold time	D7 to D0	t_{DS} t_{DH}	40 15	-	-	ns	
Read access time Output disable time		t_{ACC} t_{OD}	- 10	-	140 100	ns	CL = 100pF

Figure 23. Read/Write Characteristics (6800-series Microprocessor)

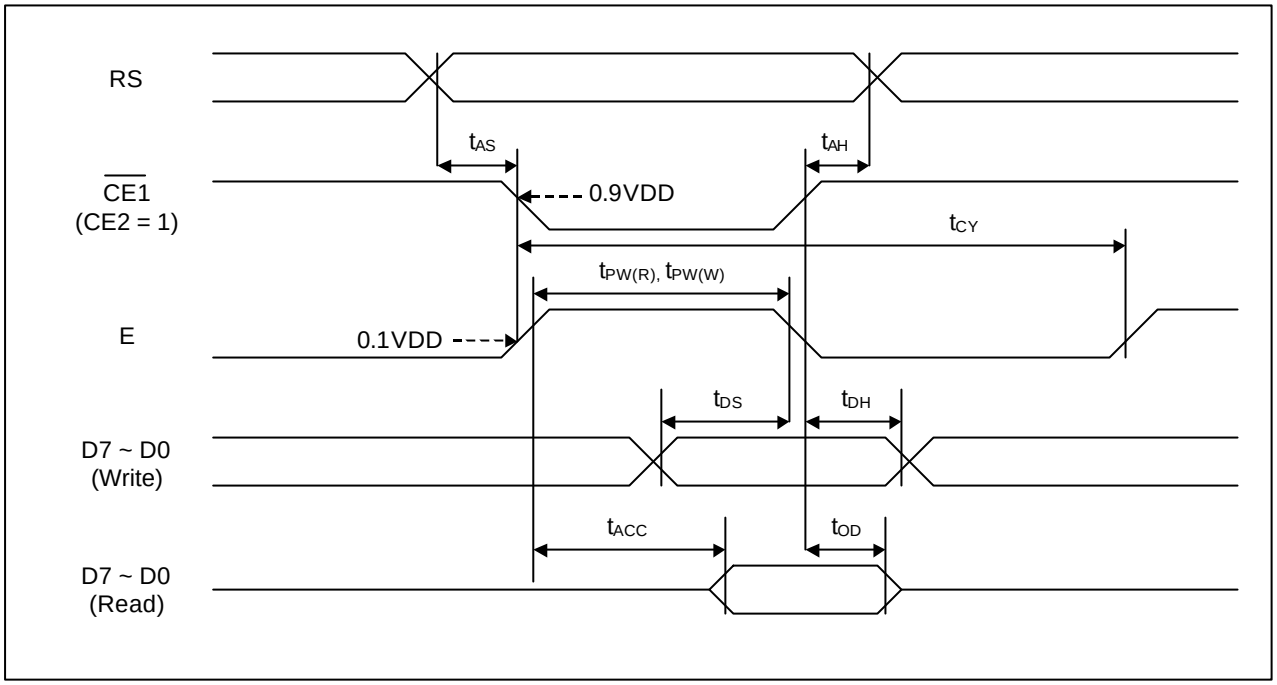


Table 24. Read/Write Characteristics (6800-series Microprocessor) (VDD = 2.4 to 3.6V, ta =-40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS} t_{AH}	0 0	-	-	ns	
System cycle time	RS	t_{CY}	300	-	-	ns	
Pulse width (R)	E(RDB)	t_{RD}	120	-	-	ns	
Pulse width (W)	E(RDB)	t_{WR}	60	-	-	ns	
Data setup time Data hold time	D7 to D0	t_{DS} t_{DH}	40 15	-	-	ns	
Read access time Output disable time		t_{ACC} t_{OD}	- 10	-	140 100	ns	CL = 100pF

Figure 24. Serial Interface Characteristics

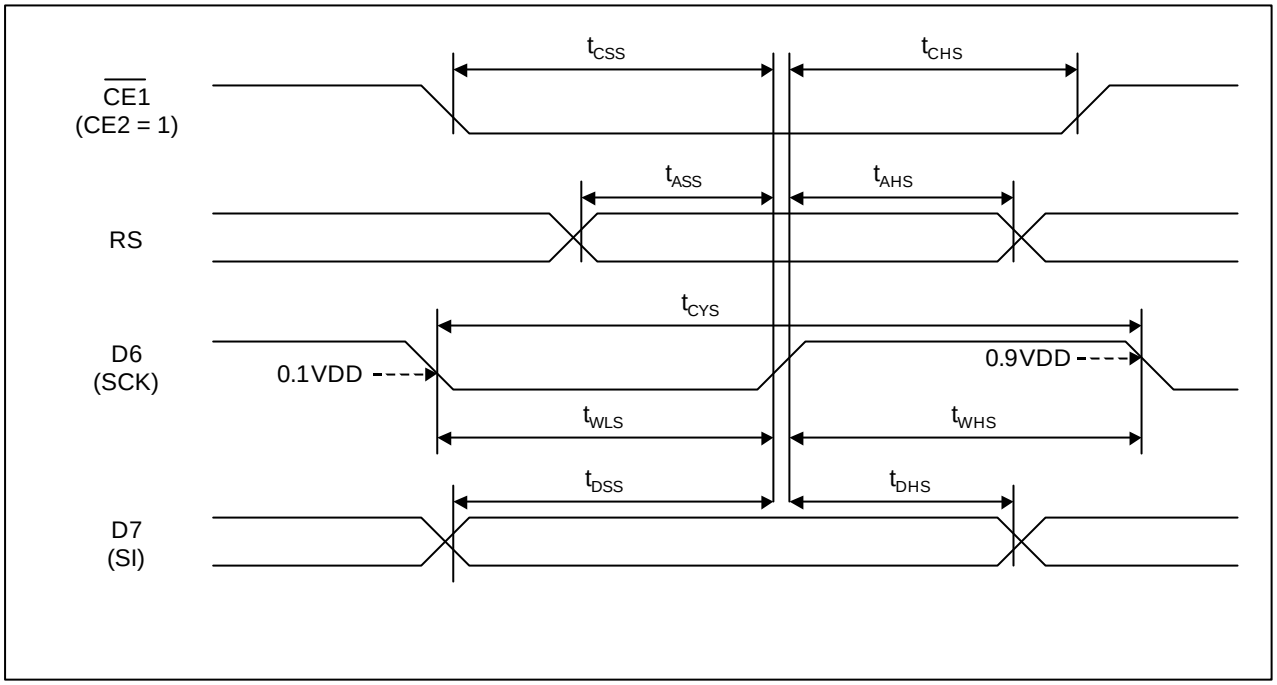


Table 25. Serial Interface Characteristics (VDD = 2.4 to 3.6V, ta =-40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCLK high pulse width SCLK low pulse width	D6 (SCLK)	t_{CYS} t_{WHS} tWLS	250 100 100	- - -		ns	
Address setup time Address hold time	RS	t_{ASS} t_{AHS}	150 150	- -		ns	
Data setup time Data hold time	D7 (SID)	t_{DSS} t_{DHS}	100 100	- -		ns	
$\overline{CE1}$ setup time $\overline{CE1}$ hold time	$\overline{CE1}$	t_{CSS} t_{CHS}	150 150	- -		ns	

Figure 25. Reset Input Timing

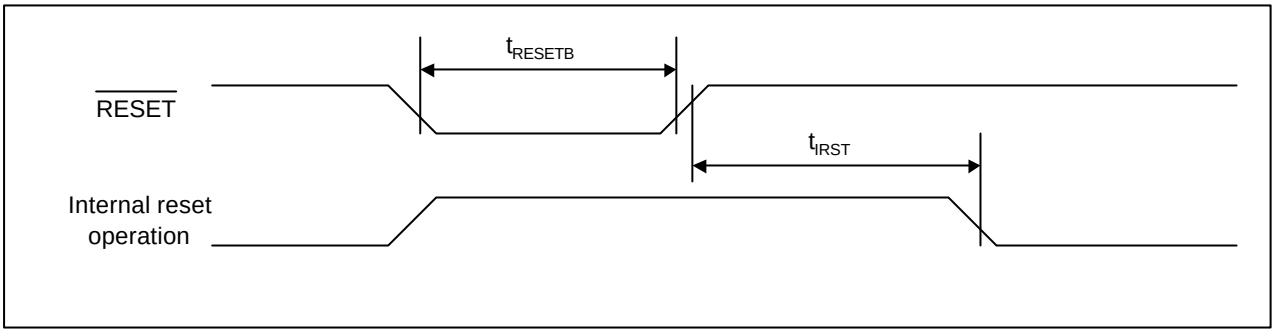


Table 26. Reset Input Timing (VDD = 2.4 to 3.6V, ta =-40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
$\overline{\text{RESET}}$ low pulse width	$\overline{\text{RESET}}$	t_{RESETB}	30.0	-	-	ns	
Reset time	-	t_{IRST}	-	-	60.0	ns	

Figure 26. Display Control Output Timing

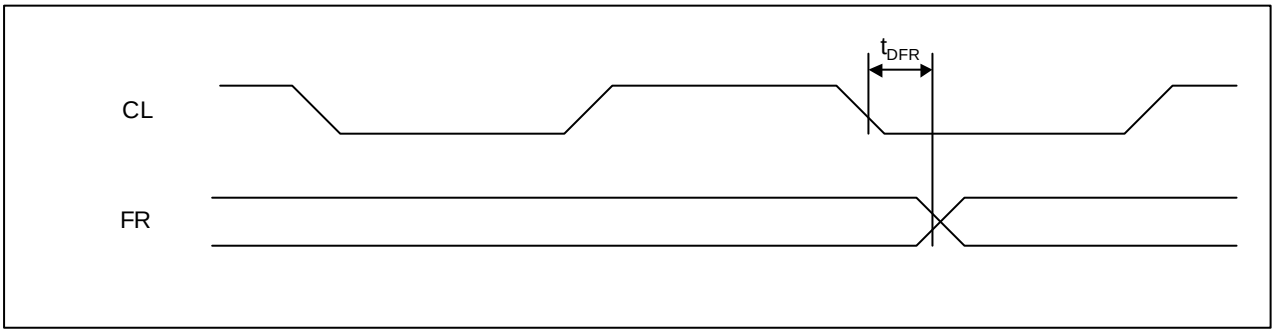


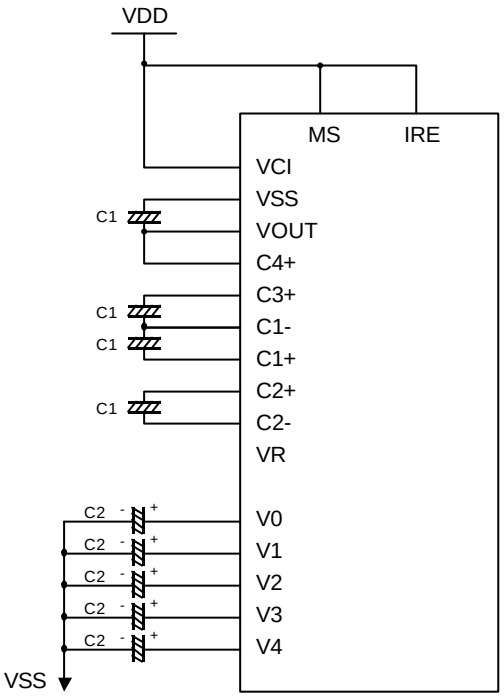
Table 27. Display Control Output Timing (VDD = 2.4 to 3.6V, ta =-40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
FR delay time	FR	t_{DFR}	-	20	80	ns	CL=50pF

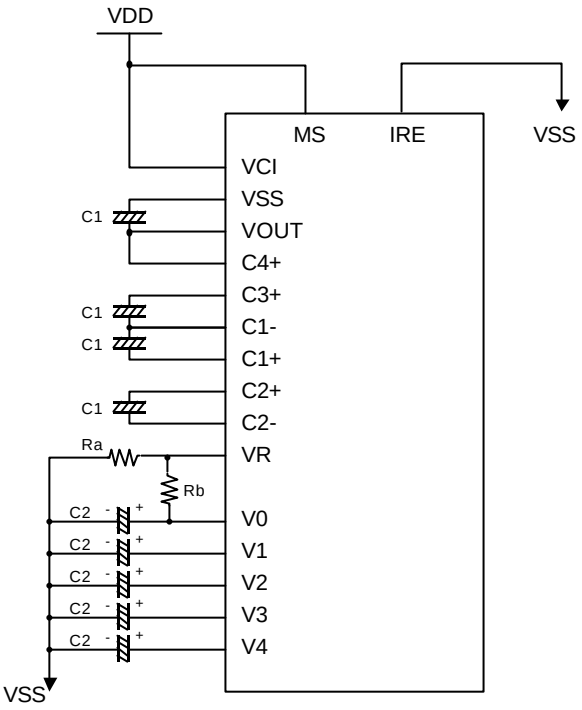
REFERENCE APPLICATIONS

LCD power supply configuration

Example 1 : When using internal LCD power circuit (4-time voltage boost / VCI = VDD)

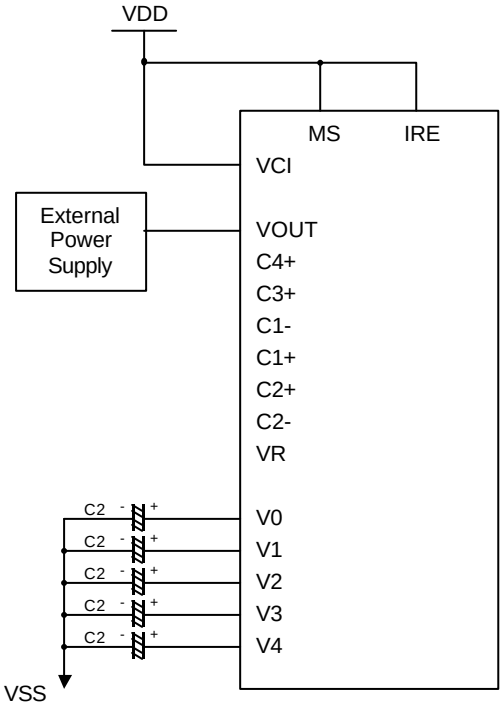


(a) Using internal voltage regulator resistors (IRE=1)

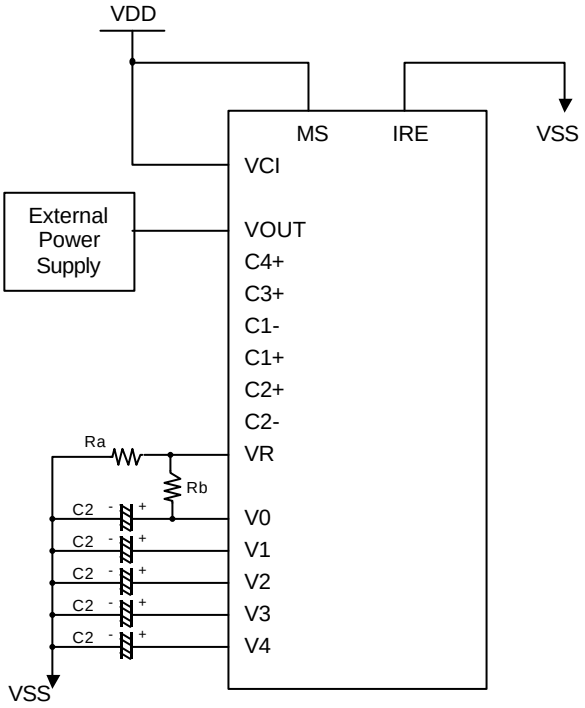


(b) Using external voltage regulator resistors (IRE=0)

Example 2 : Using Internal LCD power circuit (not using voltage booster circuit)

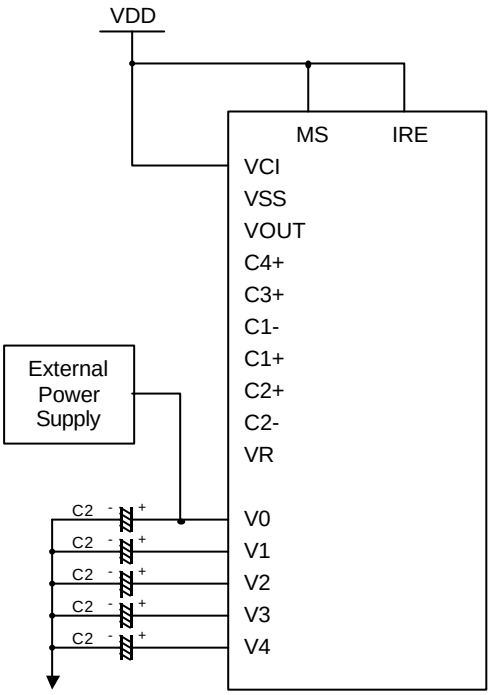


(c) Using internal voltage regulator resistors (IRE=1)

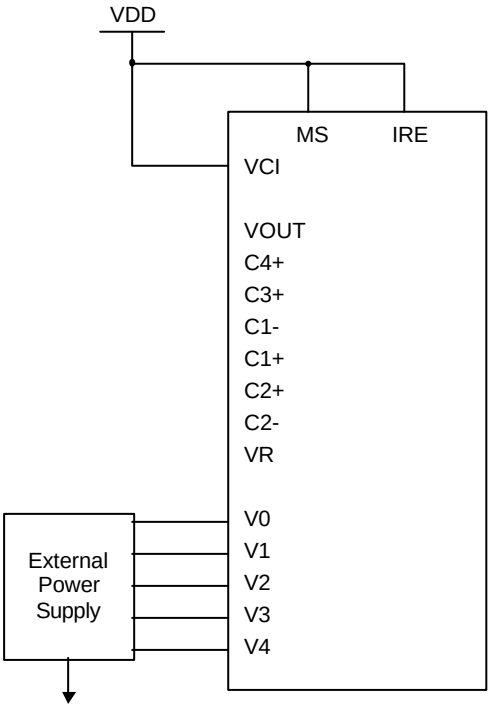


(d) Using external voltage regulator resistors (IRE=0)

Example 3 : Using Internal LCD power circuit (Only use voltage follower circuit)

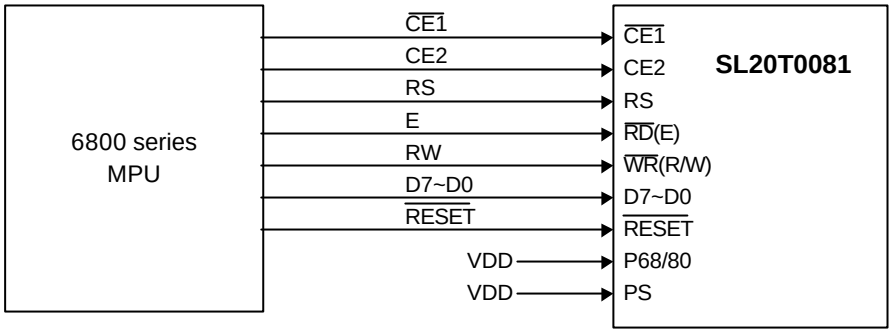


Example 4 : Using External LCD power supply

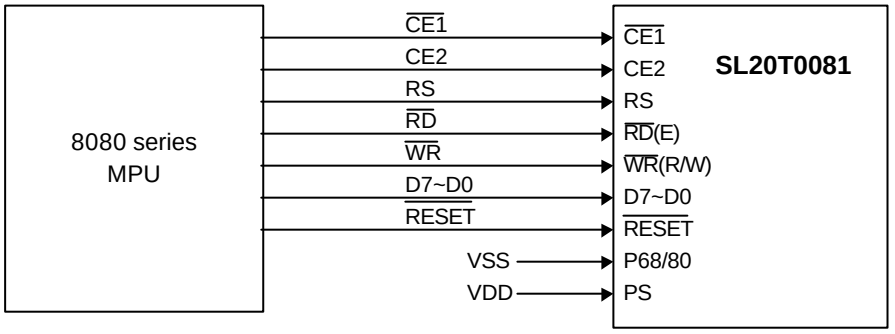


Data transfer interface

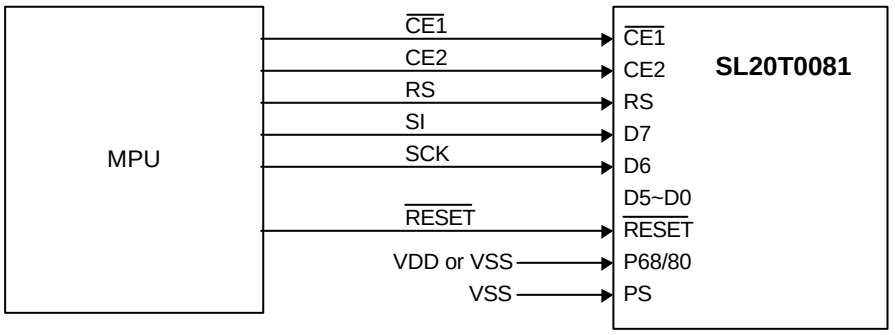
Figure 27. Data transfer interface



(a) 6800 Bus type interface



(b) 8080 Bus type interface



(c) Serial interface