MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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4M x 9

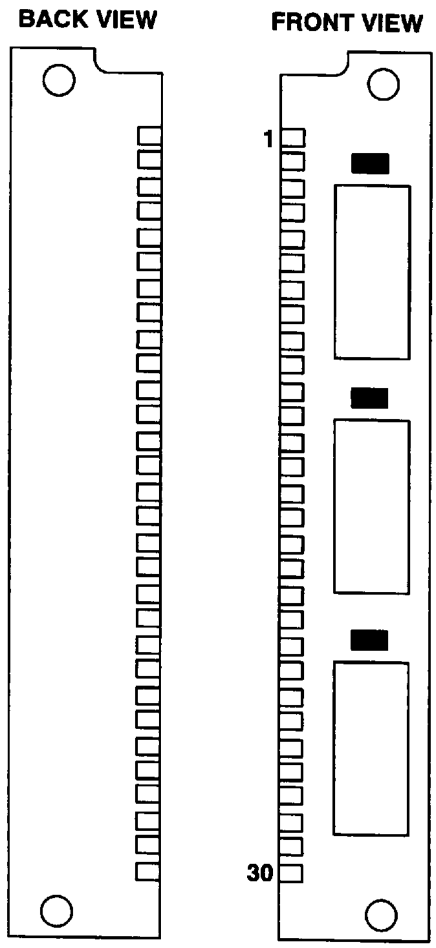
5 V, FPM, Unbuffered

DRAM Single-In-Line Memory Module (SIMM)

4 Megabyte

- JEDEC–Standard 30–Lead Single–In–Line Memory Module (SIMM)
- Single 5 V Power Supply, TTL–Compatible Inputs and Outputs
- Fast Page Mode (FPM)
- $\overline{RAS}$–Only Refresh, $\overline{CAS}$ Before $\overline{RAS}$ Refresh, Hidden Refresh
- 4MB: 2048 Cycle Refresh: 32 ms (Max)

4M x 9 (4MB)
30–LEAD SIMM
CASE 839A–01



PART NUMBERS (See Last Page for Definitions)

Organization	60	70
4MB	MCM94C430S60 MCM94CT430S60	MCM94C430S70 MCM94CT430S70

KEY TIMING PARAMETERS

Speed	t_{RC} (ns)	t_{RAC} (ns)	t_{CAC} (ns)	t_{AA} (ns)	t_{PC} (ns)
60	110	60	15	30	40
70	130	70	20	35	45

ADDITIONAL PARAMETERS

Configuration	Speed	Active Power Dissipation (mW) (Max)	Standby Power Dissipation (mW) (Max)	
			TTL	CMOS
4MB	60	1623	33	17
	70	1403		

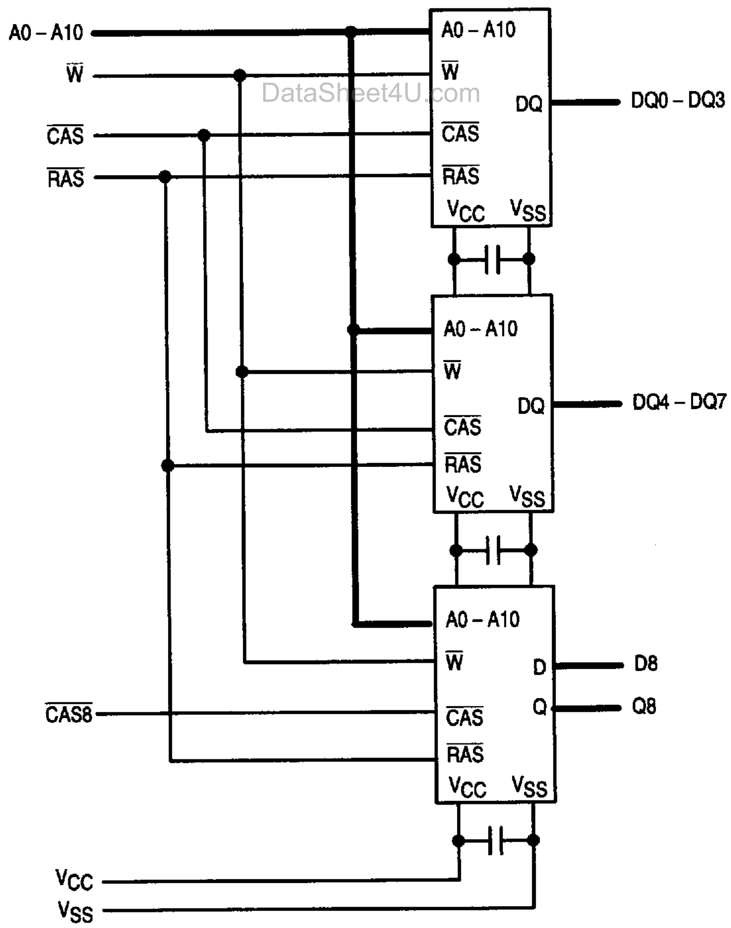
12/19/96

PIN ASSIGNMENTS

Pin	Name	Pin	Name
1	V_{CC}	16	DQ4
2	$\overline{CAS}$	17	A8
3	DQ0	18	A9
4	A0	19	A10
5	A1	20	DQ5
6	DQ1	21	$\overline{W}$
7	A2	22	V_{SS}
8	A3	23	DQ6
9	V_{SS}	24	NC
10	DQ2	25	DQ7
11	A4	26	Q8
12	A5	27	$\overline{RAS}$
13	DQ3	28	$\overline{CAS8}$
14	A6	29	D8
15	A7	30	V_{CC}

PIN NAMES	
A0 – A10	Address Inputs
DQ0 – DQ7	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 0.5 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	2.4	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ± 10% V, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All Voltages Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	V_{CC} + 0.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 0.5*	—	0.8	V
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	– 25	—	25	µA
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{lkg(O)}$	– 10	—	10	µA
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	—	0.4	V

* – 2.0 V at pulse widths ≤ 20 ns.

DC CHARACTERISTICS AND SUPPLY CURRENTS (All Voltages Referenced to V_{SS})

Characteristic		Symbol	4MB Min	4MB Max	Unit	Notes
V_{CC} Power Supply Current (t_{RC} = t_{RC} Min)	60 70	I_{CC1}	— —	295 255	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	6	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles (t_{RC} = t_{RC} Min)	60 70	I_{CC3}	— —	295 255	mA	1, 2
V_{CC} Power Supply Current During FPM Cycle (t_{PC} = t_{PC} Min)	60 70	I_{CC4}	— —	195 165	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)		I_{CC5}	—	3	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle (t_{RC} = t_{RC} Min)	60 70	I_{CC6}	— —	295 255	mA	1

NOTES:
1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Input Capacitance	Symbol	Max	Unit
Addresses	C_{in}	25	pF
$\overline{WE}$	C_{in}	31	pF
$\overline{RAS}$	C_{in}	31	pF
$\overline{CAS}$	C_{in}	24	pF
DQ, D, Q	C_{out}	17	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		60		70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	—	70	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	15	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	6
$\overline{CAS}$ to Output in Low–Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn–Off Delay	t_{CEHQZ}	t_{OFF}	0	15	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	100 k	70	200 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	15	—	20	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (Fast Page Mode)	t_{CEHREH}	t_{RHCP}	35	—	40	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	15	10 k	20	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	45	20	50	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power–up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

READ AND WRITE CYCLES (continued)

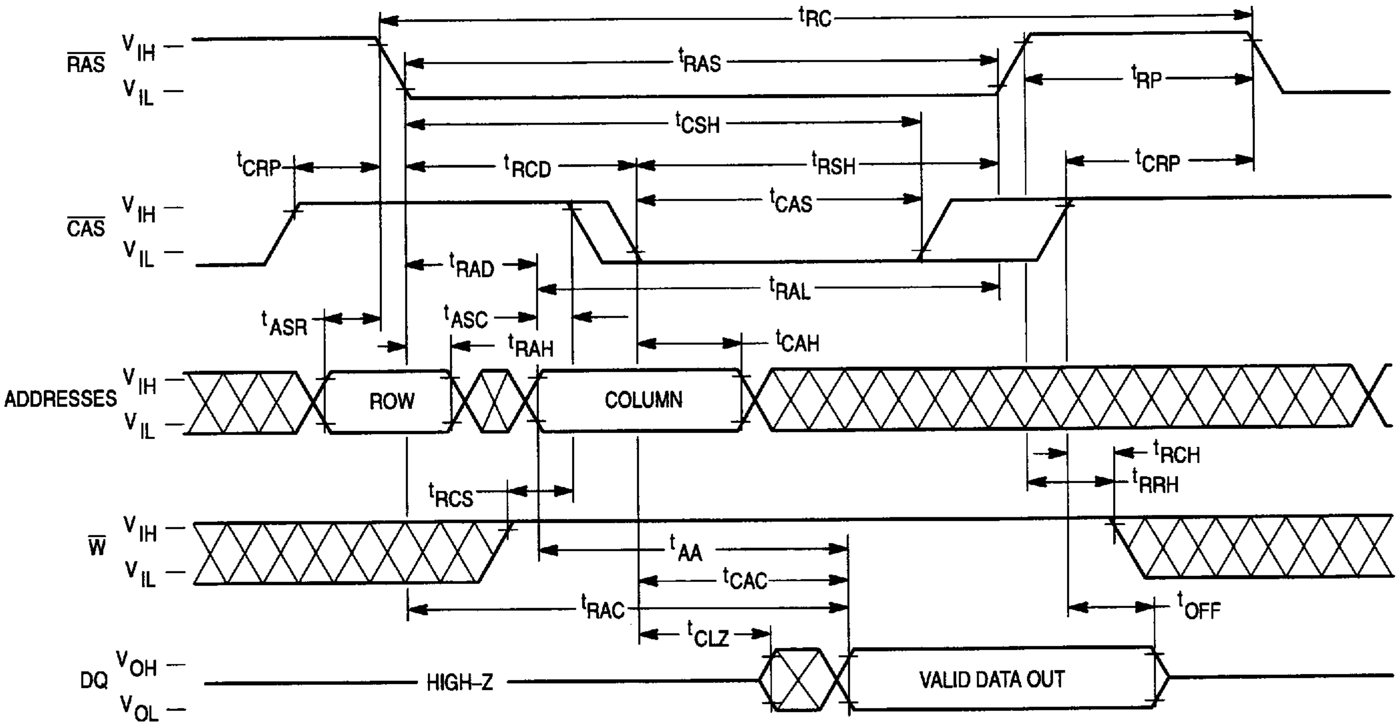
Parameter	Symbol		60		70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	10	—	15	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	10	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	15	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	15	—	20	—	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14
Data In Hold Time	t_{CELDX}	t_{DH}	10	—	15	—	ns	14
Refresh Period	t_{RVRV}	t_{RFSH}	—	32	—	32	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	10	—	15	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Time	t_{CEHCEL}	t_{CPT}	20	—	30	—	ns	

NOTES:

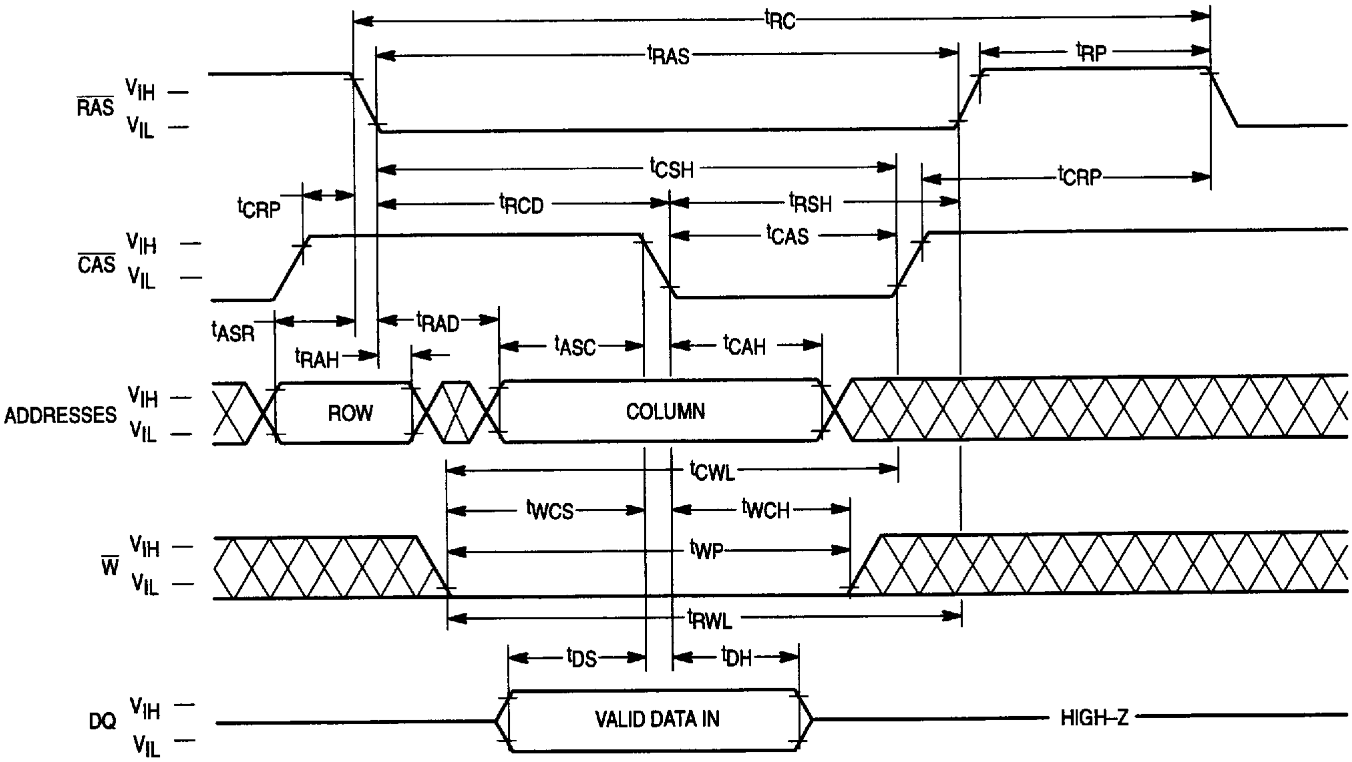
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisifed, the condition of the data out (at access time) is indeterminate.

TIMING DIAGRAMS

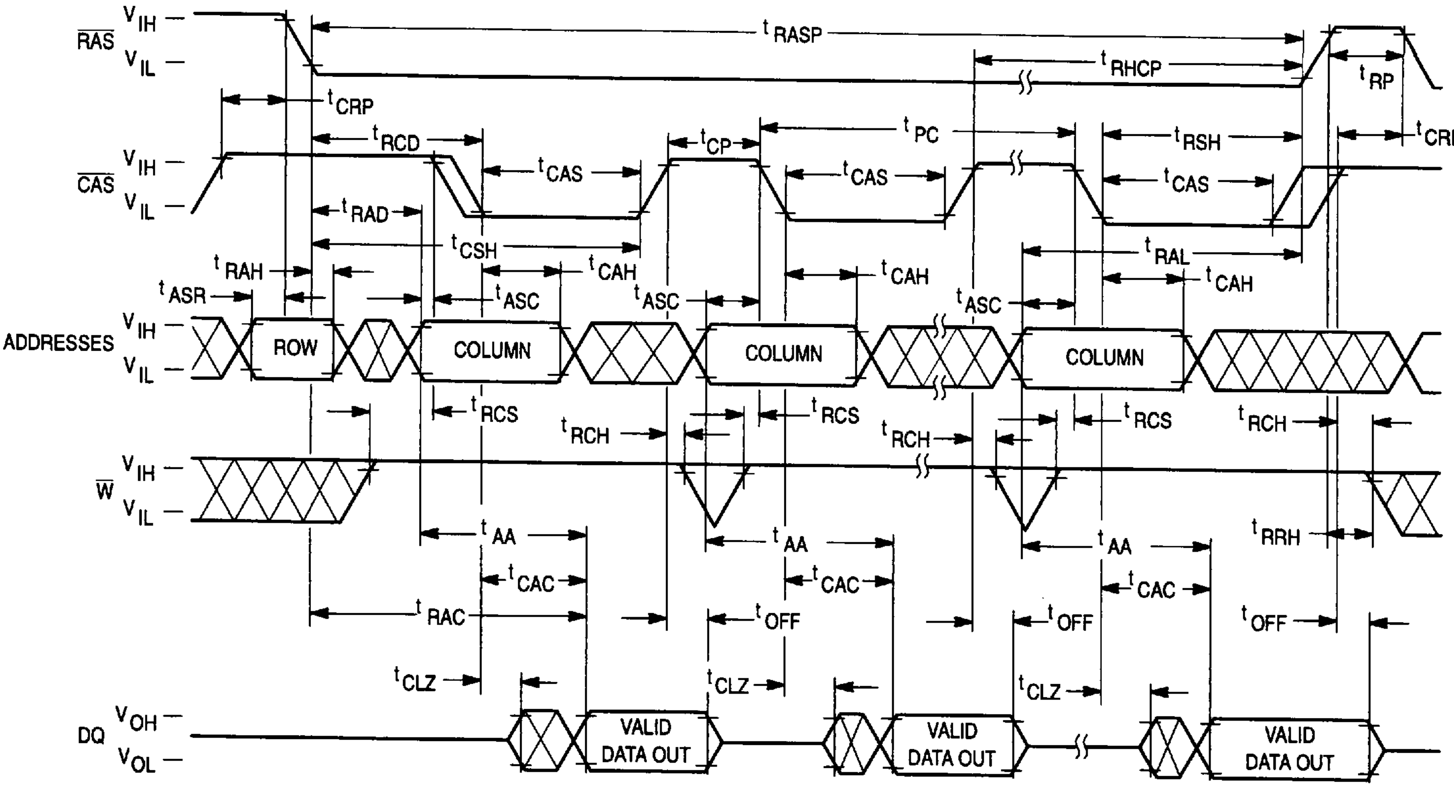
READ CYCLE



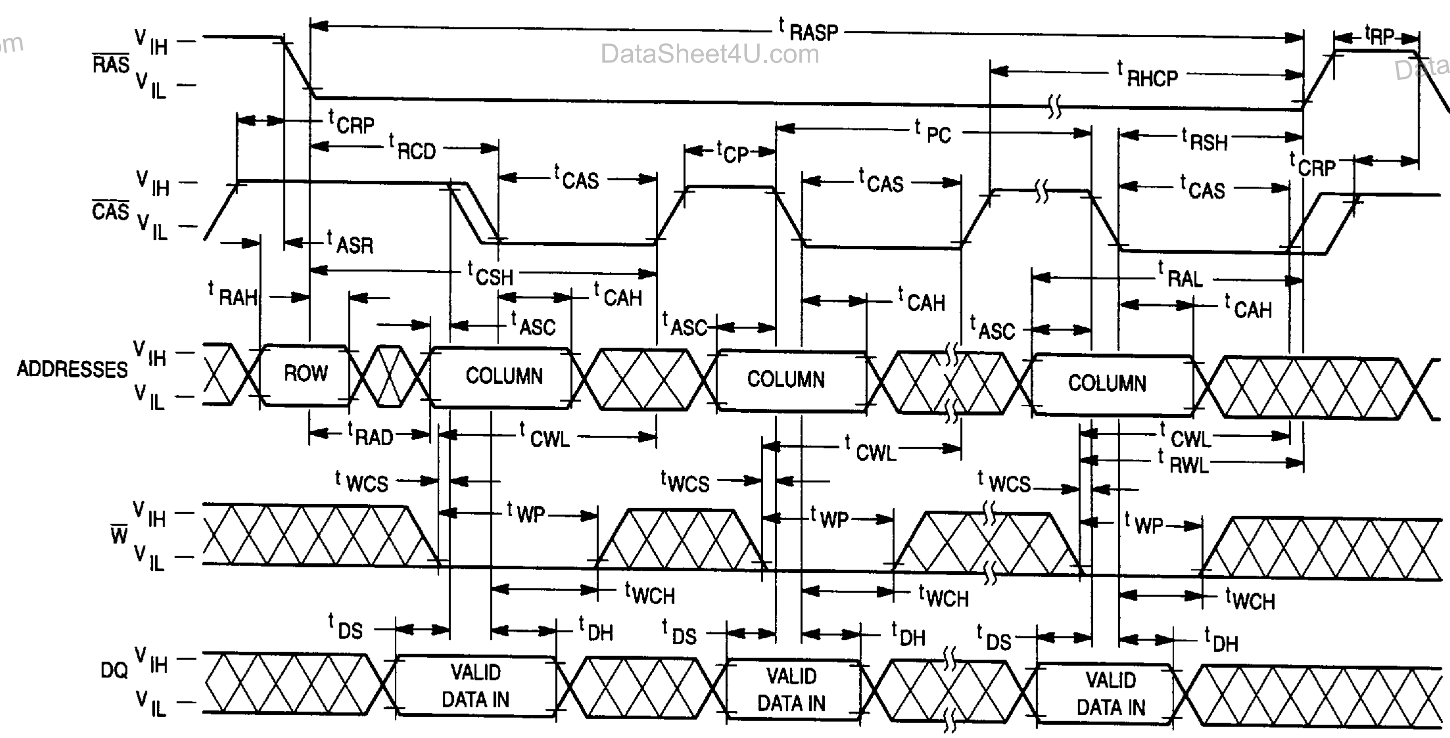
WRITE CYCLE



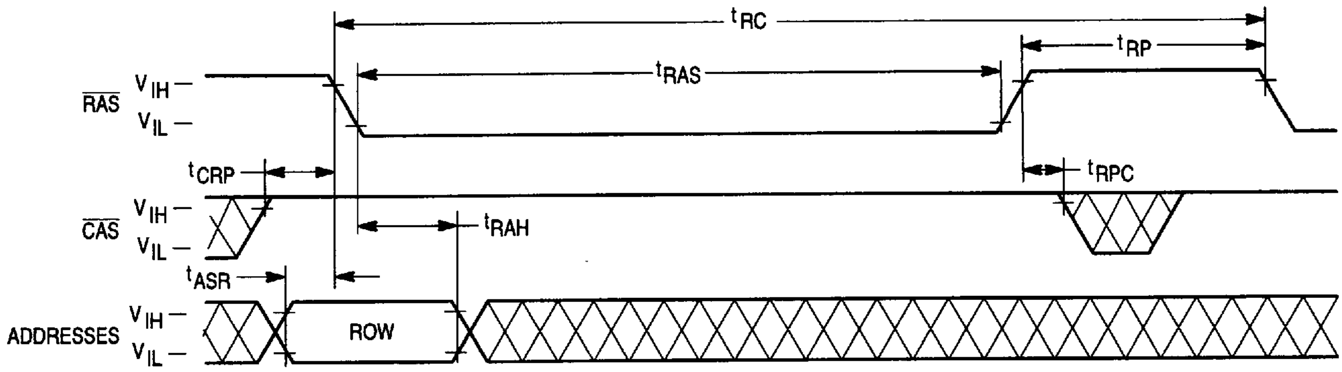
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE

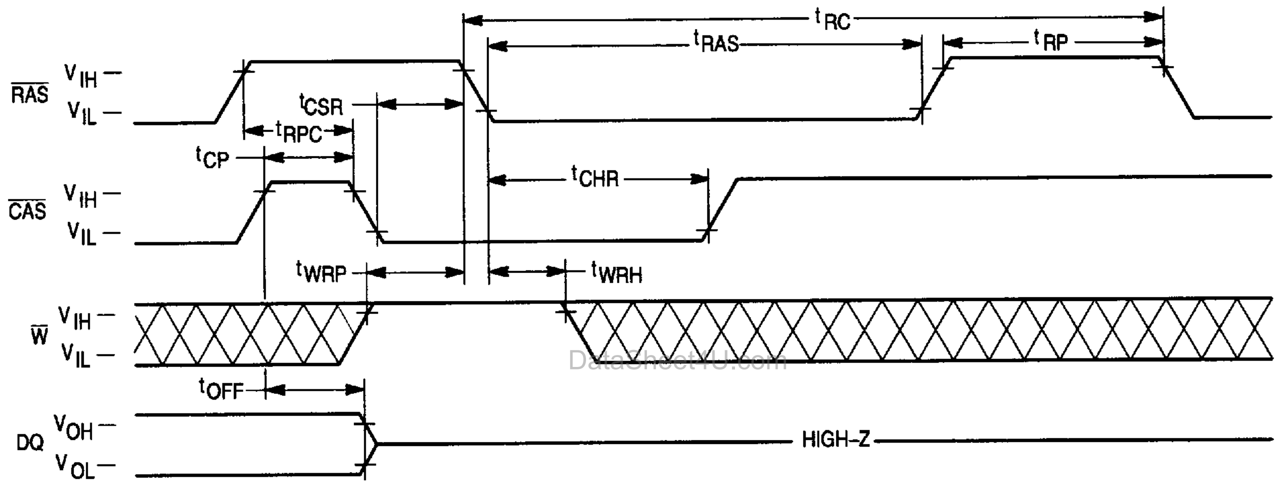


$\overline{RAS}$–ONLY REFRESH CYCLE



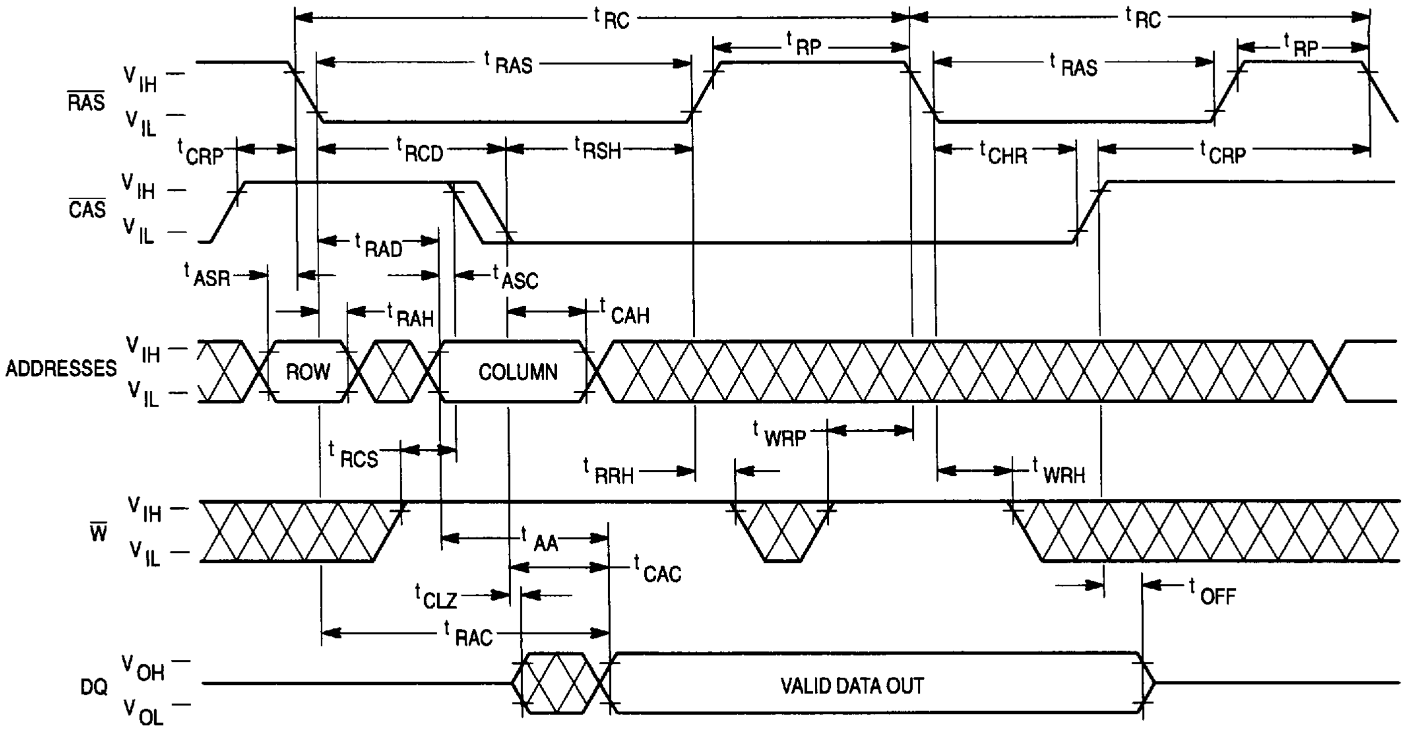
NOTE: $\overline{W}$ = H or L.
DQ = Open.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

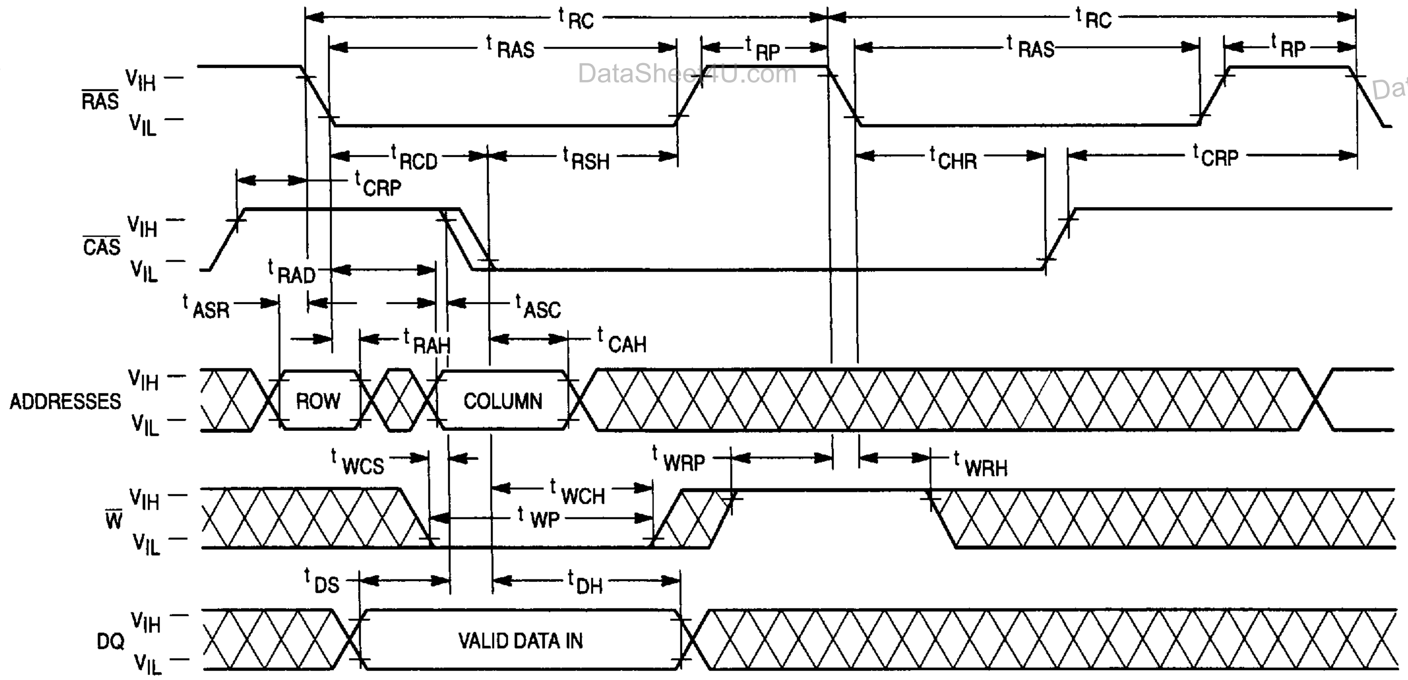


NOTE: Addresses = H or L.
$\overline{W}$ must be as shown to avoid switching into component test mode.

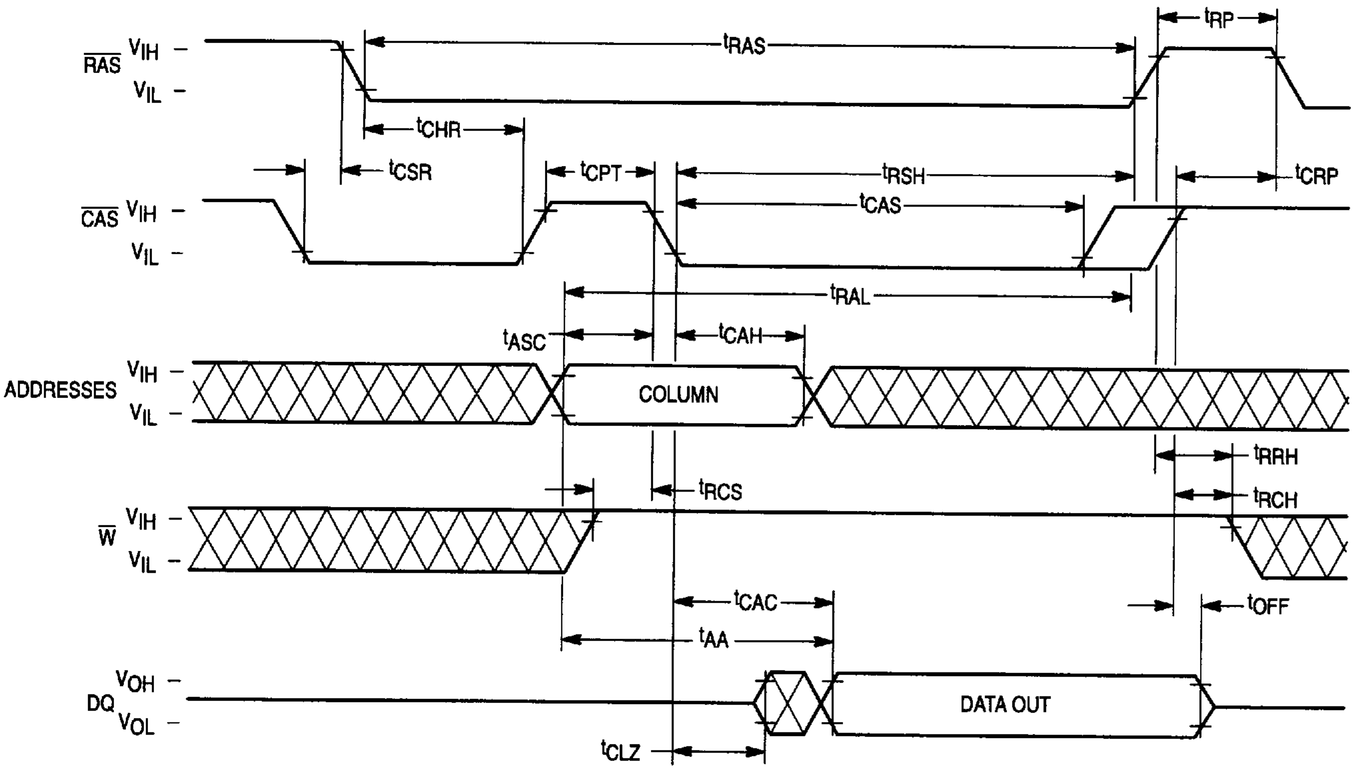
HIDDEN REFRESH CYCLE (READ)



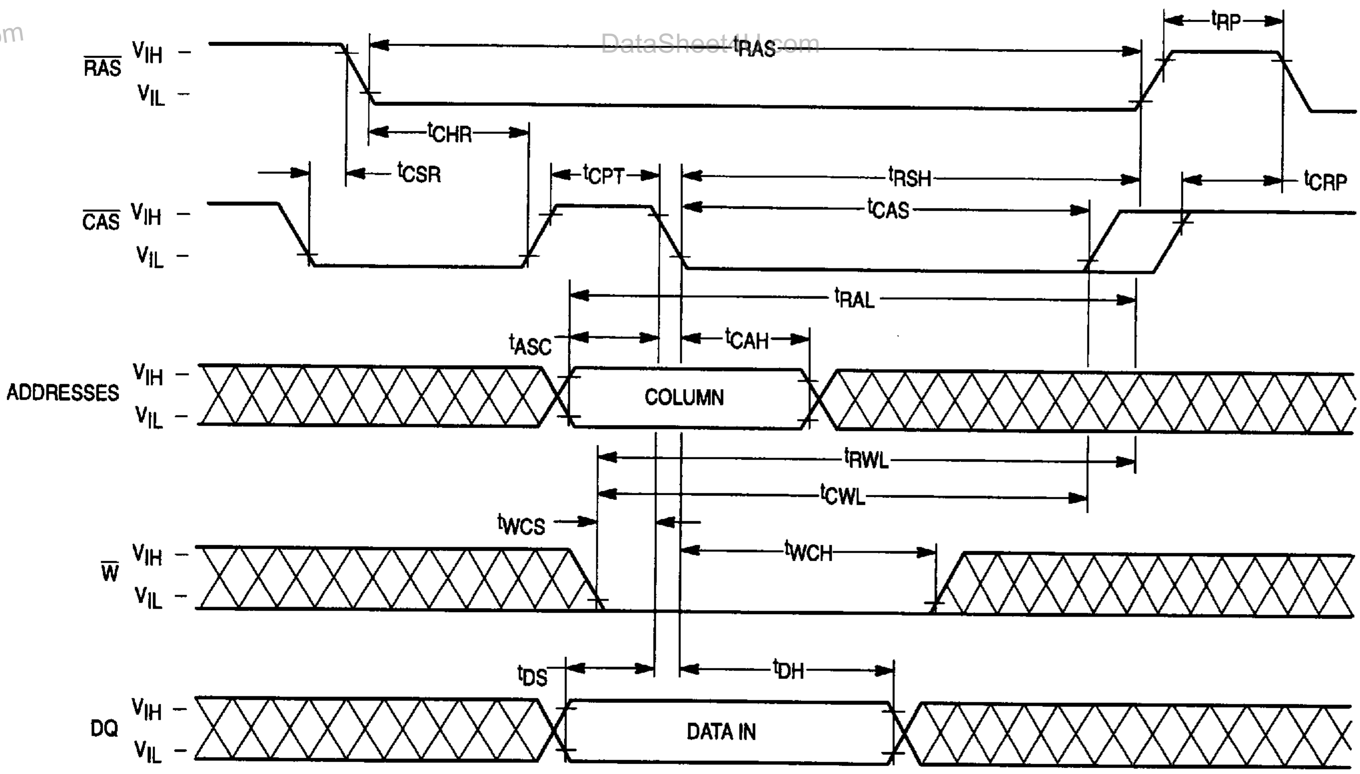
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



DEVICE INITIALIZATION

On power–up, an initial pause of 200 µs is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 ms), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate address fields. A total of 22 address bits, 11 rows and 11 columns, will decode one of the word locations. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are three other variations in addressing the module family per device: $\overline{RAS}$–only refresh cycle, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, and page mode. All are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, fast page mode read cycle, read–write cycle, and fast page mode read–write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ or active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window.

Both $\overline{CAS}$ and output enable ($\overline{G}$) control read access time: $\overline{CAS}$ must be active before or at t_{RCD} maximum and $\overline{G}$ must be active t_{RAC}–t_{GA} (both minimum) after $\overline{RAS}$ active transition to guarantee valid data out (Q) at t_{RAC}. If the t_{RCD} maximum is exceeded and/or $\overline{G}$ active transition does not occur in time, read access time is determined by either the $\overline{CAS}$ or $\overline{G}$ clock active transition (t_{CAC} or t_{GA}).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, fast page mode early write, and fast page mode read–write. Early and late write modes are discussed here, while fast page mode write operation is covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP}, apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Column address setup and hold times (t_{ASC}, t_{CAH}) and data in (D) setup and hold times (t_{DS}, t_{DH}) are referenced to in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three–state condition throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CAS}$ active transition, keeping data–out buffers disabled.

A late–write cycle (referred to as $\overline{G}$–controlled write) occurs when $\overline{W}$ active transition is made after $\overline{CAS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 µs after $\overline{CAS}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T$) $\leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D timing parameters are referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CAS}$ active transition. Outputs are switched off by $\overline{G}$ inactive transition, which is required to write to the device. Q may be indeterminate (see note 15 in the AC Operating Conditions table). $\overline{RAS}$ and $\overline{CAS}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{W}$ active transition to complete the write cycle. $\overline{G}$ must remain inactive for t_{GH} after $\overline{W}$ active transition to complete the write cycle.

READ–WRITE CYCLE

A read–write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} and/or t_{AWD} minimum, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all column locations on a selected row. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read–write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read–write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits require refresh every t_{RFSH}.

This is accomplished by cycling through the row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 µs. Burst refresh, a refresh of all rows consecutively, must be performed every t_{RFSH}.

A normal read, write, or read–write operation to the RAM will refresh all the bits associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$–only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$–Only Refresh

$\overline{\text{RAS}}$–only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter should be employed to ensure that all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1).

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test.** This test is performed with a read–write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after completing one cycle for every column, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write 0s into all memory cells with normal write mode.
2. Select a column address, read 0 out and write 1 into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read–write cycle.** Repeat this operation for every column.
3. Read the 1s that were written in step two in normal read mode.
4. Using the same starting column address as in step two, read 1 out and write 0 into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read–write cycle.** Repeat this operation for every column.
5. Read 0s which were written in step four in normal read mode.
6. Repeat steps one through five using complement data.

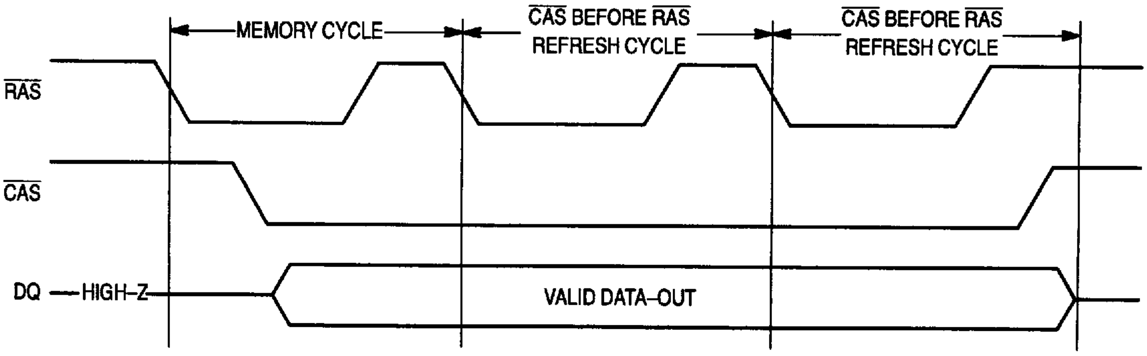
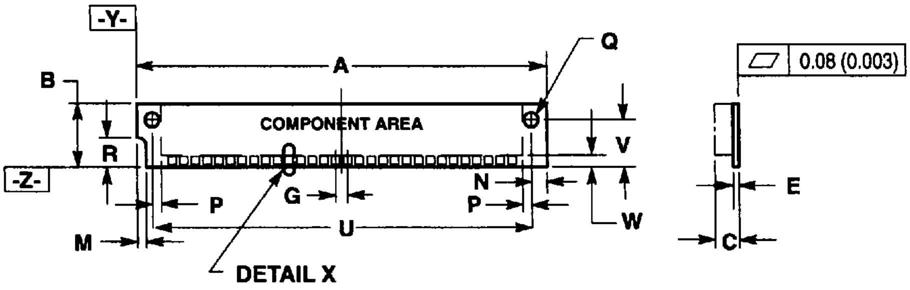
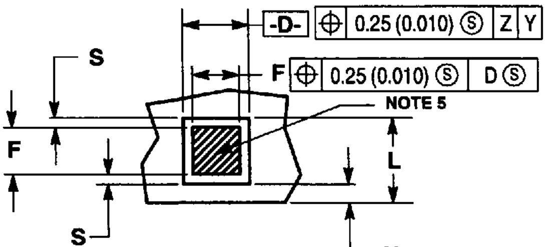


Figure 1. Hidden Refresh Cycle

PACKAGE DIMENSIONS

4M x 8 (4MB)
30–LEAD SIMM
CASE 839A–01





DETAIL X
60 PL

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TABS TO BE ELECTRICALLY CONNECTED BOTH SIDES OF CARD.
4. DIMENSION E INCLUDES PLATING AND/OR METALIZATION.
5. CONTACT ZONE MUST BE FREE OF HOLES.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	3.495	3.505	88.78	89.02
B	0.545	0.555	13.85	14.09
C	—	0.208	—	5.28
D	0.065	0.075	1.66	1.90
E	0.047	0.053	1.20	1.34
F	0.045	0.055	1.15	1.39
G	0.100 BSC		2.54 BSC	
H	—	0.010	—	0.25
L	0.080	—	2.04	—
M	0.075	0.085	1.91	2.15
N	0.128	0.138	3.26	3.50
P	0.045	—	1.15	—
Q	0.123	0.127	3.13	3.22
R	0.245	0.255	6.23	6.47
S	0.005	0.015	0.13	0.38
U	3.229	3.239	82.02	82.27
V	0.395	0.405	10.04	10.28
W	0.100	—	2.54	—

ORDERING INFORMATION
(Order by Full Part Number)

MCM 94 XX 430 X XX

- MCM — Motorola Memory Prefix
- 94 — Configuration (4M x 9)
- XX — Component Die Revision
  - C = C Die Revision
  - T = TSOP Component
- 430 — Part Numbers
- X — Package (S = SIMM)
- XX — Speed (60 = 60 ns, 70 = 70 ns)

Full Part Numbers — MCM94C430S60 MCM94CT430S60
MCM94C430S70 MCM94CT430S70