Advanced Communication Devices

PRELIMINARY

Data Sheet: ACD81024

24 Ports Single Chip 10Base-T Ethernet Switch Designed For Desktop Environment

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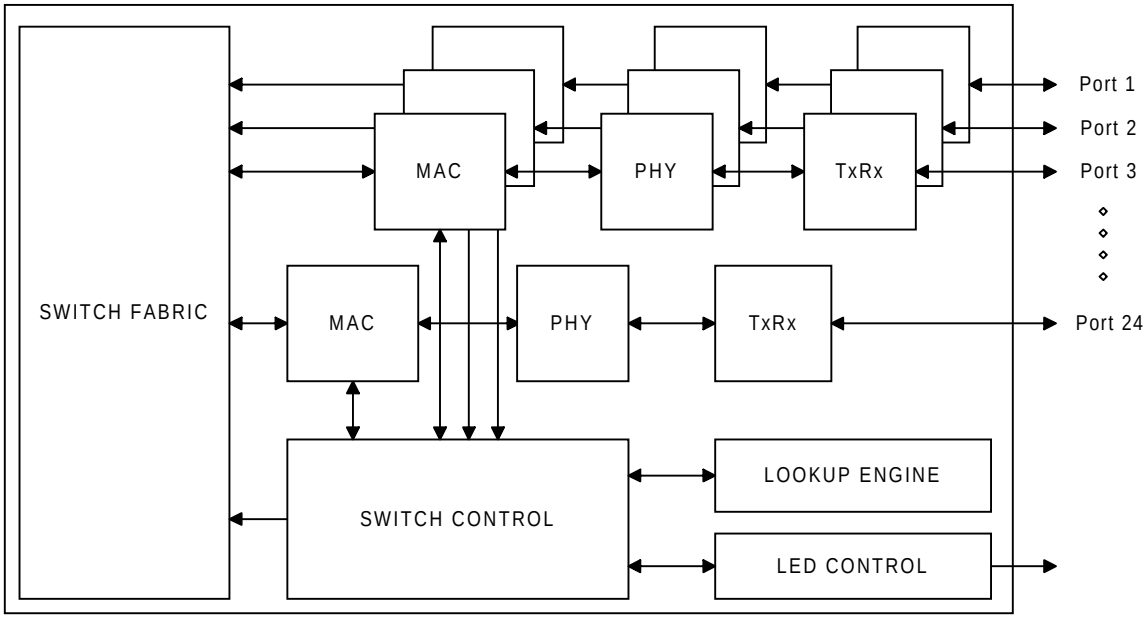
1. GENERAL DESCRIPTION

ACD81024 is a single chip system integration of an entire 24 port Ethernet switch, specifically designed for networks compliance with IEEE 802.3 10Base-T standard. All active components of a 24 port Ethernet switch system, including the 10BASE-T transceivers, clock and data recovery circuitry, Manchester ENDEC, Media Access Control logic, Lookup Engine, Switch Fabric, and Switch Control logic are all integrated into a single semiconductor chip. ACD81024 can be used to build a desktop class 10BASE-T Ethernet switch system with very low cost and very short time-to-market cycle. To build a marketable Ethernet switch system using ACD81024 requires no more than a DC power supply, EMI/RFI filter/transformer modules, RJ45 connectors, LEDs, and LED drivers.

2. MAIN FEATURES

- Single chip integration of a Ethernet switch system
- Supports 24 10Base-T ports
- Very short time-to-market cycle
- No need of external memory
- No need of external glue logic
- Built-in 10BASE-T transceiver
- Built-in clock and data recovery circuitry
- Smart squelch intelligence
- Polarity detection and correction
- Link integrity pulse detection and generation
- Manchester ENDEC
- Media Access Control logic
- FCS verification
- Storage of one MAC address per port
- Lookup Engine
- Non-blocking Switching Fabric
- Fabric Control logic
- Back-pressure congestion control
- Automatic MAC address learning
- Cut-through switching mode with constant low latency < 16 us
- LED display of each port's Link Status, Transmit, Receive, Collision, Congestion, Jabber, and FCS Error indication
- One expansion port for connecting with other interconnection devices
- Line speed forwarding rate
- 208 pin PQFP package with built-in Heat-Sink
- Single 5V power supply

System Block Diagram



3. OPERATIONAL DESCRIPTION

ACD81024 Ethernet switch is composed by six types of logic modules: the Physical Layer (PHY) circuitry, the Media Access Control (MAC) logic, the Lookup Engine, the Switching Fabric, the Fabric Control logic, and the LED Control logic. On the receiving side, the PHY circuitry converts the analog voltages coming from the unshielded twist pair cable into digital signals suitable for digital processing, and decodes the received data in Manchester code into NRZ code. On the transmitting side, the PHY circuitry translates the data to be transmitted from NRZ code into Manchester code, and then converts the data into analog signals suitable to drive unshielded twist pair cable. The MAC logic of a port controls the transmit, receive, defer, and congestion control process of the port. The Lookup Engine provides mapping between a destination MAC address and a destination port number. The Switching Fabric is used to establish communication channels between the source ports and the associated destination ports. The Fabric Control logic controls the construction/destruction of the communication channels. The LED Control logic displays various kinds of port status of the switch.

ACD81024 is designed as a desktop class Ethernet switch. Only one DTE with one MAC address can be connected to each port of ACD81024, except the expansion port.

When an Ethernet frame comes from a data termination device (DTE) through a 10Base-T network media (UTP) into a source port of ACD81024 switch, the signal, encoded in Manchester code, is amplified by the twist pair receiver circuitry of the source port and converted into a NRZ data signal and a recovered clock signal by the decoder circuitry of the source port. The NRZ data signal is then processed by the MAC logic of the source port. The information of the destination address (DA) and the source address (SA) embedded inside the frame are retrieved. The SA is used to update the port's MAC address stored in the Lookup Engine. The DA is used to identify the destination port. Once the destination port is identified, the Fabric Control logic checks the status of the destination port(s) to see if the destination port(s) is ready to receive the data. If so, the Fabric Control logic establishes the communication channel(s) between the source port and the destination port(s) inside the Switching Fabric. The MAC logic of the source port forwards the received data to the established the communication channel in the Switching Fabric. The MAC logic of the destination port(s) receives the data from the communication channel in the Switching Fabric and forwards the data to the destination port's Physical Layer circuitry. The Manchester encoder circuitry translates the data into Manchester code and sends to the port's twist pair transmitter circuitry. The transmitter circuitry converts the data into analog levels suitable to drive the 10Base-T network media between the switch and the destination DTE. If collision is detected during a transmission process, the destination port MAC logic will end the frame with a Jam pattern. The source port MAC logic will stop forwarding the frame data and send a Jam pattern back to the source DTE.

If the destination port headed by an incoming frame is not ready to receive the data, the MAC logic of the source port will send a Jam pattern to the source DTE. According to IEEE 802.3 CSMA/CD scheme, the source DTE will retransmit the frame after a predetermined back-off time period. In order to prevent the source DTE from sending the frame before the destination port is ready, ACD81024 continuously sends a Back Pressure signal to the source DTE to cause its Carrier Sense signal to be asserted. The transmit-defer-on-carrier-sense nature of CSMA/CD scheme will prevent the source DTE from sending the frame as long as the Carrier Sense signal is asserted. The Back Pressure signal is released when the destination port(s) is ready to receive new frame.

Different from a typical Ethernet frame switch, ACD81024 does not store the received data into data buffer. Instead, it sends the data directly to the destination port in cut-through mode. In collision domain isolation perspective, ACD81024 behaves like a shared-media repeater. Once collision is detected on the destination port, a Jam pattern is sent to the source DTE to force collision detection. Different from a shared-media repeater, collision is caused by concurrent transmission activities of the source DTE and the destination DTE(s), not any DTE connected with the switch. In other words, the collision domain is minimized to the source port and the corresponding destination port(s).

4. FUNCTIONAL DESCRIPTION

4.1 PHY Module

ACD81024 provides built-in twist pair transmitter/receiver (transceiver) circuitry for each port. Besides, each PHY module also contains the logic for polarity detection and automatic correction, Manchester code encoding and decoding, clock data recovery, and link pulse detection and generation. All circuits are implemented to be 100% compatible with IEEE 802.3 requirement.

Twist Pair Transmitter

The twist pair transmitter converts the digital output signal into analog voltages necessary to drive unshielded twist pair cable. Different from most other implementations, the transmitter circuitry inside ACD81024 uses two output pins (as opposed to four) and internally generates emphasis/de-emphasis voltage levels required to compensate for the twist pair cable. The waveform of each kind of output signal is described in the chapter of “Signal Waveforms.”

Twist Pair Receiver

The Twist Pair Receiver converts the analog voltages coming from the unshielded twist pair cable into TTL level signals suitable for digital processing.

Each Twist Pair Receiver of ACD81024 is equipped with a smart squelch circuitry to ensure that noise on the receive pair will not be treated as valid frame data signals. The squelch circuitry employs a combination of both amplitude and timing measurement to determine the validity of received data signal. Only valid data will be passed to the Manchester Decoder circuitry. Validity of data is determined by following three conditions:

1 The signal crosses the positive threshold level of +365 mV or negative threshold level of -365 mV.
2 The signal has to cross the other threshold level within 150 ns.
3 The signal has to cross the original threshold within 150 ns.

The waveform of signal received by the smart squelch circuitry is described in the chapter of “Signal Waveforms.”

Polarity Detection and Correction

Polarity Detection circuitry uses the incoming link pulses to check for polarity reversal. If the polarity of the signal is detected to be reversed, the Polarity Correction logic automatically inverts the receiving pair. Therefore, the MAC logic circuitry will always receive the signal in correct polarity.

Manchester Decoding

On the receive side, after passing through the polarity detection and automatic correction circuitry, the incoming signal is processed by the Manchester decoder circuitry. The Manchester decoder converts the Manchester code data signal into NRZ data signal and at same time, generates a recovered clock signal. The recovered clock signal is used to latch the NRZ data into a synchronization FIFO. The NRZ data is read out of the FIFO using the system clock.

Manchester Encoding

On the transmit side, the NRZ data coming from the MAC logic is converted into Manchester code by the Manchester encoder circuitry. The data is then passed to the 10Base-T transceiver circuitry for transmission onto the network media.

Link Pulse Detection

On the receive side, each PHY module has a link pulse detection circuitry. If no link pulse is received for 50 ms, a link test fail signal will be sent to the port’s MAC logic circuitry to cause it enter the Link Fail state. In Link Fail state, the Link LED signal of the port is deserted. However, transmission from the port is not disabled. Any traffic heading for this port will still be forwarded to it. When the PHY circuitry receives a valid link pulse, or receives a continuous bit stream, it signals the MAC logic for valid link status and causes MAC logic enter the Link Pass state immediately. The waveform of a link pulse to be detected by the link pulse detector is shown in the chapter of “Signal Waveforms.” The link pulse detection function can be disabled by pulling low the LNKE signal.

Link Integrity Pulse Generation

On the transmit side, each PHY module has a link pulse generation circuitry. When there is no transmission activity on the transmission pair, the link pulse generation circuitry generates one link pulse for every 16 ms. The width of the link pulse is 100ns. The waveform of the link pulse generated by ACD81024 is shown in the chapter of “Signal Waveforms.”

4.2 MAC Module

The MAC module controls the transmit, receive, defer, and congestion control process of a port, according to IEEE 802.3 standard.

Frame Format

ACD81024 assumes the data frame coming into the switch have the following format:

Where,

Preamble	SFD	DA	SA	Type/Len	Data	FCS

- Preamble is repetitive pattern of 1010…. of any length longer than 30 bits.

- SFD (Start Frame Delimiter) is defined as an octet pattern of 10101011.

- DA is a 48-bit field which specifies the MAC address of the DTE to which the frame is heading. If the first bit of DA is 1, ACD81024 will treat the frame as a broadcast/multicast frame and will forward the frame to all ports except the source port itself.

- SA is a 48-bit field which contains the MAC address of the DTE which is transmitting the frame to ACD81024.

- Type/Len field is a 2-byte field which specifies the type (DIX Ethernet frame) or length (IEEE 802.3 frame) of the frame. ACD81024 will not try to interpret this field.

- Data could be any information which is totally transparent to ACD81024.

- FCS (Frame Check Sequence) is a 32-bit field of CRC (Cyclic Redundancy Check) value based on the destination address, the source address, the type/length and the data field. ACD81024 will verify the FCS field for each frame. The procedure of computing FCS is described in section of "FCS Calculation".

Destination Address Processing

As a frame comes into a port of ACD81024, the destination address field embedded inside the frame is retrieved and passed to the Lookup Engine to match it with the MAC addresses stored in source MAC address registers of all ports. The destination port is found if a match is found.

Source Address Learning

As a frame comes into a port of ACD81024, the value of the source address embedded inside the frame is automatically read into a data register. At the end of the frame, if there is no FCS error and, if there is no value stored in the MAC address register of the source port, or if the value of this new source address is different than the port's current MAC address, the recorded value is used to update the MAC address register of the source port inside the Lookup Engine module. The value will be used by the Lookup Engine to match with the destination address embedded in a frame to identify the destination port.

A port's MAC address register is cleared on power-up, by hardware reset, or when the MAC logic circuitry enters its Link Fail state due to loss of link pulse reported by the PHY module.

Unicast Frame Forwarding

If the first bit of the destination address is 0, the frame is a unicast frame. The destination address is passed to the Lookup Engine which returns a destination port(s) number(s) to identify which port(s) should the frame be forwarded. If the Lookup Engine cannot find any match for the destination address, the frame will be forwarded to all the ports which has not learned its source address, plus the expansion port. The returned destination port number is passed to the Fabric Control logic which checks if the destination port(s) is ready to receive the frame. If it is, the Switch Control Logic constructs the communication channel(s) between the source port and the destination port(s). The source port MAC logic forwards the incoming frame to the destination port(s) MAC logic through the communication channel(s). While the data is forwarded, the MAC logic of the destination port keeps on monitoring if collision occurs on the destination port. If so, the source port MAC logic will send a jam pattern to the source DTE. If the any one of the destination port(s) is not ready to receive the frame, the source port MAC logic will start a congestion control process. The details of congestion control is explained in the section of "Congestion Control."

Broadcast/Multicast Traffic Handling

If the first bit of the destination address is a 1, the frame is a multicast or broadcast frame. ACD81024 treats multicast frame the same as broadcast frame. For a broadcast frame, the destination port contains all the ports of the switch except the source port itself. The Fabric Control logic checks if all the destination ports are ready for receiving this broadcast frame. If all of the destination ports are ready to receive the frame, the source port will forward the frame data to all destination ports in cut-through mode. If any one of the destination ports is not ready, the source port MAC logic will send a Jam pattern to the source DTE, followed by Back Pressure signal. When all ports are ready to transmit the broadcast frame, the Back Pressure signal applied to the source DTE will be removed. Upon the time the source DTE retransmits the broadcast frame to the switch, the frame data is forwarded to all destination ports.

FCS Calculation

Each port of ACD81024 has a CRC checking logic to

verify if the received frame has a valid FCS value. Wrong FCS value is an indication of a fragmented frame or a frame with frame bit error. The method of calculating the CRC value of the frame data is by using following polynomial

$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$$

as a divider to divide the bit sequence of the incoming frame, beginning with the first bit of destination address field, up to the end of the data field. The result of the calculation, which is the residue after the polynomial division, is the value of frame check sequence. The value should be equal to the FCS field appended at the end of the frame. If the value does not match with the FCS field of the frame, the Frame Bit Error LED of the port will be turned on once.

Short Frame Handling

If a frame is shorter than 140 bits after the SFD fields, it will not be forwarded to the destination port(s). Frames longer than 140 bits will be forwarded to the destination port(s) no matter if it passes the FCS checking or not.

Jabber Lockup Protection

If an incoming frame is detected to be longer than 50,000 bits, it will be broken by the Jabber Protection circuitry inside the MAC logic. The frame bits later than 50,000 bit will be forwarded to nowhere. A Jabber error is reported through the Jabber error LED of the port. After proper inter-frame-spacing time, the MAC logic of the port will be ready to receive next frame.

Transmit Time Watchdog Control

The watchdog circuitry inside each MAC logic keeps on monitoring the number of bits transmitted by the destination MAC logic. If the length of the transmitted frame is longer than 38,000 bit, the watchdog circuitry will break the frame and append a Jam pattern to the end. This function can be disabled by pulling the WCHE signal low.

Preamble Bit Handling

The preamble bit in the header of each frame will be used to synchronize the MAC logic circuitry with the incoming bit stream. The minimum length of the preamble is 30 bits and there is no limit on the maximum length of preamble. The preamble will be regenerated by MAC logic of ACD81024 with exact length of 56 bits as the frame is transmitted out of the destination port(s).

Inter Frame Spacing Handling

If the silent time between frames coming from a DTE is less than the minimum IFS requirement of 96BT, ACD81024 will send a jam pattern to the corresponding source DTE just like a congestion has occurred.

Collision Detection and Handling

While the MAC logic of a destination port is transmitting data to the destination DTE, if there is any data coming from the destination DTE (or say if the carrier sense signal is raised up by the PHY module of the destination port), collision is detected. Collision will cause the MAC logic of both the destination port and the source port to enter a collision handling state. On the destination port side, current transmit process is aborted and a Jam pattern is appended to the end of the broken frame. On the source port side, a Jam pattern is sent to the source DTE, beginning with 56 bit preamble and a valid Start of Frame Delimiter. The Jam pattern will cause the source DTE to stop transmitting and retransmit the frame after proper back-off time.

Congestion Detection and Handling

If a destination port headed by an incoming frame is in the process of receiving or transmitting or deferring on inter-frame-spacing time, the Fabric Control logic signals the source port MAC logic that the destination port is not ready. The source port MAC logic then enters a Congestion Control state. In Congestion Control state, the MAC logic of the source port first sends a Jam pattern to the source DTE to force a collision, and then, after proper inter-frame-spacing time, sends a continuous Back Pressure signal to the source DTE. If collision is detected on the Back Pressure signal, the MAC logic will end the Back Pressure pattern with a Jam pattern, wait for minimum IFS time, and send the Back Pressure signal again. When the destination port(s) is available, the Back Pressure signal is ended with a Jam pattern.

Expansion Port Handling

Port 24 of ACD81024 is designed to be the expansion port (or say the dumping port). It can be used for uplink connection or for ordinary desktop connection. That is, port 24 can be connected with a repeater hub, a work-group switch, a router, or any type of interconnection device compliance with IEEE 802.3 10Base-T standard. ACD81024 will direct following frames to the expansion port:

1 frame with unicast destination address and does not match with any port MAC address of the switch
2 frame with broadcast/multicast address
3 frame dumped to keep DTE address alive (see section of “Address Keep Alive Handling”)

Address Keep Alive Handling

The address learned by an interconnection device has a limited life cycle. To keep the address of the DTEs connected with the switch alive in the interconnection device connected with the expansion port of the switch, ACD81024 can be set to dump at least one frame to the expansion port for every five minutes. This function can be disabled by pulling low of the DMPE signal.

Half Duplex Operation Mode

ACD81024 can only work in half duplex mode. Any concurrent transmit and receive activities will be treated as collision.

Spanning Tree Handling

Only port 24 of ACD81024 can be used to connect with an interconnection device which support multiple MAC addresses. All other ports of ACD81024 should only be used to connect with one desktop DTE with only one MAC address. Therefore, it is not necessary to handle Spanning Tree protocol to avoid formation of a loop.

Latency

The latency, defined by the time difference between the first bit enters into ACD81024 and first bit comes out of ACD81024, is a constant value of 146 Bit Time.

Collision Domain

Different from typical Ethernet switch, ACD81024 does not isolate the collision domain between the source DTE and the destination DTE. Therefore, the latency of ACD81024 needs to be counted as part of the delay path. The delay on the forward path is 146 Bit Times. The delay on the backward path (for collision detection) is 4 Bit Times.

4.3 Lookup Engine Module

The lookup engine is responsible to provide mapping between a MAC address and a port number. It contains one MAC address storage for each port. The value of SA embedded inside the frame is used to update the value of the MAC address storage of the source port. The value of DA is used to identify the destination port.

4.4 Switch Fabric Module

Switch Fabric is responsible for establishing the connection channel(s) from a source port to the corresponding destination port(s). ACD81024 implements a cross-bar type switch fabric that allows high efficient multiple channels of simultaneous connections.

4.5 Fabric Control Module

Fabric Control Logic controls the process of construction/destruction of the communication channel in the Switch Fabric. Before a connection can be made, Fabric Control logic first checks the status of the destination port(s), to see if it is suitable to open the path. Fabric Control logic is responsible to notify the source MAC logic if the requested connection has been made or not.

4.6 LED Control Module

Just like a shared media repeater system, ACD81024 is designed to have a wide variety of LED indicators for simple system administration. The display update is completely autonomous and merely requires low speed TTL or CMOS devices as LED drivers. The status display is designed to be flexible to allow the system designer to choose those indicators appropriate for the specification of the equipment.

There are two LED control signals. LEDVLD signal is used to indicate the start and end of the LED data signal. LEDCLK signal is a 1MHz clock signal. The rising edge of LEDCLK can be used to latch the LED data signal into the LED driver circuitry.

The LED data signals contain Lnk, Xmt, Rcv, Col, Fbe, Jbr, Addr and Bsy, which represent Link status, Transmit status, Receive status, Collision indication, Frame Bit Error, Jabber error, Port Address Learned status, and Congestion Control status respectively. These status signals are sent out sequentially from port one to port twenty-four, once every 100ms. For details about the timing diagrams of the LED signals, refer to the chapter of “Signal Waveforms.”

5. SPECIAL HANDLING ON 802.3

General speaking, ACD81024 is designed to comply with IEEE 802.3 standard. ACD81024 has also been proved to work perfectly with IEEE 802.3 compatible devices. However, there are a few creative features implemented on ACD81024 which deviate a little from IEEE 802.3 standard. The following is a description on these features:

Collision Backoff Time Period

Since ACD81024 does not store the received traffic, each output port of ACD81024 does not schedule the retransmission as a bridge type device does. When collision is detected on an output port, both the source DTE and the destination DTE will receive a Jam pattern to force collision detection on both sides. ACD81024 behaves like a middle man. It is the source and destination DTEs which will follow the truncated binary exponential backoff process defined by the CSMA/CD scheme to control the retransmission time. Moreover, if there are multiple source DTEs trying to send data to the same destination DTE at same time, ACD81024 will remove the Back Pressure signal applied to one of these source ports to allow the attached source DTE to start sending data to the destination DTE. ACD81024 also monitors the number of consecutive collisions occurred on each port. When the number of collisions on a port is higher than the threshold value of three, the port has higher priority than other input ports to get the communication channel. Therefore, ACD81024 eliminates the draw backs of the Channel Capturing feature on networks using repeater hubs.

Collision-Jam Propagation Delay

ACD81024 does not isolate the collision domain between its input port and output port. Instead, it uses Jam plus Back Pressure signal for congestion control. IEEE 802.3 specifies that the collision-jam propagation delay on a repeater set with internal 10-Base-T MAUs on input and output ports should be less than 20.5 bit times. Since ACD81024 is a switching device, collision cannot be detected until the destination port is identified. As a result, the collision-jam propagation delay on ACD81024 is 150 bit times. Therefore, care should be taken when using ACD81024 in a multisegment networking environment. The summation of the round trip delay should not exceed 512 bit times, and ACD81024 contributes 150 bit times for round trip propagation delay.

6. PIN DIAGRAM AND PIN DESCRIPTION

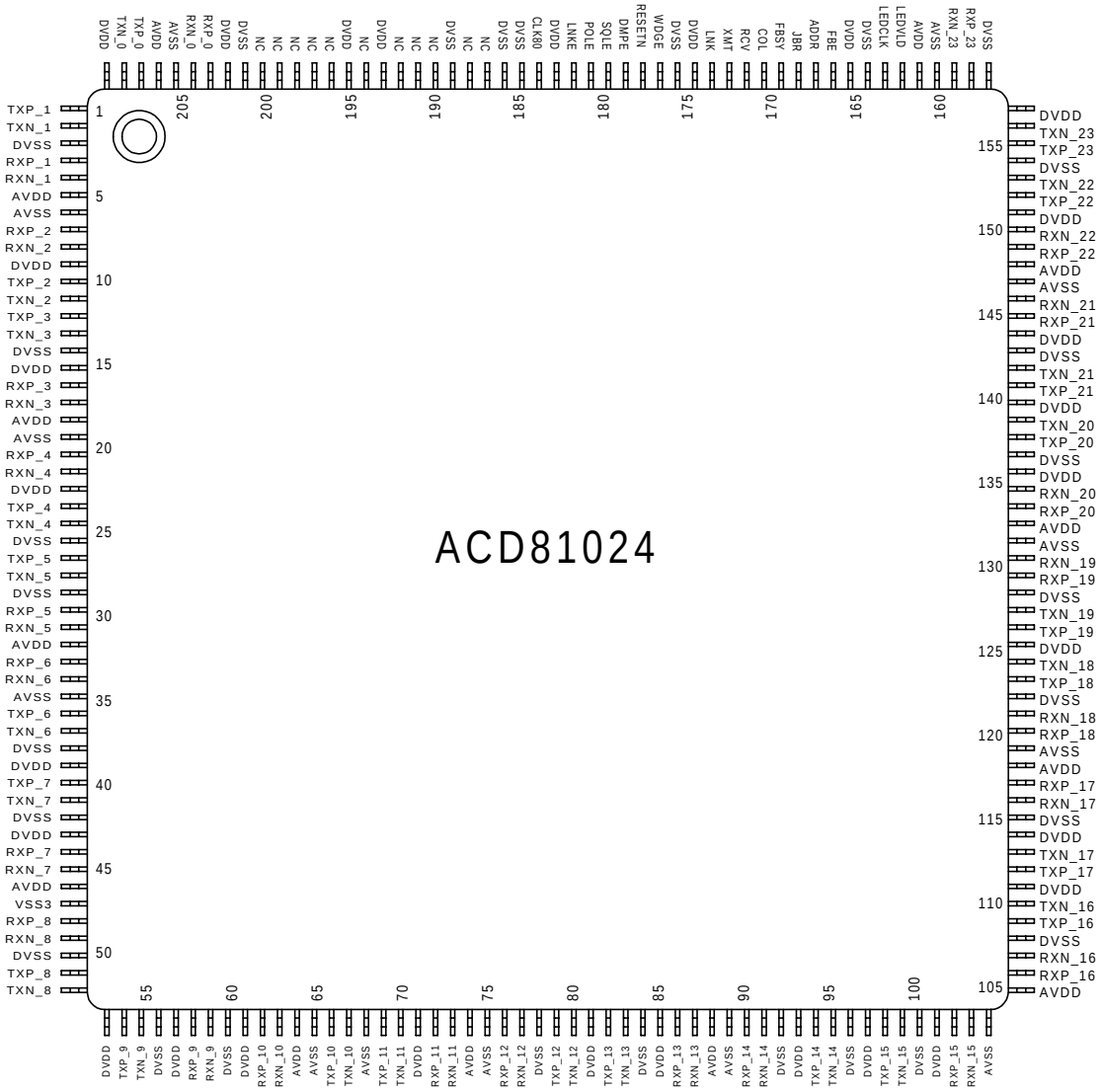


Table 6.1 - Pin List

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	TXP_1	**27**	TXP_5	**53**	DVDD	**79**	TXP_12	**105**	AVDD	**131**	AVSS	**157**	DVSS	**183**	CLK80
2	TXN_1	**28**	TXN_5	**54**	TXP_9	**80**	TXN_12	**106**	RXP_16	**132**	AVDD	**158**	RXP_23	**184**	DVSS
3	DVSS	**29**	DVSS	**55**	TXN_9	**81**	DVDD	**107**	RXN_16	**133**	RXP_20	**159**	RXN_23	**185**	DVSS
4	RXP_1	**30**	RXP_5	**56**	DVSS	**82**	TXP_13	**108**	DVSS	**134**	RXN_20	**160**	AVSS	**186**	NC
5	RXN_1	**31**	RXN_5	**57**	DVDD	**83**	TXN_13	**109**	TXP_16	**135**	DVDD	**161**	AVDD	**187**	NC
6	AVDD	**32**	AVDD	**58**	RXP_9	**84**	DVSS	**110**	TXN_16	**136**	DVSS	**162**	LEDVLD	**188**	DVSS
7	AVSS	**33**	RXP_6	**59**	RXN_9	**85**	DVDD	**111**	DVDD	**137**	TXP_20	**163**	LEDCLK	**189**	NC
8	RXP_2	**34**	RXN_6	**60**	DVSS	**86**	RXP_13	**112**	TXP_17	**138**	TXN_20	**164**	DVSS	**190**	NC
9	RXN_2	**35**	AVSS	**61**	DVDD	**87**	RXN_13	**113**	TXN_17	**139**	DVDD	**165**	DVDD	**191**	NC
10	DVDD	**36**	TXP_6	**62**	RXP_10	**88**	AVDD	**114**	DVDD	**140**	TXP_21	**166**	FBE	**192**	DVDD
11	TXP_2	**37**	TXN_6	**63**	RXN_10	**89**	AVSS	**115**	DVSS	**141**	TXN_21	**167**	ADDR	**193**	NC
12	TXN_2	**38**	DVSS	**64**	AVDD	**90**	RXP_14	**116**	RXN_17	**142**	DVSS	**168**	JBR	**194**	DVDD
13	TXP_3	**39**	DVDD	**65**	AVSS	**91**	RXN_14	**117**	RXP_17	**143**	DVDD	**169**	FBSY	**195**	NC
14	TXN_3	**40**	TXP_7	**66**	TXP_10	**92**	DVSS	**118**	AVDD	**144**	RXP_21	**170**	COL	**196**	NC
15	DVSS	**41**	TXN_7	**67**	TXN_10	**93**	DVDD	**119**	AVSS	**145**	RXN_21	**171**	RCV	**197**	NC
16	DVDD	**42**	DVSS	**68**	DVSS	**94**	TXP_14	**120**	RXP_18	**146**	AVSS	**172**	XMT	**198**	NC
17	RXP_3	**43**	DVDD	**69**	TXP_11	**95**	TXN_14	**121**	RXN_18	**147**	AVDD	**173**	LNK	**199**	NC
18	RXN_3	**44**	RXP_7	**70**	TXN_11	**96**	DVSS	**122**	DVSS	**148**	RXP_22	**174**	DVDD	**200**	DVSS
19	AVDD	**45**	RXN_7	**71**	DVDD	**97**	DVDD	**123**	TXP_18	**149**	RXN_22	**175**	DVSS	**201**	DVDD
20	AVSS	**46**	AVDD	**72**	RXP_11	**98**	TXP_15	**124**	TXN_18	**150**	DVDD	**176**	WDGE	**202**	RXP_0
21	RXP_4	**47**	AVSS	**73**	RXN_11	**99**	TXN_15	**125**	DVDD	**151**	TXP_22	**177**	RESETN	**203**	RXN_0
22	RXN_4	**48**	RXP_8	**74**	AVDD	**100**	DVSS	**126**	TXP_19	**152**	TXN_22	**178**	DMPE	**204**	AVSS
23	DVDD	**49**	RXN_8	**75**	AVSS	**101**	DVDD	**127**	TXN_19	**153**	DVSS	**179**	SQLE	**205**	AVDD
24	TXP_4	**50**	DVSS	**76**	RXP_12	**102**	RXP_15	**128**	DVSS	**154**	TXP_23	**180**	POLE	**206**	TXP_0
25	TXN_4	**51**	TXP_8	**77**	RXN_12	**103**	RXN_15	**129**	RXP_19	**155**	TXN_23	**181**	LNKE	**207**	TXN_0
26	DVSS	**52**	TXN_8	**78**	DVSS	**104**	AVSS	**130**	RXN_19	**156**	DVDD	**182**	DVDD	**208**	DVDD

7. SIGNAL DESCRIPTION

The interface signals of ACD81024 can be divided into four groups. The description of all kinds of signals in each group are shown below:

Table 7.1 - 10Base-T Interface Group:

Mnemonic	TYPE	I/O	Active	Description
TXP_0 ~ TXP_23	DIFF	O		Ethernet 10Base-T twisted pair Transmit Output Positive
TXN_0 ~ TXN_23	DIFF	O		Ethernet 10Base-T twisted pair Transmit Output Negative
RXP_0 ~ RXP_23	DIFF	I		Ethernet 10Base-T twisted pair Receive Input Positive
RXN_0 ~ RXN_23	DIFF	I		Ethernet 10Base-T twisted pair Receive Input Negative

Table 7.2 - Configuration Interface Group

Mnemonic	TYPE	I/O	Active	Description
LNKE	CMOS	I	HIGH	Link integrity detection function enable
POLE	CMOS	I	HIGH	Automatic polarity detection and correction function enable
SQLE	CMOS	I	HIGH	Smart squelch intelligence function enable
DMPE	CMOS	I	HIGH	Periodic dumping function enable
WDGE	CMOS	I	HIGH	Transmit Time Watchdog function enable

Table 7.3 - LED Interface Group

Mnemonic	TYPE	I/O	Active	Description
LNK	CMOS	O	HIGH	Link status indication signal
XMT	CMOS	O	HIGH	Transmit indication signal
RCV	CMOS	O	HIGH	Receive indication signal
COL	CMOS	O	HIGH	Collision indication signal
BSY	CMOS	O	HIGH	Congestion control indication signal
JBR	CMOS	O	HIGH	Jabber error indication signal
ADDR	CMOS	O	HIGH	Port address learned status indication signal
FBE	CMOS	O	HIGH	Frame bit error (FCS error or alignment error) indication signal
LEDVLD	CMOS	O	HIGH	LED valid signal
LEDCLK	CMOS	O		LED clock signal

Table 7.4 - Misc. Signal Group

Mnemonic	TYPE	I/O	Active	Description
DVDD		I		+5V power input for digital circuitry
AVDD		I		+5V power input for analog circuitry
DVSS		I		Ground power input for digital circuitry
AVSS		I		Ground power input for analog circuitry
CLK80	CMOS	I		System clock signal from a 80.000Mhz clock oscillator
RESETN	CMOS	I	LOW	System Reset Negative, low active

8. SIGNAL WAVEFORMS

8.1 Twisted Pair Receiver

Figure 8.1: Data Receiving With Smart Squelch Intelligent

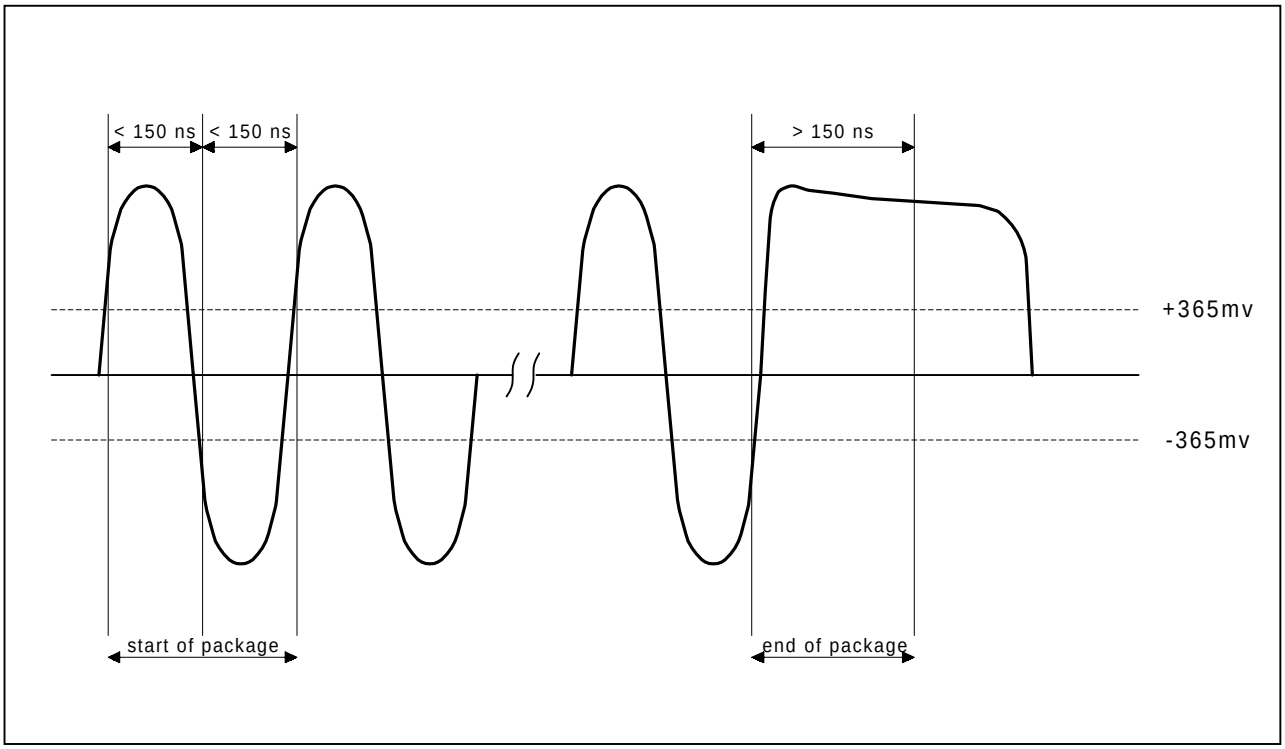
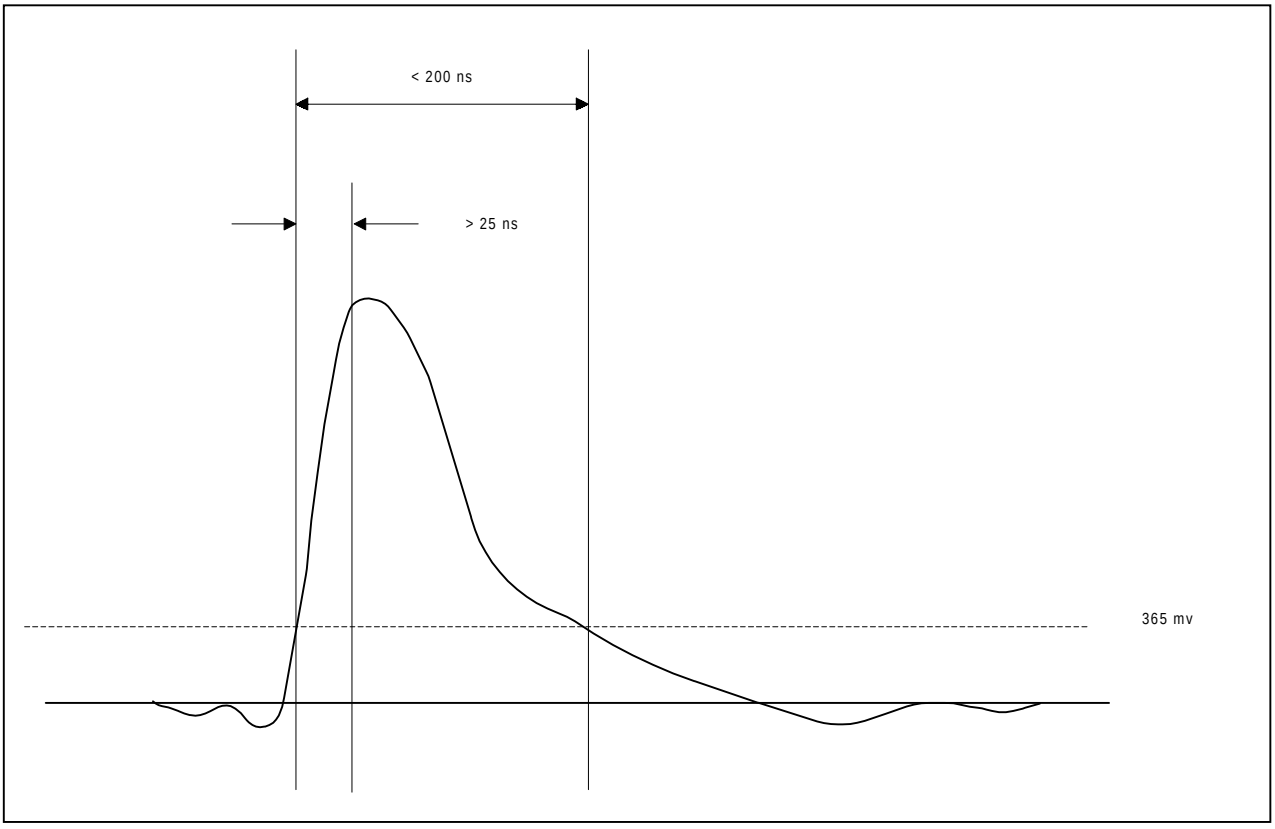


Figure 8.2: Link Pulse Detection



8.2 Twisted Pair Transmitter

Figure 8.3: Preamble Signal Generation

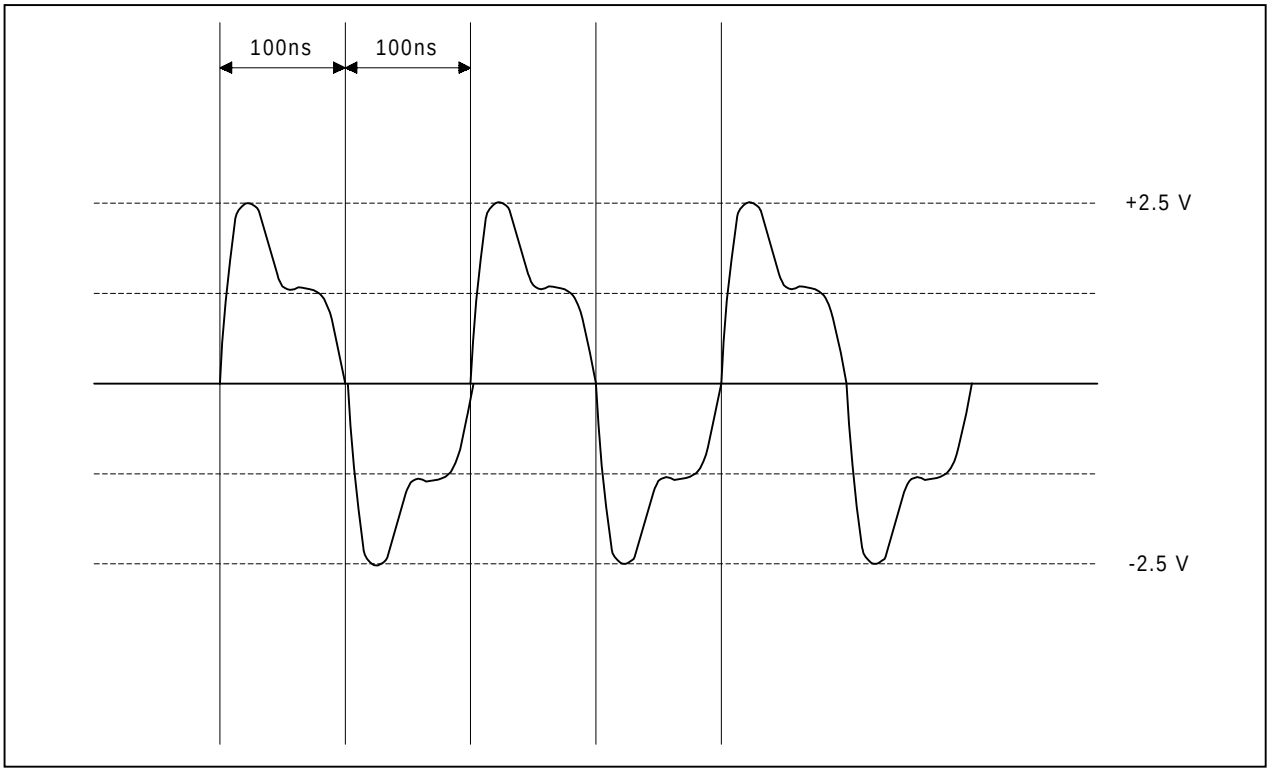
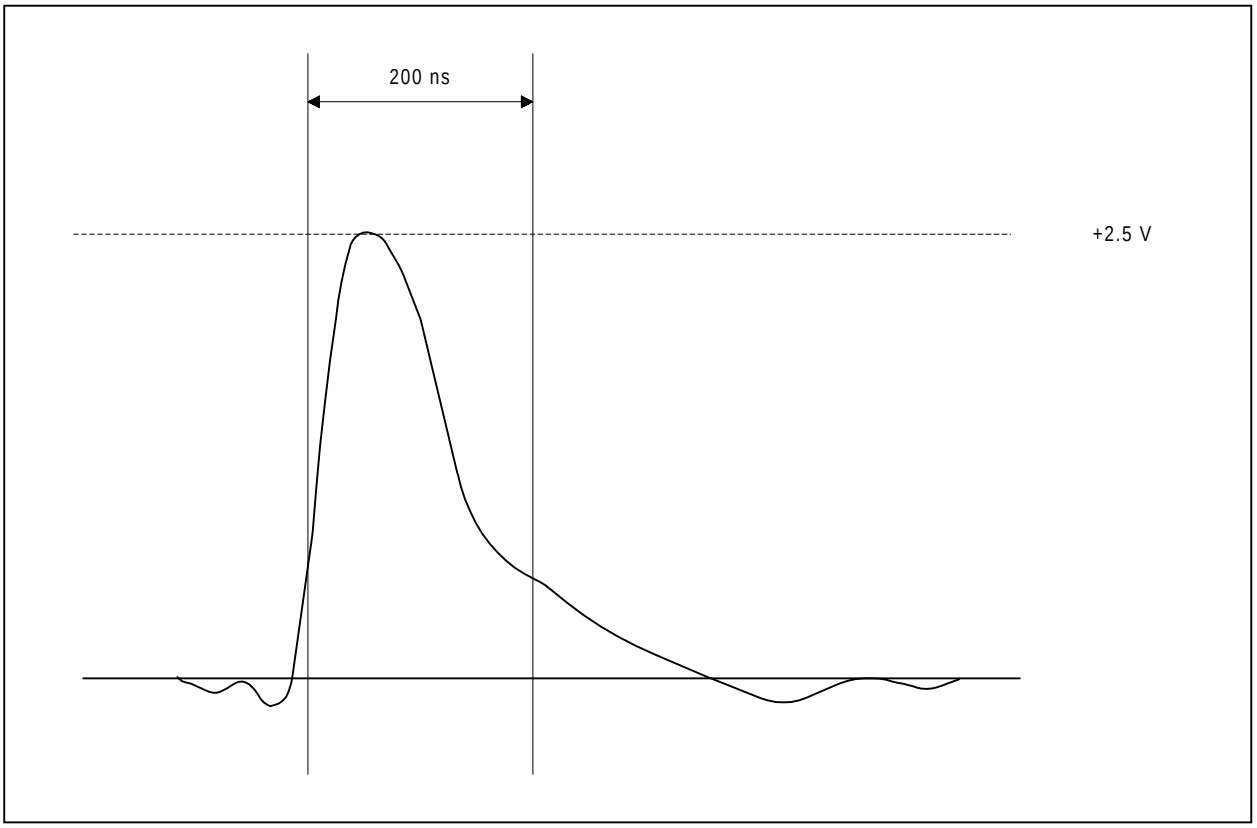


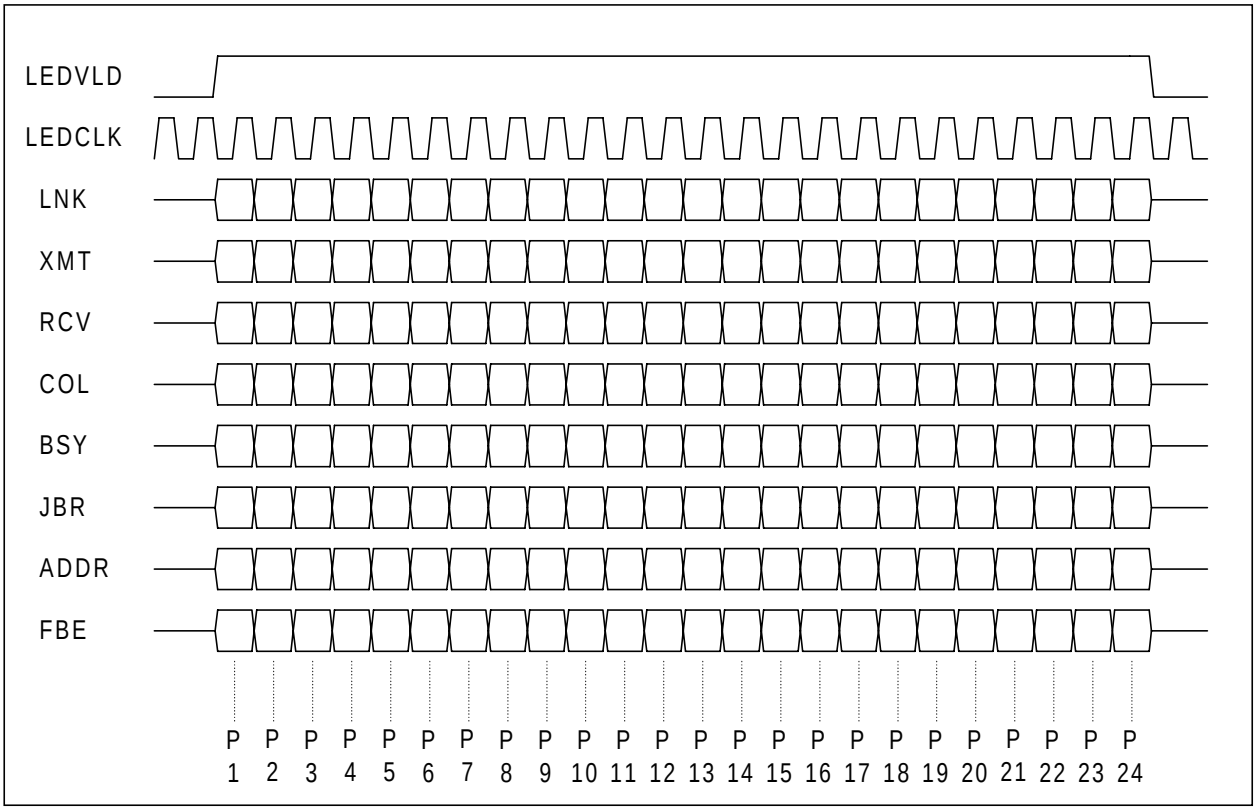
Figure 8.4: End Of Frame Pattern Generation

Figure 8.5: Link Pulse Generation



8.3 LED Data Signal

Figure 8.6: LED Data Signal



9. ELECTRICAL SPECIFICATION

Absolute Maximum Ratings

Operation at absolute maximum ratings is not implied. Exposure to stresses outside those listed could cause permanent damage to the device.

DC Supply voltage *VDD*	0.3V ~ +7.0V
DC input current *Iin*	+/ 10 mA
DC input voltage *Vin*	0.3 ~ VDD + 0.3V
DC output voltage *Vout*	0.3 ~ VDD + 0.3V
Storage temperature *Tstg*	40 to +125oC

Recommended Operation Conditions

Supply voltage *VDD*	5V, +/-5%
Operating temperature *Ta*	0oC ~ 85 oC
Power dissipation *Pd*	4W (typ.)

10. PACKAGING