

SPN1443

DESCRIPTION

The SPN1443 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

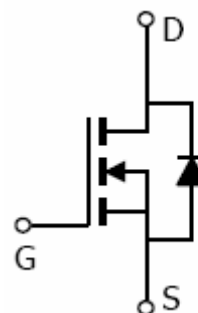
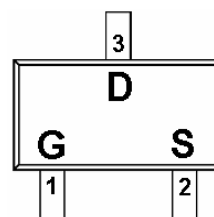
FEATURES

- ◆ 30V/2.8A, $R_{DS(ON)} = 65m\Omega @ V_{GS} = 10V$
- ◆ 30V/2.3A, $R_{DS(ON)} = 90m\Omega @ V_{GS} = 4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-323 (SC-70) package design

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION (SOT-323 ; SC-70)



PART MARKING



SPN1443

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN1443S32RG	SOT-323	43YW

※ Week Code : A ~ Z (1 ~ 26) ; a ~ z (27 ~ 52)

※ SPN1443S32RG : Tape Reel ; Pb – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	30	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	I _D	T _A =25°C	2.8
		T _A =70°C	2.3
Pulsed Drain Current	I _{DM}	10	A
Continuous Source Current(Diode Conduction)	I _S	1.25	A
Power Dissipation	P _D	T _A =25°C	0.33
		T _A =70°C	0.21
Operating Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	100	°C/W

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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		3.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=1.0V$			1	uA
		$V_{DS}=30V, V_{GS}=0.0V$ $T_J=55^\circ C$			10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 4.5V, V_{GS}=10V$	6			A
		$V_{DS} \geq 4.5V, V_{GS}=4.5V$	4			
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D=2.8A$		0.050	0.065	Ω
		$V_{GS} = 4.5V, I_D=2.3A$		0.075	0.090	
Forward Transconductance	g_{fs}	$V_{DS}=4.5V, I_D=2.8A$		4.6		S
Diode Forward Voltage	V_{SD}	$I_S=1.25A, V_{GS}=0V$		0.82	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, V_{GS}=10V$ $I_D=2.5$		4.5	10	nC
Gate-Source Charge	Q_{gs}			0.8		
Gate-Drain Charge	Q_{gd}			1.0		
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V$ $f=1MHz$		240		pF
Output Capacitance	C_{oss}			110		
Reverse Transfer Capacitance	C_{rss}			17		
Turn-On Time	$t_{d(on)}$	$V_{DD}=15V, R_L=15$ $I_D=1.0A, V_{GEN}=10$ $R_G=6\Omega$		8	20	ns
	t_r			12	30	
Turn-Off Time	$t_{d(off)}$			17	35	
	t_f			8	20	