

M5M51008P, FP-70, -85, -10, -12, -70L, -85L, -10L, -12L, -70LL, -85LL, -10LL, -12LL

1048576-BIT(131072-WORD BY 8-BIT) CMOS STATIC RAM

MITSUBISHI (MEMORY/ASIC)

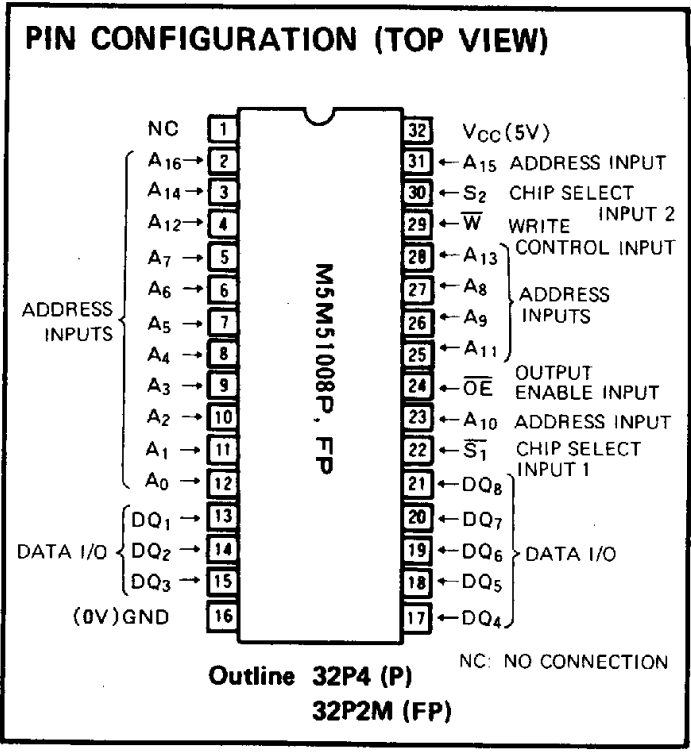
DESCRIPTION

The M5M51008P, FP are 1,048,576-bit CMOS static RAM organized as 131,072 word by 8-bit which are fabricated using high-performance triple polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high density and low power static RAM. They are ideal for the memory systems which require simple interface. The stand-by current is low enough for a battery back-up application. They are mounted in a standard 32 pin package and configured in an industrial standard 128K x 8-bit pinout.

FEATURE

TYPE	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51008P, FP-70	70ns	30mA (1MHz)	2mA
M5M51008P, FP-85	85ns		
M5M51008P, FP-10	100ns		
M5M51008P, FP-12	120ns		
M5M51008P, FP-70L	70ns	30mA (1MHz)	100µA
M5M51008P, FP-85L	85ns		(V _{CC} = 5.5V)
M5M51008P, FP-10L	100ns		50µA
M5M51008P, FP-12L	120ns		(V _{CC} = 3.0V)
M5M51008P, FP-70LL	70ns	30mA (1MHz)	20µA
M5M51008P, FP-85LL	85ns		(V _{CC} = 5.5V)
M5M51008P, FP-10LL	100ns		10µA
M5M51008P, FP-12LL	120ns		(V _{CC} = 3.0V)

- Single +5V power supply
- Easy memory expansion and power down by \overline{S}_1 , S_2
- Data hold on + 2V power supply
- \overline{OE} prevents data contention in the I/O bus
- Low stand-by current 1.0µA (TYP)



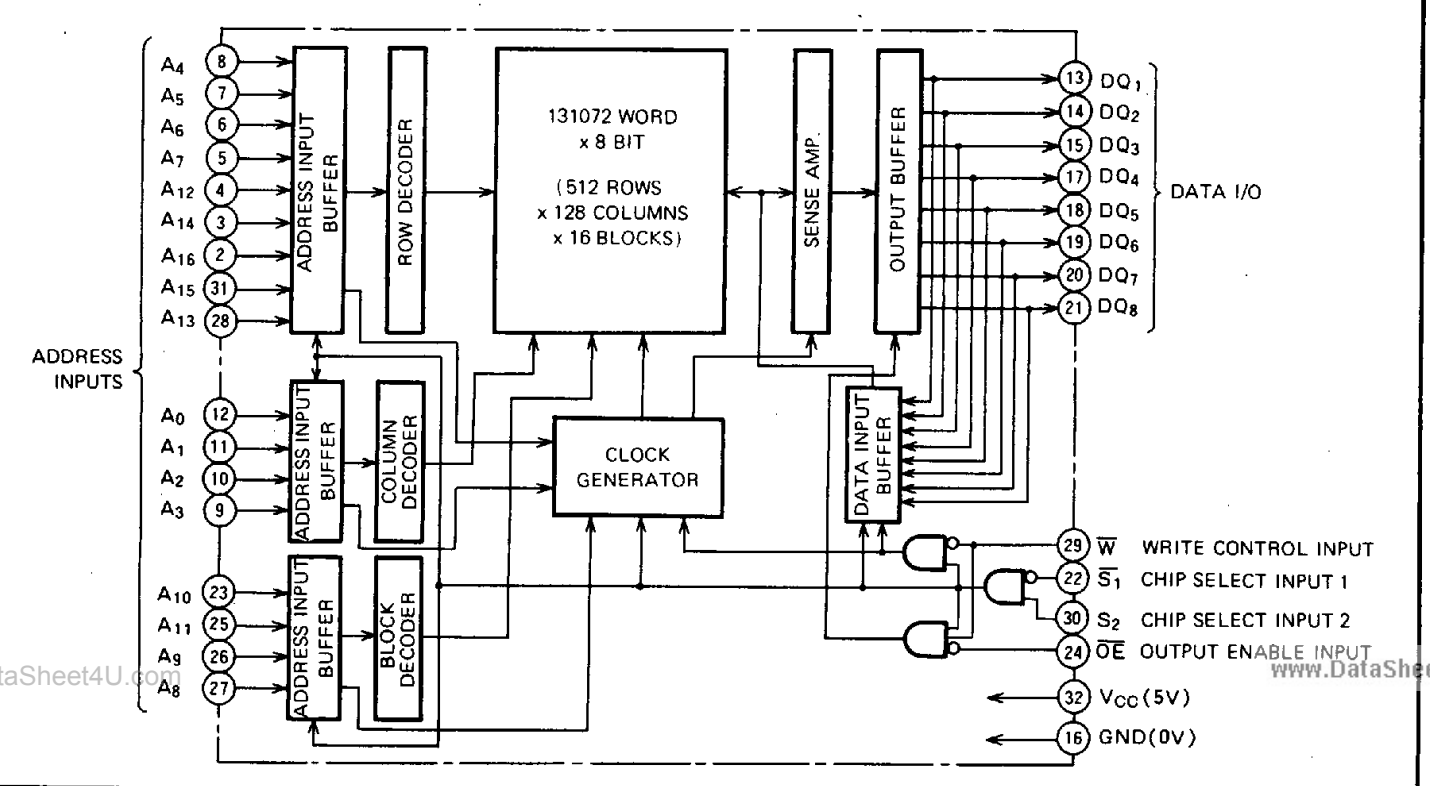
PACKAGE

- M5M51008P 32 pin 600 mil DIP
- M5M51008FP 32 pin 525 mil SOP (small outline package)

APPLICATION

Small capacity memory units.

BLOCK DIAGRAM



FUNCTION

The operation mode of the M5M51008P, FP are determined by a combination of the device control inputs \overline{S}_1 , S_2 , \overline{W} and \overline{OE} . Each mode is summarized in the function table.

A write cycle is executed whenever the low level \overline{W} overlaps with the low level \overline{S}_1 and the high level S_2 . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of \overline{W} , \overline{S}_1 or S_2 , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input \overline{OE} directly controls the output stage. Setting the \overline{OE} at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting \overline{W} at a high level and \overline{OE} at a low level while \overline{S}_1 and S_2 are in an active state ($\overline{S}_1 = L, S_2 = H$).

When setting \overline{S}_1 at a high level or S_2 at a low level, the

chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output state is in a high-impedance state, allowing OR-tie with other chips and memory expansion by \overline{S}_1 and S_2 . The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4} , and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

\overline{S}_1	S_2	\overline{W}	\overline{OE}	Mode	DQ	I_{CC}
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	D_{in}	Active
L	H	H	L	Read	D_{out}	Active
L	H	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V_{CC}	Supply voltage	With respect to GND	-0.3~7	V
V_I	Input voltage		-0.3*~ $V_{CC}+0.3$	V
V_O	Output voltage		0~ V_{CC}	V
P_d	Power dissipation	$T_a = 25^\circ\text{C}$	700	mW
T_{opr}	Operating temperature		0~70	$^\circ\text{C}$
T_{stg}	Storage temperature		-65~150	$^\circ\text{C}$

* -3.0V incase of AC (Pulse width $\leq 50\text{ns}$)

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DC ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Units	
			Min	Typ	Max		
V_{IH}	High-level input voltage		2.2		$V_{CC}+0.3$	V	
V_{IL}	Low-level input voltage		-0.3*		0.8	V	
V_{OH}	High-level output voltage	$I_{OH} = -1\text{mA}$	2.4			V	
		$I_{OH} = -0.1\text{mA}$	$V_{CC}-0.5$			V	
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{mA}$			0.4	V	
I_I	Input leakage current	$V_I = 0 \sim V_{CC}$			± 1	μA	
I_O	Output leakage current	$\overline{S}_1 = V_{IH}$ or $S_2 = V_{IL}$ or $\overline{OE} = V_{IH}$			1	μA	
		$V_{I/O} = 0 \sim V_{CC}$			-1	μA	
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S}_1 \leq 0.2\text{V}$, $S_2 \geq V_{CC}-0.2\text{V}$ other inputs $\leq 0.2\text{V}$ or $\geq V_{CC}-0.2\text{V}$ Output-open (duty 100%)	Min cycle	50	90	mA	
			1MHz	25	30		
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S}_1 = V_{IL}$, $S_2 = V_{IH}$ other inputs = V_{IH} or V_{IL} Output-open (duty 100%)	Min cycle	60	100	mA	
			1MHz	30	40		
I_{CC3}	Stand by current	$S_2 \leq 0.2\text{V}$ or $\overline{S}_1 \geq V_{CC}-0.2\text{V}$, $S_2 \geq V_{CC}-0.2\text{V}$ other inputs = $0 \sim V_{CC}$	P,FP		2	mA	
			P,FP-L		100		μA
			P,FP-LL	1.0			
I_{CC4}	Stand by current	$\overline{S}_1 = V_{IH}$ or $S_2 = V_{IL}$ other inputs = $0 \sim V_{CC}$			3	mA	

* -3.0V incase of AC (Pulse width $\leq 50\text{ns}$)

CAPACITANCE ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted)

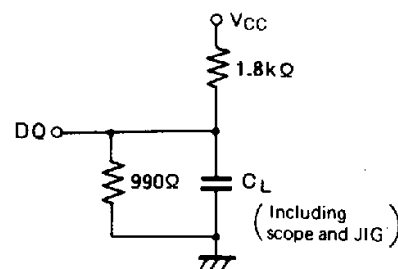
Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
C_I	Input capacitance	$V_I = \text{GND}$, $V_I = 25\text{mVrms}$, $f = 1\text{MHz}$			6	pF
C_O	Output capacitance	$V_O = \text{GND}$, $V_O = 25\text{mVrms}$, $f = 1\text{MHz}$			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark).

2: Typical value is $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$.

AC ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted)**(1) MEASUREMENT CONDITIONS**Input pulse $V_{IH} = 2.4\text{V}$, $V_{IL} = 0.6\text{V}$

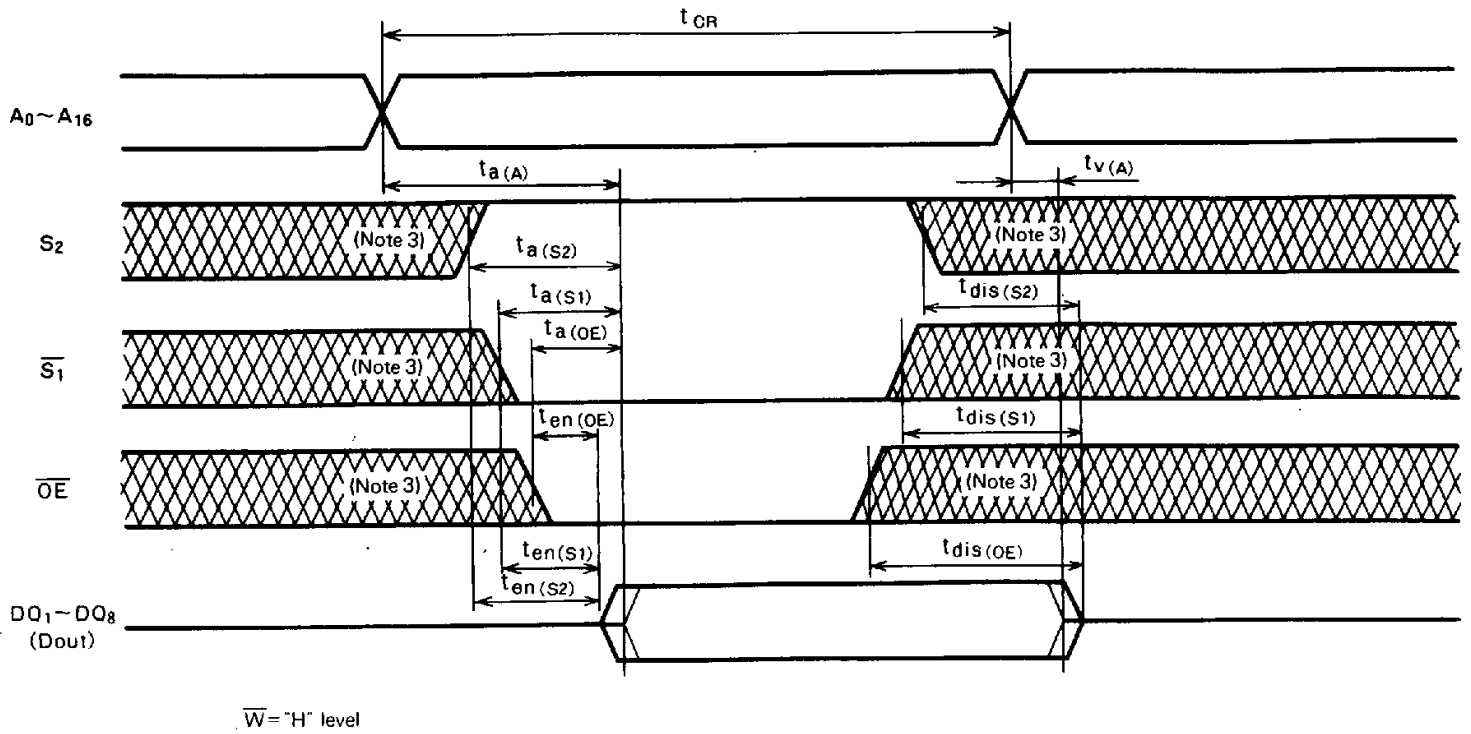
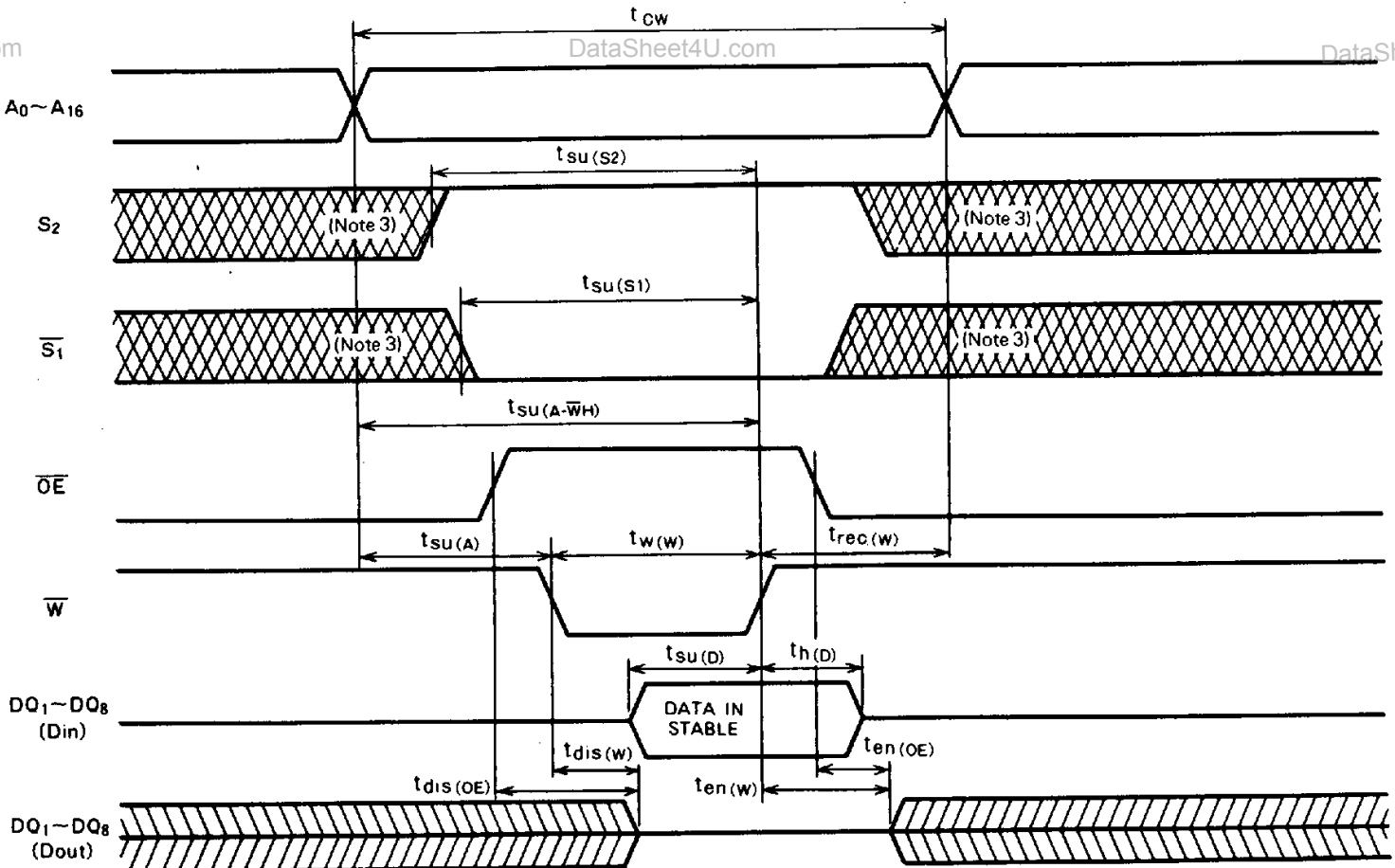
Input rise and fall time 5ns

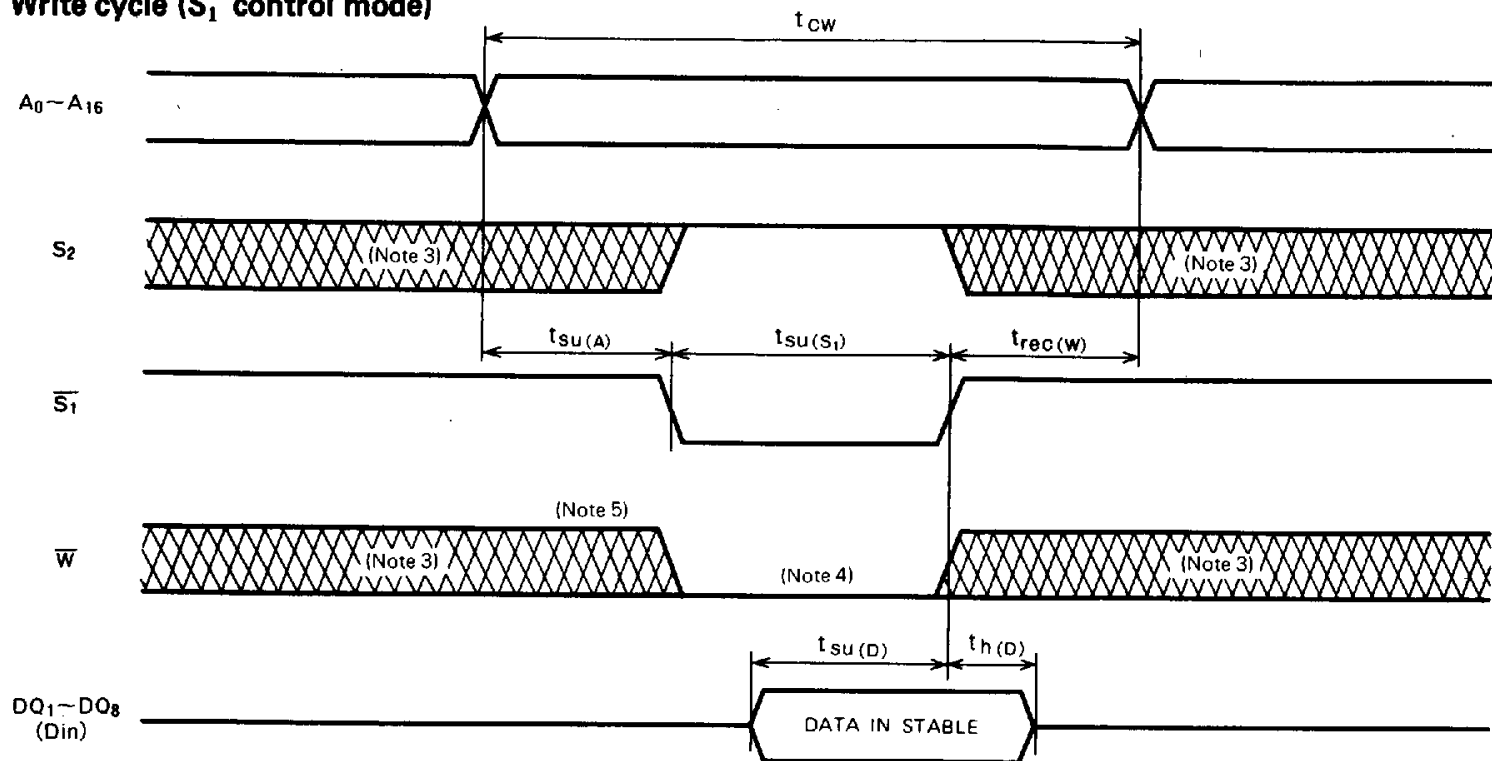
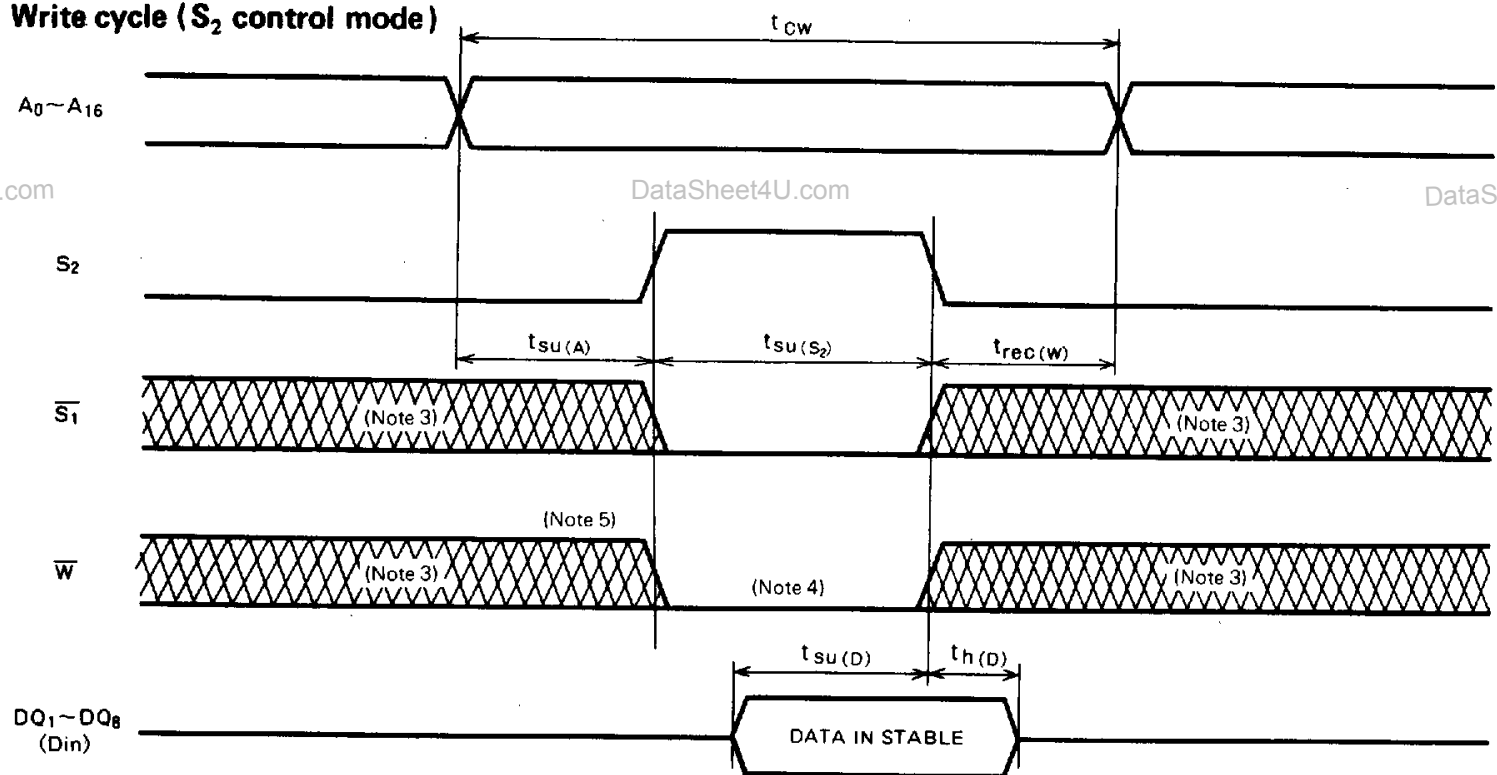
Reference level $V_{OH} = V_{OL} = 1.5\text{V}$ Transition is measured $\pm 500\text{mV}$ from steady state voltage. (for t_{on} , t_{dis})Output loads Fig. 1, $C_L = 100\text{pF}$ (P, FP-85, -10, -12, -85L, -10L, -12L, -85LL, -10LL, -12LL) $C_L = 30\text{pF}$ (P, FP-70, -70L, -70LL) $C_L = 5\text{pF}$ (for t_{on} , t_{dis})**Fig. 1 Output load****(2) READ CYCLE**

Symbol	Parameter	M5M51008P, FP								Units
		-70, -70L, -70LL		-85, -85L, -85LL		-10, -10L, -10LL		-12, -12L, -12LL		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	70		85		100		120		ns
$t_a(A)$	Address access time		70		85		100		120	ns
$t_a(S1)$	Chip select 1 access time		70		85		100		120	ns
$t_a(S2)$	Chip select 2 access time		70		85		100		120	ns
$t_a(OE)$	Output enable access time		35		45		50		60	ns
$t_{dis}(S1)$	Output disable time after $\overline{S_1}$ high		25		30		35		40	ns
$t_{dis}(S2)$	Output disable time after $\overline{S_2}$ low		25		30		35		40	ns
$t_{dis}(OE)$	Output disable time after \overline{OE} high		25		30		35		40	ns
$t_{en}(S1)$	Output enable time after $\overline{S_1}$ low	5		5		5		5		ns
$t_{en}(S2)$	Output enable time after $\overline{S_2}$ high	5		5		5		5		ns
$t_{en}(OE)$	Output enable time after \overline{OE} low	5		5		5		5		ns
$t_v(A)$	Data valid time after address	10		10		10		10		ns

(3) WRITE CYCLE

Symbol	Parameter	M5M51008P, FP								Units
		-70, -70L, -70LL		-85, -85L, -85LL		-10, -10L, -10LL		-12, -12L, -12LL		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	70		85		100		120		ns
$t_w(W)$	Write pulse width	55		65		75		85		ns
$t_{su}(A)$	Address set up time	0		0		0		0		ns
$t_{su}(A-WH)$	Address set up time with respect to \overline{W} high	65		75		85		100		ns
$t_{su}(S1)$	Chip select 1 set up time	65		75		85		100		ns
$t_{su}(S2)$	Chip select 2 set up time	65		75		85		100		ns
$t_{su}(D)$	Data set up time	30		35		40		45		ns
$t_h(D)$	Data hold time	0		0		0		0		ns
$t_{rec}(W)$	Write recovery time	0		0		0		0		ns
$t_{dis}(W)$	Output disable time from \overline{W} low		25		30		35		40	ns
$t_{dis}(OE)$	Output disable time from \overline{OE} high		25		30		35		40	ns
$t_{en}(W)$	Output enable time from \overline{W} high	5		5		5		5		ns
$t_{en}(OE)$	Output enable time from \overline{OE} low	5		5		5		5		ns

(4) TIMING DIAGRAMS**Read cycle****Write cycle (\overline{W} control mode)**

Write cycle (\overline{S}_1 control mode)Write cycle (S_2 control mode)

Note 3: Hatching indicates the state is 'don't care'.

4: Writing is executed while S_2 high overlaps \overline{S}_1 and \overline{W} low.

5: When the falling edge of \overline{W} is simultaneously or prior to the falling edge of \overline{S}_1 or rising edge of S_2 , the outputs are maintained in the high impedance state.

6: Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2			V
$V_I(\overline{S}_1)$	Chip select input \overline{S}_1	$2.2\text{V} \leq V_{CC(PD)}$	2.2			V
		$2\text{V} \leq V_{CC(PD)} \leq 2.2\text{V}$		$V_{CC(PD)}$		
$V_I(\hat{S}_2)$	Chip select input S_2	$4.5\text{V} \leq V_{CC(PD)}$			0.8	V
		$V_{CC(PD)} < 4.5\text{V}$			0.2	
$I_{CC(PD)}$	Power down supply current	$V_{CC} = 3\text{V}$ $S_2 \leq 0.2\text{V}$ or $\overline{S}_1 \geq V_{CC} - 0.2\text{V}$, $S_2 \geq V_{CC} - 0.2\text{V}$	P, FP		2	mA
			P, FP-L		50	μA
			P, FP-LL		10 note 7	μA

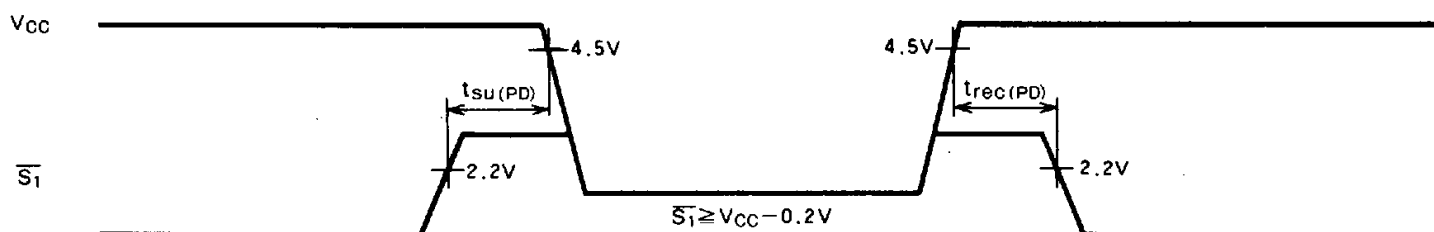
Note 7: $I_{CC(PD)} = 1\mu\text{A}$ in case of $T_a = 25^\circ\text{C}$ TIMING REQUIREMENTS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms

POWER DOWN CHARACTERISTICS

 \overline{S}_1 control mode

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 S_2 control mode