APPLICATION NOTE

(DOC No. HX8312-A-AN)

HX8312-A

240RGB x 320 dot,
262,144-Color TFT Controller
Driver with Internal RAM

Preliminary version 02 October, 2005

Himax Technologies, Inc.
http://www.himax.com.tw

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1. Introduction

This application note describes the Himax's HX8312-A mobile driver application that include hardware and software design. The HX8312-A is designed to provide a single-chip solution that combined a gate driver, a source driver, power supply circuit and internal graphics RAM for 262,144 colors to drive a TFT panel with 240RGB*320 dots at maximum.

2. Features

- Single chip solution to drive a TFT panel
- 240RGB x 320-dot graphics display LCD controller/driver and 262,144 TFT colors
- Support interface:
  - System interface
    (I80 / M68) parallel bus system interface
    Serial bus system interface
  - RGB interface
  - VSYNC interface
- Internal graphics RAM capacity: 1,328,400 bytes
- The 262,144 colors can be displayed at the same time with gamma correction
- The vertical scroll display function in line units
- Internal operation circuit of liquid crystal display:
  - Source channel: 720
  - Gate line: 320
- To write data in a window-RAM address area by using a window address area access function
- Low-power consumption architecture supports:
  - VCI = 2.5 to 3.3 V (internal reference voltage)
  - VCC = 2.2 to 3.3 V (corresponding low-voltage operation)
  - IOVCC = 1.65 to 3.3 V (Interface I/O operation)
  - VLCD=4.5~5.5V
  - Power-saving functions
    - 8-color mode
    - standby mode
    - Off mode
- N-line inversion AC liquid-crystal drive
- Partial liquid crystal drive to display two screens at arbitrary positions
- Internal oscillator and hardware / software reset function

3. Block Diagram

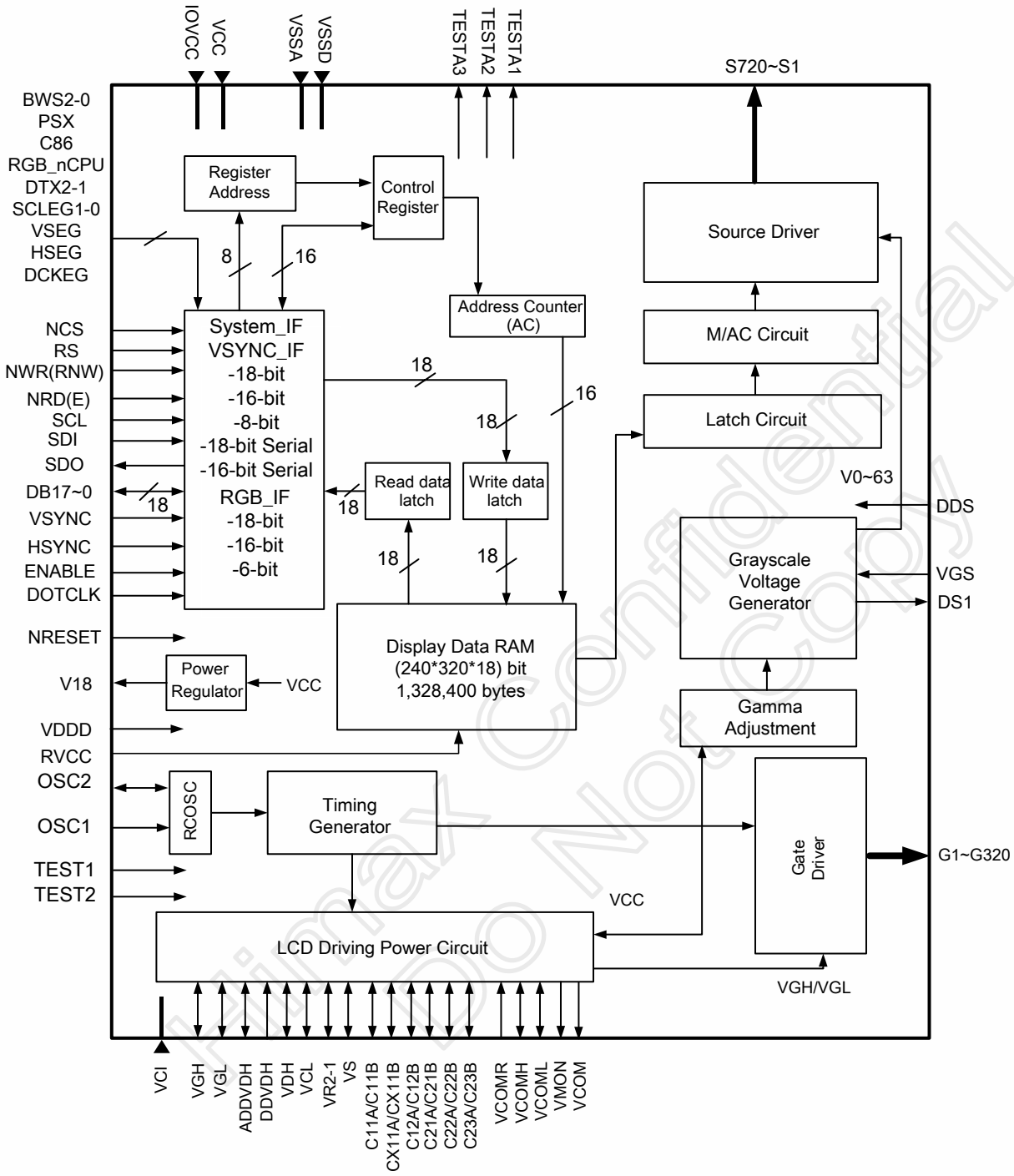


Figure 3. 1 Chip Block Diagram

4. PAD Assignment

PAD Coordinate

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	DUMMY1	-11928	-547.5	62	DUMMY16	-10285	-701.5	123	IOVCCDUM7	-5100	-701.5	184	SCL	85	-701.5
2	DUMMY2	-11904	-702.5	63	VCOM1	-10200	-701.5	124	BWS2	-5015	-701.5	185	SCL	170	-701.5
3	DUMMY3	-11880	-547.5	64	VCOM1	-10115	-701.5	125	IOGNDDUM7	-4930	-701.5	186	NCS	255	-701.5
4	DUMMY4	-11856	-702.5	65	DS1	-10030	-701.5	126	RGBNCPU	-4845	-701.5	187	NCS	340	-701.5
5	DUMMY5	-11832	-547.5	66	VGH	-9945	-701.5	127	IOVCCDUM8	-4760	-701.5	188	CSTB	425	-701.5
6	DUMMY6	-11808	-702.5	67	VGH	-9860	-701.5	128	NRESET	-4675	-701.5	189	CSTB	510	-701.5
7	DUMMY7	-11784	-547.5	68	VGH	-9775	-701.5	129	NRESET	-4590	-701.5	190	TEST1	595	-701.5
8	DUMMY8	-11760	-702.5	69	VGH	-9690	-701.5	130	VSYNC	-4505	-701.5	191	IOGNDDUM8	680	-701.5
9	DUMMY9	-11736	-547.5	70	C23A	-9605	-701.5	131	VSYNC	-4420	-701.5	192	TEST2	765	-701.5
10	DUMMY10	-11712	-702.5	71	C23A	-9520	-701.5	132	HSYNC	-4335	-701.5	193	IOGNDDUM9	850	-701.5
11	DUMMY11	-11688	-547.5	72	C23B	-9435	-701.5	133	HXYNC	-4250	-701.5	194	VDDD	935	-701.5
12	DUMMY12	-11664	-702.5	73	C23B	-9350	-701.5	134	DOTCLK	-4165	-701.5	195	VDDD	1020	-701.5
13	THROUGH1	-11640	-547.5	74	C22A	-9265	-701.5	135	DOTCLK	-4080	-701.5	196	VDDD	1105	-701.5
14	THROUGH2	-11616	-702.5	75	C22A	-9180	-701.5	136	ENABLE	-3995	-701.5	197	VDDD	1190	-701.5
15	G278	-11592	-547.5	76	C22B	-9095	-701.5	137	ENABLE	-3910	-701.5	198	RVCC	1275	-701.5
16	G279	-11568	-702.5	77	C22B	-9010	-701.5	138	DB17	-3825	-701.5	199	RVCC	1360	-701.5
17	G280	-11544	-547.5	78	C21A	-8925	-701.5	139	DB17	-3740	-701.5	200	RVCC	1445	-701.5
18	G281	-11520	-702.5	79	C21A	-8840	-701.5	140	DB16	-3655	-701.5	201	RVCC	1530	-701.5
19	G282	-11496	-547.5	80	C21B	-8755	-701.5	141	DB16	-3570	-701.5	202	V18	1615	-701.5
20	G283	-11472	-702.5	81	C21B	-8670	-701.5	142	DB15	-3485	-701.5	203	V18	1700	-701.5
21	G284	-11448	-547.5	82	C12A	-8585	-701.5	143	DB15	-3400	-701.5	204	V18	1785	-701.5
22	G285	-11424	-702.5	83	C12A	-8500	-701.5	144	DB14	-3315	-701.5	205	V18	1870	-701.5
23	G286	-11400	-547.5	84	C12A	-8415	-701.5	145	DB14	-3230	-701.5	206	DUMMYR1	1955	-701.5
24	G287	-11376	-702.5	85	C12A	-8330	-701.5	146	DB13	-3145	-701.5	207	DUMMYR2	2040	-701.5
25	G288	-11352	-547.5	86	C12B	-8245	-701.5	147	DB13	-3060	-701.5	208	OSC1	2125	-701.5
26	G289	-11328	-702.5	87	C12B	-8160	-701.5	148	DB12	-2975	-701.5	209	OSC1	2210	-701.5
27	G290	-11304	-547.5	88	C12B	-8075	-701.5	149	DB12	-2890	-701.5	210	OSC2	2295	-701.5
28	G291	-11280	-702.5	89	C12B	-7990	-701.5	150	DB11	-2805	-701.5	211	OSC2	2380	-701.5
29	G292	-11256	-547.5	90	VR2	-7905	-701.5	151	DB11	-2720	-701.5	212	VSSD	2465	-701.5
30	G293	-11232	-702.5	91	VR2	-7820	-701.5	152	DB10	-2635	-701.5	213	VSSD	2550	-701.5
31	G294	-11208	-547.5	92	VR2	-7735	-701.5	153	DB10	-2550	-701.5	214	VSSD	2635	-701.5
32	G295	-11184	-702.5	93	VR2	-7650	-701.5	154	DB9	-2465	-701.5	215	VSSD	2720	-701.5
33	G296	-11160	-547.5	94	VGL	-7565	-701.5	155	DB9	-2380	-701.5	216	VSSD2	2805	-701.5
34	G297	-11136	-702.5	95	VGL	-7480	-701.5	156	DB8	-2295	-701.5	217	VSSD2	2890	-701.5
35	G298	-11112	-547.5	96	VGL	-7395	-701.5	157	DB8	-2210	-701.5	218	VSSD2	2975	-701.5
36	G299	-11088	-702.5	97	VGL	-7310	-701.5	158	DB7	-2125	-701.5	219	VSSD2	3060	-701.5
37	G300	-11064	-547.5	98	VGL	-7225	-701.5	159	DB7	-2040	-701.5	220	VSSA	3145	-701.5
38	G301	-11040	-702.5	99	IOVCCDUM1	-7140	-701.5	160	DB6	-1955	-701.5	221	VSSA	3230	-701.5
39	G302	-11016	-547.5	100	DDS	-7055	-701.5	161	DB6	-1870	-701.5	222	VSSA	3315	-701.5
40	G303	-10992	-702.5	101	IOGNDDUM1	-6970	-701.5	162	DB5	-1785	-701.5	223	VSSA	3400	-701.5
41	G304	-10968	-547.5	102	SCLEG1	-6885	-701.5	163	DB5	-1700	-701.5	224	VSSA	3485	-701.5
42	G305	-10944	-702.5	103	IOVCCDUM2	-6800	-701.5	164	DB4	-1615	-701.5	225	VSSA	3570	-701.5
43	G306	-10920	-547.5	104	SCLEG0	-6715	-701.5	165	DB4	-1530	-701.5	226	IOVCC	3655	-701.5
44	G307	-10896	-702.5	105	IOGNDDUM2	-6630	-701.5	166	DB3	-1445	-701.5	227	IOVCC	3740	-701.5
45	G308	-10872	-547.5	106	HSEG	-6545	-701.5	167	DB3	-1360	-701.5	228	IOVCC	3825	-701.5
46	G309	-10848	-702.5	107	IOVCCDUM3	-6460	-701.5	168	DB2	-1275	-701.5	229	IOVCC	3910	-701.5
47	G310	-10824	-547.5	108	VSEG	-6375	-701.5	169	DB2	-1190	-701.5	230	VCI	3995	-701.5
48	G311	-10800	-702.5	109	IOGNDDUM3	-6290	-701.5	170	DB1	-1105	-701.5	231	VCI	4080	-701.5
49	G312	-10776	-547.5	110	DCKEG	-6205	-701.5	171	DB1	-1020	-701.5	232	VCI	4165	-701.5
50	G313	-10752	-702.5	111	IOVCCDUM4	-6120	-701.5	172	DB0	-935	-701.5	233	VCI	4250	-701.5
51	G314	-10728	-547.5	112	PSX	-6035	-701.5	173	DB0	-850	-701.5	234	VCI	4335	-701.5
52	G315	-10704	-702.5	113	IOGNDDUM4	-5950	-701.5	174	NRD(E)	-765	-701.5	235	VCI	4420	-701.5
53	G316	-10680	-547.5	114	C86	-5865	-701.5	175	NRD(E)	-680	-701.5	236	VCC	4505	-701.5
54	G317	-10656	-702.5	115	IOVCCDUM5	-5780	-701.5	176	NWR(RNW)	-595	-701.5	237	VCC	4590	-701.5
55	G318	-10632	-547.5	116	DTX1	-5695	-701.5	177	NWR(RNW)	-510	-701.5	238	VCC	4675	-701.5
56	G319	-10608	-702.5	117	IOGNDDUM5	-5610	-701.5	178	RS	-425	-701.5	239	VCC	4760	-701.5
57	G320	-10584	-547.5	118	DTX2	-5525	-701.5	179	RS	-340	-701.5	240	VGS	4845	-701.5
58	G321	-10560	-702.5	119	IOVCCDUM6	-5440	-701.5	180	SDO	-255	-701.5	241	VGS	4930	-701.5
59	DUMMY13	-10536	-547.5	120	BWS0	-5355	-701.5	181	SDO	-170	-701.5	242	VCOMR	5015	-701.5
60	DUMMY14	-10512	-702.5	121	IOGNDDUM6	-5270	-701.5	182	SDI	-85	-701.5	243	VCOMR	5100	-701.5
61	VMON	-10488	-547.5	122	BWS1	-5185	-701.5	183	SDI	0	-701.5	244	VS	5185	-701.5

No.	Pad name	X	Y
245	VS	5270	-701.5
246	VS	5355	-701.5
247	VS	5440	-701.5
248	VCOML	5525	-701.5
249	VCOML	5610	-701.5
250	VCOML	5695	-701.5
251	VCOML	5780	-701.5
252	VCOMH	5865	-701.5
253	VCOMH	5950	-701.5
254	VCOMH	6035	-701.5
255	VCOMH	6120	-701.5
256	VCL	6205	-701.5
257	VCL	6290	-701.5
258	VCL	6375	-701.5
259	VCL	6460	-701.5
260	TESTA1	6545	-701.5
261	TESTA1	6630	-701.5
262	VR1	6715	-701.5
263	VR1	6800	-701.5
264	VR1	6885	-701.5
265	VR1	6970	-701.5
266	ADDVDH	7055	-701.5
267	ADDVDH	7140	-701.5
268	ADDVDH	7225	-701.5
269	ADDVDH	7310	-701.5
270	DDVDH	7395	-701.5
271	DDVDH	7480	-701.5
272	DDVDH	7565	-701.5
273	DDVDH	7650	-701.5
274	CX11B	7735	-701.5
275	CX11B	7820	-701.5
276	CX11B	7905	-701.5
277	CX11B	7990	-701.5
278	CX11B	8075	-701.5
279	CX11B	8160	-701.5
280	CX11A	8245	-701.5
281	CX11A	8330	-701.5
282	CX11A	8415	-701.5
283	CX11A	8500	-701.5
284	CX11A	8585	-701.5
285	CX11A	8670	-701.5
286	C11B	8755	-701.5
287	C11B	8840	-701.5
288	C11B	8925	-701.5
289	C11B	9010	-701.5
290	C11B	9095	-701.5
291	C11B	9180	-701.5
292	C11A	9265	-701.5
293	C11A	9350	-701.5
294	C11A	9435	-701.5
295	C11A	9520	-701.5
296	C11A	9605	-701.5
297	C11A	9690	-701.5
298	TESTA2	9775	-701.5
299	DUMMY18	9860	-701.5
300	VCOM2	9945	-701.5
301	VCOM2	10030	-701.5
302	VCOM2	10115	-701.5
303	VCOM2	10200	-701.5
304	TESTA4	10285	-701.5
305	DUMMY20	10488	-547.5
306	DUMMY21	10512	-702.5
307	G1	10536	-547.5
308	G2	10560	-702.5
309	G3	10584	-547.5
310	G4	10608	-702.5
311	G5	10632	-547.5
312	G6	10656	-702.5
313	G7	10680	-547.5
314	G8	10704	-702.5
315	G9	10728	-547.5
316	G10	10752	-702.5
317	G11	10776	-547.5
318	G12	10800	-702.5
319	G13	10824	-547.5
320	G14	10848	-702.5
321	G15	10872	-547.5
322	G16	10896	-702.5
323	G17	10920	-547.5
324	G18	10944	-702.5
325	G19	10968	-547.5
326	G20	10992	-702.5
327	G21	11016	-547.5
328	G22	11040	-702.5
329	G23	11064	-547.5
330	G24	11088	-702.5
331	G25	11112	-547.5
332	G26	11136	-702.5
333	G27	11160	-547.5
334	G28	11184	-702.5
335	G29	11208	-547.5
336	G30	11232	-702.5
337	G31	11256	-547.5
338	G32	11280	-702.5
339	G33	11304	-547.5
340	G34	11328	-702.5
341	G35	11352	-547.5
342	G36	11376	-702.5
343	G37	11400	-547.5
344	G38	11424	-702.5
345	G39	11448	-547.5
346	G40	11472	-702.5
347	G41	11496	-547.5
348	G42	11520	-702.5
349	G43	11544	-547.5
350	G44	11568	-702.5
351	G45	11592	-547.5
352	THROUGH3	11616	-702.5
353	THROUGH4	11640	-547.5
354	DUMMY22	11664	-702.5
355	DUMMY23	11688	-547.5
356	DUMMY24	11712	-702.5
357	DUMMY25	11736	-547.5
358	DUMMY26	11760	-702.5
359	DUMMY27	11784	-547.5
360	DUMMY28	11808	-702.5
361	DUMMY29	11832	-547.5
362	DUMMY30	11856	-702.5
363	DUMMY31	11880	-547.5
364	DUMMY32	11904	-702.5
365	DUMMY33	11928	-547.5
366	DUMMY34	11736	702.5
367	VGLDMY	11712	547.5
368	DUMMY35	11688	702.5
369	DUMMY36	11664	547.5
370	THROUGH5	11640	702.5
371	THROUGH6	11616	547.5
372	G46	11592	702.5
373	G47	11568	547.5
374	G48	11544	702.5
375	G49	11520	547.5
376	G50	11496	702.5
377	G51	11472	547.5
378	G52	11448	702.5
379	G53	11424	547.5
380	G54	11400	702.5
381	G55	11376	547.5
382	G56	11352	702.5
383	G57	11328	547.5
384	G58	11304	702.5
385	G59	11280	547.5
386	G60	11256	702.5
387	G61	11232	547.5
388	G62	11208	702.5
389	G63	11184	547.5
390	G64	11160	702.5
391	G65	11136	547.5
392	G66	11112	702.5
393	G67	11088	547.5
394	G68	11064	702.5
395	G69	11040	547.5
396	G70	11016	702.5
397	G71	10992	547.5
398	G72	10968	702.5
399	G73	10944	547.5
400	G74	10920	702.5
401	G75	10896	547.5
402	G76	10872	702.5
403	G77	10848	547.5
404	G78	10824	702.5
405	G79	10800	547.5
406	G80	10776	702.5
407	G81	10752	547.5
408	G82	10728	702.5
409	G83	10704	547.5
410	G84	10680	702.5
411	G85	10656	547.5
412	G86	10632	702.5
413	G87	10608	547.5
414	G88	10584	702.5
415	G89	10560	547.5
416	G90	10536	702.5
417	G91	10512	547.5
418	G92	10488	702.5
419	G93	10464	547.5
420	G94	10440	702.5
421	G95	10416	547.5
422	G96	10392	702.5
423	G97	10368	547.5
424	G98	10344	702.5
425	G99	10320	547.5
426	G100	10296	702.5
427	G101	10272	547.5
428	G102	10248	702.5
429	G103	10224	547.5
430	G104	10200	702.5
431	G105	10176	547.5
432	G106	10152	702.5
433	G107	10128	547.5
434	G108	10104	702.5
435	G109	10080	547.5
436	G110	10056	702.5
437	G111	10032	547.5
438	G112	10008	702.5
439	G113	9984	547.5
440	G114	9960	702.5
441	G115	9936	547.5
442	G116	9912	702.5
443	G117	9888	547.5
444	G118	9864	702.5
445	G119	9840	547.5
446	G120	9816	702.5
447	G121	9792	547.5
448	G122	9768	702.5
449	G123	9744	547.5
450	G124	9720	702.5
451	G125	9696	547.5
452	G126	9672	702.5
453	G127	9648	547.5
454	G128	9624	702.5
455	G129	9600	547.5
456	G130	9576	702.5
457	G131	9552	547.5
458	G132	9528	702.5
459	G133	9504	547.5
460	G134	9480	702.5
461	G135	9456	547.5
462	G136	9432	702.5
463	G137	9408	547.5
464	G138	9384	702.5
465	G139	9360	547.5
466	G140	9336	702.5
467	G141	9312	547.5
468	G142	9288	702.5
469	G143	9264	547.5
470	G144	9240	702.5
471	G145	9216	547.5
472	G146	9192	702.5
473	G148	9168	547.5
474	G148	9144	702.5
475	G149	9120	547.5
476	G150	9096	702.5
477	G151	9072	547.5
478	G152	9048	702.5
479	G153	9024	547.5
480	G154	9000	702.5
481	G155	8976	547.5
482	G156	8952	702.5
483	G157	8928	547.5
484	G158	8904	702.5
485	G159	8880	547.5
486	G160	8856	702.5
487	G161	8832	547.5
488	DUMMY37	8808	702.5
489	DUMMY38	8784	547.5
490	VCOM3	8760	702.5
491	VCOM3	8736	547.5
492	DUMMY39	8712	702.5
493	DUMMY40	8688	547.5
494	DUMMY41	8664	702.5
495	S720	8640	547.5
496	S719	8616	702.5
497	S718	8592	547.5
498	S717	8568	702.5
499	S716	8544	547.5
500	S715	8520	702.5
501	S714	8496	547.5
502	S713	8472	702.5
503	S712	8448	547.5
504	S711	8424	702.5
505	S710	8400	547.5
506	S709	8376	702.5
507	S708	8352	547.5
508	S707	8328	702.5
509	S706	8304	547.5
510	S705	8280	702.5
511	S704	8256	547.5
512	S703	8232	702.5
513	S702	8208	547.5
514	S701	8184	702.5
515	S700	8160	547.5
516	S699	8136	702.5
517	S698	8112	547.5
518	S697	8088	702.5
519	S696	8064	547.5
520	S695	8040	702.5

No.	Pad name	X	Y
521	S694	8016	547.5
522	S693	7992	702.5
523	S692	7968	547.5
524	S691	7944	702.5
525	S690	7920	547.5
526	S689	7896	702.5
527	S688	7872	547.5
528	S687	7848	702.5
529	S686	7824	547.5
530	S685	7800	702.5
531	S684	7776	547.5
532	S683	7752	702.5
533	S682	7728	547.5
534	S681	7704	702.5
535	S680	7680	547.5
536	S679	7656	702.5
537	S678	7632	547.5
538	S677	7608	702.5
539	S676	7584	547.5
540	S675	7560	702.5
541	S674	7536	547.5
542	S673	7512	702.5
543	S672	7488	547.5
544	S671	7464	702.5
545	S670	7440	547.5
546	S669	7416	702.5
547	S668	7392	547.5
548	S667	7368	702.5
549	S666	7344	547.5
550	S665	7320	702.5
551	S664	7296	547.5
552	S663	7272	702.5
553	S662	7248	547.5
554	S661	7224	702.5
555	S660	7200	547.5
556	S659	7176	702.5
557	S658	7152	547.5
558	S657	7128	702.5
559	S656	7104	547.5
560	S655	7080	702.5
561	S654	7056	547.5
562	S653	7032	702.5
563	S652	7008	547.5
564	S651	6984	702.5
565	S650	6960	547.5
566	S649	6936	702.5
567	S648	6912	547.5
568	S647	6888	702.5
569	S646	6864	547.5
570	S645	6840	702.5
571	S644	6816	547.5
572	S643	6792	702.5
573	S642	6768	547.5
574	S641	6744	702.5
575	S640	6720	547.5
576	S639	6696	702.5
577	S638	6672	547.5
578	S637	6648	702.5
579	S636	6624	547.5
580	S635	6600	702.5
581	S634	6576	547.5
582	S633	6552	702.5
583	S632	6528	547.5
584	S631	6504	702.5
585	S630	6480	547.5
586	S629	6456	702.5
587	S628	6432	547.5
588	S627	6408	702.5
589	S626	6384	547.5
590	S625	6360	702.5
591	S624	6336	547.5
592	S623	6312	702.5
593	S622	6288	547.5
594	S621	6264	702.5
595	S620	6240	547.5
596	S619	6216	702.5
597	S618	6192	547.5
598	S617	6168	702.5
599	S616	6144	547.5
600	S615	6120	702.5
601	S614	6096	547.5
602	S613	6072	702.5
603	S612	6048	547.5
604	S611	6024	702.5
605	S610	6000	547.5
606	S609	5976	702.5
607	S608	5952	547.5
608	S607	5928	702.5
609	S606	5904	547.5
610	S605	5880	702.5
611	S604	5856	547.5
612	S603	5832	702.5
613	S602	5808	547.5
614	S601	5784	702.5
615	S600	5760	547.5
616	S599	5736	702.5
617	S598	5712	547.5
618	S597	5688	702.5
619	S596	5664	547.5
620	S595	5640	702.5
621	S594	5616	547.5
622	S593	5592	702.5
623	S592	5568	547.5
624	S591	5544	702.5
625	S590	5520	547.5
626	S589	5496	702.5
627	S588	5472	547.5
628	S587	5448	702.5
629	S586	5424	547.5
630	S585	5400	702.5
631	S584	5376	547.5
632	S583	5352	702.5
633	S582	5328	547.5
634	S581	5304	702.5
635	S580	5280	547.5
636	S579	5256	702.5
637	S578	5232	547.5
638	S577	5208	702.5
639	S576	5184	547.5
640	S575	5160	702.5
641	S574	5136	547.5
642	S573	5112	702.5
643	S572	5088	547.5
644	S571	5064	702.5
645	S570	5040	547.5
646	S569	5016	702.5
647	S568	4992	547.5
648	S567	4968	702.5
649	S566	4944	547.5
650	S565	4920	702.5
651	S564	4896	547.5
652	S563	4872	702.5
653	S562	4848	547.5
654	S561	4824	702.5
655	S560	4800	547.5
656	S559	4776	702.5
657	S558	4752	547.5
658	S557	4728	702.5
659	S556	4704	547.5
660	S555	4680	702.5
661	S554	4656	547.5
662	S553	4632	702.5
663	S552	4608	547.5
664	S551	4584	702.5
665	S550	4560	547.5
666	S549	4536	702.5
667	S548	4512	547.5
668	S547	4488	702.5
669	S546	4464	547.5
670	S545	4440	702.5
671	S544	4416	547.5
672	S543	4392	702.5
673	S542	4368	547.5
674	S541	4344	702.5
675	S540	4320	547.5
676	S539	4296	702.5
677	S538	4272	547.5
678	S537	4248	702.5
679	S536	4224	547.5
680	S535	4200	702.5
681	S534	4176	547.5
682	S533	4152	702.5
683	S532	4128	547.5
684	S531	4104	702.5
685	S530	4080	547.5
686	S529	4056	702.5
687	S528	4032	547.5
688	S527	4008	702.5
689	S526	3984	547.5
690	S525	3960	702.5
691	S524	3936	547.5
692	S523	3912	702.5
693	S522	3888	547.5
694	S521	3864	702.5
695	S520	3840	547.5
696	S519	3816	702.5
697	S518	3792	547.5
698	S517	3768	702.5
699	S516	3744	547.5
700	S515	3720	702.5
701	S514	3696	547.5
702	S513	3672	702.5
703	S512	3648	547.5
704	S511	3624	702.5
705	S510	3600	547.5
706	S509	3576	702.5
707	S508	3552	547.5
708	S507	3528	702.5
709	S506	3504	547.5
710	S505	3480	702.5
711	S504	3456	547.5
712	S503	3432	702.5
713	S502	3408	547.5
714	S501	3384	702.5
715	S500	3360	547.5
716	S499	3336	702.5
717	S498	3312	547.5
718	S497	3288	702.5
719	S496	3264	547.5
720	S495	3240	702.5
721	S494	3216	547.5
722	S493	3192	702.5
723	S492	3168	547.5
724	S491	3144	702.5
725	S490	3120	547.5
726	S489	3096	702.5
727	S488	3072	547.5
728	S487	3048	702.5
729	S486	3024	547.5
730	S485	3000	702.5
731	S484	2976	547.5
732	S483	2952	702.5
733	S482	2928	547.5
734	S481	2904	702.5
735	S480	2880	547.5
736	S479	2856	702.5
737	S478	2832	547.5
738	S477	2808	702.5
739	S476	2784	547.5
740	S475	2760	702.5
741	S474	2736	547.5
742	S473	2712	702.5
743	S472	2688	547.5
744	S471	2664	702.5
745	S470	2640	547.5
746	S469	2616	702.5
747	S468	2592	547.5
748	S467	2568	702.5
749	S466	2544	547.5
750	S465	2520	702.5
751	S464	2496	547.5
752	S463	2472	702.5
753	S462	2448	547.5
754	S461	2424	702.5
755	S460	2400	547.5
756	S459	2376	702.5
757	S458	2352	547.5
758	S457	2328	702.5
759	S456	2304	547.5
760	S455	2280	702.5
761	S454	2256	547.5
762	S453	2232	702.5
763	S452	2208	547.5
764	S451	2184	702.5
765	S450	2160	547.5
766	S449	2136	702.5
767	S448	2112	547.5
768	S447	2088	702.5
769	S446	2064	547.5
770	S445	2040	702.5
771	S444	2016	547.5
772	S443	1992	702.5
773	S442	1968	547.5
774	S441	1944	702.5
775	S440	1920	547.5
776	S439	1896	702.5
777	S438	1872	547.5
778	S437	1848	702.5
779	S436	1824	547.5
780	S435	1800	702.5

No.	Pad name	X	Y
781	S434	1776	547.5
782	S433	1752	702.5
783	S432	1728	547.5
784	S431	1704	702.5
785	S430	1680	547.5
786	S429	1656	702.5
787	S428	1632	547.5
788	S427	1608	702.5
789	S426	1584	547.5
790	S425	1560	702.5
791	S424	1536	547.5
792	S423	1512	702.5
793	S422	1488	547.5
794	S421	1464	702.5
795	S420	1440	547.5
796	S419	1416	702.5
797	S418	1392	547.5
798	S417	1368	702.5
799	S416	1344	547.5
800	S415	1320	702.5
801	S414	1296	547.5
802	S413	1272	702.5
803	S412	1248	547.5
804	S411	1224	702.5
805	S410	1200	547.5
806	S409	1176	702.5
807	S408	1152	547.5
808	S407	1128	702.5
809	S406	1104	547.5
810	S405	1080	702.5
811	S404	1056	547.5
812	S403	1032	702.5
813	S402	1008	547.5
814	S401	984	702.5
815	S400	960	547.5
816	S399	936	702.5
817	S398	912	547.5
818	S397	888	702.5
819	S396	864	547.5
820	S395	840	702.5
821	S394	816	547.5
822	S393	792	702.5
823	S392	768	547.5
824	S391	744	702.5
825	S390	720	547.5
826	S389	696	702.5
827	S388	672	547.5
828	S387	648	702.5
829	S386	624	547.5
830	S385	600	702.5
831	S384	576	547.5
832	S383	552	702.5
833	S382	528	547.5
834	S381	504	702.5
835	S380	480	547.5
836	S379	456	702.5
837	S378	432	547.5
838	S377	408	702.5
839	S376	384	547.5
840	S375	360	702.5
841	S374	336	547.5
842	S373	312	702.5
843	S372	288	547.5
844	S371	264	702.5
845	S370	240	547.5

No.	Pad name	X	Y
846	S369	216	702.5
847	S368	192	547.5
848	S367	168	702.5
849	S366	144	547.5
850	S365	120	702.5
851	S364	96	547.5
852	S363	72	702.5
853	S362	48	547.5
854	S361	24	702.5
855	DUMMY42	0	547.5
856	S360	-24	702.5
857	S359	-48	547.5
858	S358	-72	702.5
859	S357	-96	547.5
860	S356	-120	702.5
861	S355	-144	547.5
862	S354	-168	702.5
863	S353	-192	547.5
864	S352	-216	702.5
865	S351	-240	547.5
866	S350	-264	702.5
867	S349	-288	547.5
868	S348	-312	702.5
869	S347	-336	547.5
870	S346	-360	702.5
871	S345	-384	547.5
872	S344	-408	702.5
873	S343	-432	547.5
874	S342	-456	702.5
875	S341	-480	547.5
876	S340	-504	702.5
877	S339	-528	547.5
878	S338	-552	702.5
879	S337	-576	547.5
880	S336	-600	702.5
881	S335	-624	547.5
882	S334	-648	702.5
883	S333	-672	547.5
884	S332	-696	702.5
885	S331	-720	547.5
886	S330	-744	702.5
887	S329	-768	547.5
888	S328	-792	702.5
889	S327	-816	547.5
890	S326	-840	702.5
891	S325	-864	547.5
892	S224	-888	702.5
893	S223	-912	547.5
894	S322	-936	702.5
895	S321	-960	547.5
896	S320	-984	702.5
897	S319	-1008	547.5
898	S318	-1032	702.5
899	S317	-1056	547.5
900	S316	-1080	702.5
901	S315	-1104	547.5
902	S314	-1128	702.5
903	S313	-1152	547.5
904	S312	-1176	702.5
905	S311	-1200	547.5
906	S310	-1224	702.5
907	S309	-1248	547.5
908	S308	-1272	702.5
909	S307	-1296	547.5
910	S306	-1320	702.5

No.	Pad name	X	Y
911	S305	-1344	547.5
912	S304	-1368	702.5
913	S303	-1392	547.5
914	S302	-1416	702.5
915	S301	-1440	547.5
916	S300	-1464	702.5
917	S299	-1488	547.5
918	S298	-1512	702.5
919	S297	-1536	547.5
920	S296	-1560	702.5
921	S295	-1584	547.5
922	S294	-1608	702.5
923	S293	-1632	547.5
924	S292	-1656	702.5
925	S291	-1680	547.5
926	S290	-1704	702.5
927	S289	-1728	547.5
928	S288	-1752	702.5
929	S287	-1776	547.5
930	S286	-1800	702.5
931	S285	-1824	547.5
932	S284	-1848	702.5
933	S283	-1872	547.5
934	S282	-1896	702.5
935	S281	-1920	547.5
936	S280	-1944	702.5
937	S279	-1968	547.5
938	S278	-1992	702.5
939	S277	-2016	547.5
940	S276	-2040	702.5
941	S275	-2064	547.5
942	S274	-2088	702.5
943	S273	-2112	547.5
944	S272	-2136	702.5
945	S271	-2160	547.5
946	S270	-2184	702.5
947	S269	-2208	547.5
948	S268	-2232	702.5
949	S267	-2256	547.5
950	S266	-2280	702.5
951	S265	-2304	547.5
952	S264	-2328	702.5
953	S263	-2352	547.5
954	S262	-2376	702.5
955	S261	-2400	547.5
956	S260	-2424	702.5
957	S259	-2448	547.5
958	S258	-2472	702.5
959	S257	-2496	547.5
960	S256	-2520	702.5
961	S255	-2544	547.5
962	S254	-2568	702.5
963	S253	-2592	547.5
964	S252	-2616	702.5
965	S251	-2640	547.5
966	S250	-2664	702.5
967	S249	-2688	547.5
968	S248	-2712	702.5
969	S247	-2736	547.5
970	S246	-2760	702.5
971	S245	-2784	547.5
972	S244	-2808	702.5
973	S243	-2832	547.5
974	S242	-2856	702.5
975	S241	-2880	547.5

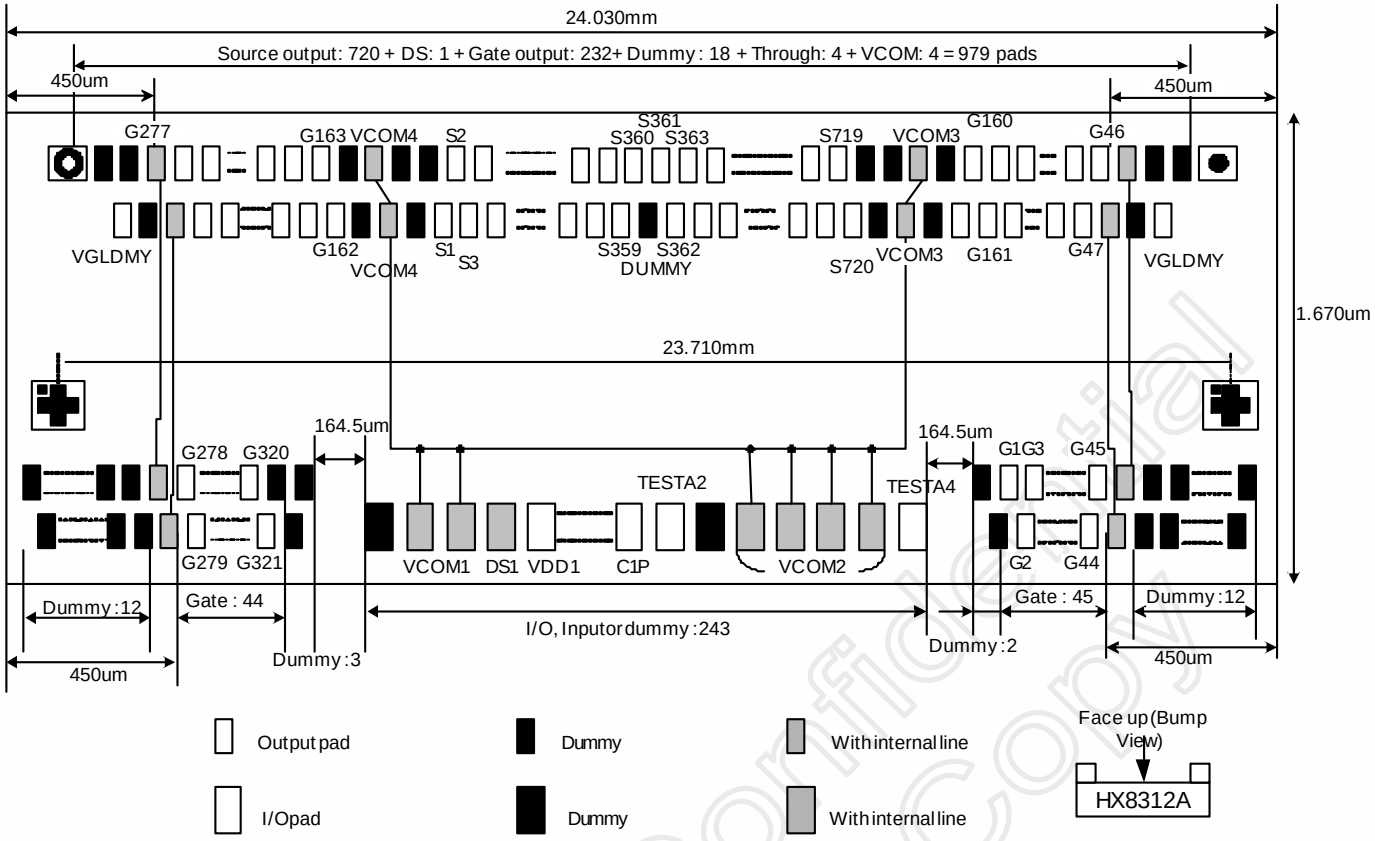
No.	Pad name	X	Y
976	S240	-2904	702.5
977	S239	-2928	547.5
978	S238	-2952	702.5
979	S237	-2976	547.5
980	S236	-3000	702.5
981	S235	-3024	547.5
982	S234	-3048	702.5
983	S233	-3072	547.5
984	S232	-3096	702.5
985	S231	-3120	547.5
986	S230	-3144	702.5
987	S229	-3168	547.5
988	S228	-3192	702.5
989	S227	-3216	547.5
990	S226	-3240	702.5
991	S225	-3264	547.5
992	S224	-3288	702.5
993	S223	-3312	547.5
994	S222	-3336	702.5
995	S221	-3360	547.5
996	S220	-3384	702.5
997	S219	-3408	547.5
998	S218	-3432	702.5
999	S217	-3456	547.5
1000	S216	-3480	702.5
1001	S215	-3504	547.5
1002	S214	-3528	702.5
1003	S213	-3552	547.5
1004	S212	-3576	702.5
1005	S211	-3600	547.5
1006	S210	-3624	702.5
1007	S209	-3648	547.5
1008	S208	-3672	702.5
1009	S207	-3696	547.5
1010	S206	-3720	702.5
1011	S205	-3744	547.5
1012	S204	-3768	702.5
1013	S203	-3792	547.5
1014	S202	-3816	702.5
1015	S201	-3840	547.5
1016	S200	-3864	702.5
1017	S199	-3888	547.5
1018	S198	-3912	702.5
1019	S197	-3936	547.5
1020	S196	-3960	702.5
1021	S195	-3984	547.5
1022	S194	-4008	702.5
1023	S193	-4032	547.5
1024	S192	-4056	702.5
1025	S191	-4080	547.5
1026	S190	-4104	702.5
1027	S189	-4128	547.5
1028	S188	-4152	702.5
1029	S187	-4176	547.5
1030	S186	-4200	702.5
1031	S185	-4224	547.5
1032	S184	-4248	702.5
1033	S183	-4272	547.5
1034	S182	-4296	702.5
1035	S181	-4320	547.5
1036	S180	-4344	702.5
1037	S179	-4368	547.5
1038	S178	-4392	702.5
1039	S177	-4416	547.5
1040	S176	-4440	702.5

No.	Pad name	X	Y
1041	S175	-4464	547.5
1042	S174	-4488	702.5
1043	S173	-4512	547.5
1044	S172	-4536	702.5
1045	S171	-4560	547.5
1046	S170	-4584	702.5
1047	S169	-4608	547.5
1048	S168	-4632	702.5
1049	S167	-4656	547.5
1050	S166	-4680	702.5
1051	S165	-4704	547.5
1052	S164	-4728	702.5
1053	S163	-4752	547.5
1054	S162	-4776	702.5
1055	S161	-4800	547.5
1056	S160	-4824	702.5
1057	S159	-4848	547.5
1058	S158	-4872	702.5
1059	S157	-4896	547.5
1060	S156	-4920	702.5
1061	S155	-4944	547.5
1062	S154	-4968	702.5
1063	S153	-4992	547.5
1064	S152	-5016	702.5
1065	S151	-5040	547.5
1066	S150	-5064	702.5
1067	S149	-5088	547.5
1068	S148	-5112	702.5
1069	S147	-5136	547.5
1070	S146	-5160	702.5
1071	S145	-5184	547.5
1072	S144	-5208	702.5
1073	S143	-5232	547.5
1074	S142	-5256	702.5
1075	S141	-5280	547.5
1076	S140	-5304	702.5
1077	S139	-5328	547.5
1078	S138	-5352	702.5
1079	S137	-5376	547.5
1080	S136	-5400	702.5
1081	S135	-5424	547.5
1082	S134	-5448	702.5
1083	S133	-5472	547.5
1084	S132	-5496	702.5
1085	S131	-5520	547.5
1086	S130	-5544	702.5
1087	S129	-5568	547.5
1088	S128	-5592	702.5
1089	S127	-5616	547.5
1090	S126	-5640	702.5
1091	S125	-5664	547.5
1092	S124	-5688	702.5
1093	S123	-5712	547.5
1094	S122	-5736	702.5
1095	S121	-5760	547.5
1096	S120	-5784	702.5
1097	S119	-5808	547.5
1098	S118	-5832	702.5
1099	S117	-5856	547.5
1100	S116	-5880	702.5
1101	S115	-5904	547.5
1102	S114	-5928	702.5
1103	S113	-5952	547.5
1104	S112	-5976	702.5
1105	S111	-6000	547.5
1106	S110	-6024	702.5
1107	S109	-6048	547.5
1108	S108	-6072	702.5
1109	S107	-6096	547.5
1110	S106	-6120	702.5
1111	S105	-6144	547.5
1112	S104	-6168	702.5
1113	S103	-6192	547.5
1114	S102	-6216	702.5
1115	S101	-6240	547.5
1116	S100	-6264	702.5
1117	S99	-6288	547.5
1118	S98	-6312	702.5
1119	S97	-6336	547.5
1120	S96	-6360	702.5
1121	S95	-6384	547.5
1122	S94	-6408	702.5
1123	S93	-6432	547.5
1124	S92	-6456	702.5
1125	S91	-6480	547.5
1126	S90	-6504	702.5
1127	S89	-6528	547.5
1128	S88	-6552	702.5
1129	S87	-6576	547.5
1130	S86	-6600	702.5
1131	S85	-6624	547.5
1132	S84	-6648	702.5
1133	S83	-6672	547.5
1134	S82	-6696	702.5
1135	S81	-6720	547.5
1136	S80	-6744	702.5
1137	S79	-6768	547.5
1138	S78	-6792	702.5
1139	S77	-6816	547.5
1140	S76	-6840	702.5
1141	S75	-6864	547.5
1142	S74	-6888	702.5
1143	S73	-6912	547.5
1144	S72	-6936	702.5
1145	S71	-6960	547.5
1146	S70	-6984	702.5
1147	S69	-7008	547.5
1148	S68	-7032	702.5
1149	S67	-7056	547.5
1150	S66	-7080	702.5
1151	S65	-7104	547.5
1152	S64	-7128	702.5
1153	S63	-7152	547.5
1154	S62	-7176	702.5
1155	S61	-7200	547.5
1156	S60	-7224	702.5
1157	S59	-7248	547.5
1158	S58	-7272	702.5
1159	S57	-7296	547.5
1160	S56	-7320	702.5
1161	S55	-7344	547.5
1162	S54	-7368	702.5
1163	S53	-7392	547.5
1164	S52	-7416	702.5
1165	S51	-7440	547.5
1166	S50	-7464	702.5
1167	S49	-7488	547.5
1168	S48	-7512	702.5
1169	S47	-7536	547.5
1170	S46	-7560	702.5
1171	S45	-7584	547.5
1172	S44	-7608	702.5
1173	S43	-7632	547.5
1174	S42	-7656	702.5
1175	S41	-7680	547.5
1176	S40	-7704	702.5
1177	S39	-7728	547.5
1178	S38	-7752	702.5
1179	S37	-7776	547.5
1180	S36	-7800	702.5
1181	S35	-7824	547.5
1182	S34	-7848	702.5
1183	S33	-7872	547.5
1184	S32	-7896	702.5
1185	S31	-7920	547.5
1186	S30	-7944	702.5
1187	S29	-7968	547.5
1188	S28	-7992	702.5
1189	S27	-8016	547.5
1190	S26	-8040	702.5
1191	S25	-8064	547.5
1192	S24	-8088	702.5
1193	S23	-8112	547.5
1194	S22	-8136	702.5
1195	S21	-8160	547.5
1196	S20	-8184	702.5
1197	S19	-8208	547.5
1198	S18	-8232	702.5
1199	S17	-8256	547.5
1200	S16	-8280	702.5
1201	S15	-8304	547.5
1202	S14	-8328	702.5
1203	S13	-8352	547.5
1204	S12	-8376	702.5
1205	S11	-8400	547.5
1206	S10	-8424	702.5
1207	S9	-8448	547.5
1208	S8	-8472	702.5
1209	S7	-8496	547.5
1210	S6	-8520	702.5
1211	S5	-8544	547.5
1212	S4	-8568	702.5
1213	S3	-8592	547.5
1214	S2	-8616	702.5
1215	S1	-8640	547.5
1216	DUMMY43	-8664	702.5
1217	DUMMY44	-8688	547.5
1218	DUMMY45	-8712	702.5
1219	VCOM4	-8736	547.5
1220	VCOM4	-8760	702.5
1221	DUMMY46	-8784	547.5
1222	DUMMY47	-8808	702.5
1223	G162	-8832	547.5
1224	G163	-8856	702.5
1225	G164	-8880	547.5
1226	G165	-8904	702.5
1227	G166	-8928	547.5
1228	G167	-8952	702.5
1229	G168	-8976	547.5
1230	G169	-9000	702.5
1231	G170	-9024	547.5
1232	G171	-9048	702.5
1233	G172	-9072	547.5
1234	G173	-9096	702.5
1235	G174	-9120	547.5
1236	G175	-9144	702.5
1237	G176	-9168	547.5
1238	G177	-9192	702.5
1239	G178	-9216	547.5
1240	G179	-9240	702.5
1241	G180	-9264	547.5
1242	G181	-9288	702.5
1243	G182	-9312	547.5
1244	G183	-9336	702.5
1245	G184	-9360	547.5
1246	G185	-9384	702.5
1247	G186	-9408	547.5
1248	G187	-9432	702.5
1249	G188	-9456	547.5
1250	G189	-9480	702.5
1251	G190	-9504	547.5
1252	G191	-9528	702.5
1253	G192	-9552	547.5
1254	G193	-9576	702.5
1255	G194	-9600	547.5
1256	G195	-9624	702.5
1257	G196	-9648	547.5
1258	G197	-9672	702.5
1259	G198	-9696	547.5
1260	G199	-9720	702.5
1261	G200	-9744	547.5
1262	G201	-9768	702.5
1263	G202	-9792	547.5
1264	G203	-9816	702.5
1265	G204	-9840	547.5
1266	G205	-9864	702.5
1267	G206	-9888	547.5
1268	G207	-9912	702.5
1269	G208	-9936	547.5
1270	G209	-9960	702.5
1271	G210	-9984	547.5
1272	G211	-10008	702.5
1273	G212	-10032	547.5
1274	G213	-10056	702.5
1275	G214	-10080	547.5
1276	G215	-10104	702.5
1277	G216	-10128	547.5
1278	G217	-10152	702.5
1279	G218	-10176	547.5
1280	G219	-10200	702.5
1281	G220	-10224	547.5
1282	G221	-10248	702.5
1283	G222	-10272	547.5
1284	G223	-10296	702.5
1285	G224	-10320	547.5
1286	G225	-10344	702.5
1287	G226	-10368	547.5
1288	G227	-10392	702.5
1289	G228	-10416	547.5
1290	G229	-10440	702.5
1291	G230	-10464	547.5
1292	G231	-10488	702.5
1293	G232	-10512	547.5
1294	G233	-10536	702.5
1295	G234	-10560	547.5
1296	G235	-10584	702.5
1297	G236	-10608	547.5
1298	G237	-10632	702.5
1299	G238	-10656	547.5
1300	G239	-10680	702.5

No.	Pad name	X	Y
1301	G240	-10704	547.5
1302	G241	-10728	702.5
1303	G242	-10752	547.5
1304	G243	-10776	702.5
1305	G244	-10800	547.5
1306	G245	-10824	702.5
1307	G246	-10848	547.5
1308	G247	-10872	702.5
1309	G248	-10896	547.5
1310	G249	-10920	702.5
1311	G250	-10944	547.5
1312	G251	-10968	702.5
1313	G252	-10992	547.5
1314	G253	-11016	702.5
1315	G254	-11040	547.5
1316	G255	-11064	702.5
1317	G256	-11088	547.5
1318	G257	-11112	702.5
1319	G258	-11136	547.5
1320	G259	-11160	702.5
1321	G260	-11184	547.5
1322	G261	-11208	702.5
1323	G262	-11232	547.5
1324	G263	-11256	702.5
1325	G264	-11280	547.5
1326	G265	-11304	702.5
1327	G266	-11328	547.5
1328	G267	-11352	702.5
1329	G268	-11376	547.5
1330	G269	-11400	702.5
1331	G270	-11424	547.5
1332	G271	-11448	702.5
1333	G272	-11472	547.5
1334	G273	-11496	702.5
1335	G274	-11520	547.5
1336	G275	-11544	702.5
1337	G276	-11568	547.5
1338	G277	-11592	702.5
1339	THROUGH7	-11616	547.5
1340	THROUGH8	-11640	702.5
1341	DUMMY48	-11664	547.5
1342	DUMMY49	-11688	702.5
1343	VGLDMY	-11712	547.5
1344	DUMMY50	-11736	702.5

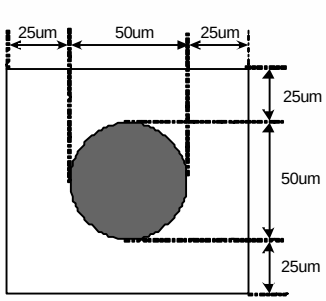
Alignment mark	X	Y
(1-a)	-11855	-394.5
(1-b)	11855	-394.5
(2-a)	-11802	715.5
(2-b)	11802	715.5

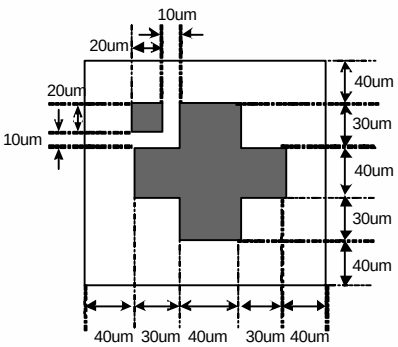
Bump Arrangement

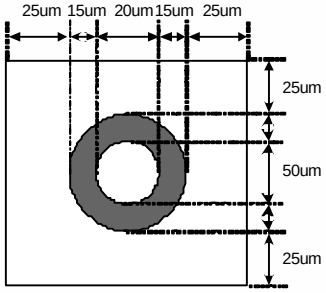


Note: There is no gold bumper on DUMMY 7,9,11, 23, 25, 27 pins.

Alignment Mark

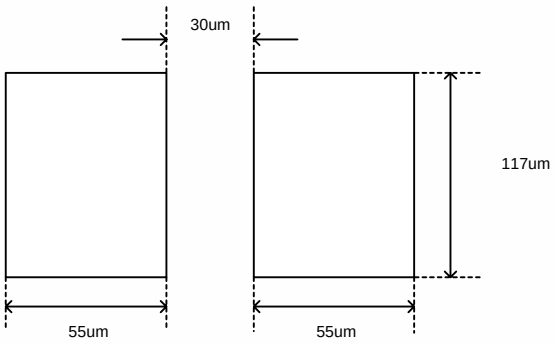




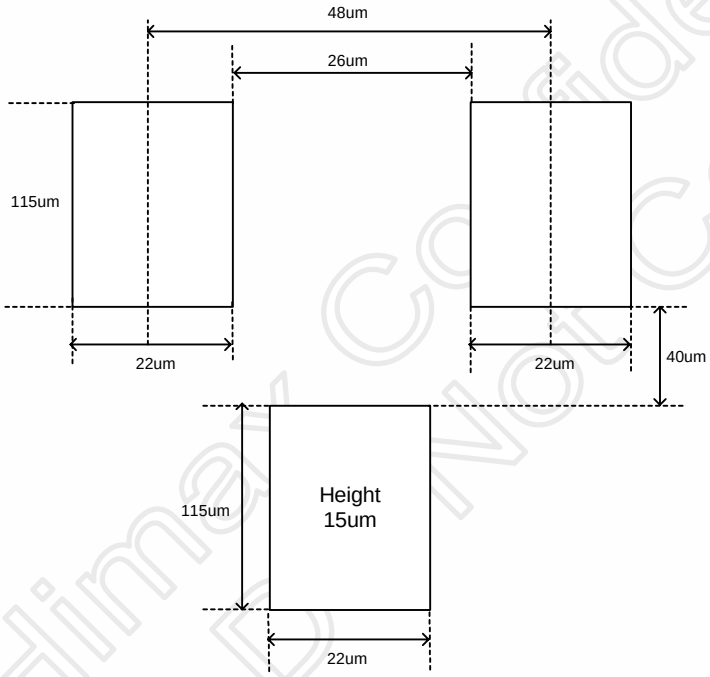


Bump size

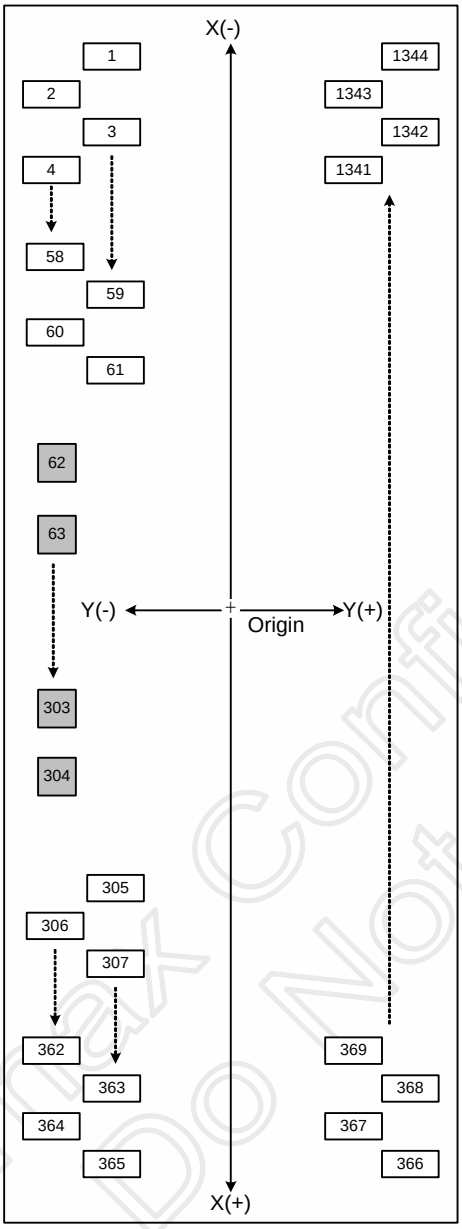
Input Bump size (type A) (pad 62~pad 304)



Output Bump size (type B) (pad 1 ~ pad 61; pad 305 ~ pad 1344)



Pad Coordinate



5. System Connection Block Diagram

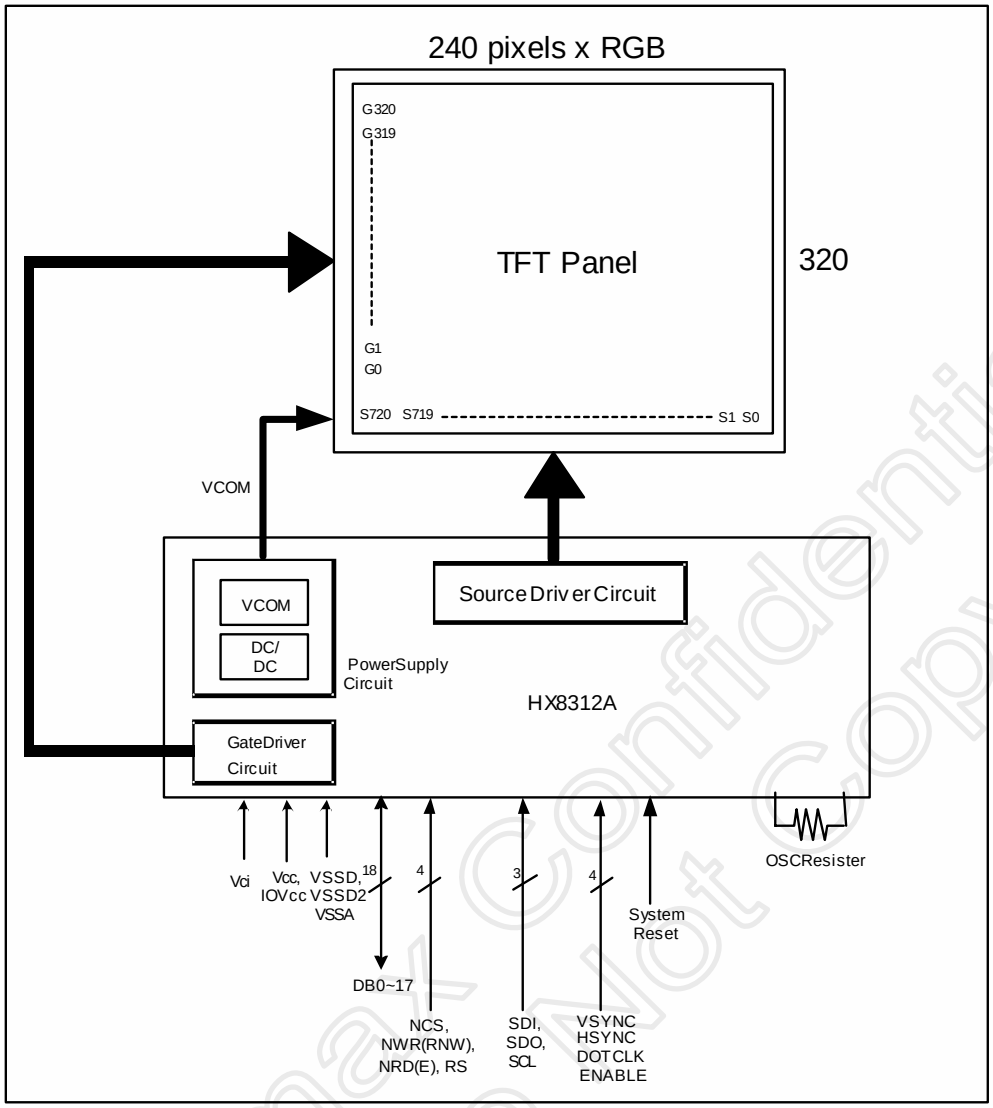


Figure 5. 1 System Connection Block Diagram

6. Layout Recommendation

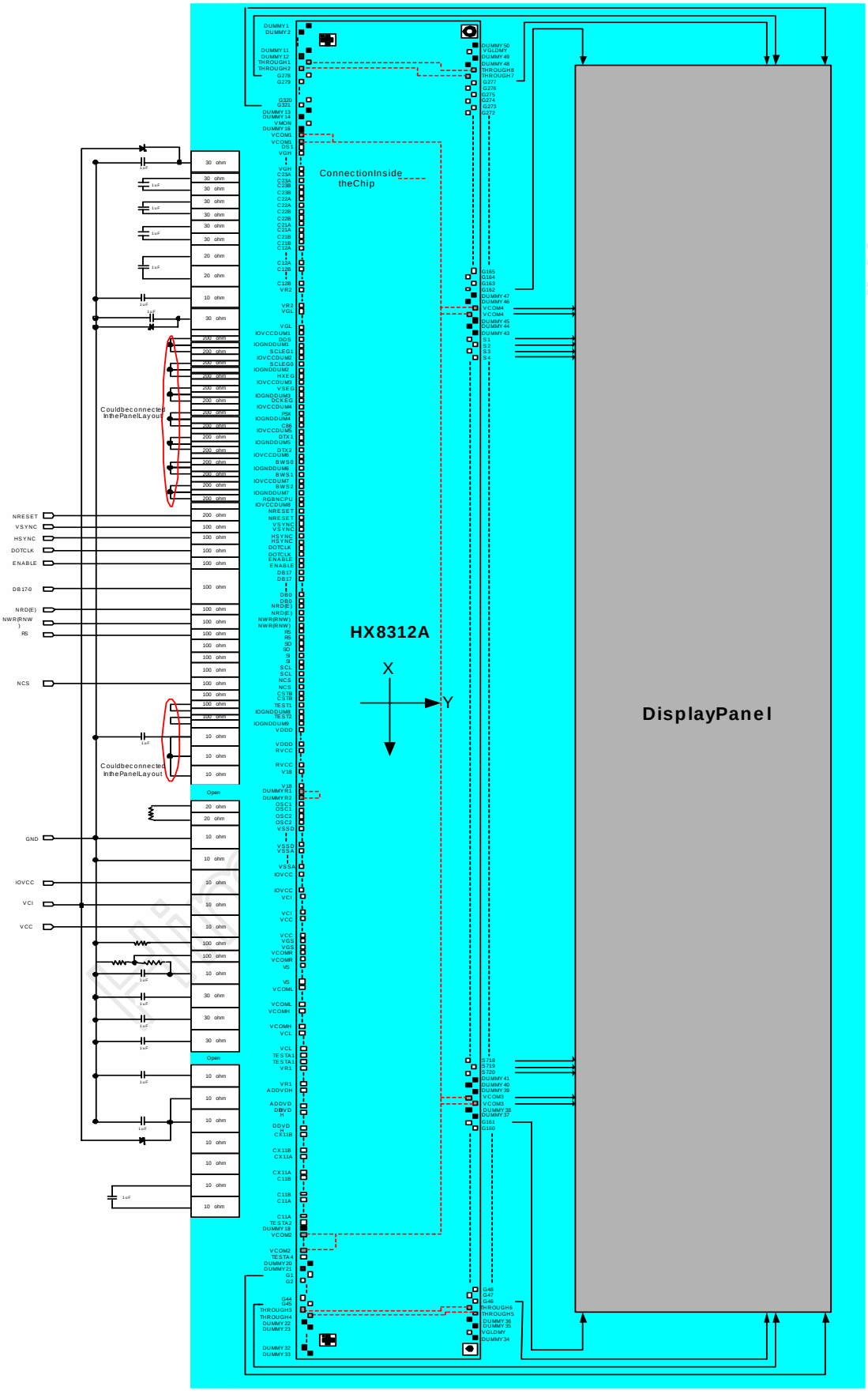
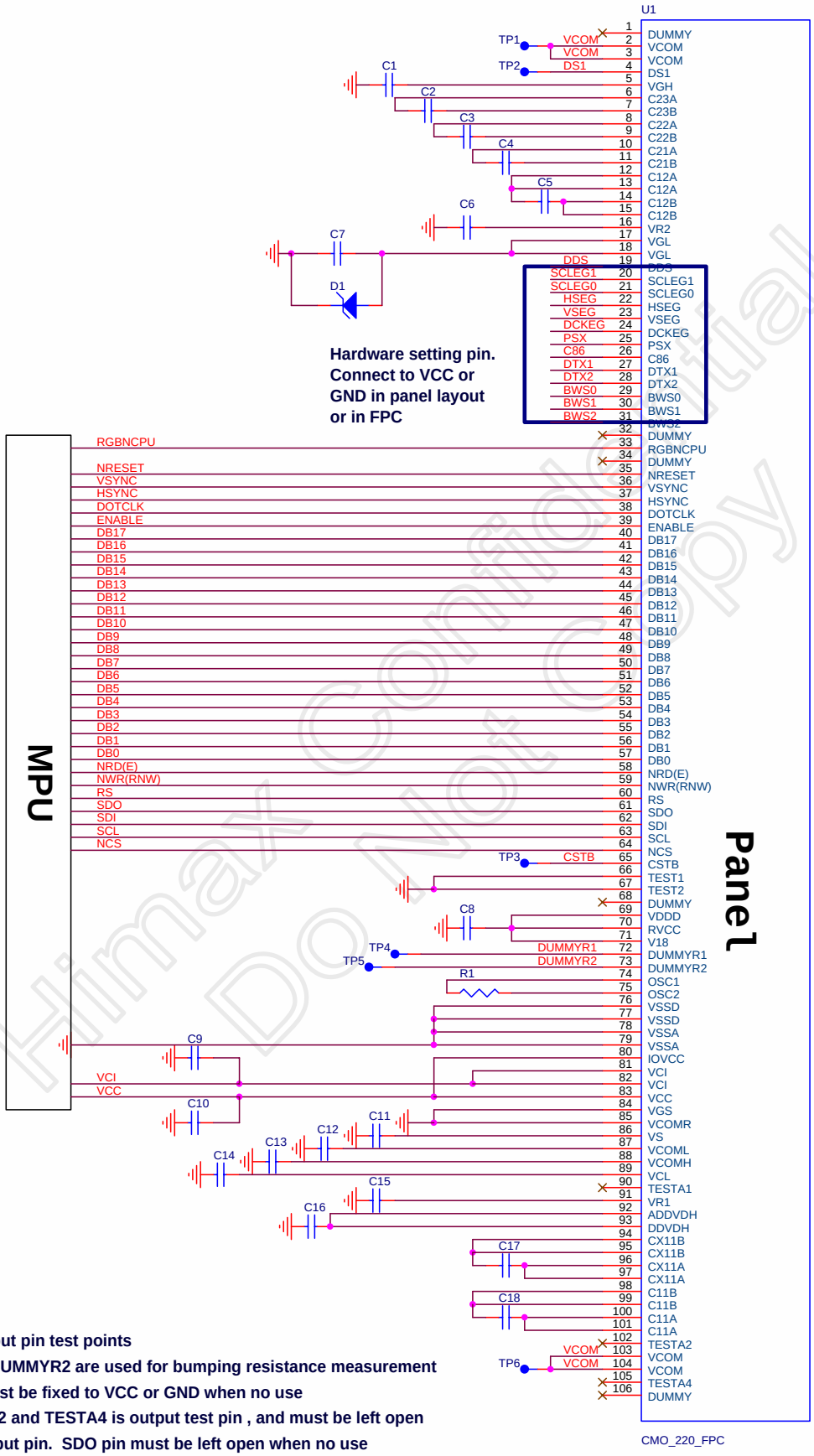


Figure 6. 1 Layout Recommendation of HX8312-A

7. FPC Circuit Example



1. "TP1~6" are output pin test points
2. DUMMYR1 and DUMMYR2 are used for bumping resistance measurement
3. The input pin must be fixed to VCC or GND when no use
4. TESTA1 , TESTA2 and TESTA4 is output test pin , and must be left open
5. SDO pin is a output pin. SDO pin must be left open when no use
6. VCC and VCI need to be separated to prevent interference

Specification of Component Connected to HX8312-A

Capacitor	Capacitor Value / Voltage on	Remarks
C1 (VGH)	1uF/25V/B (VGH)	Connect to capacitor while using VGH
C2 (C23A/B)	1uF/10V/B (DDVDH)	Connect to capacitor according register BT bit setting
C3 (C22A/B)	1uF/10V/B (DDVDH)	Connect to capacitor according register BT bit setting
C4 (C21A/B)	1uF/10V/B (DDVDH)	Connect to capacitor according register BT bit setting
C5 (C12A/B)	1uF/6.3V/B (VCI)	Connect to capacitor while using VCL
C6 (VR2)	1uF/6.3V/B (VCI)	Connect to capacitor while using VR2
C7 (VGL)	1uF/25V/B (VGL)	Connect to capacitor while using VGL
C8 (V18)	1uF/6.3V/B (VCC)	
C9 (VCI)	1uF/6.3V/B (VCC)	
C10 (VCC)	1uF/6.3V/B (VCI)	
C11 (VS)	1uF/10V/B (DDVDH)	Connect to capacitor while using VS
C12 (VCOML)	1uF/10V/B (DDVDH)	Connect to capacitor while using VCOML
C13 (VCOMH)	1uF/10V/B (DDVDH)	Connect to capacitor while using VCOMH
C14 (VCL)	1uF/6.3V/B (VCI)	Connect to capacitor while using VCL
C15 (VR1)	1uF/6.3V/B (VCI)	Connect to capacitor while using VR1
C16 (DDVDH)	1uF/10V/B (DDVDH)	Connect to capacitor while using DDVDH
C17 (CX11A/B)	1uF/10V/B (DDVDH)	Connect to capacitor while using DDVDH
C18 (C11A/B)	1uF/10V/B (DDVDH)	Connect to capacitor while using DDVDH

Other Component	Spec.	Remarks
D1 (VGL -GND)	VF < 0.4V / 20mA @ 25°C	Connect to Shottky Diode
R1 (VCC)	According to Internal oscillator frequency setting.	Suggest 100K ohm

8. Pin Description

Input Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
BWS2	I	1	MPU	The bus width selection in RGB interface circuit. 0: 18-bit, 1: 16-bit
BWS1-0	I	2	MPU	The bus width selection in system interface circuit. (see Table 2. 1)
PSX	I	1	MPU	The parallel and serial bus interface selection in system interface circuit. 0: Parallel bus interface, 1: Serial bus interface
NCS	I	1	MPU	Chip select signal. 0: chip can be accessed; 1: chip cannot be accessed.
NRESET	I	1	MPU	Reset pin. Setting either pin low initializes the LSI. Must be reset the chop after power being supplied.
NRD (E)	I	1	MPU	I80 system: Serves as a read signal and reads data at the low level. M68 system: 0: Read/Write disable ; 1: Read/Write enable Fix it to IOVCC or VSSD level when using serial buss interface.
NWR (RNW)	I	1	MPU	Serves as a write signal and writes data at the rising edge. M68 system: 0: Write ; 1: Read Fix it to IOVCC or VSSD level when using serial bus interface.
C86	I	1	MPU	MPU selection 0: i80 series MPU; 1: M68 series MPU. Fix it to IOVCC or VSSD level when using serial bus interface.
SDI	I	1	MPU	Serial bus interface data input pin. Fix it to IOVCC or VSSD level when using parallel bus interface.
SCL	I	1	MPU	Serial bus interface clock input pin Fix it to IOVCC or VSSD level when using parallel bus interface.
RGB_nCPU	I	1	MPU	0: System interface can be accessed. 1: System interface can not be accessed.
RS	I	1	MPU	Command/display Data Selection 0: Command, 1: Display data Connect to IOVCC or VSSD level when serial bus interface is selected.
DTX2-1	I	2	MPU	Specify the transferring method of one pixel data in system interface. (see Table 2. 3)
SCLEG1-0	I	1	MPU	Determine the effective edge operation of SCLK for SDI data latch and SDO data output. (see Table 2. 6)
VSYNC	I	1	MPU	Vertical synchronization signal input pin. Must be connected to IOVCC if not in use.
HSYNC	I	1	MPU	Horizontal synchronization signal input pin. Must be connected to IOVCC if not in use.
DOTCLK	I	1	MPU	Dot clock signal input used in the RGB interface circuit. Must be connected to IOVCC if not in use.
ENABLE	I	1	MPU	Enable signal pin used in RGB interface circuit. 0: disable, 1: enable when EPL (D1 bit of R157) = 0. 0: enable, 1: disable when EPL (D1 bit of R157) = 1. Must be connected to IOVCC if not in use.
VSEG	I	1	MPU	Valid VSYNC polarity selection pin 0: Start in the low level, 1: Start in the high level
HSEG	I	1	MPU	Valid HSYNC polarity selection pin 0: Start in the low level, 1: Start in the high level.
DCKEG	I	1	MPU	Valid DOTCLK polarity selection pin 0: falling edge latch, 1: rising edge latch
DDS	I	1	MPU	Selection the position of dummy line (321th line). 0: the end of the frame, 1: the beginning of the frame

Output Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
SDO	O	1	MPU	Serial bus interface data output pin. Keep it open while using parallel bus interface
CSTB	O	1	MPU	Frame synchronization signal output pin. Keep it open if not in use.
S1~S720	O	720	LCD	Source driver output pin. Output voltages to the liquid crystal.
G1~G321	O	321	LCD	Output signals to panel gate lines. VGH: the level to select the gate lines VGL: the level not to select the gate lines
VCOM1~4	O	4	LCD	VCOM output pin. They are short-circuited inside HX8312A.

Input / Output Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
DB17-0	I/O	18	MPU	Operates liked an 18-bit bi-directional data bus. Fix it to IOVCC or VSSD level when using serial bus interface. Don't set MPU output as Hi-Z when MPU has no output.
OSC2-1	I/O	2	Oscillation Resistor	Connect an external resistor for generating internal clock by internal R-C oscillation. Or an external clock signal is supplied through OSC1 with OSC2 open.
C11A , C11B CX11A , CX11B	I/O	4	Step up Capacitor	Connect to the step-up capacitors for step up circuit 1 operation. Leave this pin open if the internal step-up circuit is not used.
C21A ,C21B C22A ,C22B C23A ,C23B	I/O	6	Step up Capacitor	Connect to the step-up capacitors for step up circuit 2 operation. Leave this pin open if the internal step-up circuit is not used.
C12A ,C12B	I/O	2	Step up Capacitor	Connect to the step-up capacitors for step up circuit 3 operation. Leave this pin open if the internal step-up circuit is not used.

Power Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
VCC	I	1	Power supply	A power supply for the internal logic circuit. VCC = 2.2 ~ 3.3V
VCI	I	1	Power supply	A Power supply for step-up circuit and power supply circuit. VCI = 2.5 ~ 3.3V
IOVCC	I	1	Power supply	Power supply for I/O circuit. IOVCC = 1.65 ~ 3.3V
V18	O	1	Bypass capacitor and VDDD, RVCC	1.8V regulator output. V18, VDDD and RVCC must have the same voltage level. Connect to VDDD and RVCC on the FPC.
RVCC	I	1	V18 and VDDD	Power supply for RAM circuit.
VDDD	I	1	V18 and RVCC	Power supply for logic circuit.
VSSD	I	1	System Ground	Ground for digital circuit.
VSSD2	I	1	System Ground	Ground for internal circuit.
VSSA	I	1	System Ground	Ground for analog circuit.
VGH	O	1	Bypass Capacitor	A positive power supply for the gate line drive circuit.
VGL	O	1	Bypass Capacitor Schottky Diode	A negative power supply for the gate line drive circuit. Insert a schottky diode in a forward direction to VSSA.
ADDVDH	I	1	DDVDH	Power supply pins for VS and COMH regulators. Connected to DDVDH on FPC
DDVDH	O	1	ADDVDH and Bypass Capacitor	Output supply pin. Connected to ADVDDH on FPC.
VDH	O	1	Bypass Capacitor	Power supply for the source drive unit.
VCL	O	1	Bypass Capacitor	The voltage of Vci x (-1) output
VR2-1	O	2	Bypass Capacitor	Reference voltage output for the step-up circuit 2.
VS	O	1	Bypass Capacitor	Power supply for the source drive unit.
VGLDMY	O	1	-	A negative power supply for the gate line drive circuit.
VCOMH	O	1	Bypass Capacitor	The high level voltage output of VCOM AC voltage output.
VCOML	O	1	Bypass Capacitor	The low level voltage output of VCOM AC voltage output. When VCOML is fixed to GND level (VCOMG=0), capacitor connection is not necessary.
VGS	I	1	GND or External R	A reference level for the grayscale voltage generating circuit.
VCOMR	I	1	Variable Resistor	Adjusting VCOMH level with an variable resistor between VDH and VSSA.
IOVCCDUM 1~8	O	8	-	Pull-up pin for mode setting. These pins are connected to IOVCC inside the chip.
IOGNDDUM 1~9	O	9	-	Pull-down pin for mode setting. These pins are connected to VSSD inside the chip.

Test Pins and Other				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
TEST2-1		2	GND	Test pin. Must connect to GND.
DS1	O	1	-	Pin for gamma voltage output
VMON	O	1	-	Test pin output. Must be left open.
TESTA1, 2, 4	O	3	-	Test pin output. Must be left open.
THROUGH1	-	1	-	Dummy pads. Used to measure the COG contact resistance. THROUGH1 and THROUGH8 are short-circuited within the chip.
THROUGH8	-	1	-	
THROUGH2	-	1	-	Dummy pads. Used to measure the COG contact resistance. THROUGH2 and THROUGH7 are short-circuited within the chip.
THROUGH7	-	1	-	
THROUGH3	-	1	-	Dummy pads. Used to measure the COG contact resistance. THROUGH3 and THROUGH6 are short-circuited within the chip.
THROUGH6	-	1	-	
THROUGH4	-	1	-	Dummy pads. Used to measure the COG contact resistance. THROUGH4 and THROUGH5 are short-circuited within the chip.
THROUGH5	-	1	-	
DUMMYR1	-	1	-	Dummy pads. Used to measure the COG contact resistance. DUMMYR1 and DUMMYR2 are short-circuited within the chip.
DUMMYR2	-	1	-	
DUMMY1-14, 16, 18, 20-50	-	47	-	Dummy pin. (There is no gold bumper on DUMMY 7,9,11, 23, 25 ,27)

Note : 1. The layout of VSSA , VSSD , VSSD2 need to be separated in panel, and short together in FPC.
2. Input pin must be fixed to VCC or VSSD when no use.
3. The output pin must be left floating when no use.
4. SDO is a output pin. It must be left floating when no use.
5. TEST2 , 1 are test pin inputs. It must be connected to VSSD. And the short connection of TEST1 , TEST2 and VSSD must be located in FPC , not in panel.
6. DS1 , MON , TESTA1, 2, 4 are test pin outputs. It must be left floating.

9. Chip Access Configuration

9.1 Interface Circuit

The HX8312A has a system interface circuit for RAM data / command transferring, and a RGB interface circuit for RAM data transferring during animated display. The data bus pins (DB17-0) is used as input both in system interface circuit and RGB interface circuit.

External Setting Pin				Interface Mode	
NWRGB (R02h,D0)	PSX	RS	VSYNC, HSYNC , DENA , DOTCLK	Command transfer	Display Data Transfer
0	0	0	Fixed	System Interface Circuit (Parallel Bus)	-
0	0	1	Fixed	-	System Interface Circuit (Parallel Bus)
0	1	0	Fixed	System Interface Circuit (Serial Bus)	-
0	1	1	Fixed	-	System Interface Circuit (Serial Bus)
1	0	0	Input	System Interface Circuit (Parallel Bus)	RGB Interface Circuit
1	0	1	Input	-	RGB Interface Circuit
1	1	0	Input	System Interface Circuit (Serial Bus)	RGB Interface Circuit
1	1	1	Input	-	RGB Interface Circuit

Table 9. 1 Interface Type

Note:

1. System interface (parallel and serial bus) circuit is not available when external pin RGB_nCPU = "1". All operation from system interface input are not available.

2. Please make sure that RGB interface circuit is only used for display data RAM access, and can not be used for internal register access.

3. When NWRGB = “1”, RGB interface circuit is used for display data RAM accessed, and system interface circuit is used for internal register accessed.

4. When RGB interface and parallel bus system interface is in used, the data bus (DB17-0) is used by system interface circuit for internal register access when RS = “L”, and the data bus (DB17-0) is used by RGB interface circuit for display data RAM access when RS = “H”.

9.1.1 System Interface Circuit

C86	Input signal format selection
0	Format for I80 series MPU
1	Format for M68 series MPU

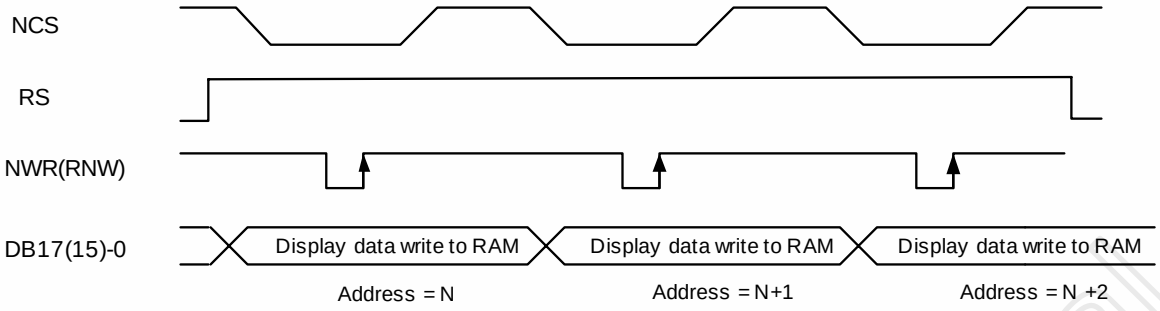
Table 9. 2 MPU selection

Interface Type	External Setting Pin					Bus Width	Bit number in a pixel	Transferring Method of RAM data	Transferring Method of Command
	PSX	BWS1	BWS0	DTX2	DTX1				
MPU1	0	0	0	x	x	18-bit parallel	18-bits	18-bit collective	16-bit collective
MPU2	0	1	0	0	1	16-bit parallel	18-bits	9-bit twice	
MPU3	0	1	0	1	1			16-bit + 2-bit	
MPU4	0	1	0	0	0		16-bits	16-bit collective	
MPU5	0	1	1	0	1	8-bit parallel	18-bits	6-bit 3 times	8-bit twice
MPU6	0	1	1	1	1			8-bit+8-bit+2-bit	
MPU7	0	1	1	1	0		16-bits	8-bit twice	
MPU8	1	0	1	x	x	18-bit serial	18-bits	18-bit serial	18-bit serial
MPU9	1	1	1	x	x	16-bit serial	16-bits	16-bit serial	16-bit serial

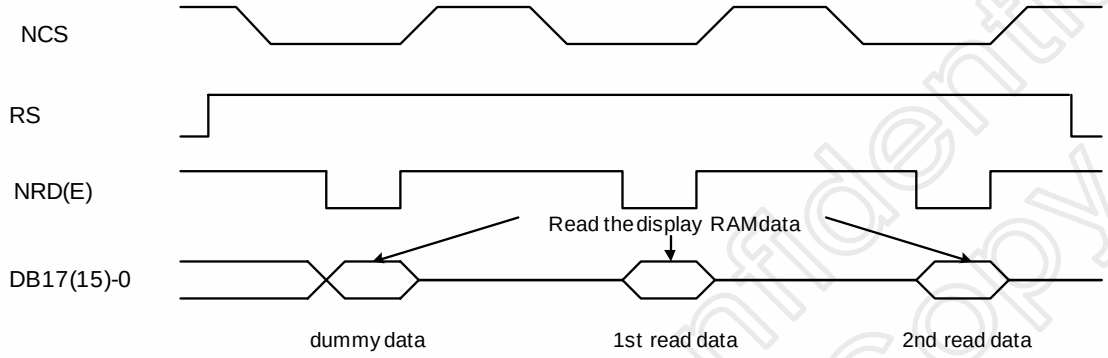
Table 9. 3 Input bus format selection of system interface circuit

Parallel Bus System Interface

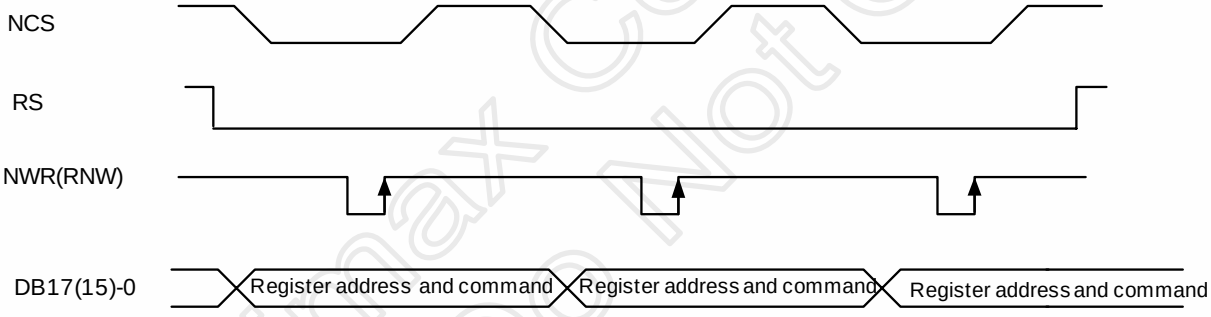
Write to the display data RAM (MPU1 , MPU4)



Read the display data RAM (MPU1 , MPU4)



Write to the register (MPU1~ MPU4)



Read the register (MPU1~MPU4)

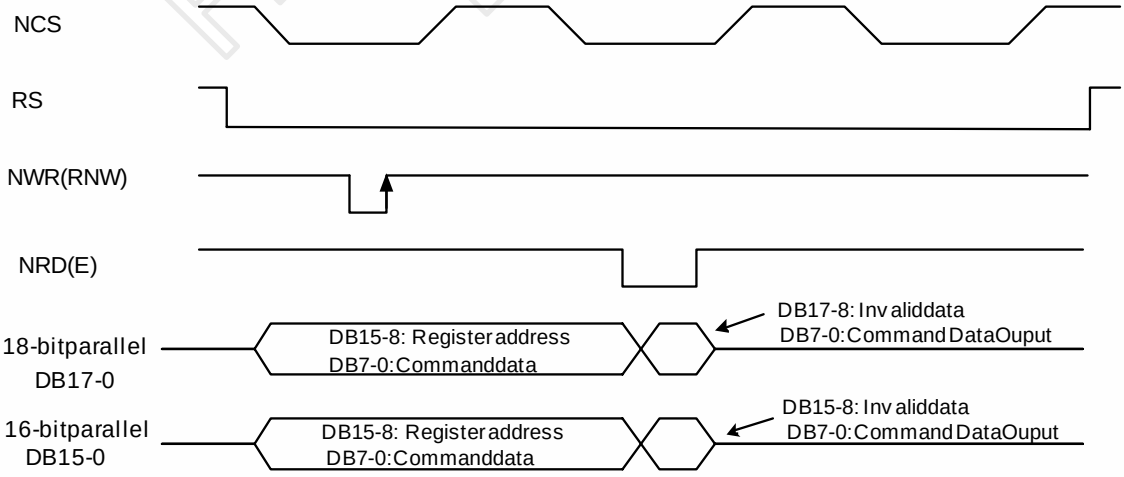


Figure 9. 1 18 / 16-bit Bus Width Parallel Bus Interface Timing (for I80 series MPU)

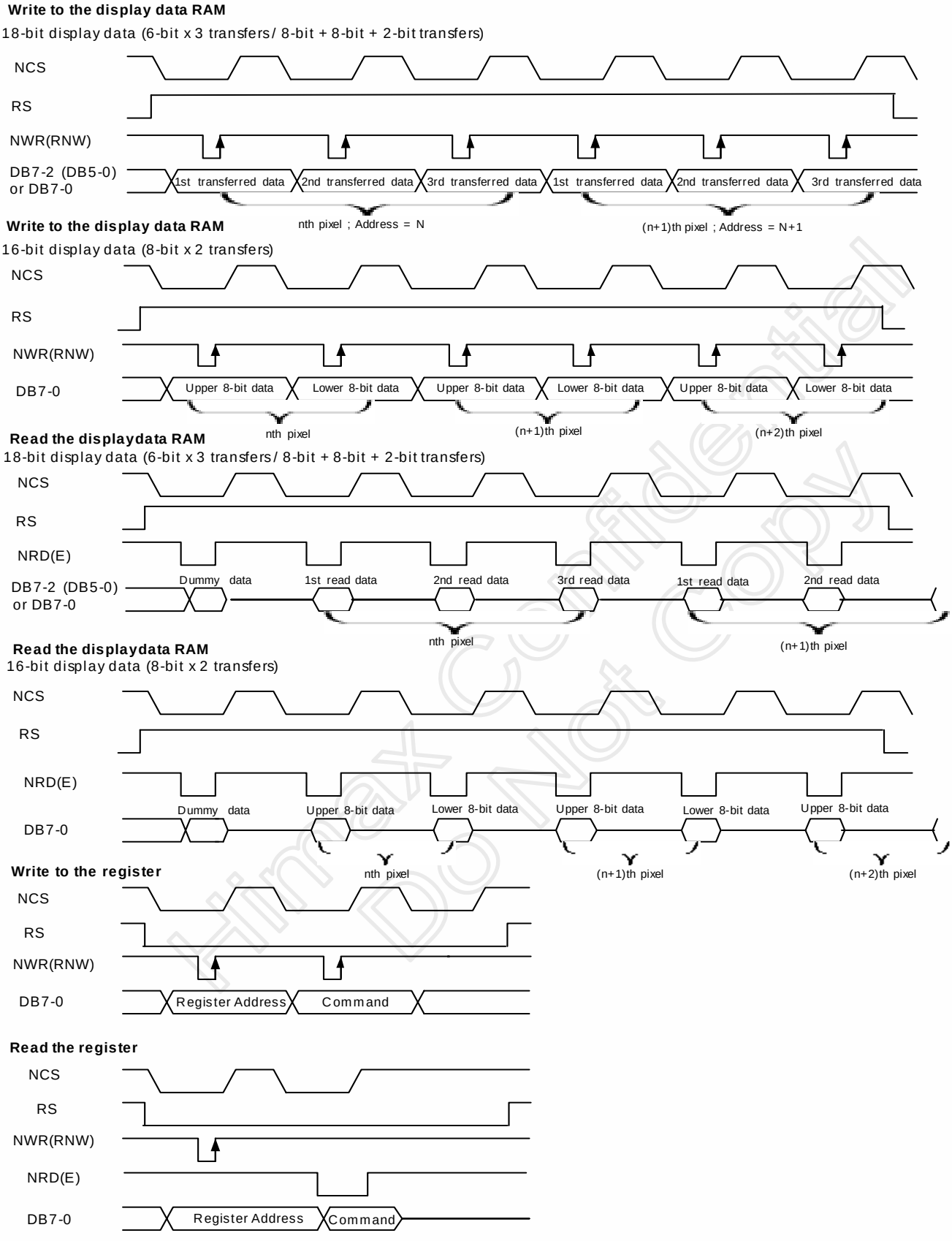


Figure 9. 2 8-bit Bus Width Parallel Bus Interface Timing (for I80 series MPU)

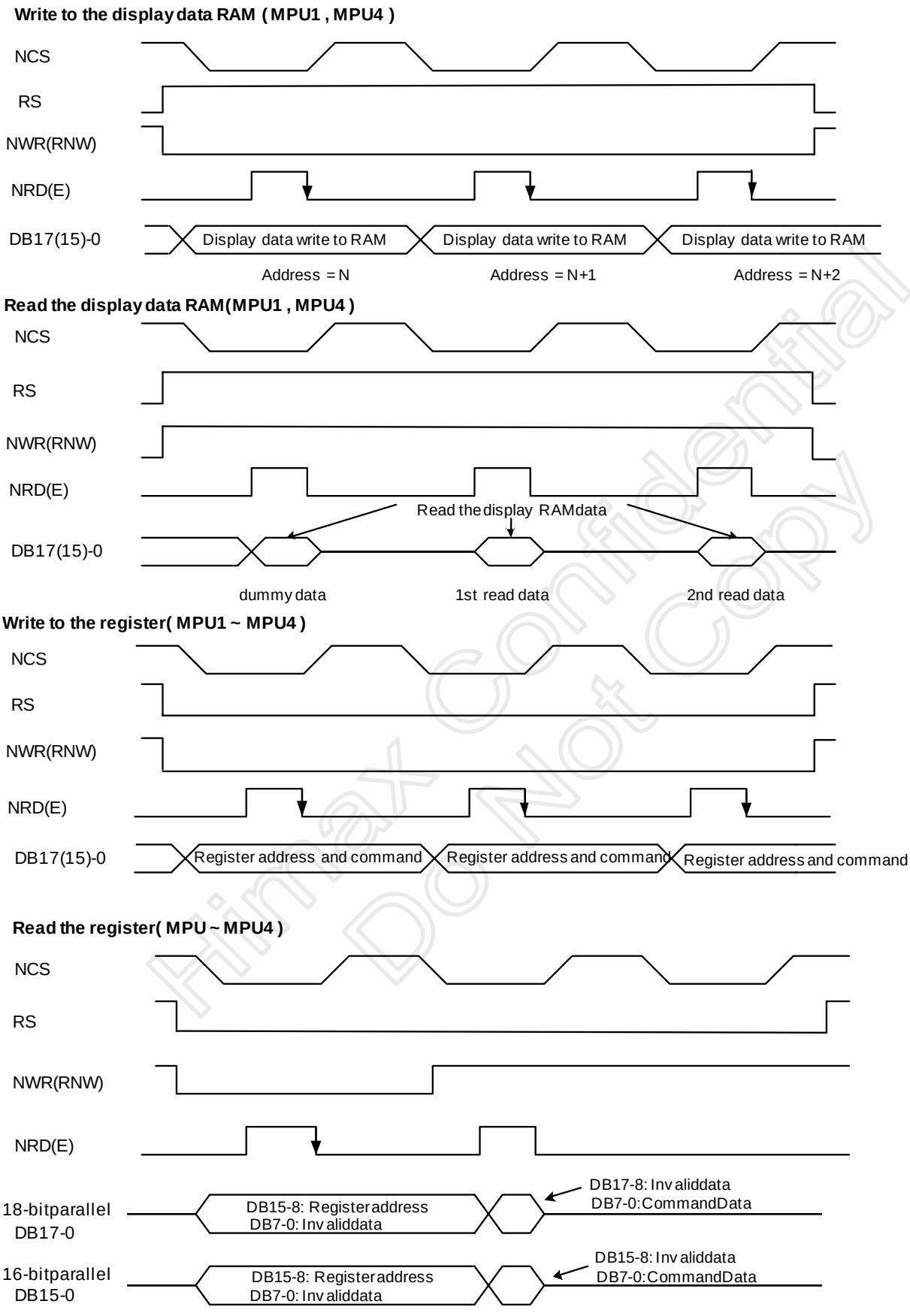
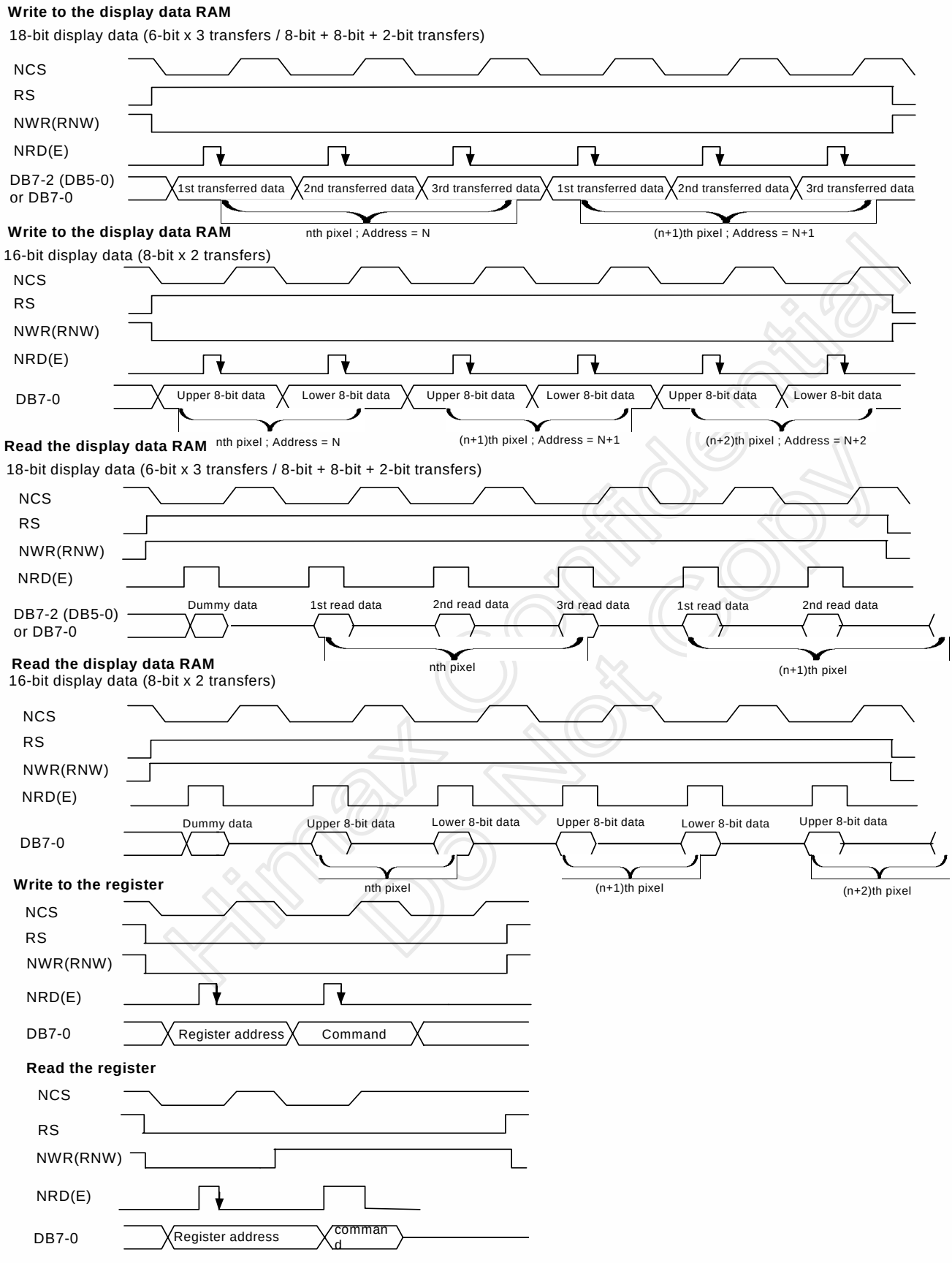


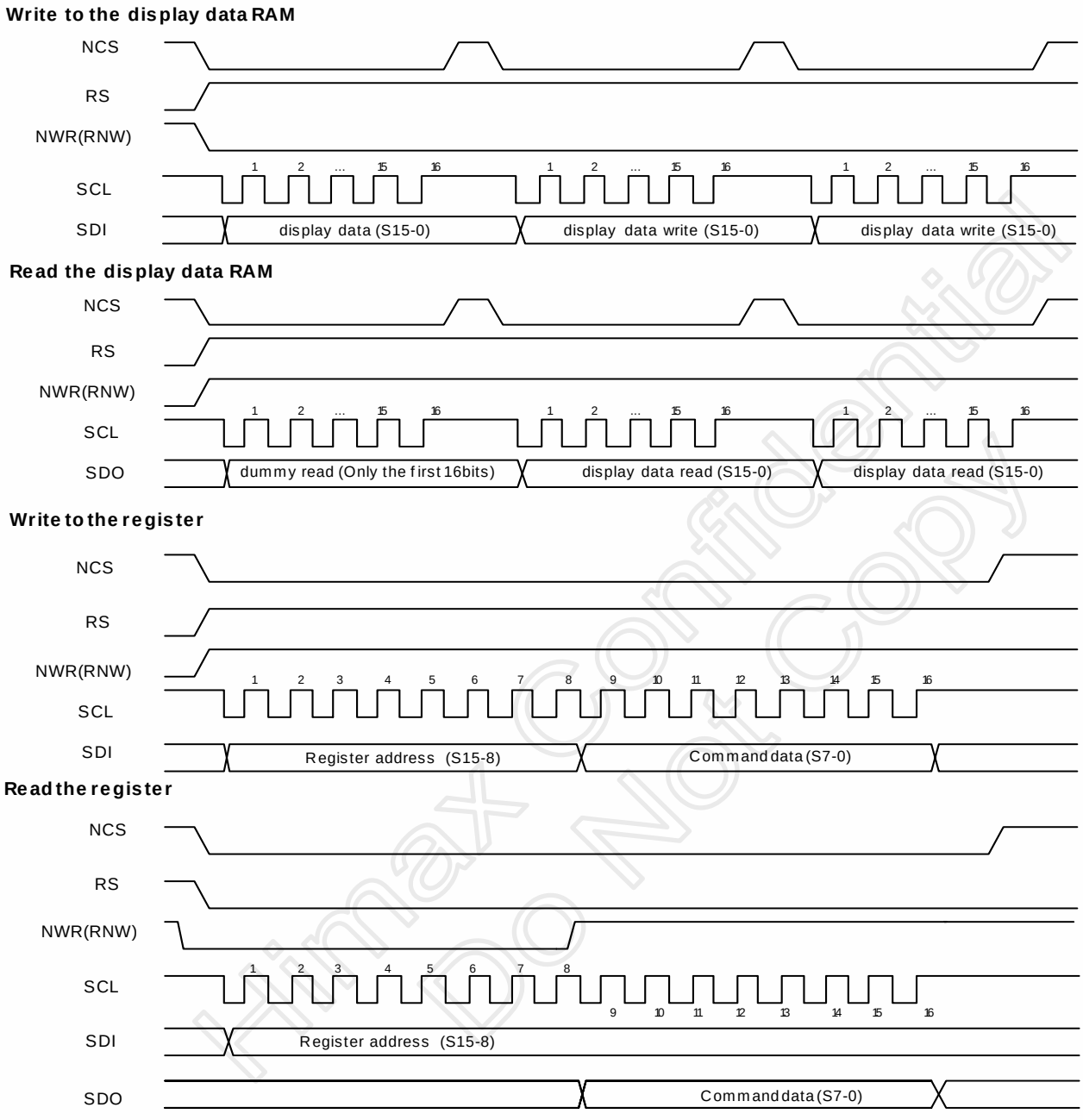
Figure 9. 3 18 / 16-bit Bus Width Parallel Bus Interface Timing (for M68 series MPU)



DB7-2 or DB5-0 used in 6-bit x 3 input mode is decided by MSBF (D0 bit) of R157

Figure 9. 4 8-bit Bus Width Parallel Bus Interface Timing (for M68 series MPU)

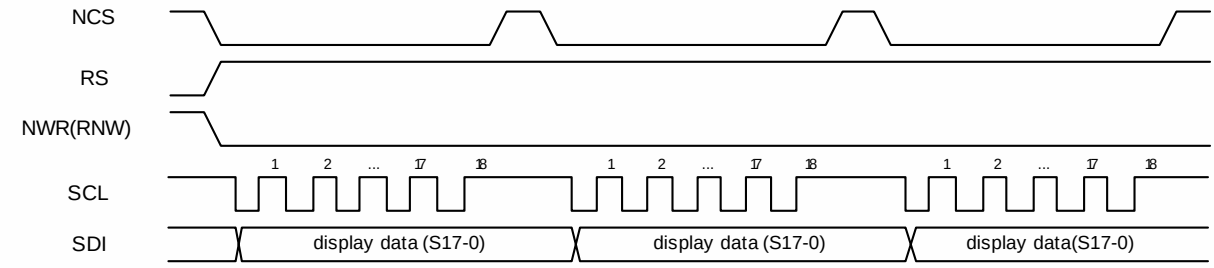
Serial Bus System Interface



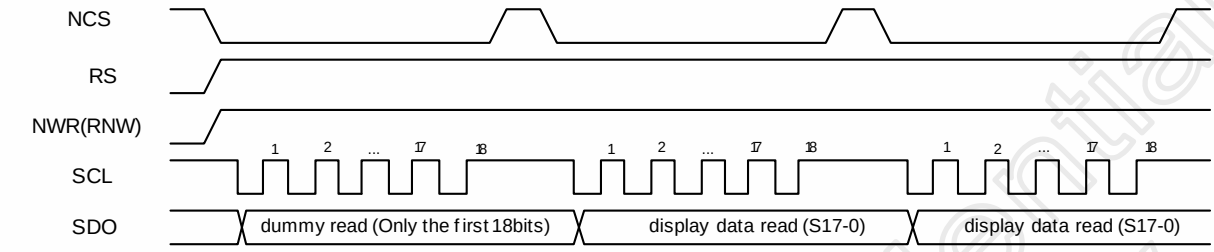
After sending a command and display data in an 16-bit unit, set nCS as "H", and then send the next command and display data.

Figure 9. 5 16–bit Serial Bus Interface Timing (SCLEG1=SCLEG2=0)

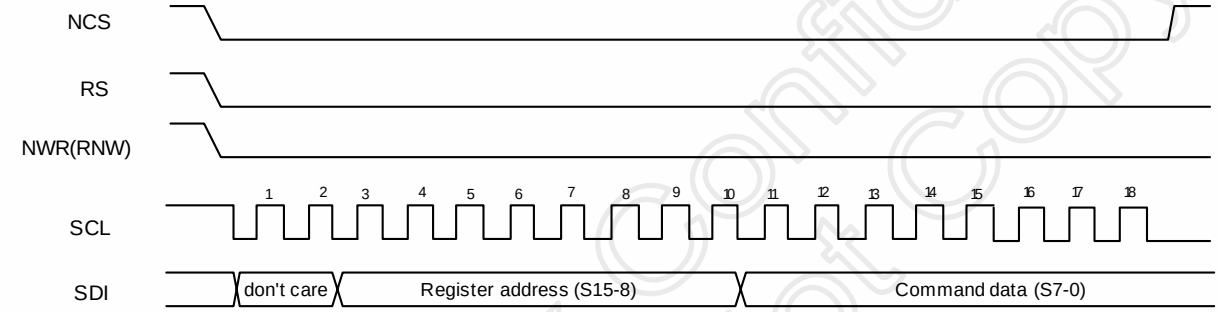
Write to the display data RAM



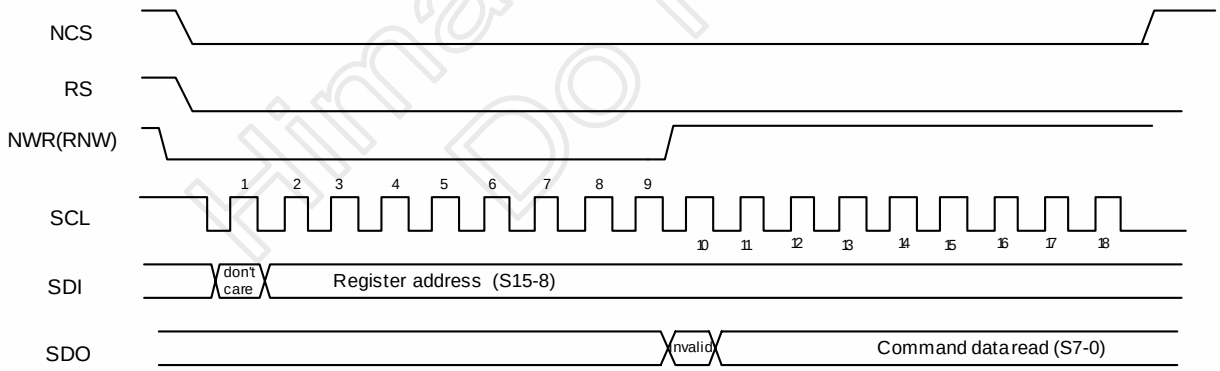
Read the displaydata RAM



Write to the registers



Read the registers

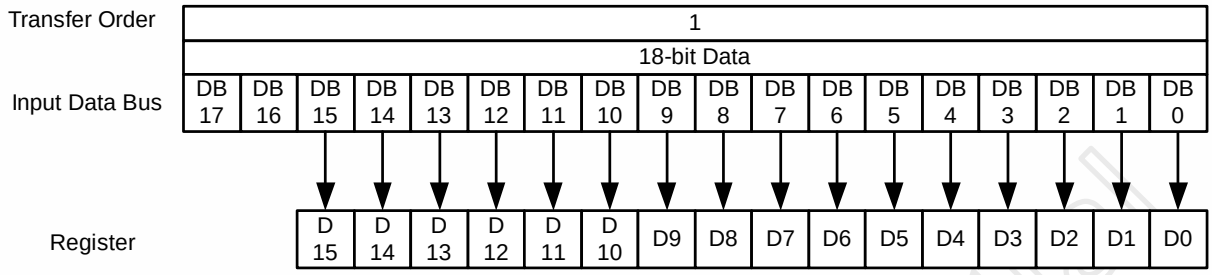


After sending a command and display data in an 18-bit unit, set nCS as "H", and then send the next command and displaydata.

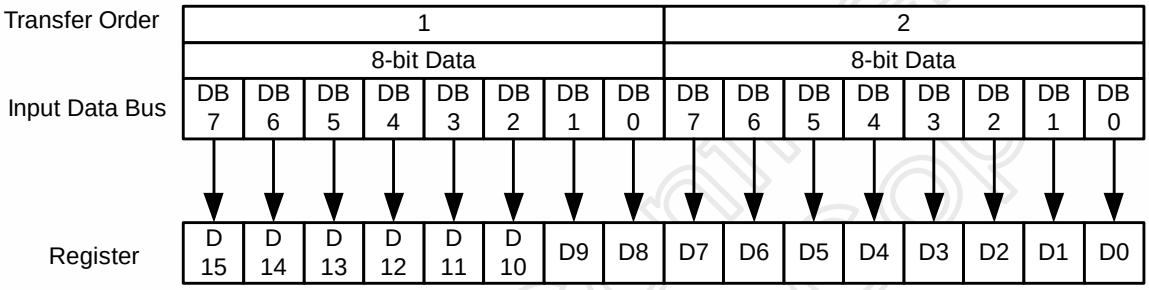
Figure 9. 6 18–bit Serial Bus Interface Timing (SCLEG1=SCLEG2=0)

Relation between Register Command Data Format and Input Bus

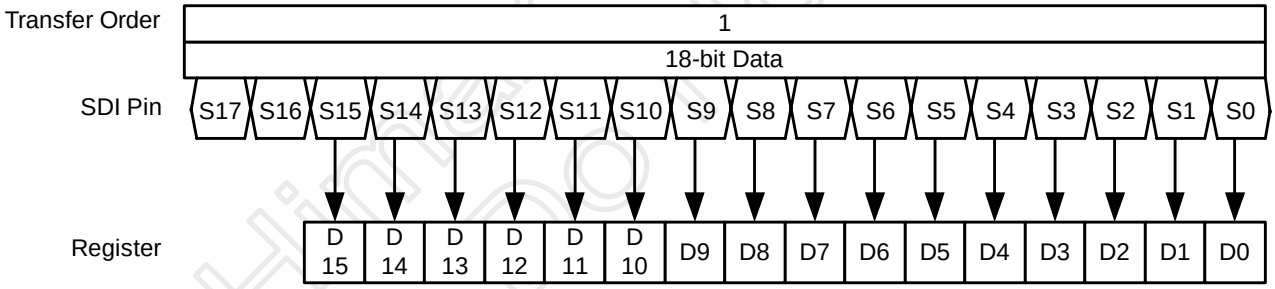
(1) MPU1, MPU2, MPU3, MPU4 Type



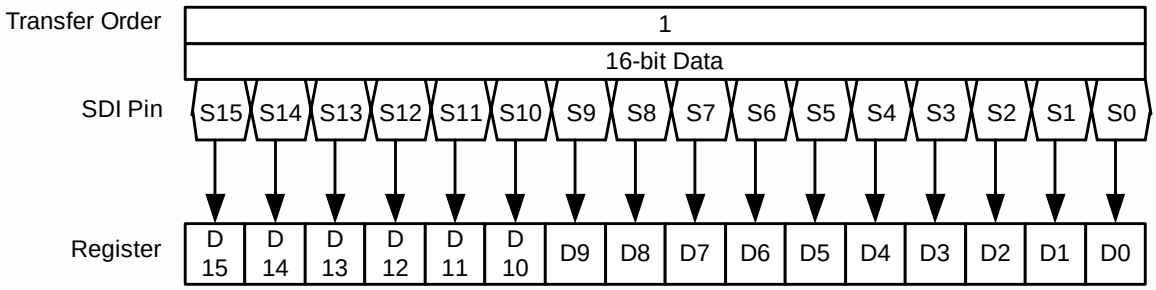
(2) MPU5, MPU6, MPU7 Type



(3) MPU8 Type



(4) MPU9 Type

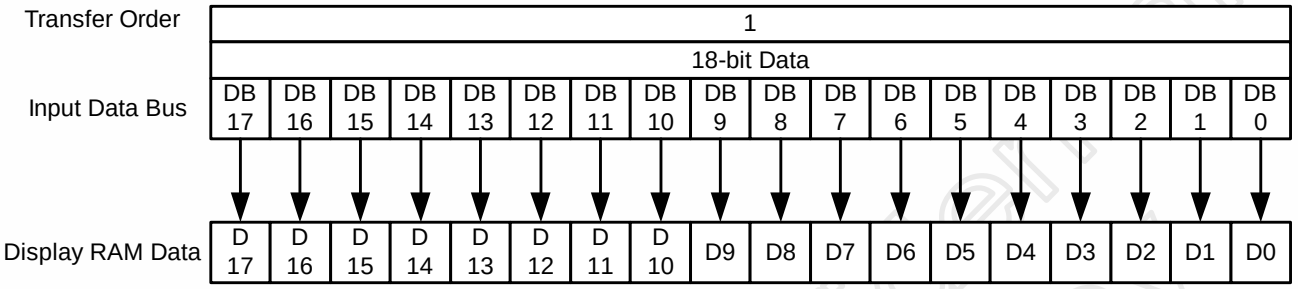


Relation between Display RAM Data Format and Input Bus in System Interface

The display RAM data is consist of 18 bits which include R-, G-, B-dot display level information.

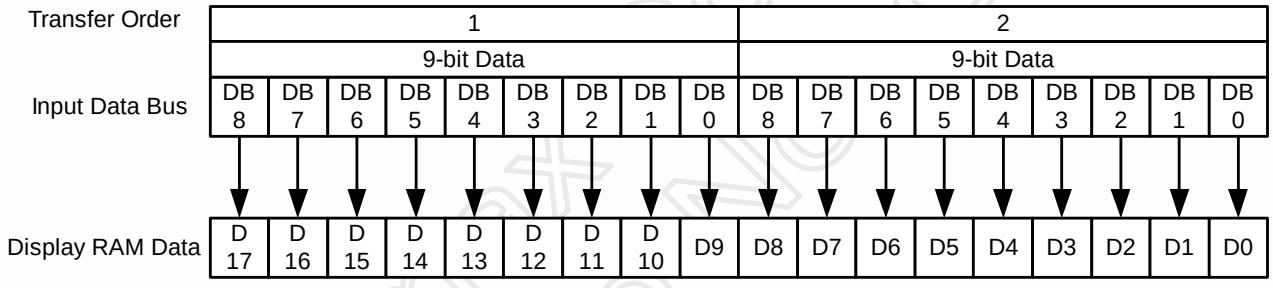
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

(1) MPU1 Type



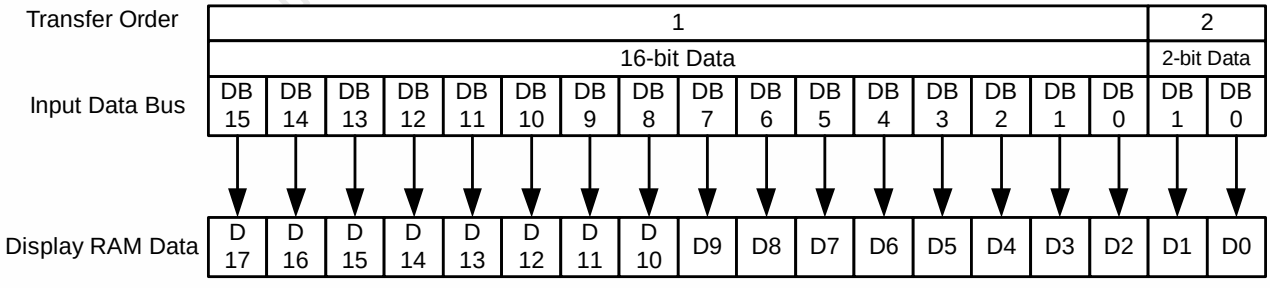
262,144 colors are avaliable

(2) MPU2 Type (9-bit × 2)



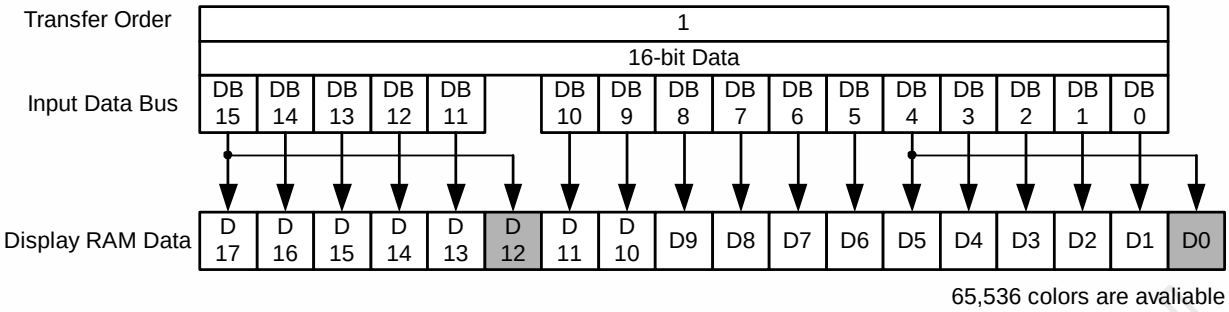
262,144 colors are avaliable

(3) MPU3 Type (16-bit + 2-bit)



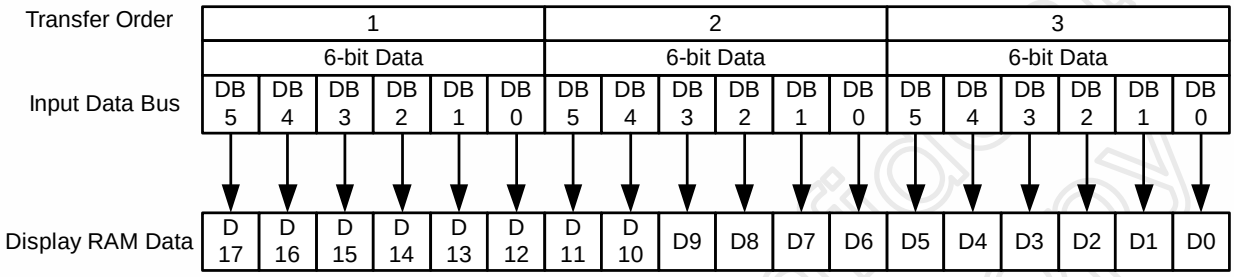
262,144 colors are avaliable

(4) MPU4 Type (16-bit × 1)



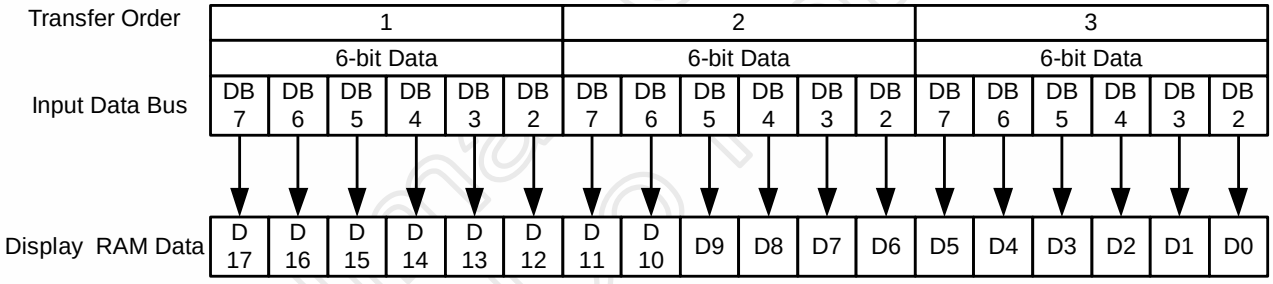
65,536 colors are avaliable

(5-1) MPU5 Type A (6-bit × 3) with (MSBF = 0 ; D0 bit of R157)



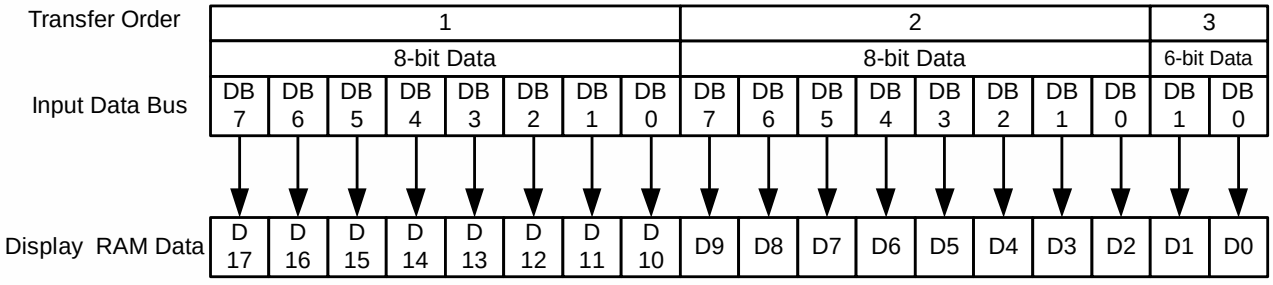
262,144 colors are avaliable

(5-2)MPU5 Type B (6-bit × 3) with (MSBF = 1; D0 bit of R157)



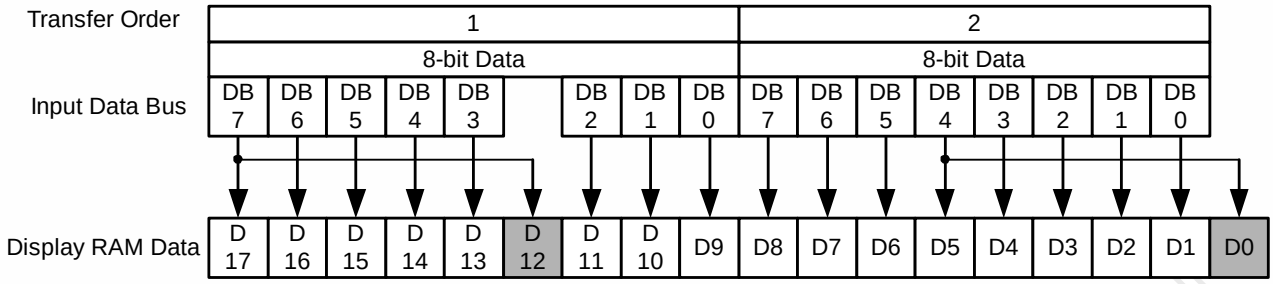
262,144 colors are avaliable

(6) MPU6 Type (8-bit + 8-bit + 2-bit)



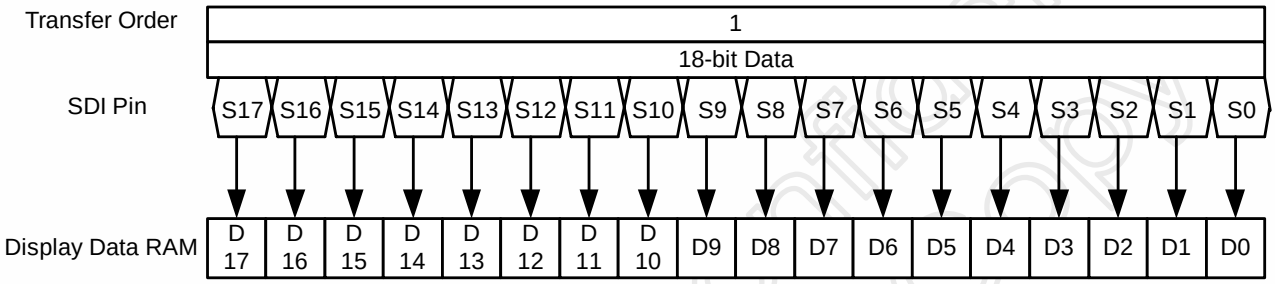
262,144 colors are avaliable

(7) MPU7 Type (8-bit × 2)



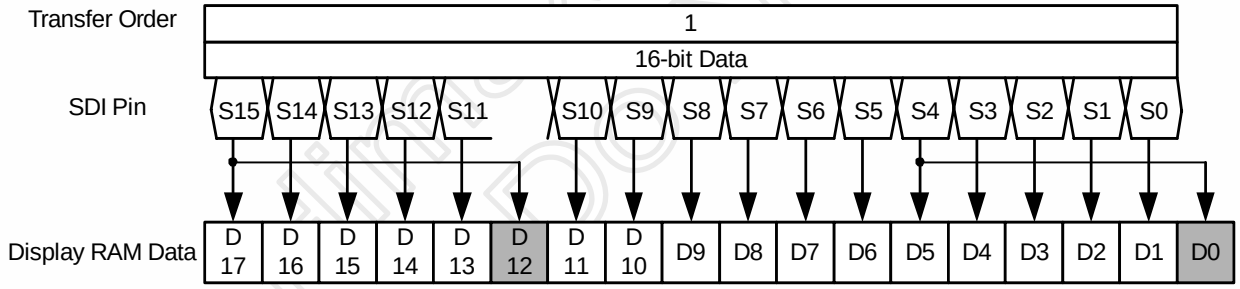
65,536 colors are avaliable

(8)MPU8 Type (18-bit serial)



262,144 colors are avaliable

(9) MPU9 Type (16-bit serial)



65,536 colors are avaliable

9.2 Display RAM Address Mapping

9.2.1 Display RAM Address Access Mapping

The HX8312A contains a display RAM bus address counter (AC) which assigns X (pixel), Y(line) address for writing pixel data to display RAM. One X address equals to one pixel allocation. The display data will be written at a pixel which address is specified by X address register (R66) and Y address register 1, 2 (R67, R68).

S/G pins	S1	S2	S3	S4	S5	S6	S7	S8	S9	---------	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
	17---------0			17---------0			17---------0			---------	17---------0			17---------0			17---------0			17---------0		
G1	0000h			0001h			0002h			---------	00ECh			00EDh			00EEh			00EFh		
G2	0100h			0101h			0102h			---------	01ECh			01EDh			01EEh			01EFh		
G3	0200h			0201h			0202h			---------	02ECh			02EDh			02EEh			02EFh		
G4	0300h			0301h			0302h			---------	03ECh			03EDh			03EEh			03EFh		
G5	0400h			0401h			0402h			---------	04ECh			04EDh			04EEh			04EFh		
G6	0500h			0501h			0502h			---------	05ECh			05EDh			05EEh			05EFh		
G7	0600h			0601h			0602h			---------	06ECh			06EDh			06EEh			06EFh		
G8	0700h			0701h			0702h			---------	07ECh			07EDh			07EEh			07EFh		
G9	0800h			0801h			0802h			---------	08ECh			08EDh			08EEh			08EFh		
G10	0900h			0901h			0902h			---------	09ECh			09EDh			09EEh			09EFh		
G11	0A00h			0A01h			0A02h			---------	0AECh			0AEDh			0AEEh			0AEFh		
G12	0B00h			0B01h			0B02h			---------	0BECh			0BEDh			0BEEh			0BEFh		
G13	0C00h			0C01h			0C02h			---------	0CECh			0CEDh			0CEEh			0CEFh		
G14	0D00h			0D01h			0D01h				0DECh			0DEDh			0DEEh			0DEFh		
G15	0E00h			0E01h			0E01h				0EECh			0EEDh			0EEEh			0EEFh		
⋮	⋮			⋮			⋮			---------	⋮			⋮			⋮			⋮		
G231	13600h			13601h			13602h			---------	136ECh			136EDh			136EEh			136EFh		
G232	13700h			13701h			13702h			---------	137ECh			137EDh			137EEh			137EFh		
G233	13800h			13801h			13802h			---------	138ECh			138EDh			138EEh			138EFh		
G234	13900h			13901h			13902h			---------	139ECh			139EDh			139EEh			139EFh		
G235	13A00h			13A01h			13A02h			---------	13AECh			13AEDh			13AEEh			13AEFh		
G236	13B00h			13B01h			13B02h			---------	13BECh			13BEDh			13BEEh			13BEFh		
G237	13C00h			13C01h			13C02h			---------	13CECh			13CEDh			13CEEh			13CEFh		
G238	13D00h			13D01h			13D02h			---------	13DECh			13DEDh			13DEEh			13DEFh		
G239	13E00h			13E01h			13E02h			---------	13EECh			13EEDh			13EEEh			13EEFh		
G240	13F00h			13F01h			13F02h			---------	13FECh			13FEDh			13FEEh			13FEFh		

Table 9. 4 Display RAM Address and Display Panel Position (X Size = 240, ADX = 0)

9.2.2 Display RAM Address Update Direction

Every time when a pixel data is written into or read from the display RAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register bits AM(D2 bit of R157), ADX(D7 bit of R1) and ADR(D6 bit of R1) setting.

ADX	X Address Direction		
	X Size = 180	X Size = 208	X Size = 240
0	X0 → X179 → X0	X0 → X207 → X0	X0 → X239 → X0
1	X179 → X0 → X179	X208 → X0 → X208	X240 → X0 → X240

ADR	Y Address Direction
0	Y0 → Y319 → Y0
1	Y319 → Y0 → Y319

Table 9. 5 X Address and Y Address Update Direction Setting

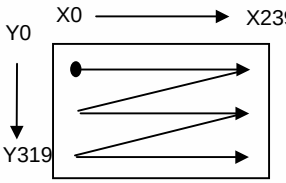
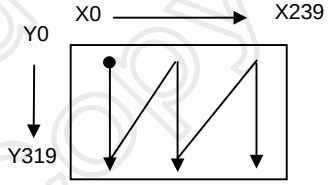
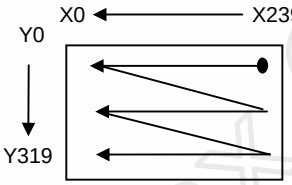
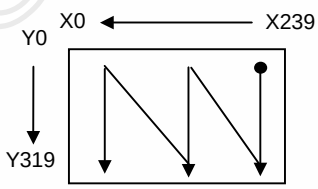
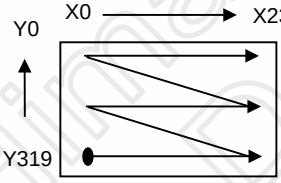
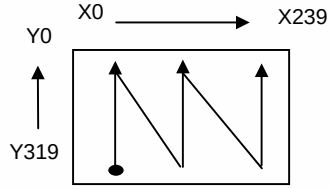
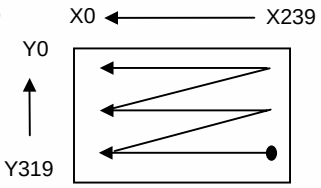
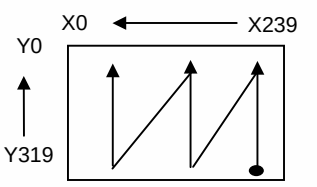
AM	ADR	ADX	Description Figure	AM	ADR	ADX	Description Figure
0	0	0		1	0	0	
		1				1	
	1	0			1	0	
		1				1	

Figure 9. 7 Address Update Direction Settings

9.2.3 Display RAM Address Mapping for Source Output Channel

R13		X Size for display panel
NSO1	NSO0	
0	0	240
0	1	208
1	0	180
1	1	Inhibited

Table 9. 6 X Size of Panel Display Setting

ADX = 0														
Source	ADC = 0	S1	S2	S3	S4	S5	S6	-------	S715	S716	S717	S718	S719	S720
Output	ADC = 1	S720	S719	S718	S717	S716	S715	-------	S6	S5	S4	S3	S2	S1
X Address		“00”h			“01”h			-------	“EE”h			“EF”h		
Bit Allocation		17-12	11-6	5-0	17-12	11-6	5-0	-------	17-12	11-6	5-0	17-12	11-6	5-0
Pixel		Pixel 1			Pixel 2			-------	Pixel 239			Pixel 240		

ADX = 1														
Source	ADC = 0	S1	S2	S3	S4	S5	S6	-------	S715	S716	S717	S718	S719	S720
Output	ADC = 1	S720	S719	S718	S717	S716	S715	-------	S6	S5	S4	S3	S2	S1
X Address		“00”h			“01”h			-------	“EE”h			“EF”h		
Bit Allocation		17-12	11-6	5-0	17-12	11-6	5-0	-------	17-12	11-6	5-0	17-12	11-6	5-0
Pixel		Pixel 1			Pixel 2			-------	Pixel 239			Pixel 240		

Table 9. 7 Display RAM X Address and Output Source Channel (X Size = 240)

ADX = 0														
Source	ADC = 0	S1	S2	S3	S4	S5	S6	-------	S715	S716	S717	S718	S719	S720
Output	ADC = 1	S720	S719	S718	S717	S716	S715	-------	S6	S5	S4	S3	S2	S1
X Address		“00”h			“01”h			-------	“CE”h			“CF”h		
Bit Allocation		17-12	11-6	5-0	17-12	11-6	5-0	-------	17-12	11-6	5-0	17-12	11-6	5-0
Pixel		Pixel 1			Pixel 2			-------	Pixel 207			Pixel 208		

ADX = 1														
Source	ADC = 0	S1	S2	S3	S4	S5	S6	-------	S715	S716	S717	S718	S719	S720
Output	ADC = 1	S720	S719	S718	S717	S716	S715	-------	S6	S5	S4	S3	S2	S1
X Address		“00”h			“01”h			-------	“CE”h			“CF”h		
Bit Allocation		17-12	11-6	5-0	17-12	11-6	5-0	-------	17-12	11-6	5-0	17-12	11-6	5-0
Pixel		Pixel 1			Pixel 2			-------	Pixel 207			Pixel 208		

S313 to S408 are invalid

Table 9. 8 Display RAM X Address and Output Source Channel (X Size = 208)

ADX = 0														
Source	**ADC = 0**	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**-------**	**S715**	**S716**	**S717**	**S718**	**S719**	**S720**
Output	**ADC = 1**	**S720**	**S719**	**S718**	**S717**	**S716**	**S715**	**-------**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**
X Address		"00"h			"01"h			-------	"B2"h			"B3"h		
Bit Allocation		17-12	11-6	5-0	17-12	11-6	5-0	-------	17-12	11-6	5-0	17-12	11-6	5-0
Pixel		Pixel 1			Pixel 2			-------	Pixel 179			Pixel 180		

ADX = 1														
Source	**ADC = 0**	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**-------**	**S715**	**S716**	**S717**	**S718**	**S719**	**S720**
Output	**ADC = 1**	**S720**	**S719**	**S718**	**S717**	**S716**	**S715**	**-------**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**
X Address		"00"h			"01"h			-------	"B2"h			"B3"h		
Bit Allocation		17-12	11-6	5-0	17-12	11-6	5-0	-------	17-12	11-6	5-0	17-12	11-6	5-0
Pixel		Pixel 1			Pixel 2			-------	Pixel 179			Pixel 180		

S271 to S450 are invalid

Table 9. 9 Display RAM X Address and Output Source Channel (X Size = 180)

10. Initial Code for Reference

For the CMO's 2.2"glass, 240 x RGB x 320 resolution, Vcc = Vci = 2.8V input , Rosc = 100Kohm.

The reference setting of chip initial on

```
// This initial for CMO's 2.2" panel,
// Rosc = 100Kohm
// External DDS pin = 1.
// Frame rate 65Hz
// Using MPU 16Bits /18Bits interface,
// Operation voltage => Vcc = Vci = 2.8V.

void LCD_HX8312A_Intial(void)
{
      Set_LCD_REG(0x0001,0x0010);   // Start oscillation
      Set_LCD_REG(0x0000,0x00A0);   // Standby mode cancel
      Set_LCD_REG(0x0003,0x0001);   // Software reset operation
      DelayX1ms(10);
      Set_LCD_REG(0x0003,0x0000);   // Software reset operation cancel
      Set_LCD_REG(0x002B,0x0004);   // Oscillator frequency adjust setting

      Set_LCD_REG(0x0059,0x0001);   // Test register setting enable
      Set_LCD_REG(0x0060,0x0022);   // Test register setting
      Set_LCD_REG(0x0059,0x0000);   // Test register setting disable   Note 1

      Set_LCD_REG(0x0028,0x0018);   // DC/DC clock frequency adjust setting
      Set_LCD_REG(0x001A,0x0005);   // Step up circuit frequency adjust setting
      Set_LCD_REG(0x0025,0x0005);   // Step up factor in step up circuit 2 setting
      Set_LCD_REG(0x0019,0x0000);   // VR1 and VR2 regulator factor setting

      //############### void Power_on_Set(void) ##################//

      Set_LCD_REG(0x001C,0x0073);   // Step up circuit operating current setting
      Set_LCD_REG(0x0024,0x0074);   // V18 and VCOM regulator current setting
      Set_LCD_REG(0x0018,0x00C1);   // VR1 and VR2 regulator on
      DelayX1ms(10);

      Set_LCD_REG(0x001E,0x0001);   // Extra step up circuit1 operation
      Set_LCD_REG(0x0018,0x00C5);   // DDVDH turn on
      Set_LCD_REG(0x0018,0x00E5);   // VCL turn on
      DelayX1ms(60);
      Set_LCD_REG(0x0018,0x00F5);   // VGH and VGL turn on
      DelayX1ms(60);
      Set_LCD_REG(0x001B,0x0009);   // VS/VDH turn on and set
      DelayX1ms(10);
      Set_LCD_REG(0x001F,0x0011);   // VCOM amplitude voltage setting
      Set_LCD_REG(0x0020,0x000E);   // VCOMH voltage setting
      Set_LCD_REG(0x001E,0x0081);   // VCOM operation start
      DelayX1ms(10);
```

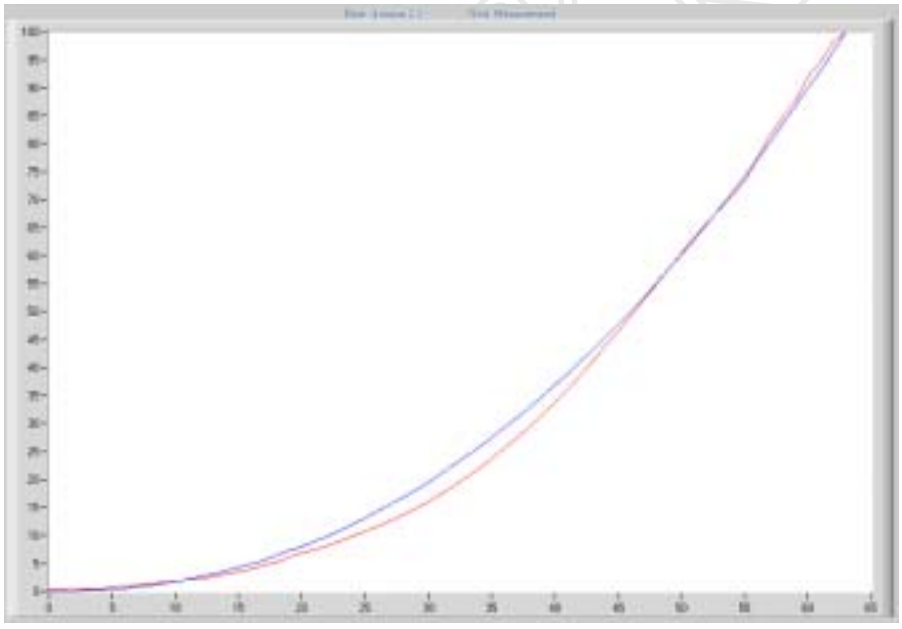
```
//############### void Chip_Set (void) ##################//

Set_LCD_REG(0x009D,0x0000);
Set_LCD_REG(0x00C0,0x0000);
Set_LCD_REG(0x00C1,0x0000);    // BGR bit = “0” Note 2
Set_LCD_REG(0x000E,0x0000);
Set_LCD_REG(0x000F,0x0000);
Set_LCD_REG(0x0010,0x0000);
Set_LCD_REG(0x0011,0x0000);
Set_LCD_REG(0x0012,0x0000);
Set_LCD_REG(0x0013,0x0000);
Set_LCD_REG(0x0014,0x0000);
Set_LCD_REG(0x0015,0x0000);
Set_LCD_REG(0x0016,0x0000);
Set_LCD_REG(0x0017,0x0000);
Set_LCD_REG(0x0034,0x0001);
Set_LCD_REG(0x0035,0x0000);
Set_LCD_REG(0x004B,0x0000);
Set_LCD_REG(0x004C,0x0000);
Set_LCD_REG(0x004E,0x0000);
Set_LCD_REG(0x004F,0x0000);
Set_LCD_REG(0x0050,0x0000);

Set_LCD_REG(0x003C,0x0000);
Set_LCD_REG(0x003D,0x0000);
Set_LCD_REG(0x003E,0x0001);
Set_LCD_REG(0x003F,0x003F);
Set_LCD_REG(0x0040,0x0002);
Set_LCD_REG(0x0041,0x0002);

Set_LCD_REG(0x0042,0x0000);
Set_LCD_REG(0x0043,0x0000);
Set_LCD_REG(0x0044,0x0000);
Set_LCD_REG(0x0045,0x0000);
Set_LCD_REG(0x0046,0x00EF);
Set_LCD_REG(0x0047,0x0000);
Set_LCD_REG(0x0048,0x0000);
Set_LCD_REG(0x0049,0x0001);
Set_LCD_REG(0x004A,0x003F);

Set_LCD_REG(0x001D,0x0008);    // Gate scan direction setting
Set_LCD_REG(0x0086,0x0000);
Set_LCD_REG(0x0087,0x0030);
Set_LCD_REG(0x0088,0x0002);
Set_LCD_REG(0x0089,0x0005);
Set_LCD_REG(0x008D,0x0001);    // Register set-up mode for one line clock number
Set_LCD_REG(0x008B,0x0030)    // One line SYSCLK number in one-line scan
Set_LCD_REG(0x0033,0x0001);    // N line inversion setting
Set_LCD_REG(0x0037,0x0001);    // Scanning method setting
Set_LCD_REG(0x0076,0x0000);
```

```
//############### void Gamma_Set(void) ##################//

Set_LCD_REG(0x008F,0x0000);
Set_LCD_REG(0x0090,0x0077);
Set_LCD_REG(0x0091,0x0007);
Set_LCD_REG(0x0092,0x0054);
Set_LCD_REG(0x0093,0x0007);
Set_LCD_REG(0x0094,0x0000);
Set_LCD_REG(0x0095,0x0077);
Set_LCD_REG(0x0096,0x0045);
Set_LCD_REG(0x0097,0x0000);
Set_LCD_REG(0x0098,0x0006);
Set_LCD_REG(0x0099,0x0003);
Set_LCD_REG(0x009A,0x0000);

//############### void Display_On(void) ##################//

Set_LCD_REG(0x003B,0x0001);
DelayX1ms(40);
Set_LCD_REG(0x0000,0x0020);

}
```

Note:

1. **Change the default setting of internal test register for normal display.**
2. **Change the default setting of the nee-added register in new-version chip for BGR setting.**

3. When using initial code as above for CMO 2.2" glass, the gamma curve is as follow



Blue Line : Ideal γ = 2.2
Red Line : Measure Data

The reference setting of into standby mode

```
// This initial for CMO's 2.2" panel,
// Using MPU 16Bits /18Bits interface,
// Operation voltage => Vcc = Vci = 2.8V.

void LCD_HX8312A_INTO_STB(void)
{
      //################ void Display_Off_Set(void) ###################//

      Set_LCD_REG(0x0000,0x00A0);
      DelayX1ms(40);
      Set_LCD_REG(0x003B,0x0000);

      //################ void Power_Off_Set(void) ###################//

      Set_LCD_REG(0x001E,0x0001);   // VCOM off
      Set_LCD_REG(0x001B,0x0008);   // VS / VDH Power off
      Set_LCD_REG(0x001C,0x0000);   // Step up circuit operating current off
      Set_LCD_REG(0x0024,0x0000);   // V18 and VCOM regulator current off
      Set_LCD_REG(0x0018,0x0000);

      //################ Into stand by mode    ###################//

      Set_LCD_REG(0x0001,0x0011);   // Internal oscillator stop
      Set_LCD_REG(0x0000,0x0028);   // Into stand by mode

}
```

Note:

1. **In standby mode, only register can be updated and the display RAM can not be updated. The display RAM data can be retained in the stand by mode operation.**

.

The reference setting of stand by mode cancel

```
void LCD_HX8312A_STB_Cancel(void)
{
    //############### Stand by mode cancel    ##################//

    Set_LCD_REG(0x0000,0x00A0);    // Stand by mode cancel
    Set_LCD_REG(0x0001,0x0010);    // Internal oscillator start
    DelayX1ms(10);

    //###############    Power_on_Set ##################//

    Set_LCD_REG(0x001C,0x0073);    // Step up circuit operating current setting
    Set_LCD_REG(0x0024,0x0074);    // V18 and VCOM regulator current setting

    Set_LCD_REG(0x0018,0x00C1);    // VR1 and VR2 regulator on
    DelayX1ms(10);

    Set_LCD_REG(0x0018,0x00C5);    // DDVDH turn on
    Set_LCD_REG(0x0018,0x00E5);    // VCL turn on
    DelayX1ms(60);

    Set_LCD_REG(0x0018,0x00F5);    // VGH and VGL turn on
    DelayX1ms(60);

    Set_LCD_REG(0x001B,0x0009);    // VS/VDH turn on and set
    DelayX1ms(10);

    Set_LCD_REG(0x001E,0x0081);    // VCOM operation start
    DelayX1ms(10);

    //############### void Display_On(void) ##################//

    Set_LCD_REG(0x003B,0x0001);
    DelayX1ms(40);
    Set_LCD_REG(0x0000,0x0020);
```

The reference setting of into OFF mode

```
// This initial for CMO's 2.2" panel,
// Using MPU 16Bits /18Bits interface,
// Operation voltage => Vcc = Vci = 2.8V.

void LCD_HX8312A_Into_OFF(void)
{
    //############### void Display_Off_Set(void) ##################//

    Set_LCD_REG(0x0000,0x00A0);
    DelayX1ms(40);
    Set_LCD_REG(0x003B,0x0000);

    //############### void Power_Off_Set(void) ##################//

    Set_LCD_REG(0x001E,0x0001);   // VCOM off
    Set_LCD_REG(0x001B,0x0008);   // VS / VDH Power off
    Set_LCD_REG(0x001C,0x0000);   // Step up circuit operating current off
    Set_LCD_REG(0x0024,0x0000);   // V18 and VCOM regulator current off
    Set_LCD_REG(0x0018,0x0000);

    //############### Into OFF mode   ##################//

    Set_LCD_REG(0x0001,0x0011);   // Internal oscillator stop
    Set_LCD_REG(0x00C0,0x0080);   // Into OFF mode

}
```

Note:

1. **In OFF mode, only OFFMOD bit (D7 bit of R192) can be updated. Other register and the display RAM can not be updated. The display RAM data may not be retained in the off mode operation , and need to rewrite after off mode canceling.**

The reference setting of OFF mode cancel

```
void LCD_HX8312A_OFF_Cancel(void)
{
    //############### OFF mode cancel   ##################//

    Set_LCD_REG(0x00C0,0x0000);   // OFF mode cancel
    Set_LCD_REG(0x0001,0x0010);   // Internal oscillator start
    DelayX1ms(10);

    //###############   Power_on_Set ##################//

    Set_LCD_REG(0x001C,0x0073);   // Step up circuit operating current setting
    Set_LCD_REG(0x0024,0x0074);   // V18 and VCOM regulator current setting

    Set_LCD_REG(0x0018,0x00C1);   // VR1 and VR2 regulator on
    DelayX1ms(10);

    Set_LCD_REG(0x0018,0x00C5);   // DDVDH turn on
    Set_LCD_REG(0x0018,0x00E5);   // VCL turn on
    DelayX1ms(60);

    Set_LCD_REG(0x0018,0x00F5);   // VGH and VGL turn on
    DelayX1ms(60);

    Set_LCD_REG(0x001B,0x0009);   // VS/VDH turn on and set
    DelayX1ms(10);

    Set_LCD_REG(0x001E,0x0081);   // VCOM operation start
    DelayX1ms(10);

    //############### void Display_On(void) ##################//

    Set_LCD_REG(0x003B,0x0001);
    DelayX1ms(40);
    Set_LCD_REG(0x0000,0x0020);
```

11. Reversion History

Version	EFF. Date	Description Changes
01	2005/07/14	New Setup
02	2005/10/04	1.Add Note 5 in p.22. 2.Add Note 1, 2 in p.41. 3. Add and correct the initial code (Blue Item) in p.39 ~ p.45. 4. Correct the " X address" in Table 9.7~9.9 in p.37~p.38