LCD MODULE SPECIFICATION

Products Name:APAX T14A1
35.7CM(14.1 INCH) XGA(1024x768)
262K COLOR TFT LCD MODULE
3.3V

● **Preliminary Specification**
 This technical specification is tentative and it will be changed without notice.

i Contents

1.0   Handing Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnection from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary.   At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside.   Otherwise the TFT Module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury.   Please follow local ordinances or regulations for disposal.
13) Small amount of materials having no flammability grade is used in the LCD Module. The LCD module should be supplied by power complied with requirements of Limited Power Source (2.11, IEC60950 or UL1950), or be applied exemption.
14) The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit (2.4, IEC60950 or UL1950).   Do not connect the CFL in Hazardous Voltage Circuit.

2.0   General Description

This specification applies to the 14.1 inch Color TFT/LCD Module
This Module is designed for a display unit of notebook style personal computer.
The screen format is intended to support the XGA (1024(H) x 768(V)) screen and 262k colors (RGB 6-bits data driver).
All input signals are LVDS interface compatible.
This module does not contain an inverter card for backlight.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	357(14.1")
Active Area	[mm]	285.7(H) x 214.3(V)
Pixels H x V		1024(x3) x 768
Pixel Pitch	[mm]	0.279(per one triad) x 0.279
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
Typical White Luminance(ICFL=6.5mA)	[cd/m^2]	140 Typ.(5 points average)
Contrast Ratio		200 : 1 Typ.
Optical Rise Time/Fall Time	[msec]	30 Typ., 50 Max.
Nominal Input Voltage VDD	[Volt]	+3.3 Typ.
Typical Power Consumption (VDD line + VCFL line)	[Watt]	5.2(w/o Inverter, All black pattern) 1.4(VDD) Typ., 3.8(Lamp) Typ.
Weight	[Grams]	535 Typ. (w/o Inverter)
Physical Size	[mm]	298.5(W) x 226.5(H) x 6.1(D) Typ.
Electrical Interface		R/G/B Data, 3 Sync, Signals, Clock (4 pairs LVDS)
Support Color		Native 262K colors (RGB 6-bit data driver)
Temperature Range Operating Storage (Shipping)	[^{o}C] [^{o}C]	0 to +50 -20 to +60

2.2 Functional Block Diagram

The following diagram shows the functional block of the 14.1 inches Color TFT/LCD Module:
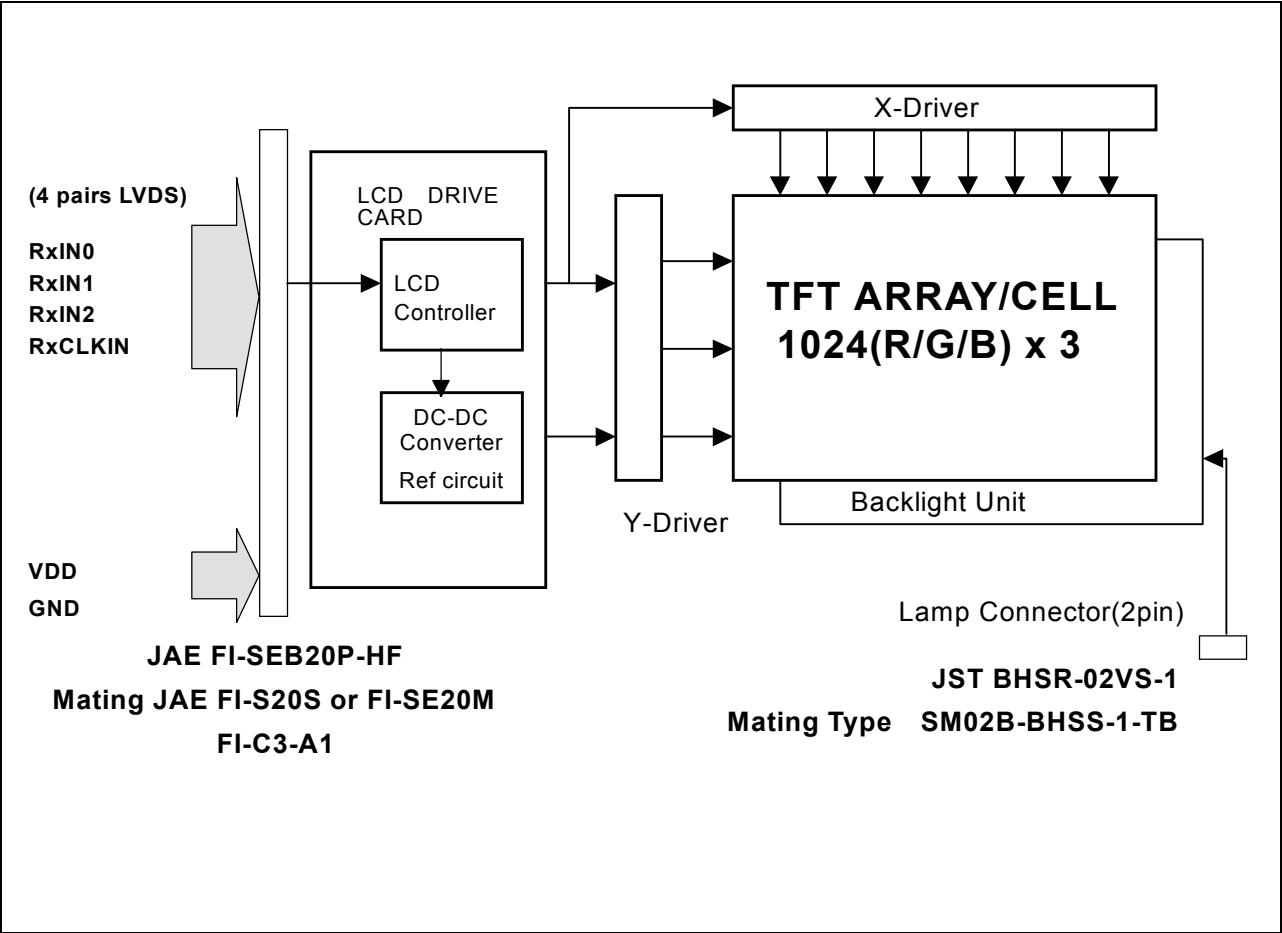
3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	[Volt]	
Input Voltage of Signal	Vin	-0.3	VDD+0.3	[Volt]	
CCFL Inrush current	ICFLL	-	20	[mA]	Note 2
CCFL Current	ICFL	-	7	[mA] rms	
CCFL Ignition Voltage	Vs	-	1,600	Vrms	
Operating Temperature	TOP	0	+50	[^{o}C]	Note 1
Operating Humidity	HOP	8	95	[%RH]	Note 1
Storage Temperature	TST	-20	+60	[^{o}C]	Note 1
Storage Humidity	HST	5	95	[%RH]	Note 1
Vibration			1.5 10-200	G Hz	
Shock			50 18	G ms	Half sine wave

Note 1 : Maximum Wet-Bulb should be 39℃ and No condensation.

Note 2 : Duration=50 msec. Max.

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25℃ condition:

Item		Conditions		Typ.	Note
Viewing Angle	[degree] [degree]	Horizontal (Right) K = 10 (Left)		40 40	— —
K: Contrast Ratio	[degree] [degree]	Vertical (Upper) K = 10 (Lower)		15 30	— —
Contrast ratio				200	—
Response Time	[msec]	Rising		30	50(Max.)
	[msec]	Falling		30	50(Max.)
Color		Red	x	0.620	±0.04
Chromaticity		Red	y	0.345	±0.03
Coordinates (CIE)		Green	x	0.299	±0.03
		Green	y	0.559	±0.03
		Blue	x	0.154	±0.03
		Blue	y	0.122	±0.04
		White	x	0.313	±0.03
		White	y	0.329	±0.03
White Luminance (CCFL 6.5mA)	[cd/m^2]			150 (Center) 140(5points average)	

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	FI-SEB20P-HF
Mating Housing/Part Number	FI-S20S or FI-SE20M or FI-S20S with Shell
Mating Contact/Part Number	FI-C3-A1

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

5.2 Signal Pin

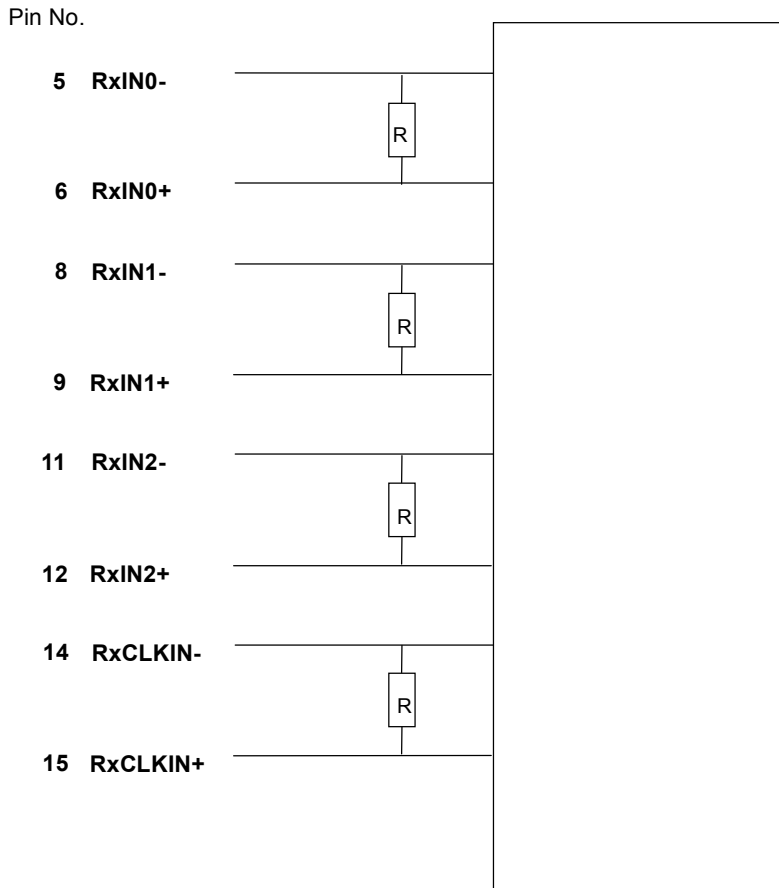| Pin#	Signal Name	Pin#	Signal Name
1	VDD	2	VDD
3	GND	4	GND
5	RxIN0-	6	RxIN0+
7	GND	8	RxIN1-
9	RxIN1+	10	GND
11	RxIN2-	12	RxIN2+
13	GND	14	RxCLKIN-
15	RxCLKIN+	16	GND
17	Reserved	18	Reserved
19	GND	20	GND

5.3 Signal Description

The module using a LVDS receiver. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84 (negative edge sampling) or compatible.

Signal Name	Description
RxIN0-, RxIN0+	LVDS differential data input(Red0-Red5, Green0)
RxIN1-, RxIN1+	LVDS differential data input(Green1-Green5, Blue0-Blue1)
RxIN2-, RxIN2+	LVDS differential data input(Blue2-Blue5, Hsync, Vsync, DSPTMG)
RxCLKIN-, RxCLKIN0+	LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

Note: Input signals shall be low or Hi-Z state when VDD is off.
Internal circuit of LVDS inputs are as following.

Signal Input

SN75LVDS86 or Compatible

Pin No.

5	RxIN0-
6	RxIN0+
8	RxIN1-
9	RxIN1+
11	RxIN2-
12	RxIN2+
14	RxCLKIN-
15	RxCLKIN+

The module uses a 100ohm resistor between positive and negative data lines of each receiver input

Signal Name	Description	
+RED5	Red Data 5 (MSB)	Red-pixel Data
+RED4	Red Data 4	Each red pixel's brightness data consists of
+RED3	Red Data 3	these 6 bits pixel data.
+RED2	Red Data 2	
+RED1	Red Data 1	
+RED0	Red Data 0 (LSB)	
	Red-pixel Data	
+GREEN 5	Green Data 5 (MSB)	Green-pixel Data

+GREEN 4 +GREEN 3 +GREEN 2 +GREEN 1 +GREEN 0	Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) **Green-pixel Data**	Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 +BLUE 4 +BLUE 3 +BLUE 2 +BLUE 1 +BLUE 0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) **Blue-pixel Data**	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
-DTCLK	**Data Clock**	The typical frequency is 65.0 MHz. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG	**Display Timing**	This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	**Vertical Sync**	The signal is synchronized to -DTCLK .
HSYNC	**Horizontal Sync**	The signal is synchronized to -DTCLK .

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

5.4 Signal Electrical Characteristics

Input signals shall be low or Hi-Z state when VDD is off.

It is recommended to refer the specifications of SN75LVDS86DGG(Taxas Instruments) in detail.
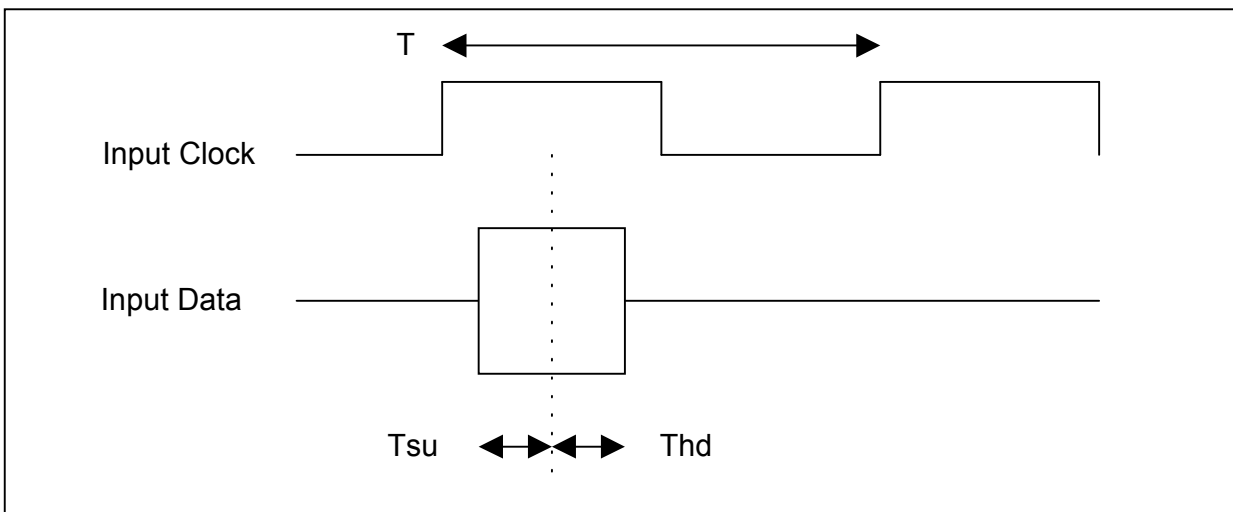
Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Voltage(Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Voltage(Vcm=+1.2V)	-100		[mV]

LVDS Macro AC characteristics are as follows:

	Min.	Max.
Clock Frequency (T)	50MHz	67MHz

Data Setup Time (Tsu)	600ps	
Data Hold Time (Thd)	600ps	

```
         T  ◄──────────────────────►
Input Clock ____┌──────┐        ┌──────┐
                │      │        │      │
            ____│      └────────┘      └──
                 ┌────┐
Input Data  _____│    │_____
                 └────┘
            Tsu  ◄─►◄─►  Thd
```

5.5 Signal for Lamp connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

6.0 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

	0	1						1022	1023	

Pixel array diagram:

1st Line: R G B R G B - - - - - - - - - - - - R G B R G B
...
768th Line: R G B R G B - - - - - - - - - - - - R G B R G B

7.0 Parameter guide line for CFL Inverter

Parameter	Min	DP-1 Note 1	DP-2 Note 2	Max	Units	Condition
White Luminance 5 points average	—	85	140	—	[cd/m^2]	(Ta=25℃)
CCFL current(ICFL)	3.0	3.8	6.5	7.0	[mA] rms	(Ta=25℃) **Note 2**
CCFL Frequency(FCFL)	40	50	50	60	[KHz]	(Ta=25℃) **Note 3**
CCFL Ignition Voltage(Vs)	1,400	—	—	—	[Volt] rms	(Ta= 0℃) **Note 4**
CCFL Voltage (Reference) (VCFL)	—	670	585	—	[Volt] rms	(Ta=25℃) **Note 5**
CCFL Power consumption (PCFL)	—	2.5	3.8	—	[Watt]	(Ta=25℃) **Note 5**

Note 1: DP-1 and DP-2 are ADT recommended Design Points.

*1 All of characteristics listed are measured under the condition using the ADT Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit ver carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be emplyed the inverter which has "Duty Dimming", if ICFL is less than 4mA.

Note 3: CFL discharge frequency shouldbe carefully determined to avoid interference between inverter and TFT LCD.

Note 4: CFL inverter should be able to give out a power that has a generating capacity of over 1,400 voltage. Lamp units need 1,400 voltage minimum for ignition.

Note 5: Calculator value for reference (ICFL×VCFL=PCFL)

8.0 Interface Timings

Basically, interface timings should match the VESA 1024x768 /60Hz (VG901101) manufacturing guide line timing.

8.1 Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit
fdck	DTCLK Frequency		65.00		[MHz]
tck	DTCLK cycle time		15.38		[nsec]
tx	X total time	1206	1344	2047	[tck]
tacx	X active time	129	1024		[tck]
tbkx	X blank time	90	320		[tck]
Hsync	H frequency		48.363		[KHz]
Hsw	H-Sync width	2	136		[tck]
Hbp	H back porch	1	160		[tck]
Hfp	H front porch	0	24		[tck]
ty	Y total time	771	806	1023	[tx]
tacy	Y active time		768		[tx]
Vsync	Frame rate	(55)	60	61	[Hz]
Vw	V-sync Width	1	6		[tx]
Vfp	V-sync front porch	1	3		[tx]
Vbp	V-sync back porch	7	29	63	[tx]

Note: Hsw(H-sync width) + Hbp(H-sync back porch) should be less than 515 tck.

8.2 Timing Definition
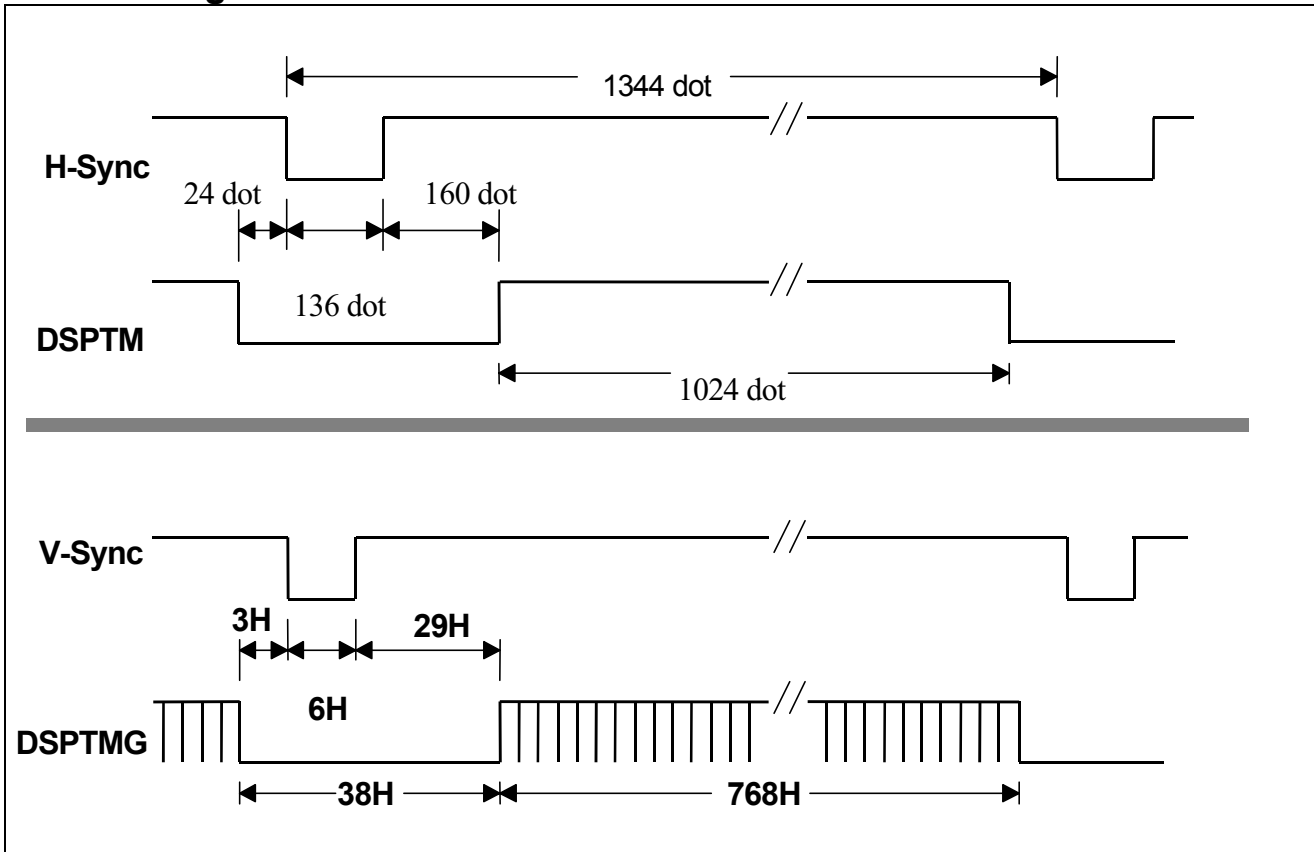
9.0 Power Consumption

Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	Load Capacitance 20uF
PDD	VDD Power		1.4		[Watt]	All Black Pattern
PDD Max	VDD Power max			1.65	[Watt]	Max Pattern **Note**
IDD	IDD Current		420		mA	All Black Pattern
IDD Max	IDD Current max			500	mA	Max Pattern **Note**
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	[mV] p-p	

10. Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.
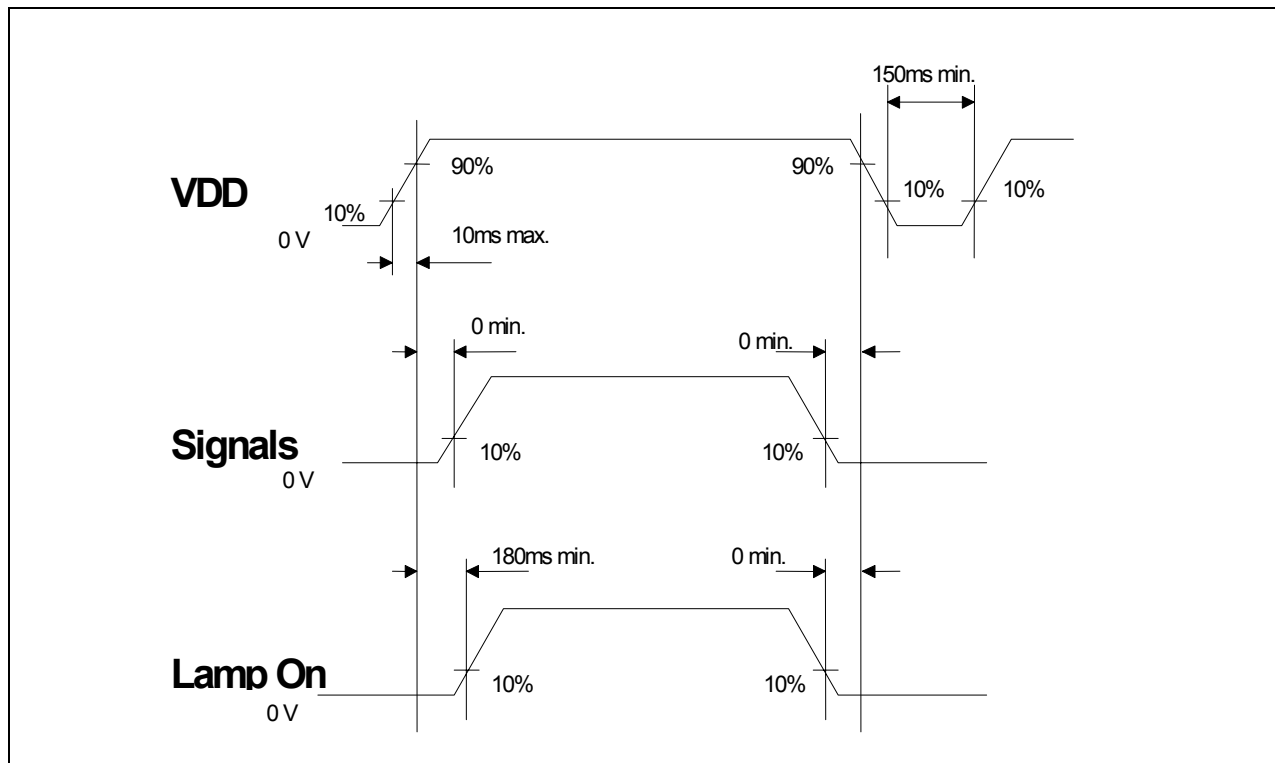
11.0 Environment

The display module will meet the provision of this specification during operating condition or after storage or shipment condition specified below. Operation at 10% beyond the specified range will not cause physical damage to the unit.

11.1 Temperature and Humidity
11.1.1 Operating Conditions

The display module operates error free, when operated under the following conditions;

Temperature	0 ^{0}C to 50 ^{0}C
Relative Humidity	8% to 95%
Wet Bulb Temperature	39.0 ^{0}C

11.1.2 Shipping Conditions

The display module operates error free, after the following conditions;

Temperature	-20 ^{0}C to 60 ^{0}C
Relative Humidity	8% to 95%
Wet Bulb Temperature	39.0 ^{0}C

11.2 Atmospheric Pressure

The display assembly is capable of being operated without affecting its operations over the pressure range as following specified;

	Pressure	Note
Maximum Pressure	1040hPa	0m = sea level
Minimum Pressure	674hPa	3048m = 10.000 feet

Note : Non-operation attitude limit of this display module = 30,000 feet. = 9145 m.

11.3 Thermal Shock

The display module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20^{0}C to 60^{0}C, and back again.

Thermal shock cycle
-20 ^{0}C for 30min
60 ^{0}C for 30min

Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before powering on.

12.0 Reliability

This display module and the packaging of that will comply following standards.

122.1 Failure Criteria

The display assembly will be considered as failing unit when it no longer meets any of the requirements stated in this specification. Only as for maximum white luminance, following criteria is applicable.

12.2 Failure Rate

The average failure rate of the display module (from first power-on cycle till 1,000 hours later) will not exceed 1.0%. The average failure rate of the display module from 1,000 hours until 10,000 hours will not exceed 0.70% per 11000 hours. Above failure rates correspond to the field performance of 0.0016/MM for 1+30 and 0.0010/MM for FF.

12.2.1 Usage

The assumed usage for the above criteria is:
- 220 power-on hours per month
- 500 power on/off cycles per month
- Maximum brightness setting
- Operation to be within office environment (25^0C typical)

12.2.2 Component De-rating

All the components used in this device will be checked the load condition to meet the failure rate criteria.

12.3 CCFL Life

The assumed CCFL Life will be longer than 20,000 hours at the general test condition.

12.4 ON/OFF Cycle

The display module will be capable of being operated over the following ON/OFF Cycles.

ON/OFF	Value	Cycle
+Vin and CCFL power	35,000	10 seconds on/10 seconds off

13.0   Safety

13.1 Sharp Edge Requirements

There will be no sharp edges or comers on the display assembly that could cause injury.

13.2 Materials
13.2.1 Toxicity

There will be no carcinogenic materials used anywhere in the display module. If toxic materials are used, they will be reviewed and approved by the responsible ADT Toxicologist.

13.2.2 Flammability

All components including electrical components that do not meet the flammability grade UL94-V1 in the module will complete the flammability rating exception approval process. The printed circuit board will be made from material rated 94-V1 or better. The actual UL flammability rating will be printed on the printed circuit board.

13.3 Capacitors

If any polarized capacitors are used in the display assembly, provisions will be made to keep them from being inserted backwards.

13.4 Hazardous Voltages

Any point exceeding 42.4 volts meets the requirement of the limited current circuit. The current through a $2K\Omega$ resistance is less than 0.7 x f (kHz) mA.

11.0 Mechanical Characteristics

SHEET 1 OF 2
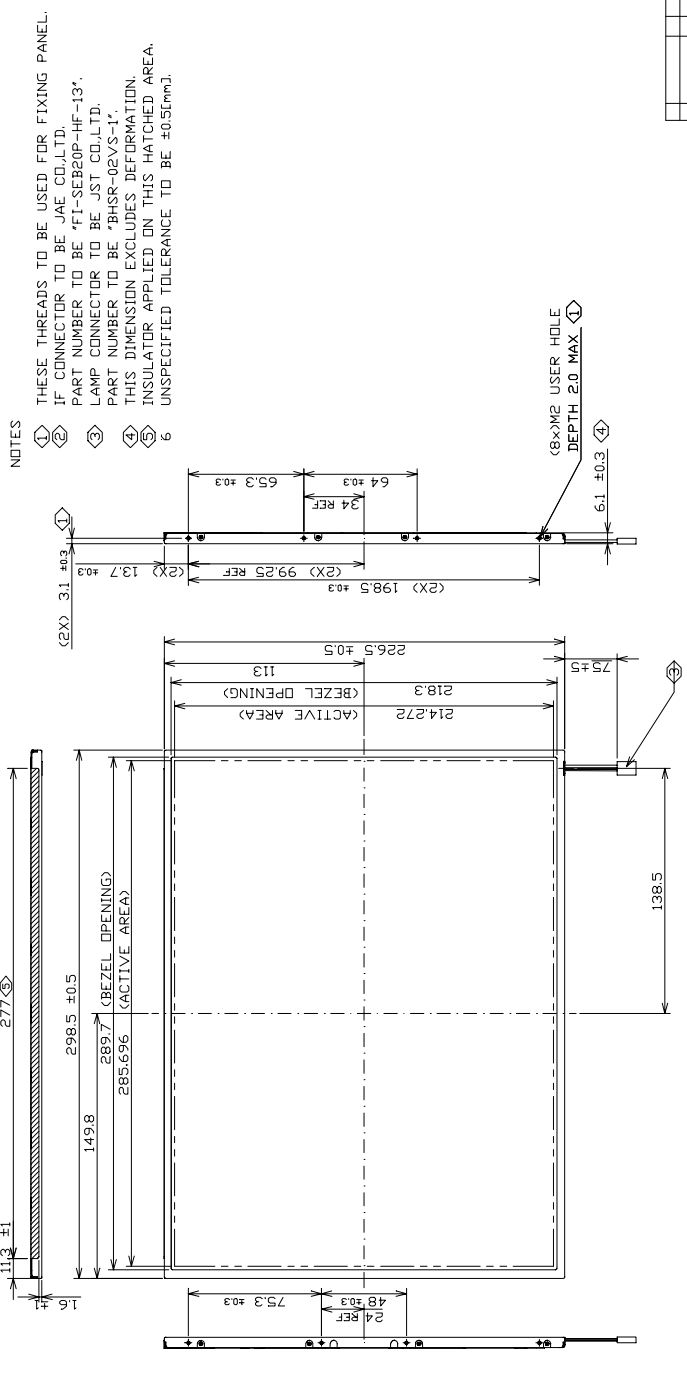
NOTES

1. THESE THREADS TO BE USED FOR FIXING PANEL.
2. IF CONNECTOR TO BE JAE CO.,LTD.
   PART NUMBER TO BE "FI-SEB20P-HF-13".
3. LAMP CONNECTOR TO BE JST CO.,LTD.
   PART NUMBER TO BE "BHSR-02VS-1".
4. THIS DIMENSION EXCLUDES DEFORMATION.
5. INSULATOR APPLIED ON THIS HATCHED AREA.
6. UNSPECIFIED TOLERANCE TO BE ±0.5(mm).

(8x)M2 USER HOLE
DEPTH 2.0 MAX

t=6.1 AREA

57.7

3.5 (t=5.8)

33.1 (t=6.1)

74.6

60

167.8 (t=5.5 to 4.1)

45

60 (t=6.1)

112.8 (t=6.1)

215.1 (2X) (t=6.1)

25 (t=6.1)

NAME REF DWG

L141X1

UNITS OR ASSEMBLY		NAME	REF DWG
DRN	STAR		
DSN			
CKD	TINY		
APPD	TINY		

Acer Display Technology, Inc.

PART NO. 97.V01S9.001

SHEET 2 OF 2