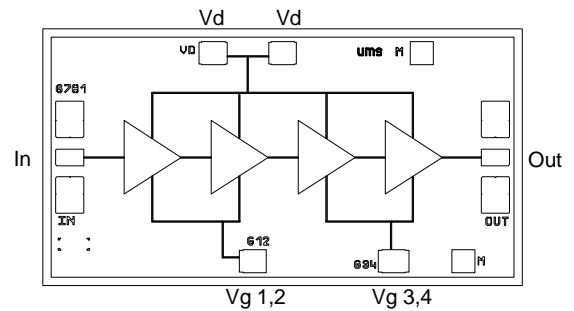


# 36-40GHz Low Noise Very High Gain Amplifier

## GaAs Monolithic Microwave IC

### Description

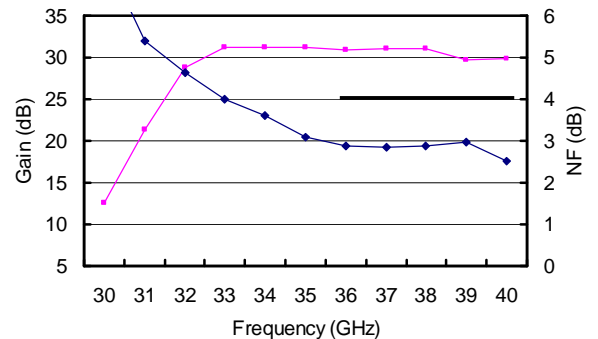
The CHA2395 is a four-stage monolithic low noise amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The circuit is manufactured with a pHEMT process: 0.25 $\mu$ m gate length, via holes through the substrate, air bridges and electron beam gate lithography. It is available in chip form.



### Main Features

- Broadband performances
- 3.0dB Noise Figure
- 30dB gain
- $\pm 1.0$ dB gain flatness
- Low DC power consumption, 90mA@3.5V
- Chip size: 2.07 X 1.11 X 0.10 mm

Typical on wafer measurements



### Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	36		40	GHz
G	Small signal gain	25	30		dB
P1dB	Output power at 1dB gain compression	8	10		dBm
NF	Noise figure		3.0	4.0	dB

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

## Electrical Characteristics

Tamb = +25°C, Vd= 3.5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	36		40	GHz
G	Small signal gain (1)	25	30		dB
ΔG	Small signal gain flatness (1)		±1.5		dB
ΔGsb	Gain ripple over 40MHz ( within -30 ; +75°C )			0.5	dBpp
Is	Reverse isolation (1)	35	40		dB
P1dB	Output power at 1dB gain compression	8	10		dBm
VSWRin	Input VSWR (1)		2.5:1	3.0:1	
VSWRout	Output VSWR (1)		2.5:1	3.0:1	
NF	Noise figure (2)		3.0	4.0	dB
Vdc	DC Voltage Vd Vg	-2	3.5	4 +0.4	V V
Id	Bias current (2)		90		mA

(1) These values are representative of on-wafer measurements that are made without bonding wires at the RF ports.

(2) 90 mA is the typical bias current used for on wafer measurements, with adjusting Vg1,2 voltage for optimum noise figure and Vg3,4 adjusting for maximum gain.

## Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5	V
Vg	Gate bias voltage	-2.0 to +0.4	V
Vdg	Maximum drain to gate voltage (Vd - Vg)	+5.0	V
Id	Drain bias current	200	mA
Pin	Maximum peak input power overdrive (2)	+15	dBm
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s.

**Typical Scattering Parameters ( On wafer Sij measurements )**

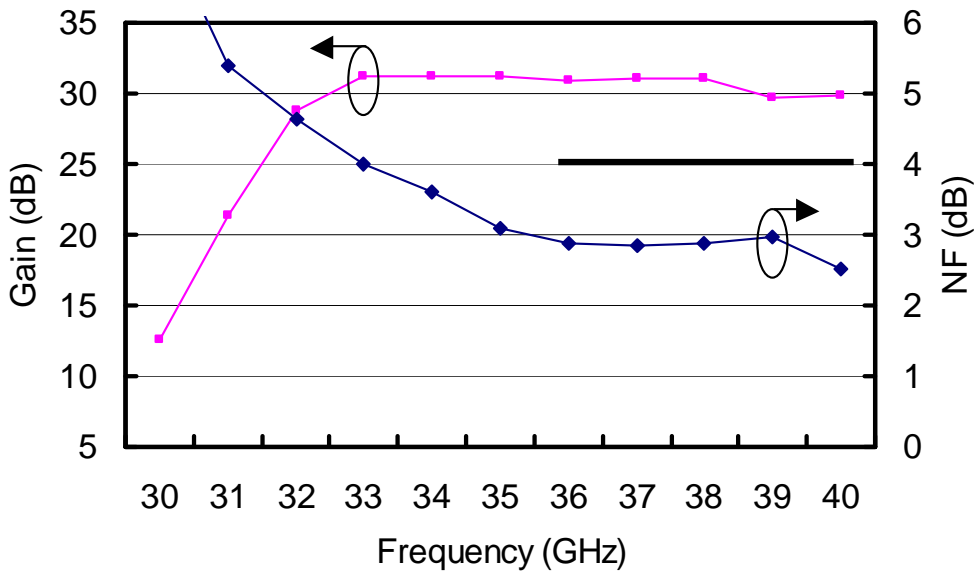
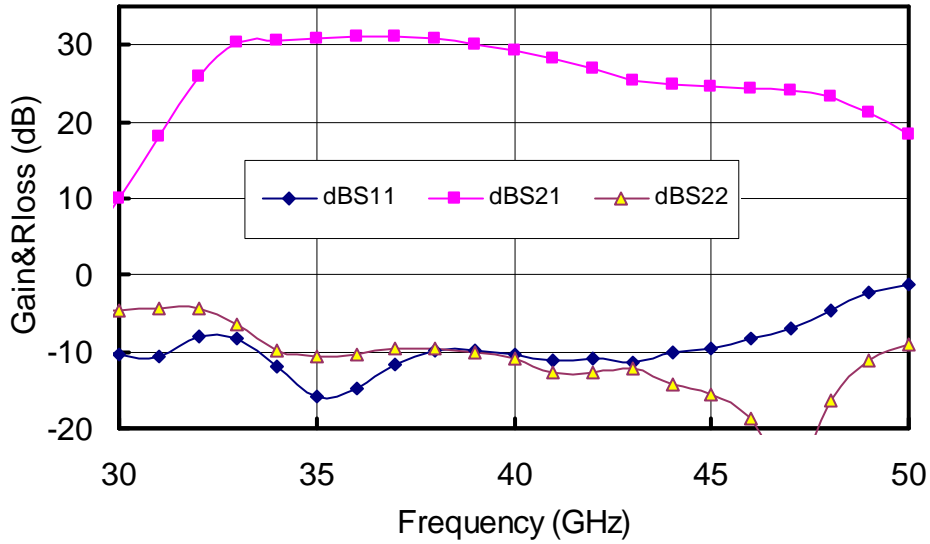
Bias Conditions : Vd= 3.5 Volt, Id = 90 mA.

Freq. GHz	S11 dB	S11 /°	S12 dB	S12 /°	S21 dB	S21 /°	S22 dB	S22 /°
10	-5,24	-150,46	-56,39	-137,29	-24,05	-93,70	-6,44	-135,98
11	-5,01	-158,16	-55,20	-143,40	-25,15	-112,11	-6,52	-142,09
12	-4,78	-165,56	-53,92	-154,87	-26,75	-128,23	-6,55	-148,02
13	-4,69	-174,08	-51,99	-164,65	-26,78	-139,11	-6,44	-151,89
14	-4,48	178,30	-50,31	175,46	-29,21	-171,28	-6,37	-157,82
15	-4,30	170,74	-50,32	148,72	-29,88	-145,86	-6,22	-163,81
16	-4,14	163,09	-49,22	142,18	-31,36	-164,90	-6,10	-169,58
17	-4,06	155,51	-49,15	127,08	-32,88	-167,67	-5,89	-175,56
18	-3,96	147,86	-48,70	105,03	-35,34	177,24	-5,79	177,73
19	-3,90	139,92	-51,67	105,23	-38,52	-157,62	-5,56	172,92
20	-3,86	131,40	-50,35	95,30	-38,79	-162,11	-5,26	165,80
21	-3,87	122,89	-49,65	83,53	-38,83	-167,49	-4,99	158,13
22	-3,89	113,01	-49,59	72,64	-46,84	157,47	-4,88	150,61
23	-4,01	103,05	-49,29	63,32	-41,57	21,50	-4,75	142,43
24	-4,20	92,06	-48,05	44,03	-30,98	8,81	-4,67	134,00
25	-4,54	79,42	-48,35	23,21	-23,89	-1,06	-4,58	124,88
26	-5,02	65,00	-49,93	-1,87	-17,47	-4,35	-4,53	115,26
27	-5,79	47,39	-52,57	-14,93	-11,19	-13,07	-4,53	104,69
28	-6,86	25,74	-58,44	-26,41	-4,59	-23,29	-4,50	93,03
29	-8,43	-4,01	-63,19	36,76	2,43	-38,25	-4,51	79,20
30	-10,32	-48,95	-55,24	45,06	10,00	-60,29	-4,54	62,45
31	-10,65	-117,68	-53,31	-1,55	18,04	-93,20	-4,40	39,47
32	-8,00	166,44	-53,65	-52,02	25,85	-144,54	-4,42	3,69
33	-8,21	89,15	-79,13	17,74	30,33	144,38	-6,32	-46,81
34	-11,99	29,31	-60,45	-9,35	30,68	82,74	-9,78	-94,59
35	-15,87	-33,40	-59,01	-74,65	30,91	36,21	-10,50	-134,35
<b>36</b>	<b>-14,87</b>	<b>-104,81</b>	<b>-57,53</b>	<b>-151,67</b>	<b>31,07</b>	<b>-6,18</b>	<b>-10,26</b>	<b>-167,64</b>
<b>37</b>	<b>-11,78</b>	<b>-165,28</b>	<b>-56,31</b>	<b>150,87</b>	<b>31,05</b>	<b>-47,23</b>	<b>-9,47</b>	<b>163,94</b>
<b>38</b>	<b>-9,85</b>	<b>150,77</b>	<b>-54,01</b>	<b>109,01</b>	<b>30,82</b>	<b>-86,98</b>	<b>-9,53</b>	<b>139,99</b>
<b>39</b>	<b>-9,90</b>	<b>110,22</b>	<b>-53,25</b>	<b>84,99</b>	<b>30,03</b>	<b>-124,36</b>	<b>-10,02</b>	<b>120,62</b>
<b>40</b>	<b>-10,31</b>	<b>70,60</b>	<b>-52,00</b>	<b>74,63</b>	<b>29,21</b>	<b>-159,55</b>	<b>-10,97</b>	<b>107,97</b>
41	-11,12	23,32	-49,03	82,09	28,21	167,67	-12,82	99,68
42	-10,97	-34,96	-44,98	72,62	26,87	135,99	-12,78	101,14
43	-11,41	-81,68	-44,03	33,59	25,36	111,44	-12,23	88,12
44	-10,12	-107,79	-43,67	15,35	24,92	87,03	-14,15	73,36
45	-9,49	-124,05	-43,94	-3,05	24,57	60,05	-15,44	63,47
46	-8,37	-137,10	-42,57	-16,03	24,33	31,65	-18,63	37,49
47	-6,94	-141,65	-42,19	-36,05	24,14	-0,62	-26,50	-44,90
48	-4,56	-148,72	-42,90	-62,08	23,38	-38,45	-16,32	-150,01
49	-2,37	-162,95	-45,30	-98,56	21,22	-76,12	-11,15	172,71
50	-1,12	-178,98	-46,39	-149,92	18,32	-110,54	-9,10	145,34

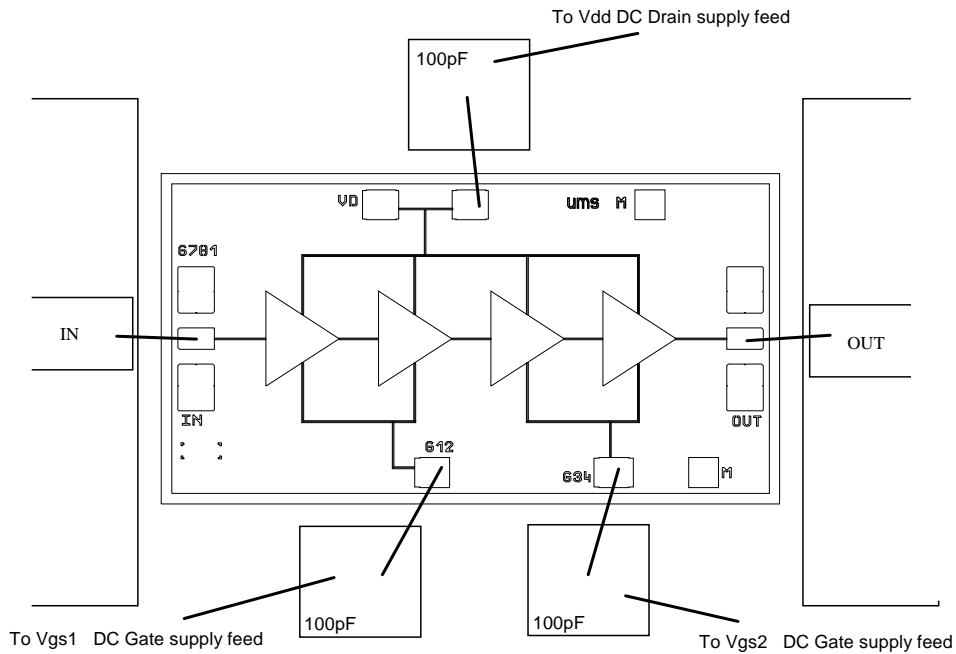
Typical on Wafer Measurements

Tamb = +25°C

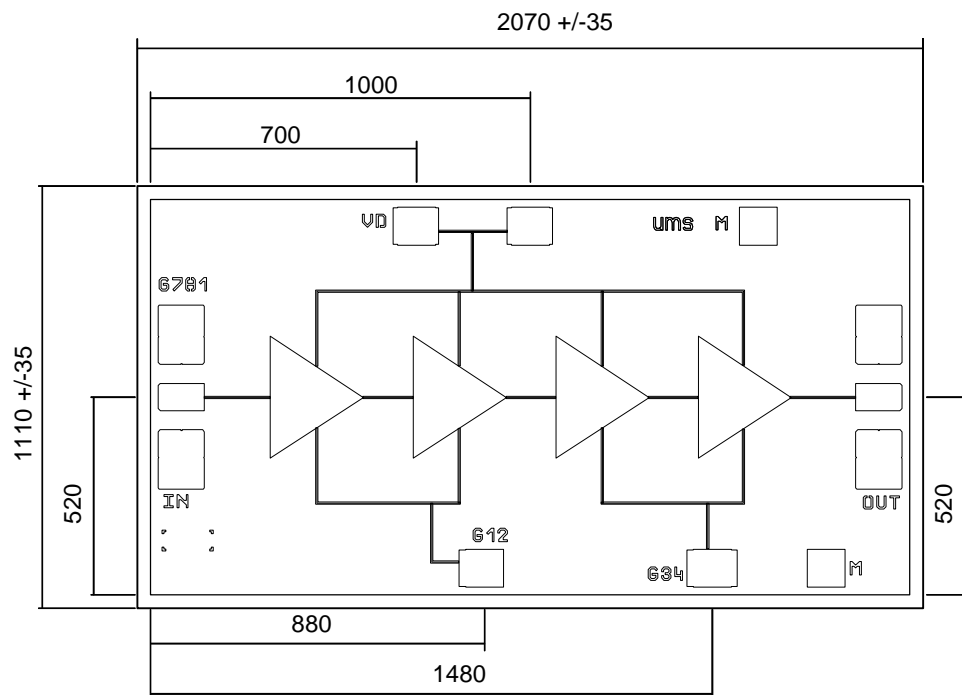
Vds=3.5V and Id=90mA



Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed.

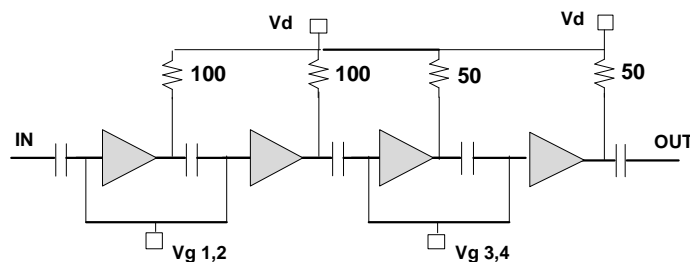


**Bonding pad positions.**

(Chip thickness: 100µm. All dimensions are in micrometers)

## Typical Bias Tuning for Low Noise Operation

The circuit schematic is given below:



For low noise operation, a separate access to the gate voltages of the two first stages ( $V_{g1,2}$ ), and of the two last stage ( $V_{g3,4}$ ) is provided. Nominal bias is obtained for a typical current of 60 mA for the output stages and 30 mA for the two first stages (90 mA for the amplifier).

The first step to bias the amplifier is to tune  $V_{g1,2} = -1V$ , and  $V_{g3,4}$  to drive 60 mA for the full amplifier. Then  $V_{g1,2}$  is increased to obtain 90 mA of current through the amplifier. A fine tuning of the noise figure may be obtained by modifying the  $V_{g1,2}$  bias voltage, but keeping the previous value for  $V_{g3,4}$ .

It is possible to reduce the total DC current by biasing  $V_{g3,4}$  to a more negative value. The consequences will be a reduction of gain and of the output power capabilities of the amplifier.

$V_d$  could be adjust in such a way that the  $V_d$ s (Drain to Source voltage of the internal transistor) is kept below 3.5V, knowing that all the transistors have the same sizes and with the given resistors.

## Ordering Information

Chip form : CHA2395-99F/00

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