Low Dropout Linear Regulator Controller

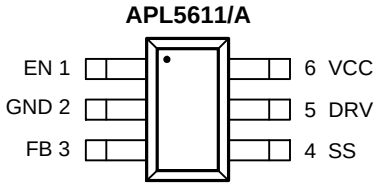
## Features

- **Wide Supply Voltage Range from 4.5 to 13.5V**
- **High Output Accuracy Over Operating Temperature and Loading Ranges**
- **Fast Transient Response**
- **Power-On-Reset Monitoring on VCC**
- **Programmable Soft-Start**
- **Low Shutdown Current**
- **Enable Control Function**
- **Under-Voltage Protection**
- **Two Versions of IC Available:**
  **- APL5611: UVP Activated after $V_{OUT}$ is Ready**
  **- APL5611A: UVP Activated after $V_{CC}$ is Supplied**
- **SOT-23-6 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

## Applications

- **Notebook PC Applications**
- **Motherboard Applications**

## Pin Configuration




**SOT-23-6**
**(Top View)**

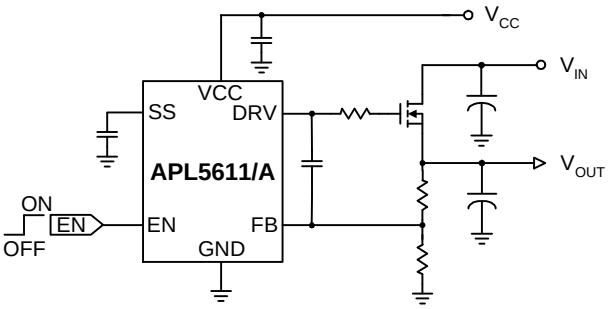
## General Description

The APL5611/A is a low dropout linear regulator controller. The APL5611/A could drive an external N-Channel MOSFET and provide an adjustable output by using an external resistive divider.

The APL5611/A integrates various functions. For example, a Power-On-Reset (POR) circuit monitors VCC supply voltage to prevent wrong operations; the function of Under-Voltage Protection (UVP) protects the device from short circuit condition. The soft-start of output voltage is adjustable by the external capacitor on SS pin. Moreover, the APL5611/A can be enabled by other power system; namely, holding the EN above 1.6V enables output and pulling the EN under 0.4 disables output.

The APL5611/A is available in a SOT-23-6 package.

## Simplified Application Circuit

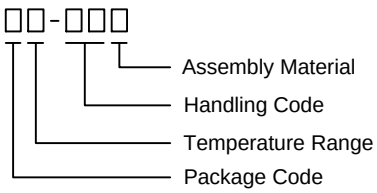



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.




Rev. A.5 - Oct., 2012

## Ordering and Marking Information

| | |
|---|---|
| APL5611<br>APL5611A<br>  | Package Code<br>C : SOT-23-6<br>Operating Ambient Temperature Range<br>I : -40 to 85 °C<br>Handling Code<br>TR : Tape & Reel<br>Assembly Material<br>G : Halogen and Lead Free Device |
| APL5611 C:  | X - Date Code |
| APL5611A C:  | X - Date Code |

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Absolute Maximum Ratings (Note 1 )

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{CC}$ | VCC Input Voltage (VCC to GND) | -0.3 to 15 | V |
| | EN, SS, to GND Voltage | -0.3 to 7 | V |
| $V_{FB}$ | FB to GND Voltage | -0.3 to 7 | V |
| $V_{DRV}$ | DRV to GND Voltage | -0.3 to $V_{CC}$+0.3 | V |
| $T_J$ | Maximum Junction Temperature | 150 | °C |
| $T_{STG}$ | Storage Temperature | -65 to 150 | °C |
| $T_{SDR}$ | Maximum Lead Soldering Temperature, 10 Seconds | 260 | °C |

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Thermal Characteristic

| Symbol | Parameter | Typical Value | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-Ambient Resistance in Free Air (Note 2)<br>SOT-23-6 | 250 | °C/W |

Note 2: $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air.

## Recommended Operating Conditions (Note 3)

| Symbol | Parameter | Range | Unit |
|---|---|---|---|
| $V_{CC}$ | VCC Input Voltage (VCC to GND) | 4.5 to 13.5 | V |
| $V_{EN}$ | EN to GND Voltage | 0 to 5.5 | V |
| $V_{OUT}$ | VOUT Output Voltage (Note4) | 0.8 ~ $V_{IN}$ - $V_{DROP}$ | V |
| $T_A$ | Ambient Temperature | -40 to 85 | °C |
| $T_J$ | Junction Temperature | -40 to 125 | °C |

Note 3: Refer to the typical application circuit.

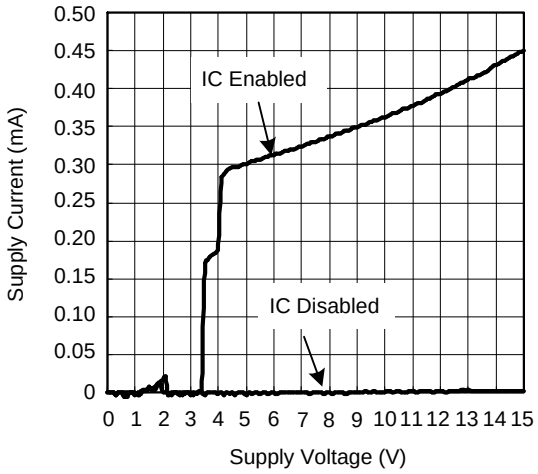
Note 4: $V_{DROP}$ defined as the $V_{IN}$ -$V_{OUT}$ voltage at $V_{OUT}$ = 98% normal $V_{OUT}$. The linear regulator must provide the output MOSFET with sufficient Gate-to-Source voltage ($V_{GS}$ = $V_{CC}$ - $V_{OUT}$) to regulate the output voltage.

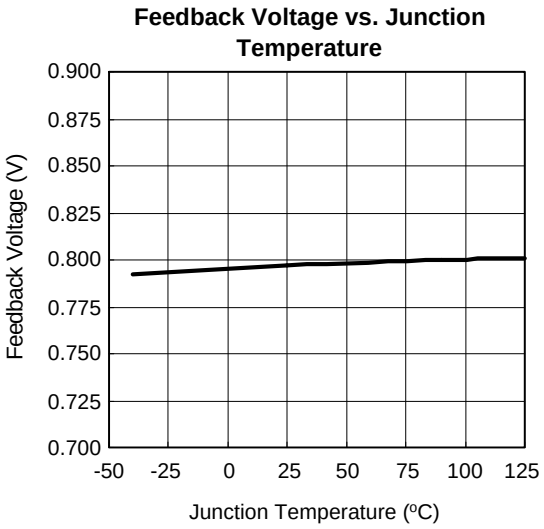
## Electrical Characteristics

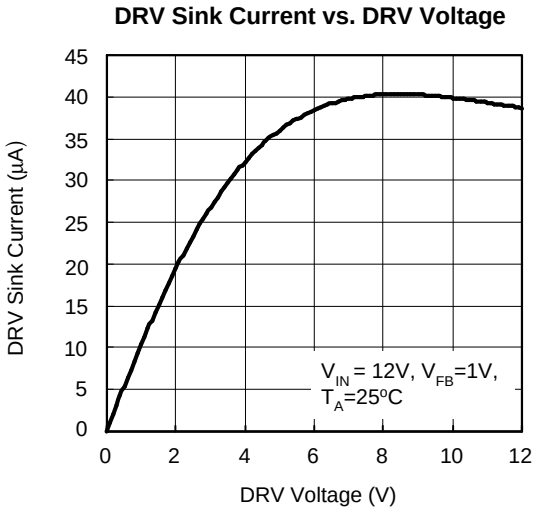
Unless otherwise specified, these specifications apply over $V_{CC}$ = 5/12V, $T_A$ = -40 to 85 °C. Typical values are at $T_A$ =25°C.

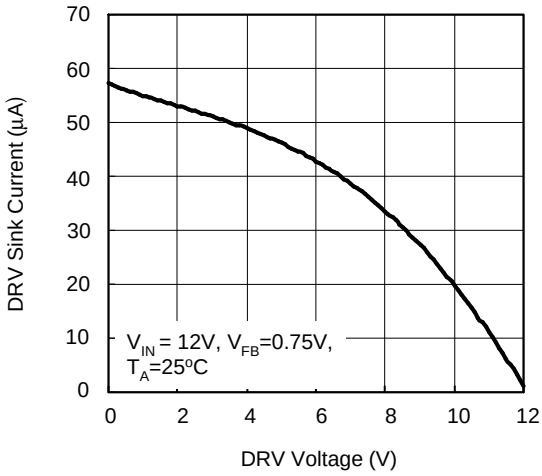
| Symbol | Parameter | Test Conditions | APL5611/A | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| **SUPPLY CURRENT** | | | | | | |
| $I_{CC}$ | VCC Supply Current | $V_{CC}$ = 12V | - | 0.8 | 1.0 | mA |
| | | $V_{CC}$ = 5V | - | 0.8 | 1.0 | |
| $I_{SD}$ | VCC Shutdown Current | $V_{CC}$ = 12V, EN=GND | - | - | 5 | µA |
| | | $V_{CC}$ = 5V, EN=GND | - | - | 5 | |
| **POWER-ON-RESET (POR)** | | | | | | |
| | VCC POR Threshold | $V_{CC}$ rising | 3.8 | 4.0 | 4.2 | V |
| | VCC POR Hysteresis | | - | 0.4 | - | V |
| **REFERENCE VOLTAGE** | | | | | | |
| $V_{REF}$ | Reference Voltage | $V_{CC}$ = 12V, $T_A$ = 25 °C | - | 0.8 | - | V |
| | Reference Voltage Accuracy | $V_{CC}$ = 12V | -1 | - | 1 | % |
| | Line Regulation | $V_{CC}$ = 4.5V to 13.2V | -1.5 | - | 1.5 | % |
| | FB Input Current | | -100 | - | 100 | nA |
| **ERROR AMPLIFIER** | | | | | | |
| | Unity Gain Bandwidth | $V_{CC}$ = 5/12V | - | 2 | - | MHz |
| | Open Loop DC Gain | $V_{CC}$ =12V, No Load | 60 | 80 | - | dB |
| PSRR | Power Supply Rejection Ratio | $V_{CC}$ =12V, 100Hz, No Load | 50 | - | - | dB |
| $V_{DRV (high)}$ | DRV High Voltage | $V_{CC}$ =12V, $I_{DRV (SOURCE)}$ = 5mA, $V_{FB}$ = 0.6V | 11.2 | 11.5 | - | V |
| | | $V_{CC}$ =5V, $I_{DRV (SOURCE)}$ = 5mA, $V_{FB}$ = 0.6V | - | 4.7 | - | |
| $V_{DRV (low)}$ | DRV Low Voltage | $V_{CC}$ =12V, $I_{DRV (SINK)}$ = 5mA, $V_{FB}$ = 1V | - | 0.5 | 1 | V |
| | | $V_{CC}$ =5V, $I_{DRV (SINK)}$ = 5mA, $V_{FB}$ = 1V | - | 0.8 | - | |
| $I_{DRV (source)}$ | DRV Source Current | $V_{CC}$ =12V, $V_{DRV}$ =6V, $V_{FB}$ = 0.6V | - | 50 | - | mA |
| | | $V_{CC}$ =5V, $V_{DRV}$ =2.5V, $V_{FB}$ = 0.6V | - | 10 | - | |
| $I_{DRV (sink)}$ | DRV Sink Current | $V_{CC}$ =12V, $V_{DRV}$ =6V, $V_{FB}$ = 1V | - | 40 | - | mA |
| | | $V_{CC}$ =5V, $V_{DRV}$ =2.5V, $V_{FB}$ = 1V | - | 10 | - | |
| **ENABLE** | | | | | | |
| $V_{EN (TH)}$ | EN Logic High Threshold Voltage | $V_{EN}$ rising, $T_A$=25°C | 0.55 | 0.8 | 1.05 | V |
| | EN Hysteresis | | - | 50 | - | mV |
| | EN Shutdown Debounce | $V_{EN}$ falling | - | 2 | - | µs |
| | EN Internal Pull High Current | | - | 5 | - | µA |
| **SOFT-START** | | | | | | |
| $I_{SS}$ | SS Current | | 3 | 4.5 | 6 | µA |
| **UNDER-VOLTAGE PROTECTION (UVP)** | | | | | | |
| $V_{UV (TH)}$ | Under-Voltage Threshold | $V_{EN}$ =5V, $V_{FB}$ falling | 68 | 75 | 82 | % |
| | UVP Debounce Interval | | - | 5 | - | µs |

## Typical Operating Characteristics



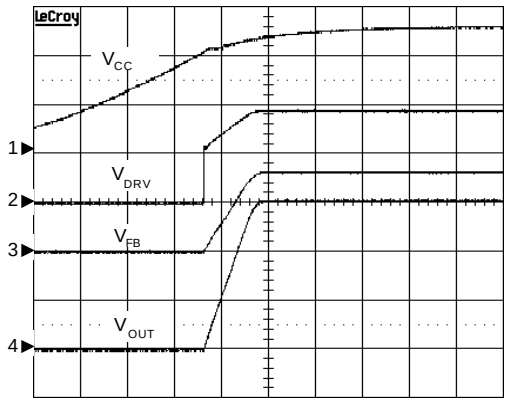



## Operating Waveforms

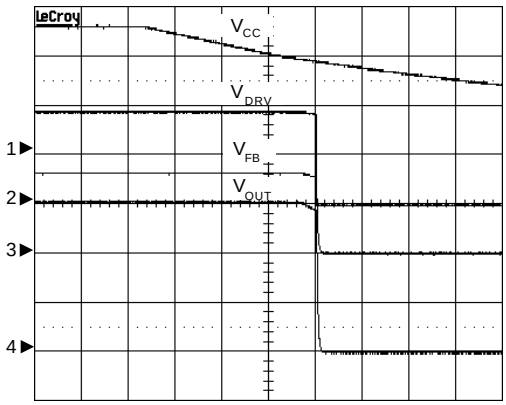
The test condition $T_A$= 25°C unless otherwise specified.

**Turn On Response**



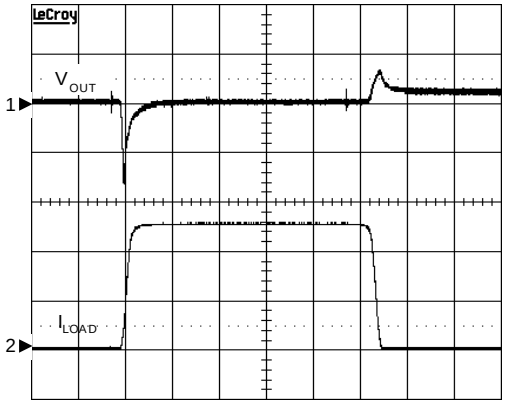

$V_{CC}$=5V, $V_{IN}$ =5V, $V_{OUT}$ =1.5V, $C_{IN}$ =33µF/ Electrolytic, $C_{OUT}$ =120µF/Electrolytic, $C_{SS}$ =0.01µF
CH1: $V_{CC}$, 2V/Div, DC
CH2: $V_{DRV}$, 2V/Div, DC
CH3: $V_{FB}$, 0.5V/Div, DC
CH4: $V_{OUT}$, 0.5V/Div, DC
TIME: 2ms/Div

**Turn Off Response**



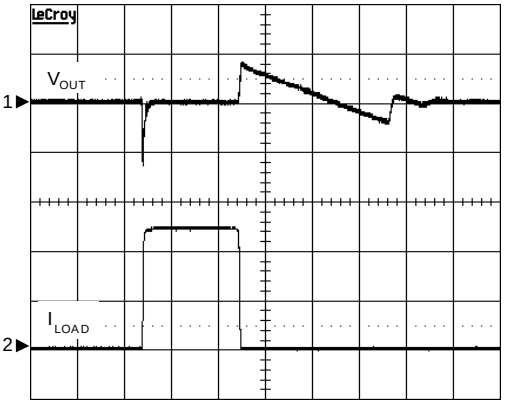

$V_{CC}$=5V, $V_{IN}$ =5V, $V_{OUT}$ =1.5V, $C_{IN}$ =33µF/ Electrolytic, $C_{OUT}$ =120µF/Electrolytic, $C_{SS}$ =0.01µF
CH1: $V_{CC}$, 2V/Div, DC
CH2: $V_{DRV}$, 2V/Div, DC
CH3: $V_{FB}$, 0.5V/Div, DC
CH4: $V_{OUT}$, 0.5V/Div, DC
TIME: 50ms/Div

**Load Transient Response-1**




$V_{CC}$=5V, $V_{IN}$ =5V, $V_{OUT}$=1.2V,
$I_{LOAD}$ =0-5-0A(rising/falling edge=1A/µs ),
$C_{IN}$ =22µF/MLCC, $C_{OUT}$ =100µF/Electrolytic,
CH1: $V_{OUT}$, 50mV/Div, AC
CH2: $I_{OUT}$, 2A/Div, DC
TIME:20µs/Div

**Load Transient Response-2**

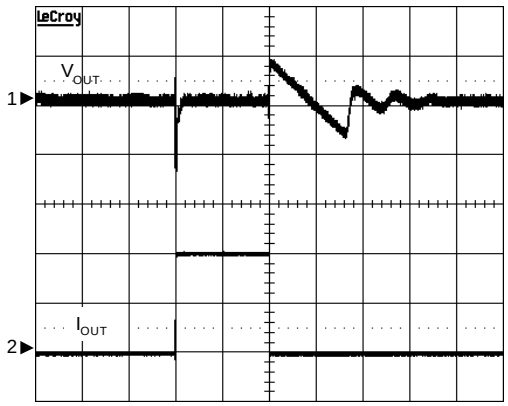



$V_{CC}$=5V, $V_{IN}$ =5V, $V_{OUT}$=1.5V,
$I_{LOAD}$ =0-5-0A(rising/falling edge=1A/µs ),
$C_{IN}$ =22µF/MLCC, $C_{OUT}$ =22µF/MLCC,
CH1: $V_{OUT}$, 50mV/Div, AC
CH2: $I_{OUT}$, 2A/Div, DC
TIME:100µs/Div

## Operating Waveforms (Cont.)

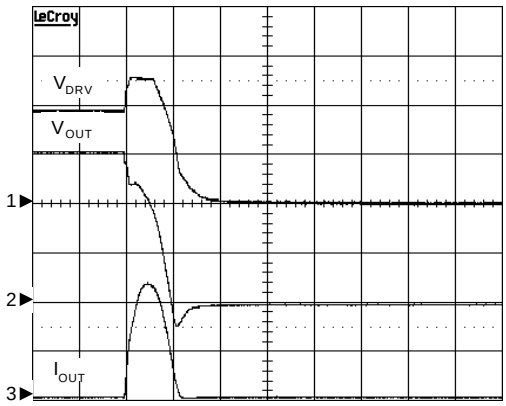
The test condition $T_A$= 25°C unless otherwise specified.

**Load Transient Response-3**




$V_{CC}$=5V, $V_{IN}$ =5V, $V_{OUT}$=1.5V,
$I_{LOAD}$ =0-0.2-0A(rising/falling edge=1A/µs ),
$C_{IN}$ =22µF/MLCC, $C_{OUT}$ =22µF/MLCC,
CH1: $V_{OUT}$, 20mV/Div, AC
CH2: $I_{OUT}$, 100mA/Div, DC
TIME:100µs/Div

**Short Circuit Response**

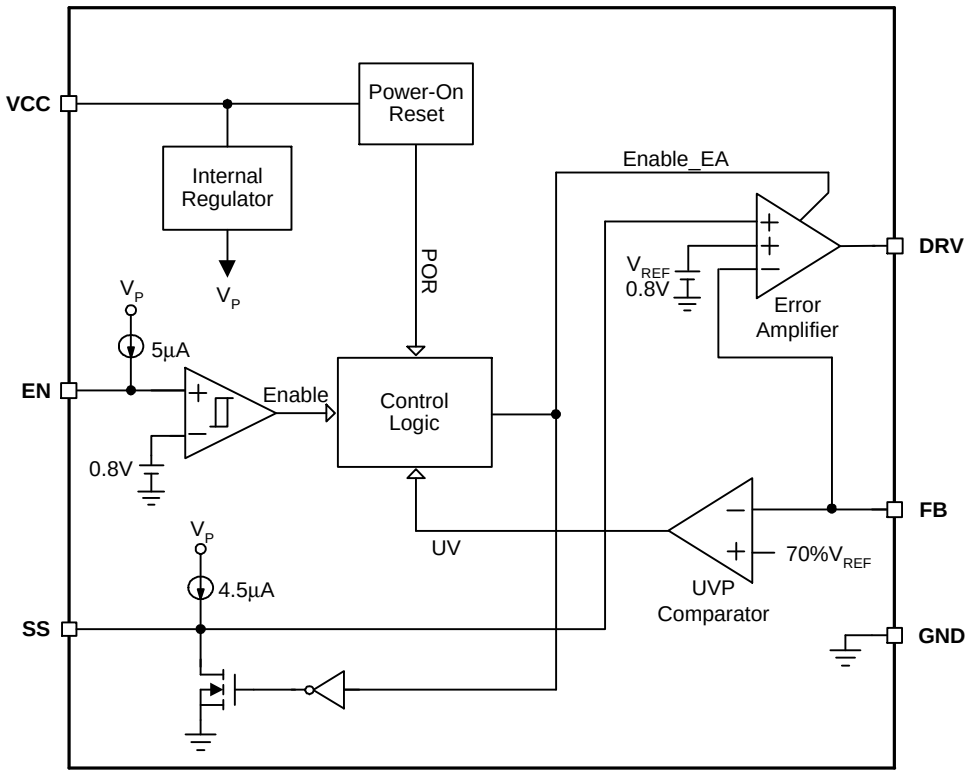



$V_{CC}$=5V, $V_{IN}$ =5V, $V_{OUT}$ =1.5V,
$C_{IN}$ =22µF/MLCC,$C_{OUT}$ =22µF/MLCC,
CH1: $V_{DRV}$, 2V/Div, DC
CH2: $V_{OUT}$, 0.5V/Div, DC
CH3: $I_{OUT}$, 20A/Div, DC
TIME: 50µs/Div

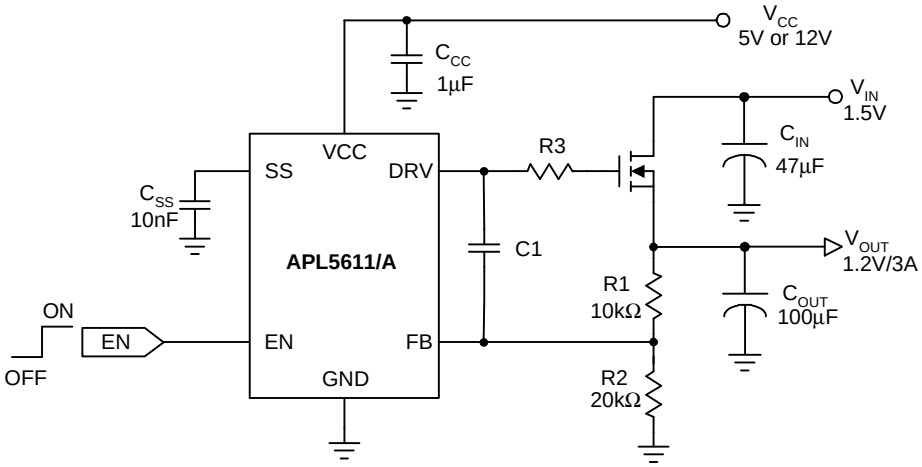
## Pin Description

| PIN | | FUNCTION |
|---|---|---|
| NO. | NAME | |
| 1 | EN | Enable control pin. Pulling the EN high enables the $V_{OUT}$; forcing the EN low ($V_{EN}$<0.4V) disables the $V_{OUT}$. When re-enabled, the IC undergoes a new soft-start process. The EN pin is pulled high internally, hence it can be left open if the EN control is not used. |
| 2 | GND | Ground pin of the circuitry. All voltage levels are measured with respect to this pin. |
| 3 | FB | Voltage Feedback Pin. Connecting this pin to an external resistor divider receives the feedback voltage of the regulator. |
| 4 | SS | Connect this pin to a capacitor for soft-start. |
| 5 | DRV | This pin drives the gate of an external N-channel MOSFET for linear regulator. |
| 6 | VCC | Power input pin of the device. The voltage at this pin is monitored for Power-On-Reset purpose. |

## Block Diagram



## Typical Application Circuit




R3, C1: Optional

## Function Description

### Power-On-Reset (POR)

The APL5611/A monitors the VCC pin voltage ($V_{CC}$) for power-on-reset function to prevent wrong operation. The built-in POR circuit keeps the output shutting off until internal circuit is operating properly. Typical POR threshold is 4.0V with 0.4V hysteresis.

### Soft-Start

The APL5611/A provides an adjustable soft-start circuitry to control rise rate of the output voltage and limit the current surge during start-up. The soft-start time is set with a capacitor from the SS pin to the ground. The capacitor is charged to VP with a constant 4.5 μA (typ.) current source.

### Under-Voltage Protection (UVP)

The APL5611/A monitors the voltage on FB. When the voltage on FB falls below the under-voltage threshold, the UVP circuit shuts off the output voltage immediately by pulling down DRV to 0V and latches APL5611/A off, requiring either a $V_{CC}$ POR or EN re-enable again to restart. The UVP activation timing is different in these 2 variants of IC, APL5611 and APL5611A. The APL5611 UVP is activated after $V_{OUT}$ voltage has reached 90% POK threshold while the APL5611A UVP is activated after $V_{CC}$ has been applied to VCC pin. In order to avoid erroneous UVP latch-off in APL5611A, please make sure the power sequence is a proper one when you use the APL5611A. For the suggested power sequence of APL5611A, you can refer to the Power Sequencing in Application Information.

### Enable Control

The APL5611/A has a dedicated enable pin (EN). A logic low signal applied to this pin shuts down the output. Following a shutdown, a logic high signal re-enables the output through initiation of a new soft-start cycle. It's not necessary to use an external transistor to save cost.

### Power-OK and Delay

The APL5611/A indicates the status of the output voltage by monitoring the feedback voltage ($V_{FB}$) on FB pin. As the $V_{FB}$ rises and reaches the rising Power-OK voltage threshold ($V_{POKTH}$), an internal delay function starts to work. At the end of the delay time, the IC turns off the internal NMOS of the POK to indicate that the output is ok. As the $V_{FB}$ falls and reaches the falling Power-OK voltage threshold, the IC turns on the NMOS of the POK (after a debounce time of 5μs typical).

### Output Voltage Regulation

The APL5611/A is a linear regulator controller. An external N-channel MOSFET should be connected to DRV as the pass element. The output voltage set by the resistor divider is determined by:

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R1}{R2}\right)$$

Where R1 is connected from VOUT to FB and R2 is connected from FB to GND.

## Application Information

### Input Capacitor

The APL5611/A requires proper input capacitor of $V_{IN}$ (connected to the external MOSFET's drain) to supply surge current during stepping load transients to prevent the input rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the $V_{IN}$ limits the slew rate of the surge current, it is necessary to place the input capacitor near the MOSFET's drain as close as possible. If the MOSFET is located near the bulk capacitor for upstream voltage regulator, this input capacitor may not be required. The Input capacitor for $V_{IN}$ should be larger than 1μF. Higher capacitance of this $V_{IN}$ input capacitor is needed if the stepping load transients are large and fast.

Another input capacitor for $V_{CC}$ is recommended. Placing the input capacitor of $V_{CC}$ as close to VCC pin as possible prevents outside noise from entering APL5611/A's control circuitry. The recommended capacitance of VCC input capacitor is 1μF.

### Output Capacitor

The APL5611/A needs a proper output capacitor to maintain circuit stability and to improve transient response over temperature and current. In order to insure the circuit stability, the proper output capacitor value should be larger than 10μF. With X5R and X7R dielectrics, 22μF is sufficient at all operating temperatures.

### Soft-Start Capacitor

The soft-start capacitor on SS pin can reduce the inrush current and overshoot of output voltage. The capacitor is charge to $V_{CC}$ with a constant 4.5μA (typ.) current source, $I_{SS}$. This results in a linear charge of the soft-start capacitor and thus the output voltage. The soft-start period, tss, ends once the capacitor voltage reaches 0.8V (typ.). The soft-start capacitor is calculated using the equation:

$$C_{SS} = (I_{SS} \times t_{SS}) / 0.8$$

Where $C_{SS}$ is the soft-start capacitor. $I_{SS}$ is the soft-start current of SS pin. $T_{SS}$ is the soft-start time you set for your application.

### MOSFET Selection

APL5611/A requires an N-channel MOSFET as a pass element. There are some parameters must be considered in selecting a MOFSET, including: Threshold Voltage $V_{TH}$, $R_{DS(on)}$, Continuous $I_{DS}$ current and Package Thermal Resistance. The MOSFET selection guidelines are listed as below:

1. Threshold Voltage $V_{TH}$: Select the MOSFET $V_{TH}$ rating to meet the following equation:

$$V_{TH} < V_{CC(min)} - V_{OUT(max)}$$

2. $R_{DS(on)}$ : Select the MOSFET $R_{DS(on)}$ to ensure that the output voltage will never enter dropout:

$$R_{DS(on)(max)} < (V_{IN(min)} - V_{OUT(max)}) / I_{OUT(max)}$$

(Note: $R_{DS(on)(max)}$ must be met at all temperatures and at the minimum $V_{GS}$ condition)

3. Continuous $I_{DS(max)}$: Select the $I_{DS(max)}$ that can support the output current:

$$\text{Continuous } I_{DS(max)} > I_{OUT(max)}$$

4. Package Thermal Resistance $\theta_{(JA)}$: Select a package of MOSFET that can dissipate the heat, $\theta_{(JA)} < (T_J - T_A)/P_D$, where $T_J$ is the maximum allowable Junction temperature of MOSFET, $T_A$ is the ambient temperature, $P_D$ is the maximum power dissipation on MOSFET, calculated as below:

$$P_D = (V_{IN(max)} - V_{OUT(min)}) \times I_{OUT(max)}$$

### Power Sequencing (Only for APL5611A)

At start-up, it is necessary to ensure that the $V_{IN}$ (the voltage supplied to MOSFET drain), $V_{CC}$ and $V_{EN}$ are sequenced correctly to avoid erroneous latch-off. To avoid UVP latch-off happened at start-up due to sequencing issues, the key method is the $V_{IN}$ should be larger than the output under-voltage threshold plus the drop through the pass MOSFET when that output is enabled.

Figure 1 and 2 show the two types of power on sequence. Figure 1 shows the $V_{CC}$ comes up before the $V_{IN}$, and then the output would be enabled when the $V_{EN}$ is applied. Figure 2 shows the $V_{IN}$ comes up before the $V_{CC}$, and then the output can either be enabled with the $V_{CC}$ or $V_{EN}$. Recommended power on sequence is shown in Figure1 and 2.

## Application Information (Cont.)

**Power Sequencing (Only for APL5611A) (Cont.)**

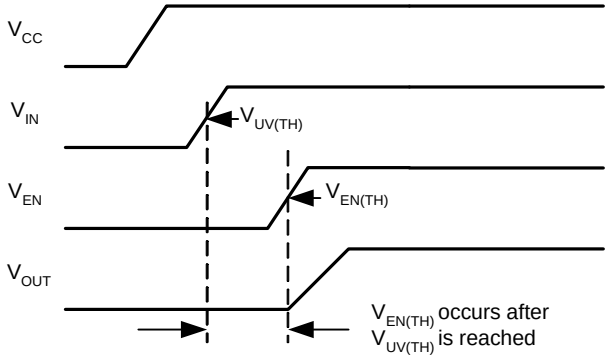



Figure 1. APL5611A supply comes up before MOSFET drain supply

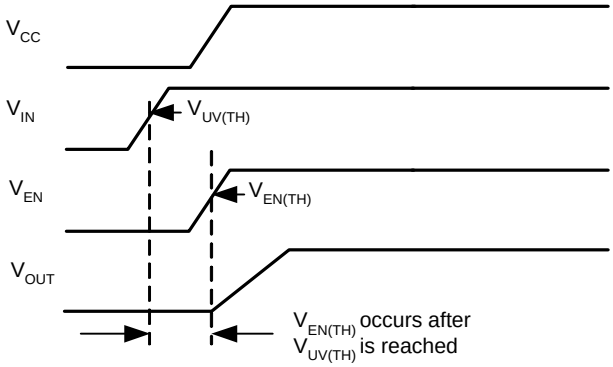



Figure 2. MOSFET drain supply comes up before APL5611A supply

**Short Circuit Concerns (Only for APL5611)**

Since the APL5611 UVP function is activated after the $V_{OUT}$ reaches 90% level, any combinations of sequence among $V_{IN}$, $V_{CC}$, and $V_{EN}$ are allowable. However, please note that the advantage of none-power-sequencing brings a drawback. If and only if a short circuit condition of output voltage occurs before $V_{IN}$ supply, the UVP won't be activated. Thus, the short circuit current persists to flow and could impair the MOSFET. If in your application the short circuit is most likely to be encountered before $V_{IN}$ supply, we suggest you use the APL5611A instead of the APL5611, who can provide this short circuit protection. Nevertheless, if the $V_{IN}$ supply can provide the OCP protection, this short circuit won't be an issue in APL5611.

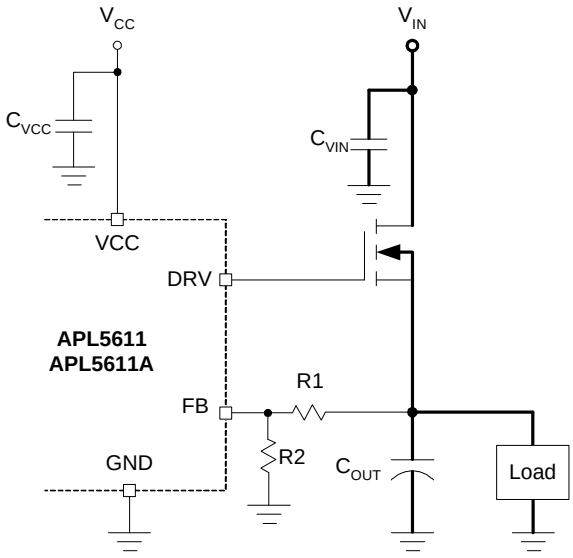



Figure 3

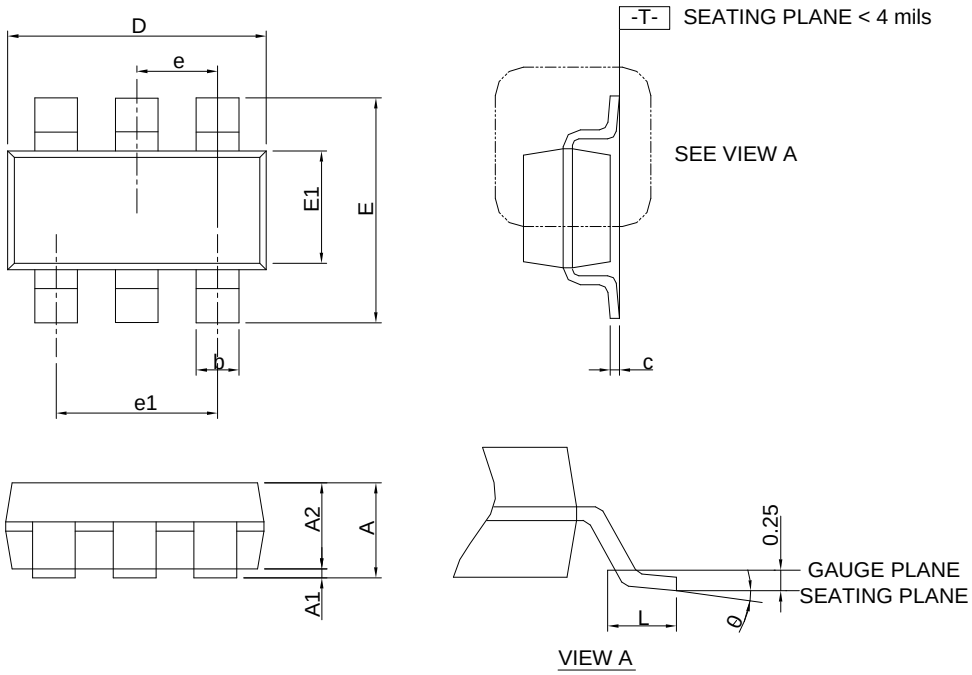
**Layout Consideration**

Figure 3 illustrates the layout. Below is a checklist for your layout:

1. Please place the input capacitor $C_{VCC}$ close to the VCC pin.
2. Please place the $C_{VIN}$ close to the MOSFET's drain.
3. Layout a copper plane for N-channel MOSFET's drain to improve the heat dissipation.
4. Output capacitor $C_{OUT}$ for load must be placed near the load as close as possible.
5. Large current paths, the bold lines in figure 3, must have wide tracks.

## Package Information

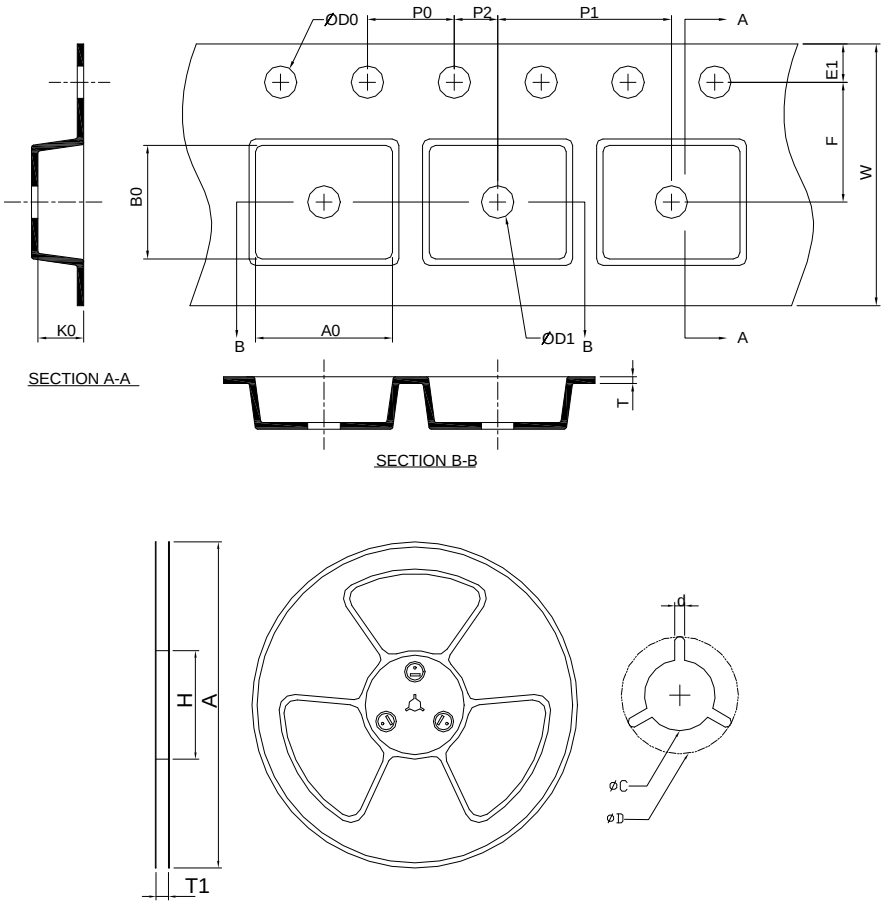
**SOT-23-6**




| SYMBOL | SOT-23-6 | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | | 1.45 | | 0.057 |
| A1 | 0.00 | 0.15 | 0.000 | 0.006 |
| A2 | 0.90 | 1.30 | 0.035 | 0.051 |
| b | 0.30 | 0.50 | 0.012 | 0.020 |
| c | 0.08 | 0.22 | 0.003 | 0.009 |
| D | 2.70 | 3.10 | 0.106 | 0.122 |
| E | 2.60 | 3.00 | 0.102 | 0.118 |
| E1 | 1.40 | 1.80 | 0.055 | 0.071 |
| e | 0.95 BSC | | 0.037 BSC | |
| e1 | 1.90 BSC | | 0.075 BSC | |
| L | 0.30 | 0.60 | 0.012 | 0.024 |
| θ | 0° | 8° | 0° | 8° |

Note : 1. Follow JEDEC TO-178 AB.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

## Carrier Tape & Reel Dimensions




| Application | A | H | T1 | C | d | D | W | E1 | F |
|---|---|---|---|---|---|---|---|---|---|
| SOT-23-6 | 178.0±2.00 | 50 MIN. | 8.4+2.00 -0.00 | 13.0+0.50 -0.20 | 1.5 MIN. | 20.2 MIN. | 8.0±0.30 | 1.75±0.10 | 3.5±0.05 |
| | **P0** | **P1** | **P2** | **D0** | **D1** | **T** | **A0** | **B0** | **K0** |
| | 4.0±0.10 | 4.0±0.10 | 2.0±0.05 | 1.5+0.10 -0.00 | 1.0 MIN. | 0.6+0.00 -0.40 | 3.20±0.20 | 3.10±0.20 | 1.50±0.20 |

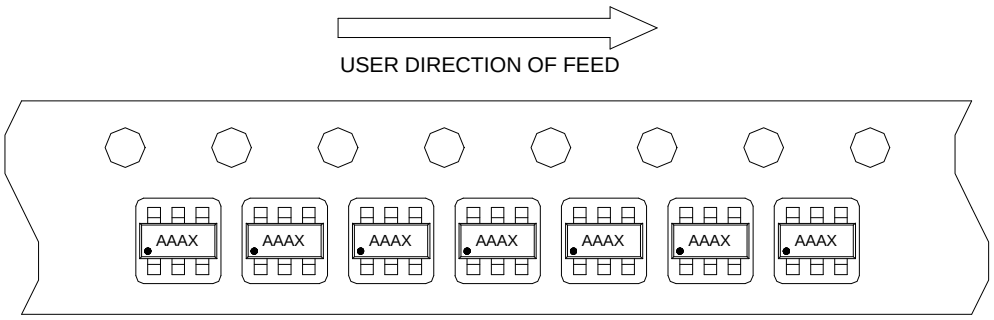
(mm)

## Devices Per Unit

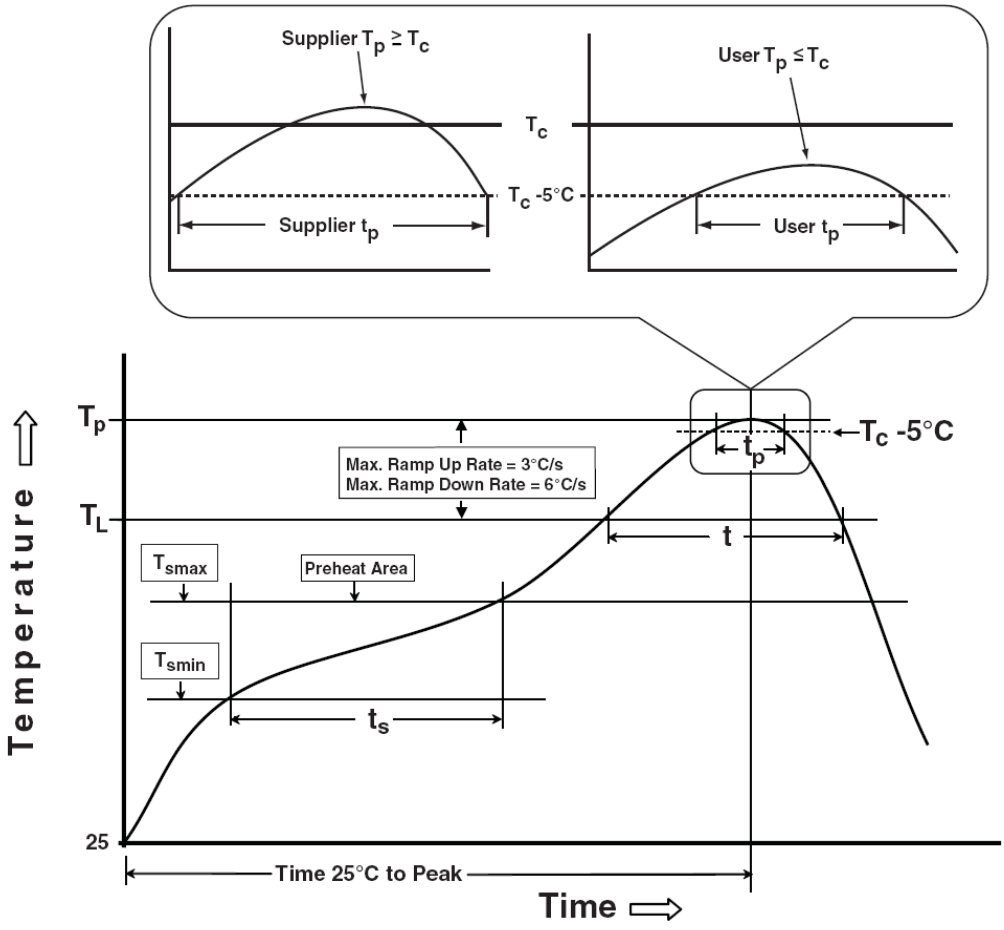
| Package Type | Unit | Quantity |
|---|---|---|
| **SOT-23-6** | Tape & Reel | 3000 |

## Taping Direction Information

**SOT-23-6**




## Classification Profile



## Classification Reflow Profiles

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|---|---|---|
| **Preheat & Soak**<br>Temperature min ($T_{smin}$)<br>Temperature max ($T_{smax}$)<br>Time ($T_{smin}$ to $T_{smax}$) ($t_s$) | 100 °C<br>150 °C<br>60-120 seconds | 150 °C<br>200 °C<br>60-120 seconds |
| Average ramp-up rate ($T_{smax}$ to $T_P$) | 3 °C/second max. | 3°C/second max. |
| Liquidous temperature ($T_L$)<br>Time at liquidous ($t_L$) | 183 °C<br>60-150 seconds | 217 °C<br>60-150 seconds |
| Peak package body Temperature ($T_p$)* | See Classification Temp in table 1 | See Classification Temp in table 2 |
| Time ($t_P$)** within 5°C of the specified classification temperature ($T_c$) | 20** seconds | 30** seconds |
| Average ramp-down rate ($T_p$ to $T_{smax}$) | 6 °C/second max. | 6 °C/second max. |
| Time 25°C to peak temperature | 6 minutes max. | 8 minutes max. |
| * Tolerance for peak profile Temperature ($T_p$) is defined as a supplier minimum and a user maximum.<br>** Tolerance for time at peak profile temperature ($t_p$) is defined as a supplier minimum and a user maximum. | | |

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ ³350 |
|---|---|---|
| <2.5 mm | 235 °C | 220 °C |
| ≥2.5 mm | 220 °C | 220 °C |

Table 2. Pb-free Process – Classification Temperatures (Tc)

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ 350-2000 | Volume $mm^3$ >2000 |
|---|---|---|---|
| <1.6 mm | 260 °C | 260 °C | 260 °C |
| 1.6 mm – 2.5 mm | 260 °C | 250 °C | 245 °C |
| ≥2.5 mm | 250 °C | 245 °C | 245 °C |

## Reliability Test Program

| Test item | Method | Description |
|---|---|---|
| SOLDERABILITY | JESD-22, B102 | 5 Sec, 245°C |
| HOLT | JESD-22, A108 | 1000 Hrs, Bias @ $T_j$=125°C |
| PCT | JESD-22, A102 | 168 Hrs, 100%RH, 2atm, 121°C |
| TCT | JESD-22, A104 | 500 Cycles, -65°C~150°C |
| HBM | MIL-STD-883-3015.7 | VHBM≧2KV |
| MM | JESD-22, A115 | VMM≧200V |
| Latch-Up | JESD 78 | 10ms, $1_{tr}$≧100mA |

## Customer Service

**Anpec Electronics Corp.**
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838