AN4009
Application note

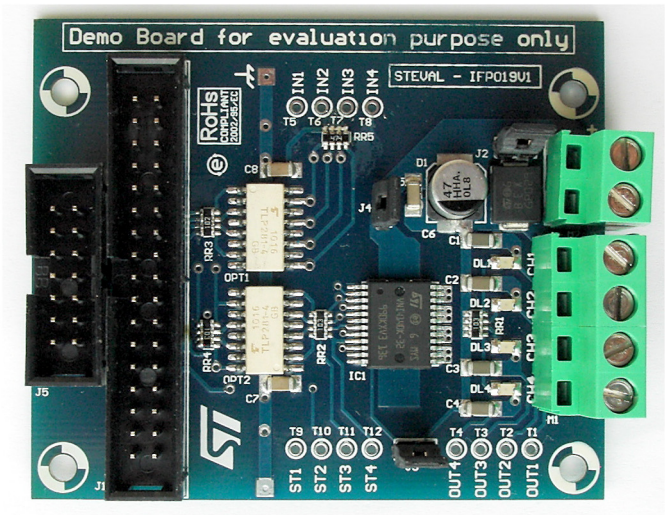
STEVAL-IFP019V1: design with VNI4140K-32 quad high-side smart power solid-state relay ICs

Introduction

The STEVAL-IFP019V1 demonstration board has been developed to show the new VNI4140K-32 device functionalities within industrial applications such as PLCs (programmable logic controllers) which drive lamps, valves, relays, and similar loads.

This tool allows the evaluation of the VNI4140K-32 features, in particular all kinds of embedded self-protections, power-handling capabilities, operation and diagnostic feedback, thermal behavior, and conformity to inherent IEC standards.

Figure 1. STEVAL-IFP019V1



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A double-sided PCB allows the obtaining of the best trade-off between a routing solution and thermal management results.

The main features of the demonstration board are:

- Four output channels (4 x 1 A)
- Four input channels
- Four feedback channels for diagnostic purposes
- Bi-directional opto-isolated interface for MCU safe connection
- TTL/CMOS compatible signals for MCU direct connection
- LEDs to indicate output state
- Compliance to IEC61000-4-4, IEC61000-4-5, and IEC61000-4-2
- 10.5 V to 36 V DC power supply voltage range.

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1 Electrical characteristics

The electrical characteristics of the VNI4140K-32 demonstration board (STEVAL-IFP019V1) are given in *Table 1*.

Table 1. STEVAL-IFP019V1 electrical characteristics

Parameter	Value			Notes
	Min.	Typ.	Max.	
Operating conditions				
Ambient operating temperature			85 °C	If the VNI4140K-32 junction temperature exceeds 170 °C, the device shuts down
Power supply				
Vcc supply voltage	10.5 V	24 V	36 V	
Vdd logic supply voltage		5 V		
Supply current on Vdd		250 µA		All channels in OFF state
		2.4 mA	4.8 mA	ON state with V_{in} = 5 V
Output stage				
Output channel on current limitation	1 A		2.6 A	IC internally limited V_{CC} = 24 V; R_{LOAD} < 10 mΩ
Maximum DC output current				
dV/dt (on) turn-on voltage slope		4 V/µs		I_{OUT} = 0.5 A, resistive load
dV/dt (off) turn-off voltage slope		4 V/µs		I_{OUT} = 0.5 A, resistive load
Demagnetization protection				
Output voltage on inductive turn-off	V_{CC}-41	V_{CC}-45	V_{CC}-52	I_{OUT} = 0.5 A; L_{LOAD} >= 1 mH

2 Safety precautions

The board must be used only by expert technicians. The copper areas around the VNI4140K-32 device have a heatsink function, visible in the top layer layout view, refer to *Figure 8*. In case of short-circuit, current limiting or hard demagnetization, the STEVAL-IFP019V1 board, or part of it, may reach a very high temperature with consequent dangers.

No specific protections are implemented for reverse DC accidental connection. Remember that an electrolytic capacitor is connected to the supply bus, therefore a reverse continuous DC voltage applied to it may produce a dangerous explosion.

Warning: ST assumes no responsibility for any consequences which may result from the improper use of this tool.

3 VNI4140K-32 quad high-side smart power solid-state relay IC description

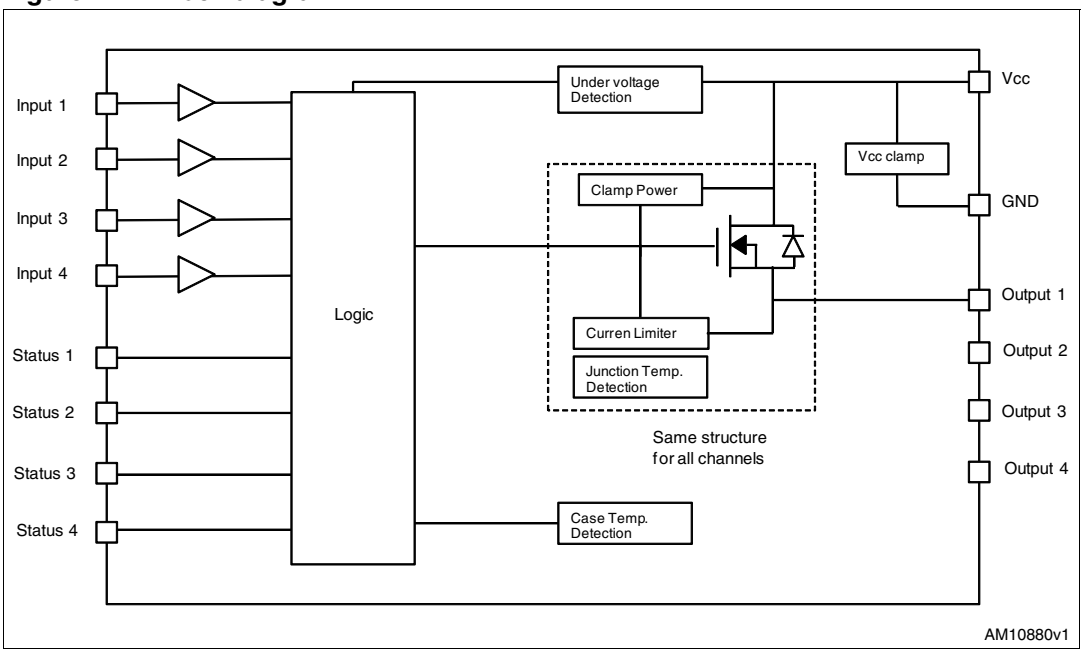
The VNI4140K-32 is a monolithic 4-channel driver featuring a very low supply current. The IC, which uses STMicroelectronics VIPower™ technology, is intended for driving loads with one side connected to ground.

Active channel current limitation, combined with thermal shutdown (independent for each channel), and automatic restart, protect the device against overload.

The main features of the VNI4140K-32 IC are:

- Output current: 1 A per channel
- Shorted load protections for each channel
- Junction overtemperature protection
- Case overtemperature protection for thermal independence of the channels
- Thermal case shutdown and restart not simultaneous in each single channel
- Protection against ground disconnection
- Current limitation
- Undervoltage shutdown
- Open drain diagnostic outputs
- 3.3 V CMOS/TTL compatible inputs
- Fast demagnetization of inductive loads
- Conforms to IEC 61131-2.

Figure 2. Block diagram



Active current limitation avoids that the system power supply drops in case of a shorted load. In overload condition, the channel turns off and back on automatically after the IC temperatures decrease below a threshold fixed by a temperature hysteresis so that junction

temperature is controlled. If this condition causes the case temperature to reach the case temperature limit (T_{CSD}), overloaded channels (i.e. the ones for which junction temperature has exceeded the junction protection threshold, T_{jSD}, and has not fallen below the junction protection reset threshold, T_{jR}) are turned off. These channels restart, non-simultaneously, only when the case temperature decreases below the case protection reset threshold (T_{CR}). Non-overloaded channels continue to operate normally.

The open drain diagnostic outputs indicate related channel overtemperature conditions.

4 STEVAL-IFP019V1 demonstration board description

4.1 Overview

The VNI4140K-32 demonstration board is composed of two main sections:

- Opto-isolated interface for input and status signals
- A four-channel self-protect power stage section with STMicroelectronics Transil™ diode protection

The demonstration board consists of a double-sided FR4 printed circuit board with 35 µm copper plating. The PCB dimensions are 52 mm x 68 mm. The top and bottom views are shown below.

Figure 3. STEVAL-IFP019V1 top view

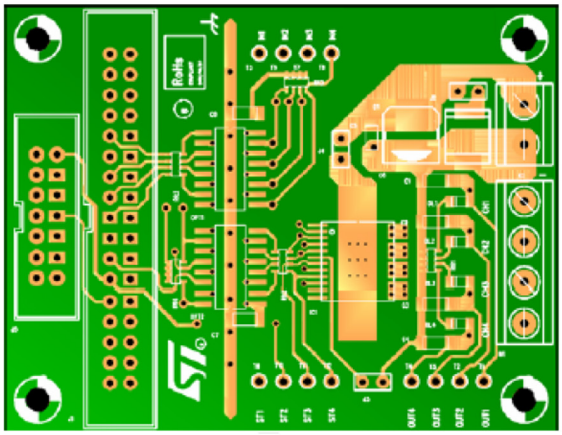


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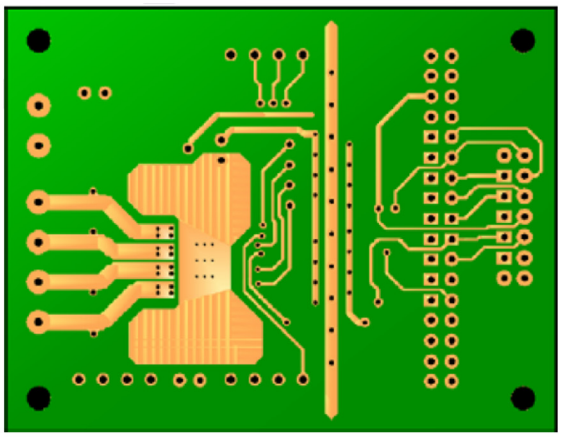
Figure 4. STEVAL-IFP019V1 bottom view



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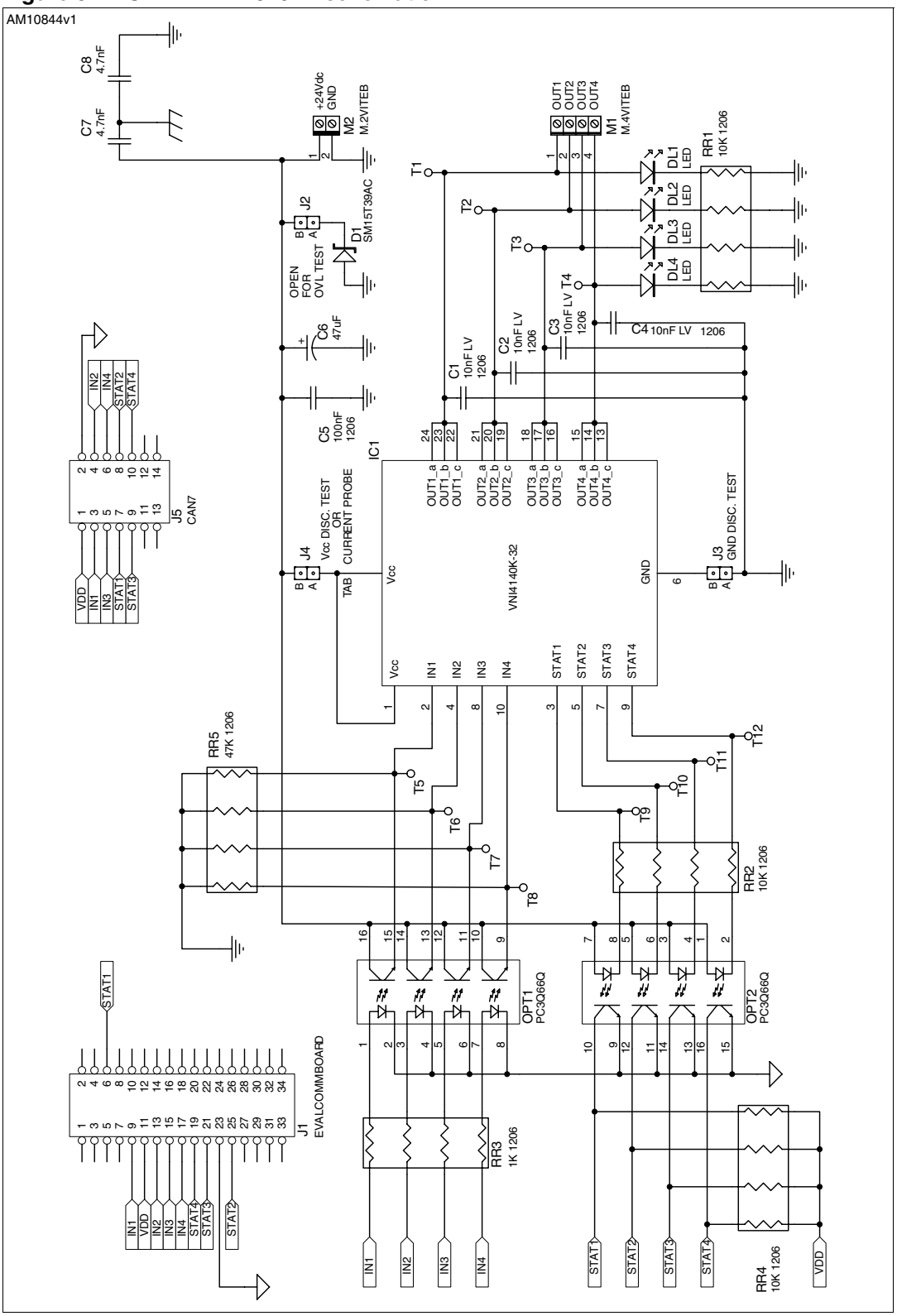
4.2 STEVAL-IFP019V1 schematic

Figure 5. STEVAL-IFP019V1 schematic



4.3 STEVAL-IFP019V1 connectors

The demonstration board is equipped with input and output connectors. Specifically, there are two input header connectors (J5 and J1), one 4-channel output connector (M1), and a supply voltage connector (M2).

Both input connectors, J5 and J1, provide the same bi-directional signals guaranteeing the maximum compatibility with existing STMicroelectronics tools such as the industrial communication board (see AN2451) and similar products.

Figure 6. J1 connector pinout

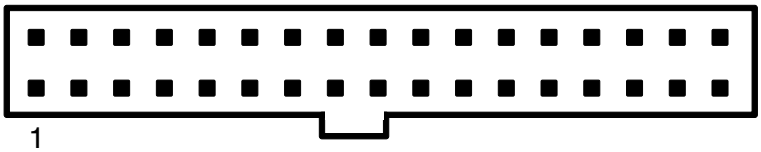


Figure 7. J5 connector pinout

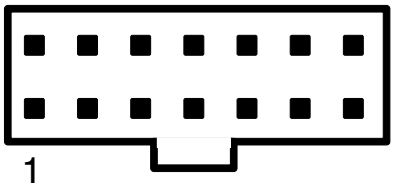


Table 2. J1 and J5 pin description

J1 pin number	J5 pin number	Signal	Type
11	1	Vdd	5/3.3 V supply voltage
23	2	GND	Signal ground
9	3	IN1	Input channel 1
13	4	IN2	Input channel 2
15	5	IN3	Input channel 3
17	6	IN4	Input channel 4
6	7	STAT1	Status channel 1
25	8	STAT2	Status channel 2
21	9	STAT3	Status channel 3
19	10	STAT4	Status channel 4

4.4 STEVAL-IFP019V1 thermal management

The STEVAL-IFP019V1 PCB has two heatsinks: approximately 1 sq. cm on the top layer and 3 sq. cm on the bottom layer, thermally interconnected through 9 vias, as shown in *Figure 8*.

In a steady-state condition, low $R_{DS(on)}$ ensures a very low dissipation but in current limitation and in fast demagnetization, the power dissipation is much higher, requiring a low thermal resistance through the device exposed tab, soldering space, top layer, vias and bottom layer path. A 35 µm copper (10 oz/sq. ft) thickness and 0.3 mm diameter for the vias are used according to EIA/JESD51-5.

Figure 8. STEVAL-IFP019V1 PCB copper heatsink

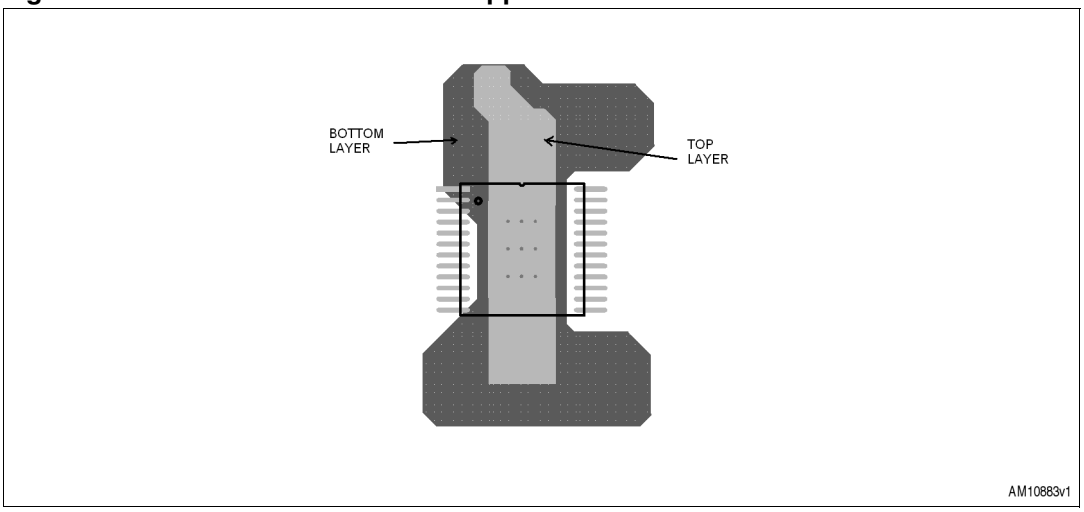


Figure 9 and *11* show the STEVAL-IFP019V1 temperature map with all channels permanently switched on with 48 Ω loads, 24 V supply voltage and ambient temperature of 25 °C. The IC temperature increase is only about a few degrees.

Figure 10 and *12* show a similar map when the IC is cycling at 1 Hz, 50% duty cycle, 48 Ω 1.2 H loads, 24 V supply voltage and ambient temperature of 25 °C.

Figure 9. Thermal map in steady-state condition

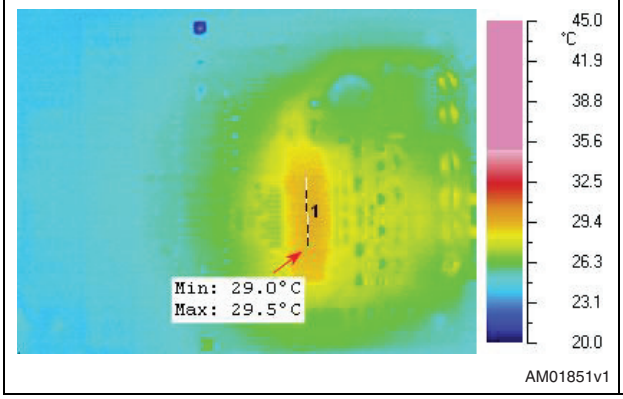


Figure 10. Thermal map in demagnetization condition (1 Hz repetitive cycling on 48 Ω 1.2 H load)

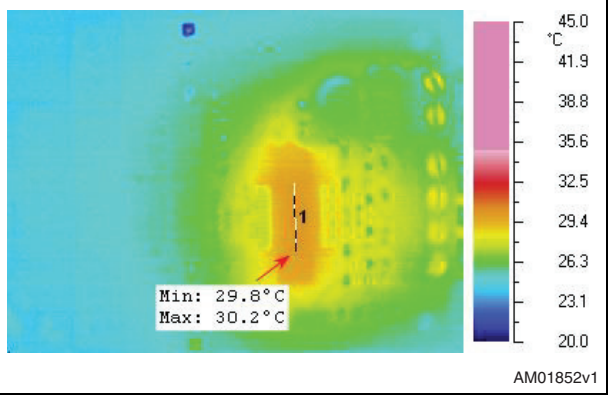


Figure 11. Steady-state thermal behavior 3D simulation

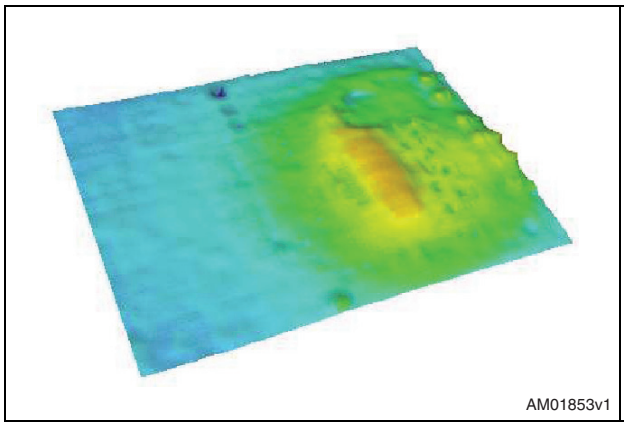
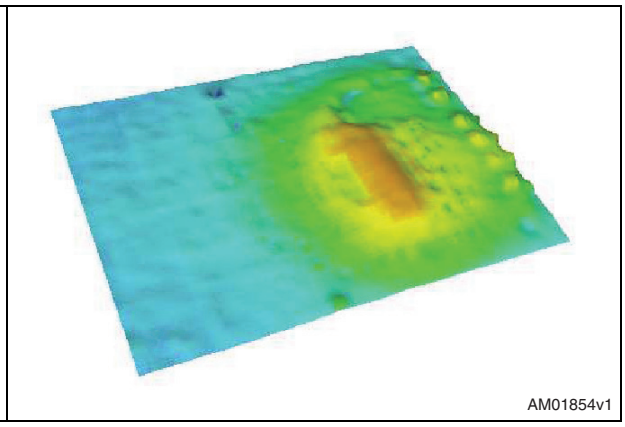


Figure 12. Repetitive demagnetization thermal behavior 3D simulation (1 Hz repetitive cycling on 48 Ω 1.2 H load)



In particular, *Figure 11* and *12* show 3D thermal modeling of the device.

4.5 EMC immunity test

4.5.1 Description

The STEVAL-IFP019V1 has been tested according IEC61000-4-4, IEC61000-4-5 and IEC61000-4-2. (Burst, surge and electrostatic discharge). The evaluation criteria (shown below) reported in the standards has been used to verify the acceptance of the results.

- Normal performance
- Temporary degradation or loss of function or performance, with automatic return to normal operation
- Temporary degradation or loss of function with of external intervention to recover normal operation
- Degradation or loss of function, need substitution of damaged components to recover normal operation.

4.5.2 Burst immunity test

The signal according the IEC61000-4-4:

- Pulse duration: 5 ns +/- 30%
- Pulse duration: 50 ns +/- 30%
- Polarity: positive/negative
- Burst duration (td): 15 ms+/- 20% at 5 kHz
- Burst period (tr): 300 ms+/- 20%
- Duration time T: 1 minute
- Applied to: supply voltage lines, output line through capacitive clamp and directly through embedded coupling capacitor in the generator.

Figure 13 below shows the standard timing waveform applied during the burst test.

Figure 13. Burst timing waveform

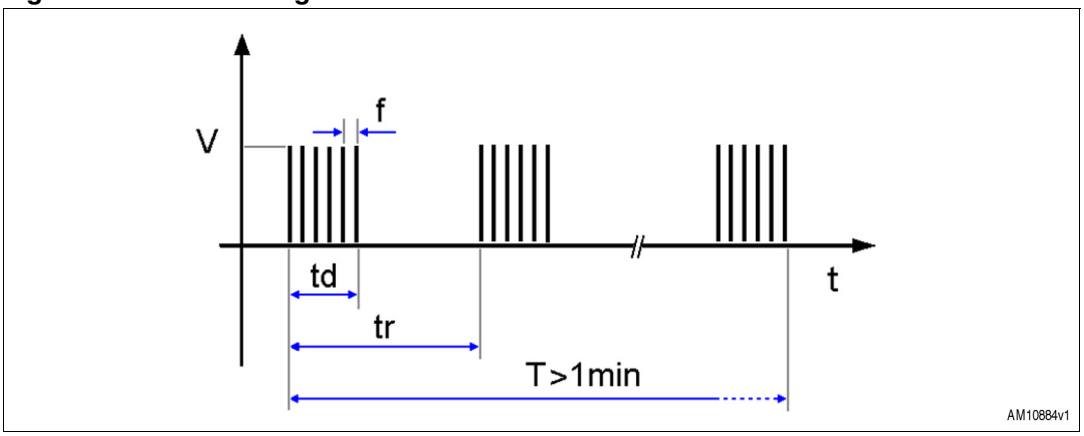


Table 3 shows the results of an inherent burst test. Normal performance has been observed when applying four different disturbance levels on the output ports and Vcc main voltage power supply.

Table 3. Application EFT (burst) robustness, applied to supply voltage lines

Configuration	EFT test signal amplitude, test result @ polarity (+/-)				
	1 kV	2 kV	3 kV	4 kV	5 kV
Standard	A / A	A / A	A / A	B / B	B / B
Primary and secondary GNDs shorted	A / A	A / A	B / A	B / B	B / B

Note: 1 Outputs floating.

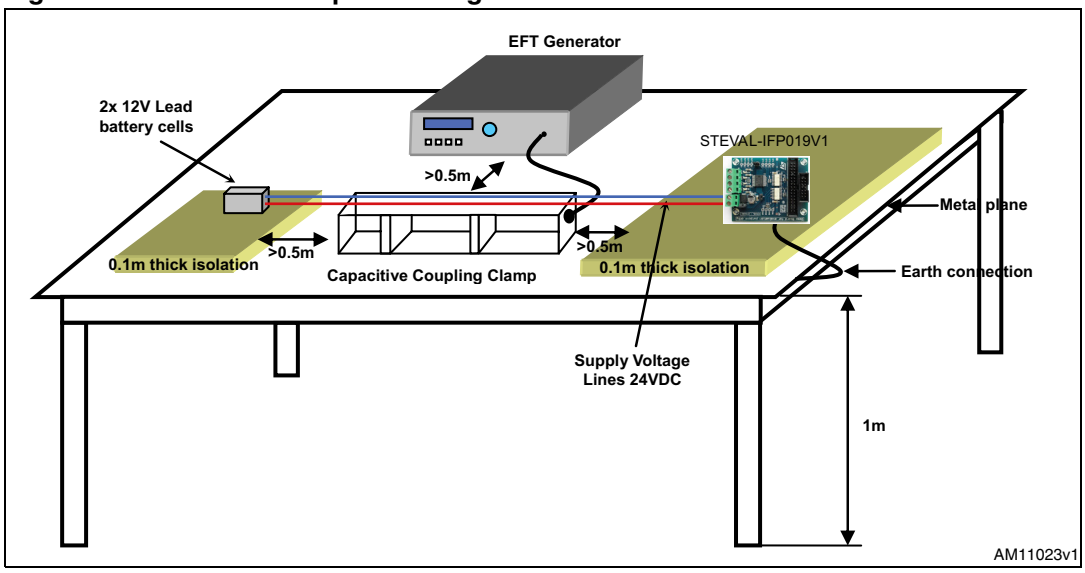
2 To reach same results reported in the tables above, it is necessary to replace C7 and C8 with two high voltage capacitors.

Table 4. Application EFT (burst) robustness, applied to output lines

Configuration	EFT test signal amplitude, test result @ polarity (+/-)				
	1 kV	2 kV	3 kV	4 kV	5 kV
Standard	A / A	A / A	B / B	B / B	B / B

Note: Outputs loaded by 1 kΩ resistors.

Figure 14. EFT test set-up according to IEC 61000-4-4

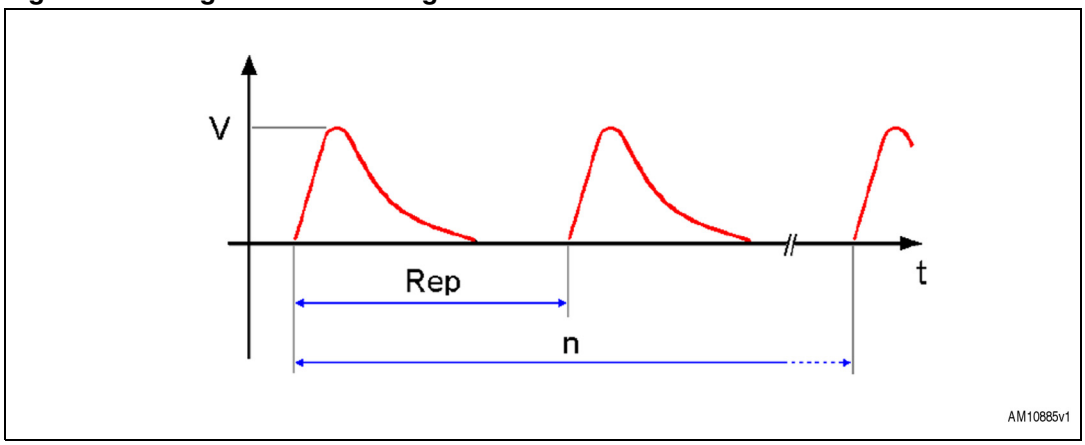


4.5.3 Surge test

A high energy surge test was performed in differential mode. A high surge signal was injected on the DUT (device under test) through a 42 Ω decoupling resistor. The test consisted of three positive and three negative discharges with a repetition rate of 1 discharge per minute.

Figure 15 shows the standard timing waveform applied on the DUT.

Figure 15. Surge standard timing waveform



- Test signal according the IEC 61000-4-5:
  - 5 positive and 5 negative surges
  - Repetition rate: 1 minute
  - Coupling: 42 Ω/0.5 µF

  Applied to:
  - Supply lines (Vcc, GND)
  - Differential mode (DM), Vcc vs. GND
  - Common mode (CM), Vcc vs. Earth
  - OUTPUT lines (OUT1)
  - Differential mode (DM), Vcc vs. GND
  - Common mode (CM), Vcc vs. Earth

Table 5. Application test results, surge applied to supply lines

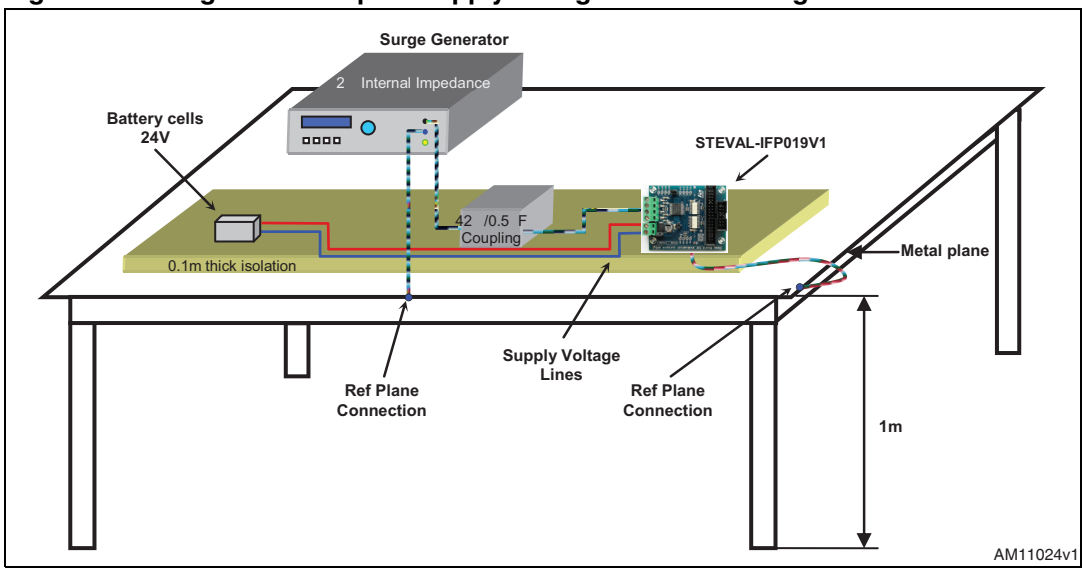
Configuration	Mode	Surge test signal amplitude, test result @ polarity (+/-)				
		1 kV	1.5 kV	2 kV	2.5 kV	3 kV
Standard evalboard	Differential	B / A	-	B / B	-	B / B
	Common	A / B	-	B / A	-	B / B

Table 6. Application test results, surge applied to supply lines

Configuration	Mode	Surge test signal amplitude, test result @ polarity (+/-)				
		1 kV	1.5 kV	2 kV	2.5 kV	3 kV
Standard evalboard	Differential	B / B	-	B / B	-	B / B
	Common	B / B	-	B / B	-	B / B

Note: to reach same results reported in the tables above, it is necessary to replace C7 and C8 with two high voltage capacitors.

Figure 16. Surge test set-up on supply voltage lines according to IEC 61000-4-5



4.5.4 ESD test

The test signal according the IEC 61000-4-2:

- Contact discharge/ air discharge
- Polarity: positive/negative
- Discharge unit: 150 pF/330 Ω
- Applied to: board output terminal

Figure 17. ESD test set-up according to IEC 61000-4-2

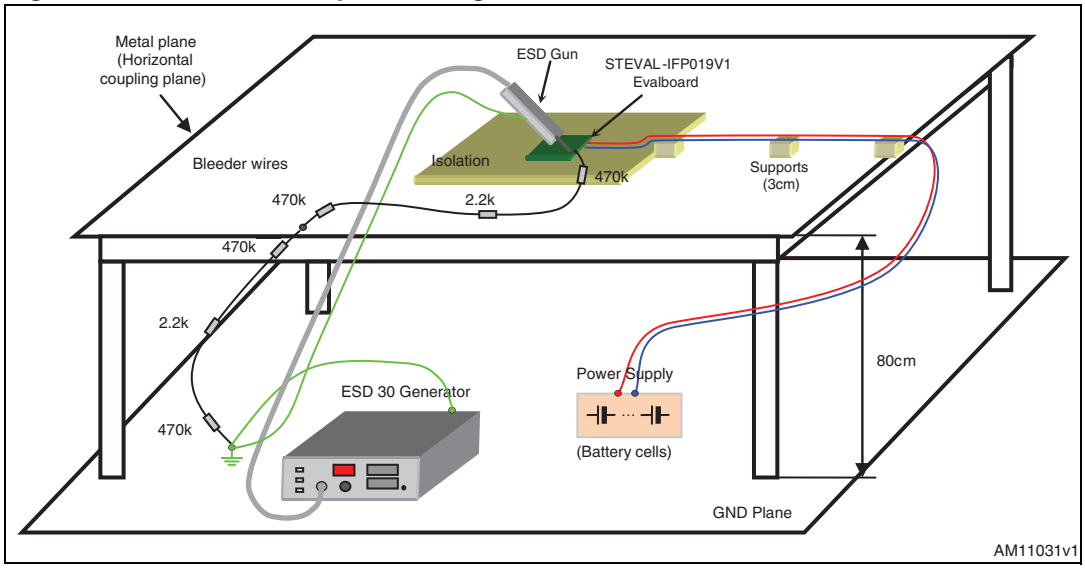


Table 7. Application ESD robustness

Discharge mode	ESD test signal amplitude, test result @ polarity (+ / -)				
	5 kV	10 kV	15 kV	20 kV	25 kV
Contact	B / B	B / B	B / B	B / B	B / B
Air	B / B	B / B	B / B	B / B	B / B

Appendix A Bill of material

Table 8. STEVAL-IFP019V1 demonstration board bill of material

Designator	Part type	Description
RR1	10 kΩ x 4	SMD resistor pack 1206 format
RR2	10 kΩ x 4	SMD resistor pack 1206 format
RR3	1 kΩ x 4	SMD resistor pack 1206 format
RR4	10 kΩ x 4	SMD resistor pack 1206 format
RR5	47 kΩ x 4	SMD resistor pack 1206 format
C1	10 nF LV	SMD capacitor 1206 format
C2	10 nF LV	SMD capacitor 1206 format
C3	10 nF LV	SMD capacitor 1206 format
C4	10 nF LV	SMD capacitor 1206 format
C5	100 nF	SMD capacitor 1206 format
C6	47 µF 50 V	SMD electrolytic capacitor
C7	4.7 nF	SMD capacitor 1206 format
C8	4.7 nF	SMD capacitor 1206 format
D1	SM15T39AC	Transil™ diode
DL1	LED diode	SMD LED diode 0805 format
DL2	LED diode	SMD LED diode 0805 format
DL3	LED diode	SMD LED diode 0805 format
DL4	LED diode	SMD LED diode 0805 format
OPT1	PC3Q66Q	4-channel opto-isolator
OPT2	PC3Q66Q	4-channel opto-isolator
IC1	VNI4140K-32	ST IC industrial 4 CH HSD
J1	Header 34-pin	Compatible EVALCOMMBOARD
J2	Jumper	Overvoltage test
J3	Jumper	Ground disconnection test
J4	Jumper	V_{cc} disconnection test
J5	Header 14-pin	Compatible ST7CANIC DB
M1	4 screw plugs	HSD output connector
M2	2 screw plugs	Power supply connector
T1	Test point	HSD output channel 1 voltage
T2	Test point	HSD output channel 2 voltage
T3	Test point	HSD output channel 3 voltage
T4	Test point	HSD output channel 4 voltage

Table 8. STEVAL-IFP019V1 demonstration board bill of material (continued)

Designator	Part type	Description
T5	Test point	HSD input channel 1 signal
T6	Test point	HSD input channel 2 signal
T7	Test point	HSD input channel 3 signal
T8	Test point	HSD input channel 4 signal
T9	Test point	HSD channel 1 status
T10	Test point	HSD channel 2 status
T11	Test point	HSD channel 3 status
T12	Test point	HSD channel 4 status

Appendix B PCB layout

Figure 18. STEVAL-IFP019V1 component layer

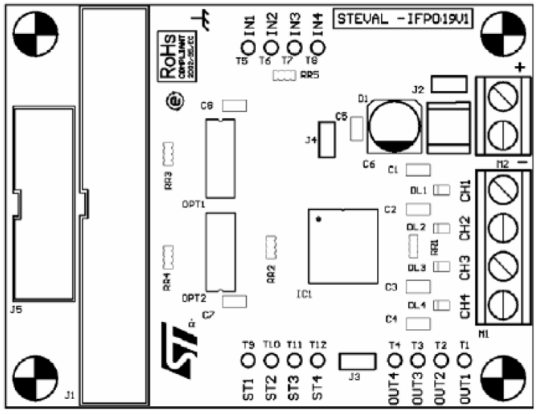


Figure 19. STEVAL-IFP019V1 copper top layer

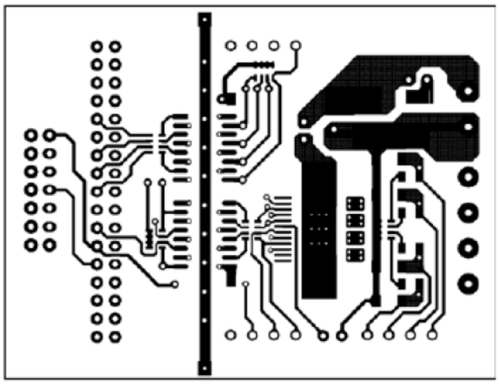
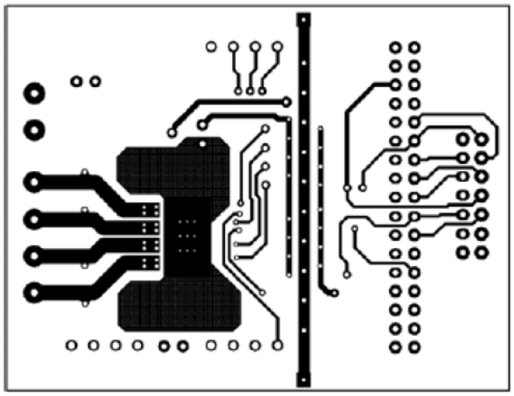


Figure 20. STEVAL-IFP019V1 copper bottom layer



Appendix C References

1. AN1351 application note

Revision history

Table 9. Document revision history

Date	Revision	Changes
10-Jan-2012	1	Initial release