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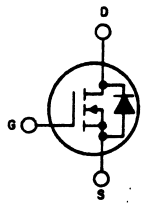
Power MOS Field-Effect Transistors

2N6802

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

3.5A, 500V
$r_{DS(on)}$ = 1.5Ω

N-CHANNEL ENHANCEMENT MODE



92CS-33761

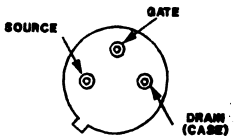
TERMINAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25°C):*

*DRAIN-SOURCE VOLTAGE, V_{DS}	500V
*DRAIN-GATE VOLTAGE (R_{GS} = 20 KΩ), V_{DGR}	500V
*GATE-SOURCE VOLTAGE, V_{GS}	±20V
*DRAIN CURRENT:	
RMS Continuous, I_D	
At T_C = 25°C	3.5A
At T_C = 100°C	1.5A
Pulsed, I_{DM}	11A
*SOURCE CURRENT:	
Continuous, I_S	2.5A
Pulsed, I_{SM}	11A
*POWER DISSIPATION, P_T:	
At T_C = 25°C	25W
Above T_C = 25°C	Derate linearly 0.20 W/°C
INDUCTIVE CURRENT, Clamped (L = 100μH), I_{LM}	11A
*OPERATING AND STORAGE TEMPERATURE, T_J, T_{stg}	-55 to +150°C
*LEAD TEMPERATURE, T_L:	
At distances 0.063 in. (1.6 mm) from seating plane for 10 s max.	300°C

*In accordance with JEDEC registration data.

TERMINAL DESIGNATION



JEDEC TO-205AF

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain - Source Breakdown Voltage	500*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$ Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSSF} Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSSR} Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = -20V, V_{DS} = 0V
I_{DSS} Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 500V, V_{GS} = 0V
	–	–	1000*	μA	V_{DS} = 400V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$ On-State Voltage①	–	–	3.75*	V	V_{GS} = 10V, I_D = 2.5A
$R_{DS(on)}$ Static Drain-Source On-State Resistance①	–	1.3	1.5*	Ω	V_{GS} = 10V, I_D = 1.5A, T_A = 25°C
	–	–	3.5*	Ω	V_{GS} = 10V, I_D = 1.5A, T_A = 125°C
V_{SD} Diode Forward Voltage①	0.70*	–	1.4*	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
g_{fs} Forward Transconductance①	1.5*	2.5	4.5*	S(℧)	V_{DS} = 5V, I_D = 1.5A
C_{iss} Input Capacitance	350*	600	900*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss} Output Capacitance	25*	100	200*	pF	See Fig. 10
C_{rss} Reverse Transfer Capacitance	15*	30	60*	pF	
$t_{d(on)}$ Turn-On Delay Time	–	–	30*	ns	V_{DD} ≅ 225V, I_D = 1.5A, Z_o = 50Ω
t_r Rise Time①	–	–	30*	ns	See Fig. 16
$t_{d(off)}$ Turn-Off Delay Time①	–	–	55*	ns	(MOSFET switching times are essentially independent
t_f Fall Time①	–	–	30*	ns	of operating temperature.)
SOA Safe Operating Area	25	–	–	W	V_{DS} = 200V, I_D = 125 mA, See Fig. 16.
	25	–	–	W	V_{DS} = 10V, I_D = 2.5A, See Fig. 16.

Thermal Resistance

R_{thJC} Junction-to-Case	–	–	5.0*	°C/W	
R_{thJA} Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr} Reverse Recovery Time	800	ns	T_J = 150°C, I_F = 2.5A, di_F/dt = 100A/μs
Q_{RR} Reverse Recovered Charge	4.6	μC	T_J = 150°C, I_F = 2.5A, di_F/dt = 100A/μs
t_{on} Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

Quality Semi-Conductors