FAIRCHILD SEMICONDUCTOR®

March 2013

FDP045N10A_F102 / FDI045N10A_F102

N-Channel PowerTrench® MOSFET

100 V, 164 A, 4.5 mΩ

Features

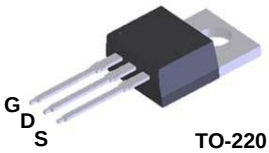
- $R_{DS(on)}$ = 3.8 mΩ (Typ.)@ V_{GS} = 10 V, I_D = 100 A
- Fast Switching Speed
- Low Gate Charge, Q_G = 54 nC(Typ.)
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

Description

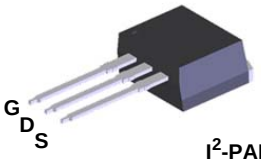
This N-Channel MOSFET is produced using Fairchild Semiconductor®'s advance PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

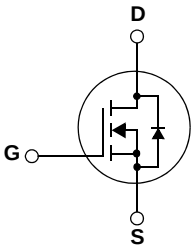
- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor drives and Uninterruptible Power Supplies
- Micro Solar Inverter



TO-220



I²-PAK
(TO-262)



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		FDP045N10A_F102 FDI045N10A_F102	Unit
V_{DSS}	Drain to Source Voltage		100	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current	- Continuous (T_C = 25°C, Silicon Limited)	164*	A
		- Continuous (T_C = 100°C, Silicon LImited)	116	
		- Continuous (T_C = 25°C, Package Limited)	120	
I_{DM}	Drain Current	- Pulsed (Note 1)	656	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	637	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	6.0	V/ns
P_D	Power Dissipation	(T_C = 25°C)	263	W
		- Derate above 25°C	1.75	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A.

Thermal Characteristics

Symbol	Parameter	FDP045N10A_F102 FDI045N10A_F102	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.57	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP045N10A	FDP045N10A_F102	TO-220	-	-	50
FDI045N10A	FDI045N10A_F102	I2PAK	-	-	50

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	100	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	-	0.07	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 80V, T_C = 150°C	-	-	500	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 100A	-	3.8	4.5	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 100A	-	132	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 50V, V_{GS} = 0V, f = 1MHz	-	3960	5270	pF
C_{oss}	Output Capacitance		-	925	1230	pF
C_{rss}	Reverse Transfer Capacitance		-	34	-	pF
C_{oss}(er)	Engry Releted Output Capacitance	V_{DS} = 50V, V_{GS} = 0V	-	1520	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{GS} = 10V, V_{DS} = 50V, I_D = 100A	-	54	74	nC
Q_{gs}	Gate to Source Gate Charge		-	17	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	8	-	nC
Q_{gd}	Gate to Drain “Miller” Charge	(Note 4)	-	13	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50V, I_D = 100A, V_{GS} = 10V, R_{GEN} = 4.7Ω	-	23	56	ns
t_r	Turn-On Rise Time		-	26	62	ns
$t_{d(off)}$	Turn-Off Delay Time		-	50	110	ns
t_f	Turn-Off Fall Time	(Note 4)	-	15	40	ns
ESR	Equivalent Series Resistance (G-S)	f = 1MHz	-	1.9	-	Ω
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	164*	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	656	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_{SD} = 100A	-	-	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, V_{DD} = 50V, I_{SD} = 100A, dI_F/dt = 100A/μs	-	75	-	ns
Q_{rr}	Reverse Recovery Charge		-	120	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 3mH, I_{AS} = 20.6A, R_G = 25Ω, Starting T_J = 25°C
3. I_{SD} ≤ 100A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

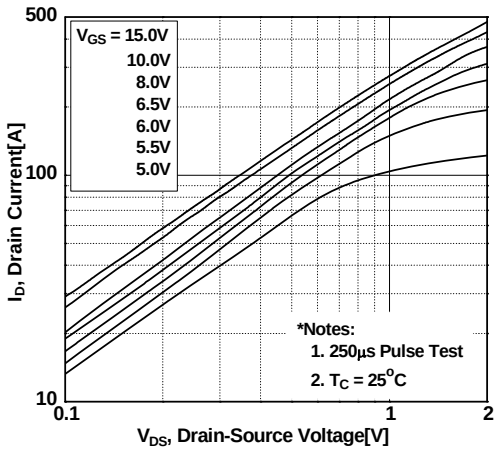


Figure 2. Transfer Characteristics

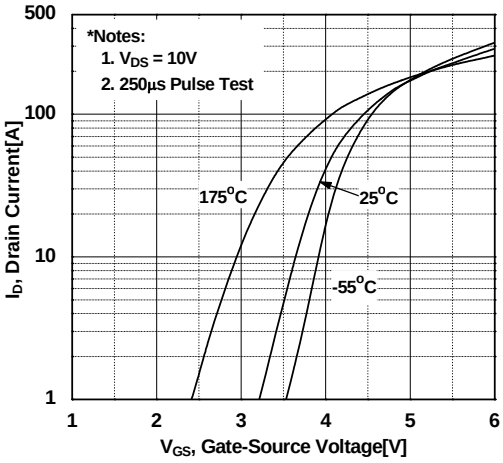


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

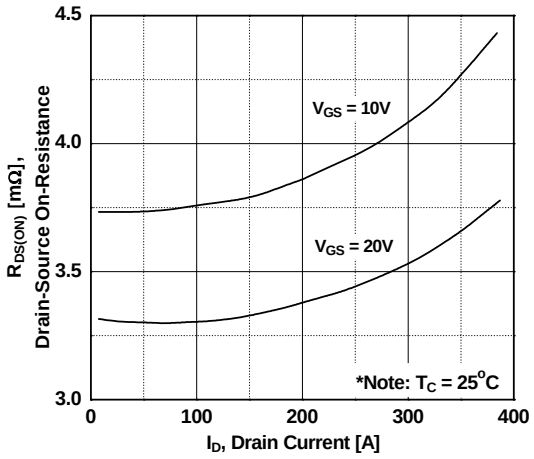


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

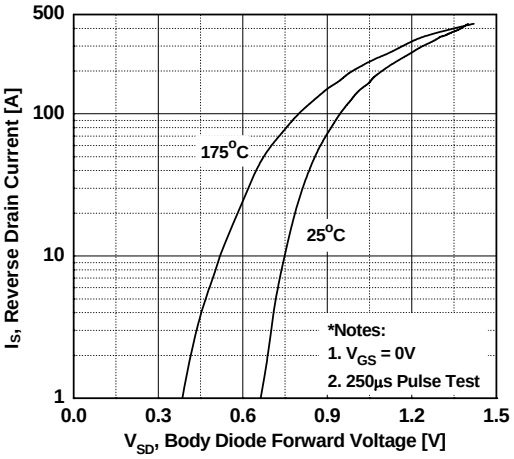


Figure 5. Capacitance Characteristics

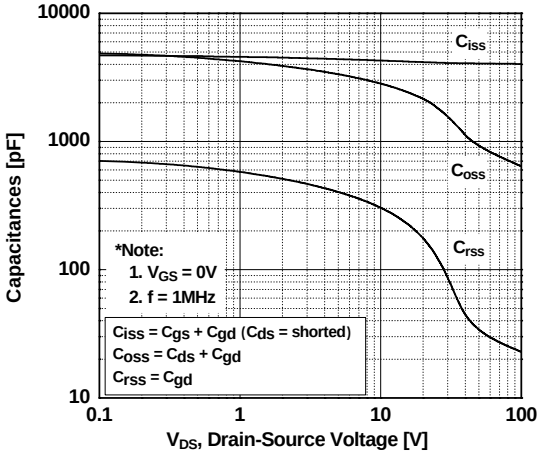
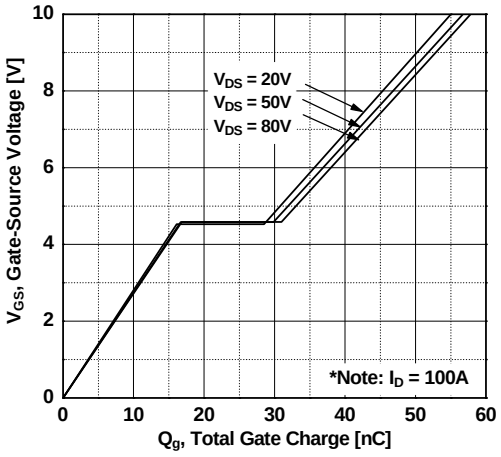


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

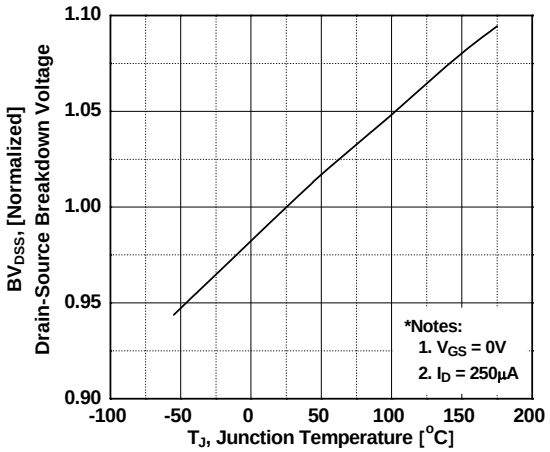


Figure 8. On-Resistance Variation vs. Temperature

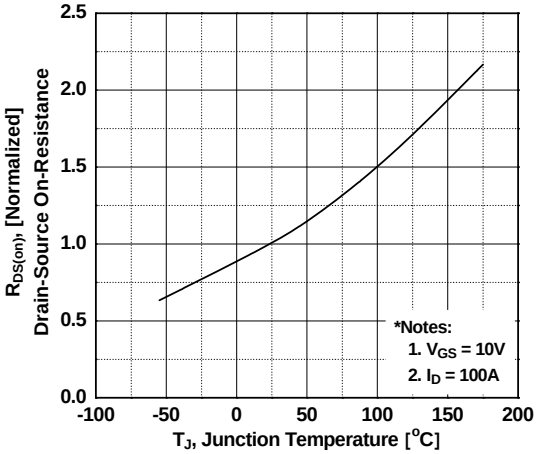


Figure 9. Maximum Safe Operating Area vs. Case Temperature

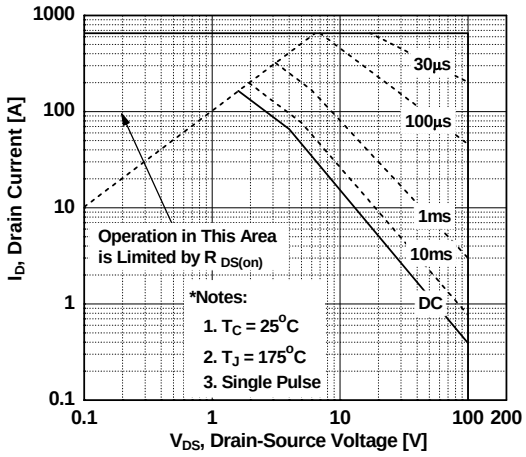


Figure 10. Maximum Drain Current

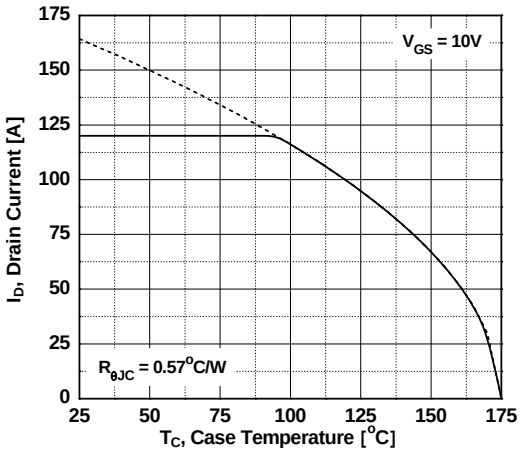


Figure 11. Eoss vs. Drain to Sourece Voltage

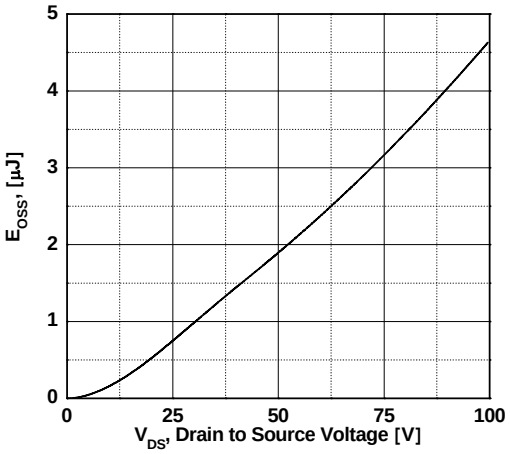
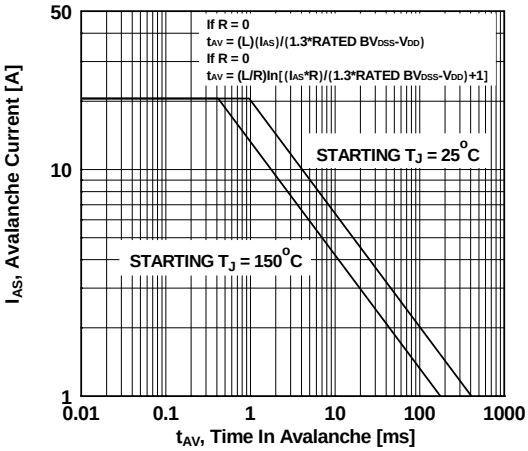
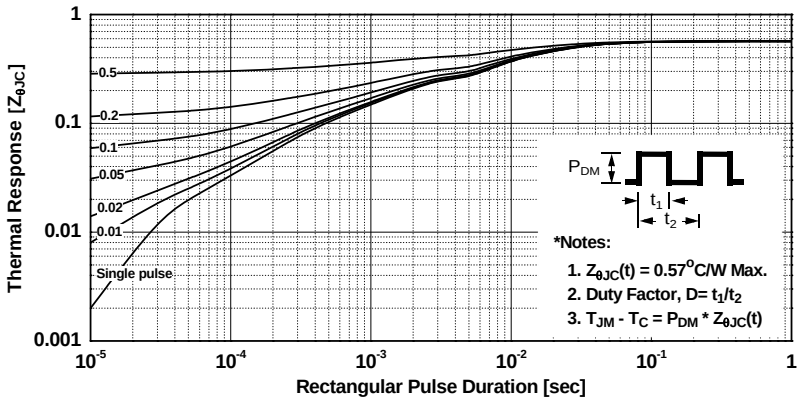


Figure 12. Unclamped Inductive Switching Capability

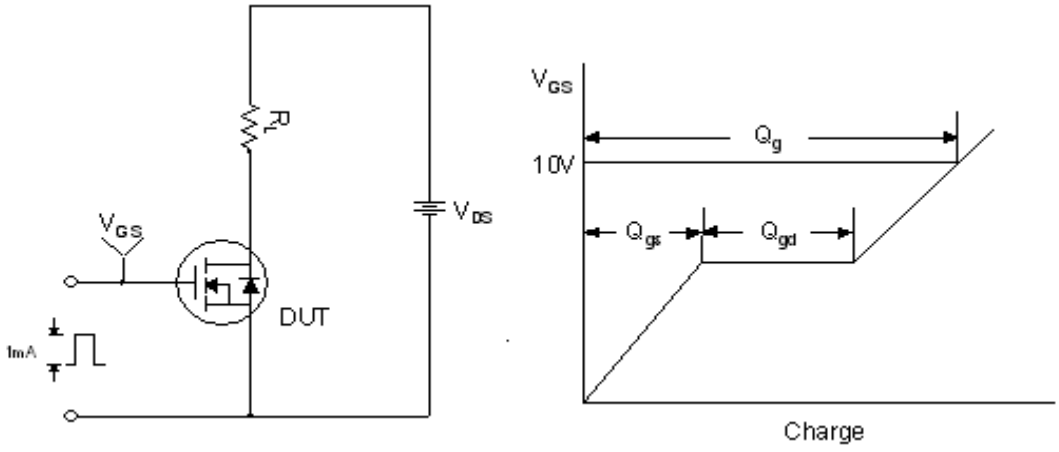


Typical Performance Characteristics (Continued)

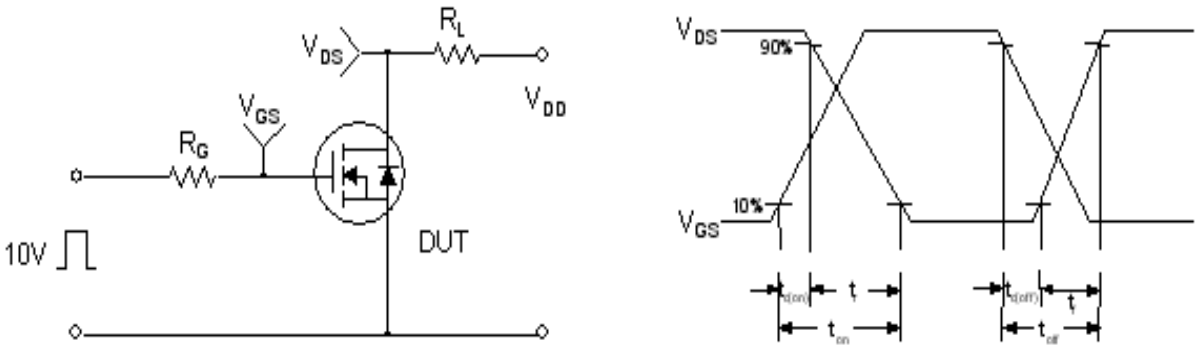
Figure 13. Transient Thermal Response Curve



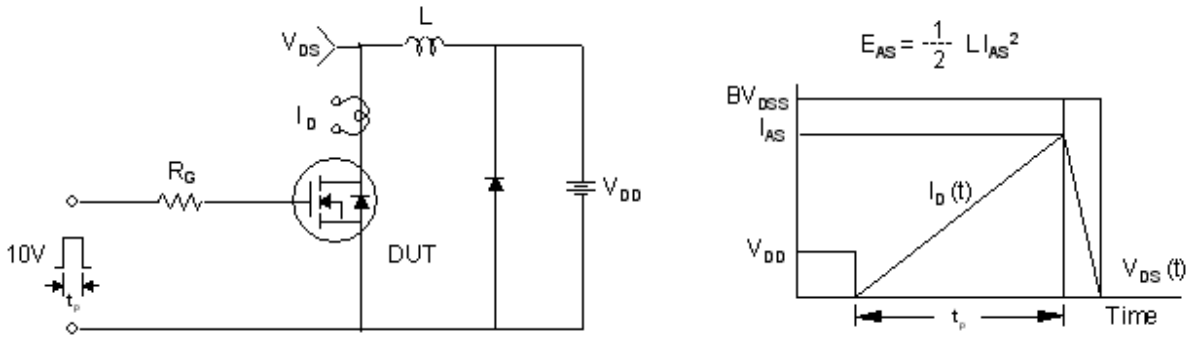
Gate Charge Test Circuit & Waveform



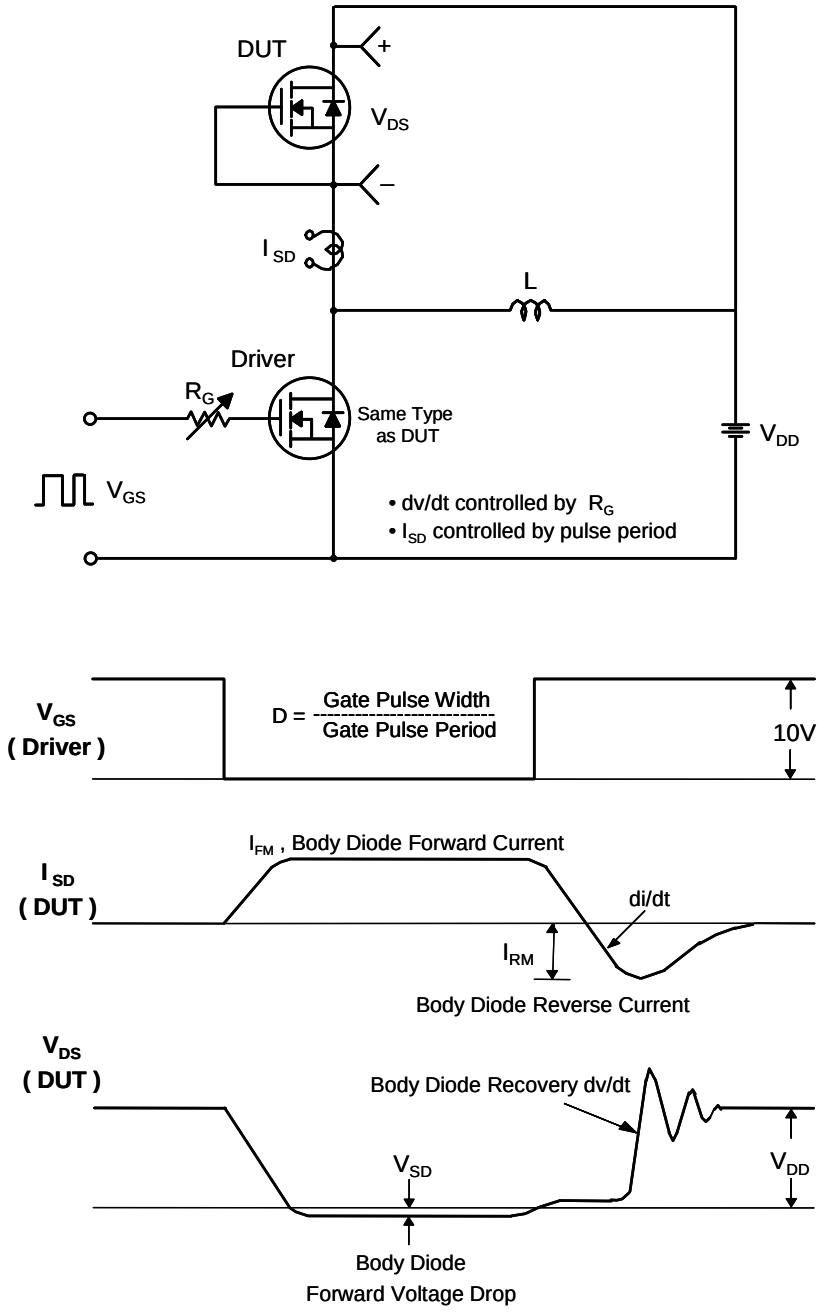
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

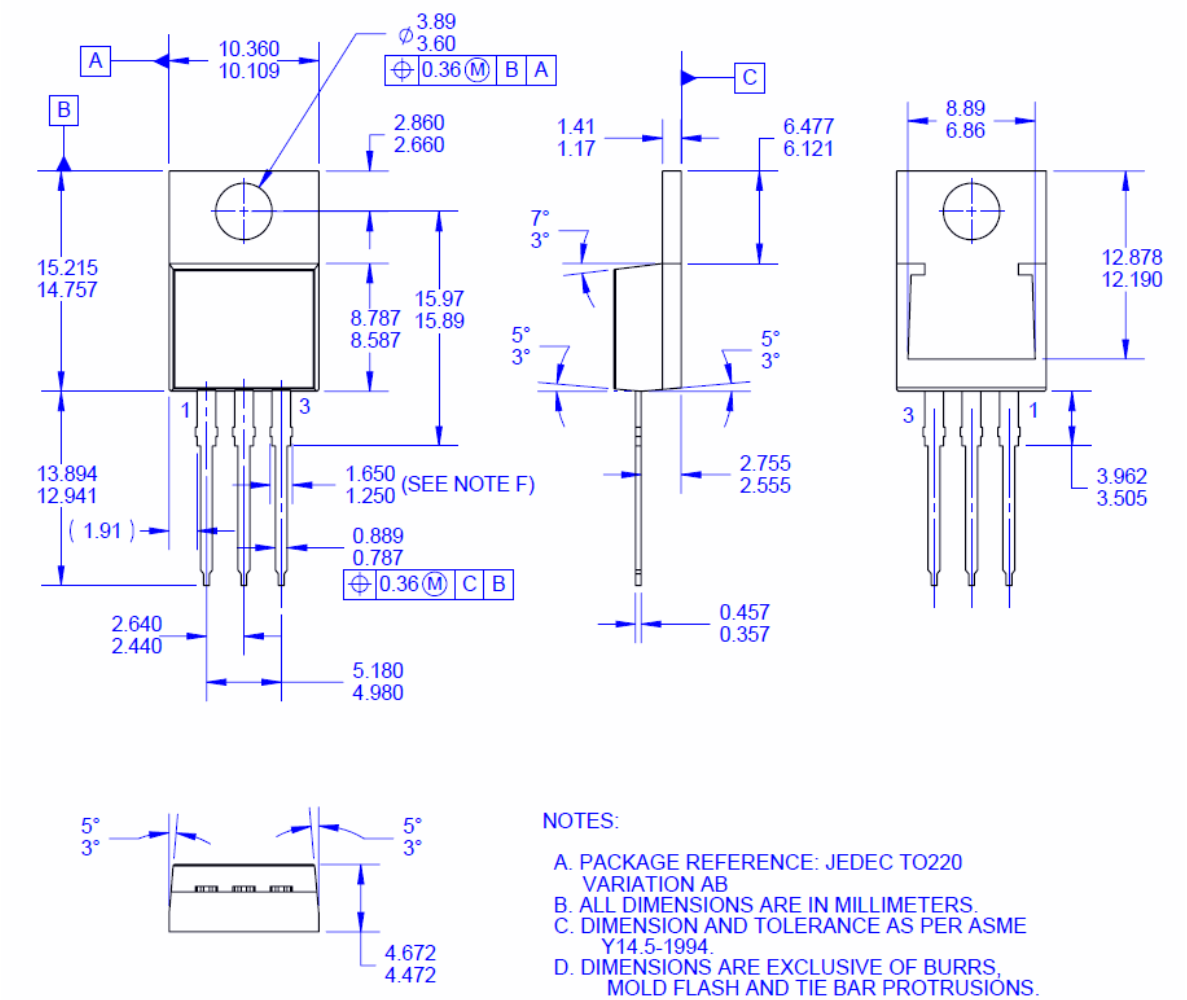


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-220



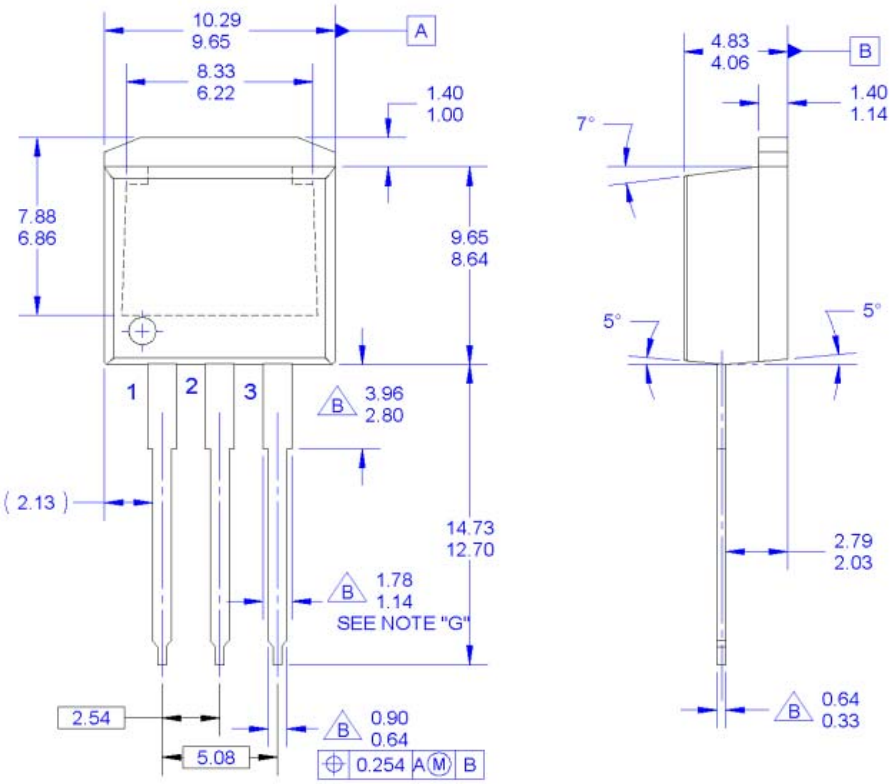
NOTES:

A. PACKAGE REFERENCE: JEDEC TO220 VARIATION AB
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. THIS PACKAGE IS FSZZ INTERNAL PRODUCTION AND INTENDED FOR DELTA CUSTOMER ONLY.
F. MAX WIDTH FOR F102 DEVICE = 1.35mm.
G. DRAWING FILE NAME: TO220T03REV3

Dimensions in Millimeters

Package Dimensions

I2PAK



NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
B. DOES NOT COMPLY JEDEC STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.
H. DRAWING FILE NAME: TO262A03REV5

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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