GENERAL DESCRIPTION

HT2279 is a high performance current mode PWM controller, optimized for low power AC/DC adapter applications.

For lower the standby power and higher RoHS compliant, the IC offers a Burst Mode control feature and ultra-low start-up current and operating current, that is, at the condition of no load or light load, HT2279 can reduce the switch frequency linearly which minimize the switching power loss; the ultra-low startup current and operating current make a reliable power for startup design, and also large resistor can be used in the startup circuit to improve switching efficiency.

The internal synchronous slope compensation circuit reduces the possible subharmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense(CS) input removes the signal glitch due to snubber diode circuit reverse recovery and thus greatly reduces the external component count and system cost in the design.

HT2279 offers comprehensive protection coverage with automatic self-recovery feature, including cycle by cycle over current protection (OCP), over load protection (OLP), over temperature protection(OTP), VDD OVP, under voltage lockout(UVLO). The gate-driven output is clamped to maximum 12V to protect the internal MOSFET.

In HT2279, OCP threshold slope is internally optimized for 65khz switching frequency application to reach constant output power limit over universal AC inout range.

Excellent EMI performance is achieved by using the soft-switching and frequency jittering at the totem-pole-gate-drive output. The tone energy at below 20KHZ is minimized in the design and audio noise is eliminated during operation. The HT2279 is the ideal substitute of the linear power supply or the RCC-mode power, for a better performance of the whole switch power system and a lower cost.

HT2279 is offered in SOP-8 and DIP-8 packages.

FEATURES

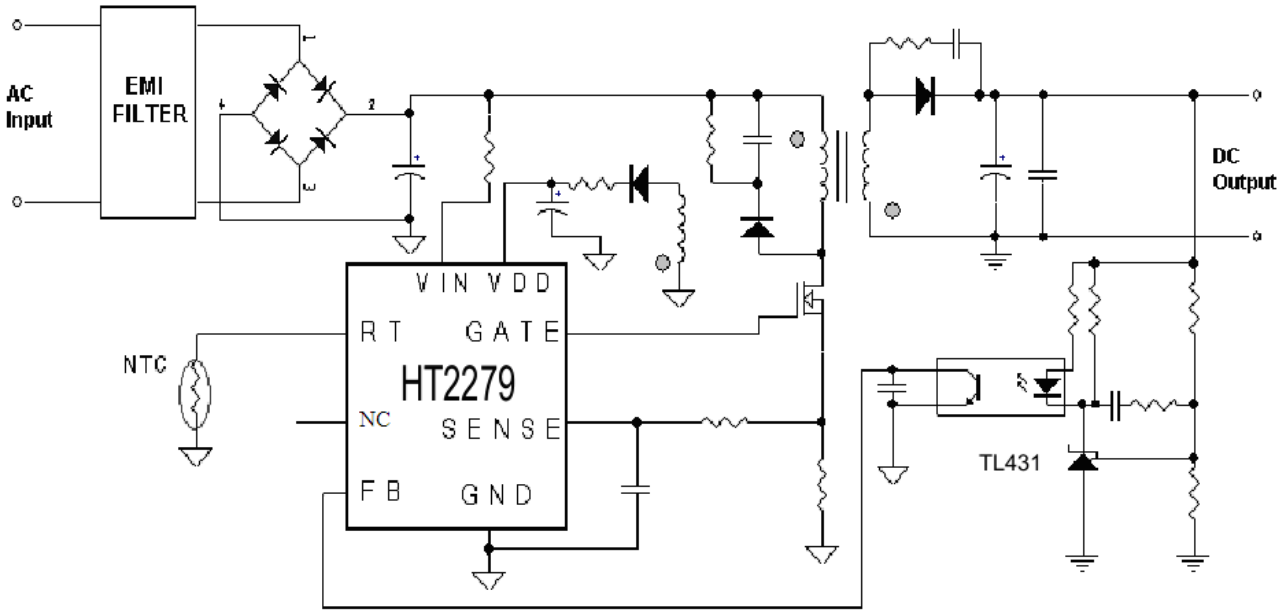
- Burst Mode function
- Low start-up current (6.5uA)
- Low operating current (2.3mA)
- 4ms soft start (the Soft-start)
- Soft-driven functions (Soft-driver)
- Optional latch for OLP, OTP, OVP
- Built-in synchronized slope compensation
- Current mode operation
- Switching frequency is internal set to be 65KHz, so no external resistor is need
- Externally programmable over-temperature protection (OTP)
- Cycle by cycle current limit protection (OCP)
- Built-in system VDD over-voltage protection (OVP)
- under voltage lockout（UVLO）
- The gate drive output voltage clamping (12V)
- Frequency jitter function
- Constant output power limit
- Overload protection (OLP)
- Free audio noise operation

APPLICATIONS

Offline AC/DC flyback converter for

- Adaptor
- Notebook Adaptor
- LCD Monitor/TV/PC/Set-Top Box Power Supplies
- Open-frame SMPS
- Printer Power

TYPICAL APPLICATION

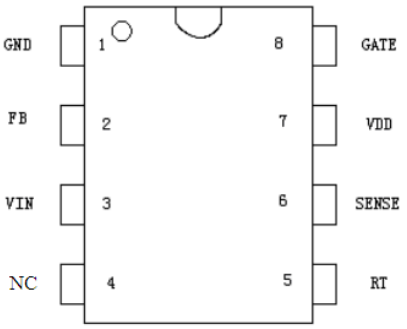


GENERAL INFORMATION

Pin Configuration

The pin map of HT2279 in DIP8 and SOP8 package is shown as below.

.



Ordering Information

Part Number	Description
HT2279DP	With Frequency Shuffling, DIP8, Pb-free, Have OVP
HT2279SP	With Frequency Shuffling, SOP8, Pb-free, Have OVP

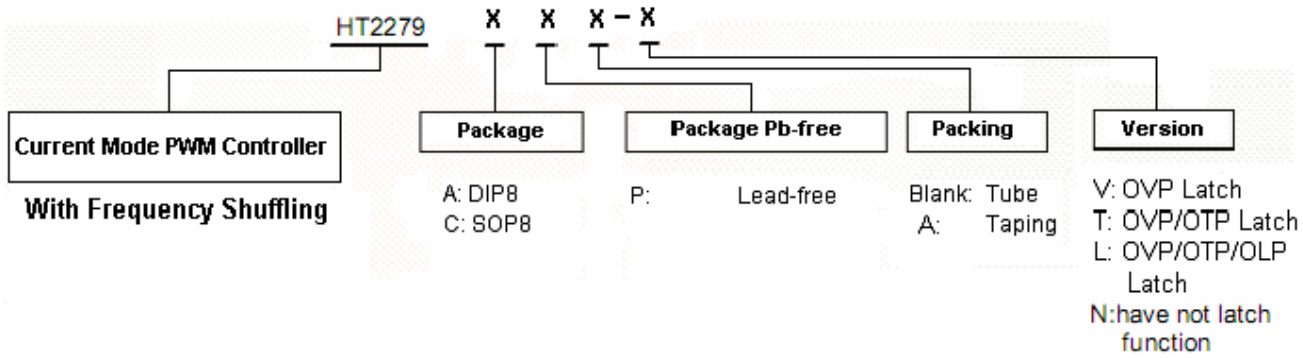
Package Dissipation Rating

Package	RθJA (°C/W)
DIP8	90
SOP8	150

Absolute Maximum Ratings

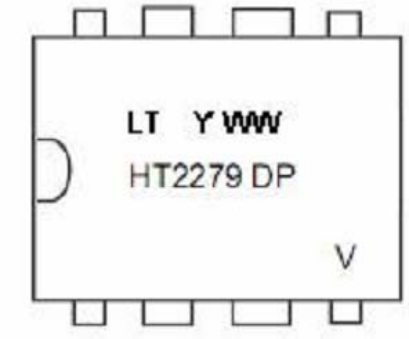
Parameter	Value
VDD/VIN DC Supply Voltage	30 V
VDD Clamp Continuous Current	10 mA
VIN / VDD Input Voltage	-0.3V to V_{clamp}
V_{FB} Input Voltage	-0.3 to 7V
V_{SENSE} Input Voltage to ense Pin	-0.3 to 7V
V_{RT} Input Voltage to RT Pin	-0.3 to 7V
Min/Max Operating Junction Temperature T_J	-20 to 150 °C
Min/Max Storage Temperature T_{stg}	-55 to 150 °C
Lead Temperature (Soldering,10secs)	260°C

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



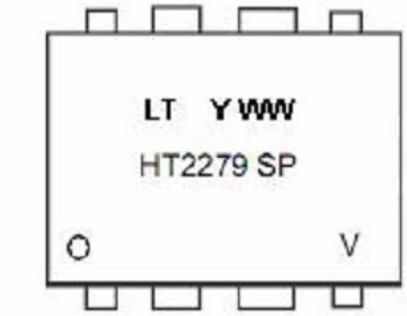
Marking Information

DIP8



D:DIP8 Package
P:pb-fee package
Y:Year Code(0-9)
WW:Week Code(01-52)
V: Internal Code

SOP8

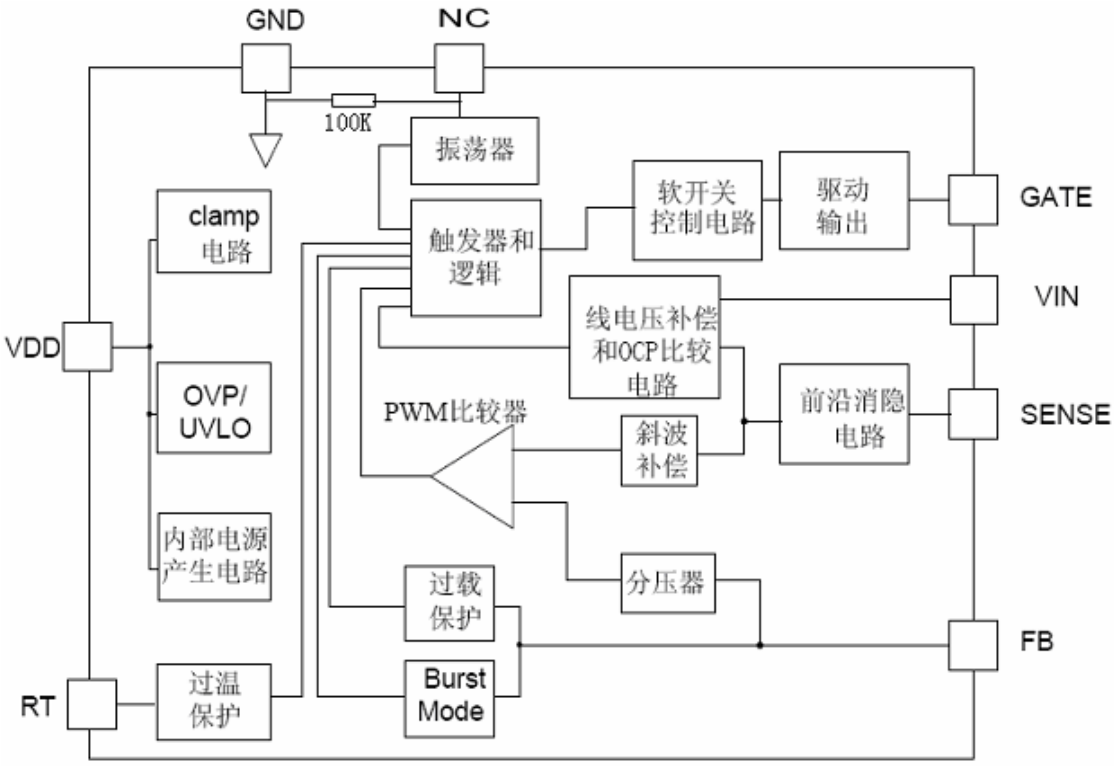


S:SOP8 Package
P:pb-fee package
Y:Year Code(0-9)
WW:Week Code(01-52)
V: Internal Code

TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	GND	P	Ground
2	FB	I	Feedback input pin. PWM duty cycle is determined by voltage level into this pin and current-sense signal level at Pin 6.
3	VIN	I	Connected through a large value resistor to rectified line input for Startup IC supply and line voltage sensing.
4	NC		
5	RT	I	Temperature sensing input pin. Connected through a NTC resistor to GND.
6	SENSE	I	Current sense input pin. Connected to MOSFET current sensing resistor node.
7	VDD	P	DC power supply pin.
8	GATE	O	Totem-pole gate drive output for power MOSFET.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min	Max	Unit
VDD	VDD Supply Voltage	12	23	V
T_A	Operating Ambient Temperature	-20	85	^oC

ESD INFORMATION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
HBM[Note]	Human Body Model on All Pins Except VIN and VDD	MIL-STD		3		KV
MM	Machine Model on All Pins	JEDEC-STD		250		V

Note: HBM all pins pass 3KV except High Voltage Input pin. The details are VIN passes 1kV, VDD passes 1.5KV, all other I/Os pass 3KV. In system application, High Voltage Input pin is either a high impedance input or connected to a cap. The lower rating has minimum impacts on system ESD performance.

ELECTRICAL CHARACTERISTICS

(T_A = 25^{O}C, VDD=16V if not otherwise noted)

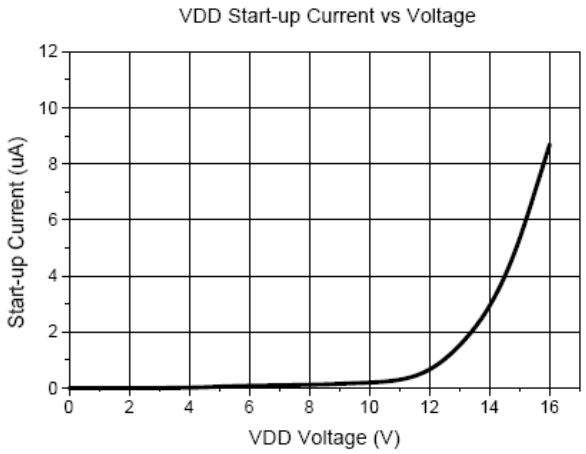
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD)						
I_VDD_Startup	VDD Start up Current	VDD =15V, Measure current into VDD		6.5	20	uA
I_VDD_Operation	Operation Current	V_{FB}=3V		2.3		mA
UVLO(Enter)	VDD Under Voltage Lockout Enter		9.5	10.5	11.5	V
UVLO(Exit)	VDD Under Voltage Lockout Exit (Startup)		16	17	18.5	V
OVP(ON)*Optional	VDD Over Voltage Protection Enter		23.5	25	26.5	V
OVP(OFF)*Optional	VDD Over Voltage Protection Exit (Recovery)		21.5	23.2	24.7	V
T_D_OVP	VDD OVP Debounce time			80		uSec
V_{DD}_Clamp	V_{DD} Zener Clamp Voltage	I(V_{DD}) = 5mA		36		V
Feedback Input Section(FB Pin)						
A_{VCS}	PWM Input Gain	$\Delta V_{FB}/\Delta V_{cs}$		2.6		V/V
V_{FB}_Open	V_{FB} Open Voltage			6		V
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND, measure current		0.80		mA
V_{TH}_0D	Zero Duty Cycle FB Threshold Voltage				0.95	V
V_{TH}_BM	Burst Mode FB Threshold Voltage			1.9		V
V_{TH}_PL	Power Limiting FB Threshold Voltage			4.4		V
T_D_PL	Power limiting Debounce Time			80		mSec
Z_{FB}_IN	Input Impedance			7.5		Kohm
Current Sense Input(Sense Pin)						
T_blanking	Sense Input Leading Edge Blanking Time			300		nS

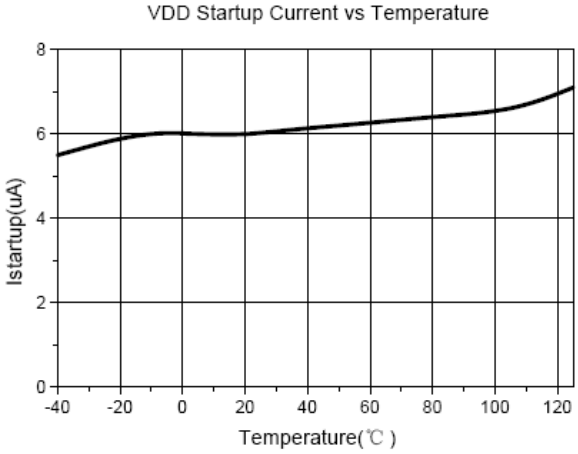
Z_{SENSE}_IN	Sense Input Impedance			39		Kohm
T_D_OC	Over Current Detection and Control Delay	CL=1nf at GATE,		120		nSec
V_{TH}_OC_0	Current Limiting Threshold at No Compensation	I(VIN) = 0uA	0.85	0.90	0.95	V
V_{TH}_OC_1	Current Limiting Threshold at Compensation	I(VIN) = 150uA		0.81		V
Oscillator						
F_{OSC}	Normal Oscillation Frequency		60	65	70	KHZ
Δf_Temp	Frequency Temperature Stability	-20°C to 100°C		5		%
Δf_VDD	Frequency Voltage Stability	VDD = 12-24V		5		%
F_BM	Burst Mode Base Frequency			22		KHZ
DC_max	Maxmum Duty Cycle		75	80	85	%
DC_min	Minimum Duty Cycle		-	-	0	%
Gate Drive Output						
VOL	Output Low Level	Io = -20 mA			0.3	V
VOH	Output High Level	Io = +20 mA	11			V
VG_Clamp	Output Clamp Voltage Level	VDD=20V		12		V
T_r	Output Rising Time	CL = 1nf		200		nSec
T_f	Output Falling Time	CL = 1nf		50		nSec
Over Temperature Protection						
I_RT	Output Current of RT pin			65		uA
V_{TH}_OTP	OTP Threshold Voltage		1.0	1.065	1.13	V
V_{TH}_OTP_off	OTP Recovery Threshold Voltage			1.165		V

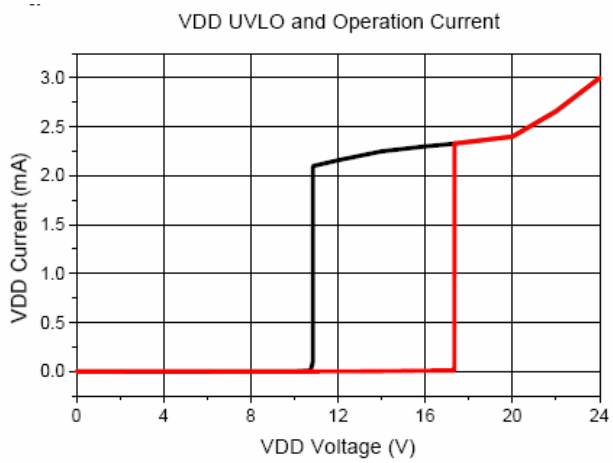
T_D_OTP	OTP De-bounce Time			100		uSec
V_RT_Open	RT Pin Open Voltage			3.5		V
Latch section						
I_VDD_latch	VDD current when latch	VDD=7.2V		35		uA
VDD_latch_release	De-latch voltage		5	6	7	V

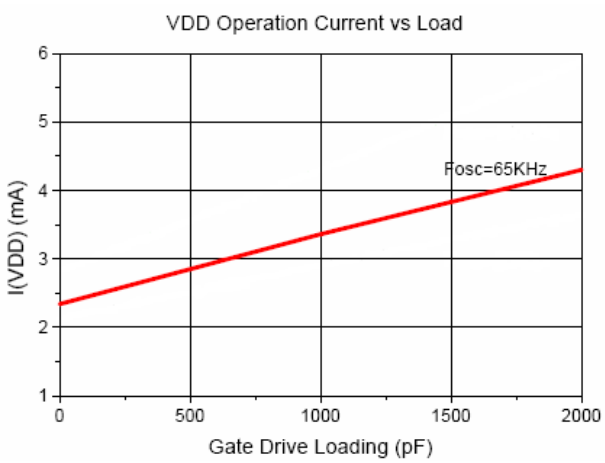
CHARACTERIZATION PLOTS

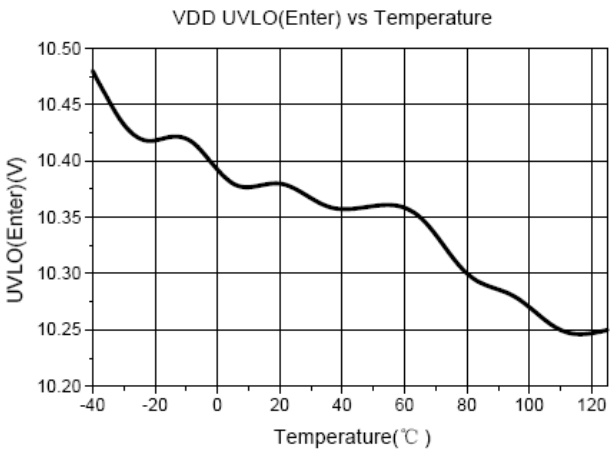
(T_A = 25^{O}C, VDD=16V, if not otherwise noted)

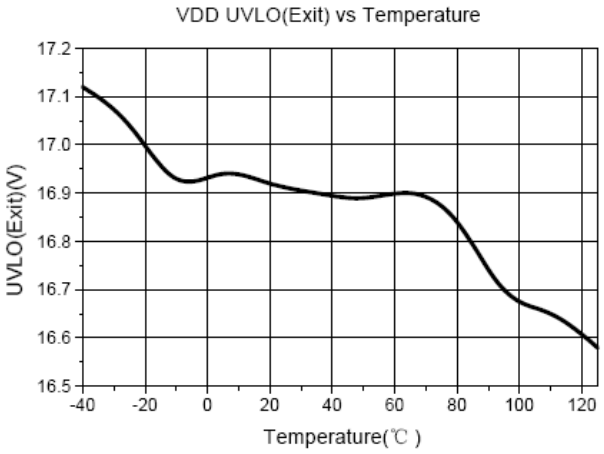


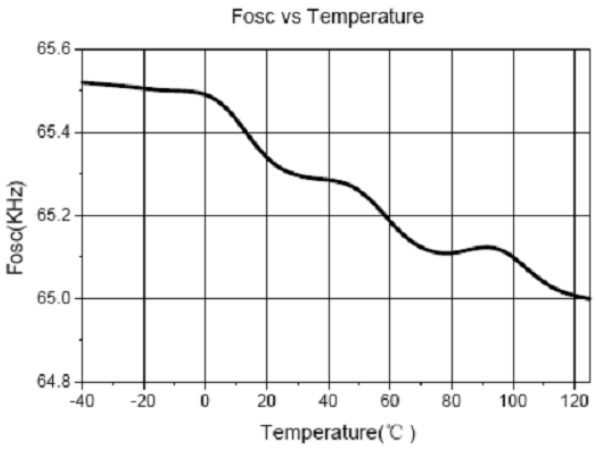


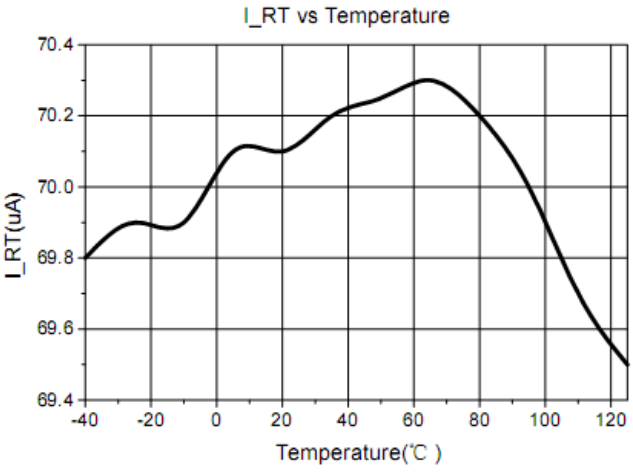





VDD UVLO(Enter) vs Temperature
UVLO(Enter)(V)
10.50
10.45
10.40
10.35
10.30
10.25
10.20
-40 -20 0 20 40 60 80 100 120
Temperature(℃)


VDD UVLO(Exit) vs Temperature
UVLO(Exit)(V)
17.2
17.1
17.0
16.9
16.8
16.7
16.6
16.5
-40 -20 0 20 40 60 80 100 120
Temperature(℃)


Fosc vs Temperature
Fosc(KHz)
65.6
65.4
65.2
65.0
64.8
-40 -20 0 20 40 60 80 100 120
Temperature(℃)


I_RT vs Temperature
I_RT(uA)
70.4
70.2
70.0
69.8
69.6
69.4
-40 -20 0 20 40 60 80 100 120
Temperature(℃)

OPERATION DESCRIPTION

HT2279 is a highly integrated, high-performance current-mode PWM Controller chip. Applicable in high-power notebook power adapter Switching power supplies and switching power converter. Extremely low startup power Flow and operating current, and under light load or no load burst mode function, can effectively reduce the switching power supply system standby Power consumption and improve power conversion efficiency. Built-in synchronized slope compensation The LEB function of the feedback pin is not only can reduce the switching power supply Number of components of the system, but also increase the stability of the system to avoid Harmonic oscillation. HT2279 also offers a variety of comprehensive Recovery protection mode. The main features of functions described as follows:

- **Startup Current and Start up Control**

Startup current of HT2279 is designed to be extremely low at 6.5uA, so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss, predigest the design of startup circuit and provides reliable startup in application. For the design of AC/DC adaptor with universal input range, a startup resistor of 2 MΩ, 1/8 W could be used together with a VDD capacitor to provide a fast startup and low power dissipation solution.

- **Operating Current**

HT2279 has a low operating current (2.3mA). The low operating current, and the burst mode control circuit can effectively improve the conversion efficiency of the switching power supply; and can reduce the requirement of VDD hold capacitor.

- **Soft-start**

As soon as VDD reaches UVLO(on), the soft-start function operates, the peak current is then gradually increased from zero. Every restart attempt is followed by 4ms soft-start.

- **Gate Drive**

HT2279 Gate is connected to the Gate of an external MOSFET for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI. Good tradeoff is achieved through the built-in totem pole gate drive design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 12V clamp is added for MOSFET gate protection at higher than expected VDD input.

- **Over Temperature Protection**

A NTC resistor in series with a regular resistor should connect between RT and GND for temperature sensing and protection. NTC resistor value becomes lower when the ambient temperature rises. With the fixed internal current IRT flowing through the resistors, the voltage at RT pin becomes lower at high temperature. The internal OTP circuit is triggered and shutdown the MOSFET when the sensed input voltage is lower than VTH_OTP.

- **Oscillator**

The switching frequency is internal set to be 65KHz,so none external resistor is needed

- **Internal synchronized slope compensation**

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

- **Current Sensing and Leading Edge Blanking**

The HT2279 Internal cycle-by-cycle current limit function (cycle-by-cyclecurrent limiting).Switch current sense resistor input to the SENSE pin. Internal leading edge blanking circuit can eliminate the MOSFET is turned on the burr of the moment caused by the induced voltage due to snubber diode reverse recovery, the SENSE input of an external RC filter circuit eliminates the need for. Limiting in the blanking period are prohibited and can not turn off the external MOSFET. PWM duty cycle is determined by the current sense input voltage and the voltage of the FB input.

- **Frequency shuffling for EMI improvement**

The frequency Shuffling/jittering (switching frequency modulation) is implemented in HT2279. The oscillation frequency is modulated with a internally generated random source so that the tone energy is evenly spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design in meeting stringent EMI requirement.

- **Burst Mode Operation**

At zero load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy.

HT2279 self adjusts the switching mode

according to the loading condition. At from no load to light/medium load condition, the FB input drops below burst mode threshold level (1.8V). Device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off stateto minimize the switching loss thus reduce thestandby power consumption to the greatest extend. The nature of high frequency switching also reduces the audio noise at any loading conditions.

- **Protection Controls**

Good system reliability is achieved with HT2279's rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), over temperature protection (OTP), on-chip VDD over voltage protection (OVP, optional) and under voltage lockout (UVLO). The OCP threshold value is self adjusted lower at higher current into VIN pin. This OCP threshold slope adjustment helps to compensate the increased output power limit at higher AC voltage caused by inherent Over-Current sensing and control delay. A constant output power limit is achieved with recommended OCP compensation scheme on HT2279.

At output overload condition, FB voltage is biased higher. When FB input exceeds power limit threshold value for more than 80mS, control circuit reacts to turnoff the power MOSFET.

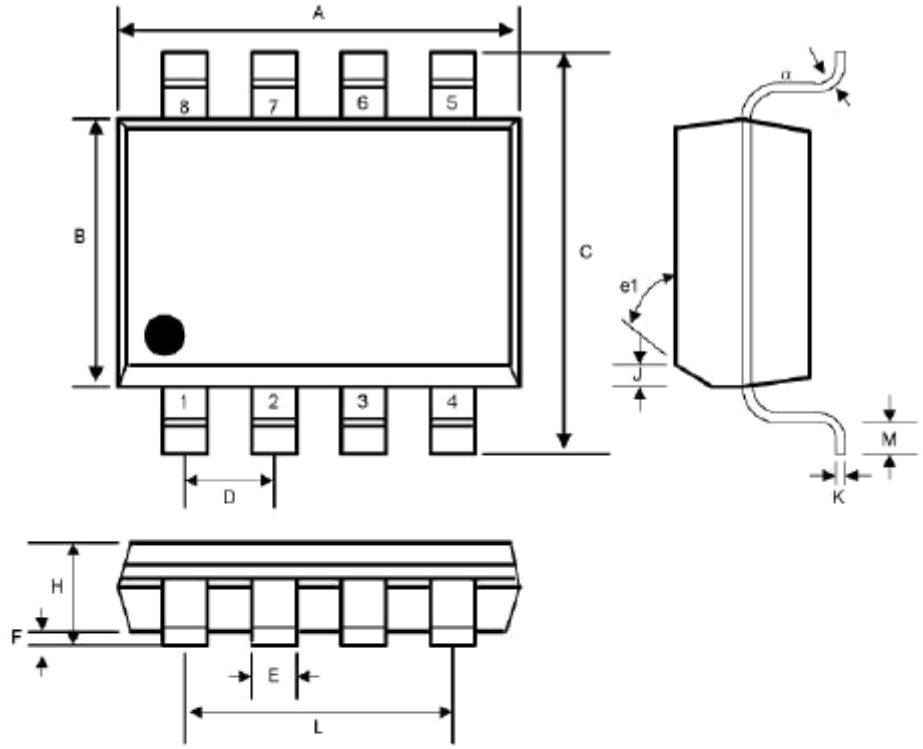
Similarly, control circuit shutdowns the power MOSFET when an Over Temperature condition is detected. HT2279 resumes the operation when temperature drops below the hysteresis value.

VDD is supplied with transformer auxiliary winding output. It is clamped when VDD is higher than 36V. MOSFET is shut down when VDD drops below UVLO(enter) limit and device enters power on startup sequence thereafter.

Optional latch can be select for OLP、OVP、OTP. The recovery of the AC/DC system could only start by resetting internal latch when VDD voltage drops below VDD_De-latch value. This could be achieved by unplugging/re-plugging of AC source

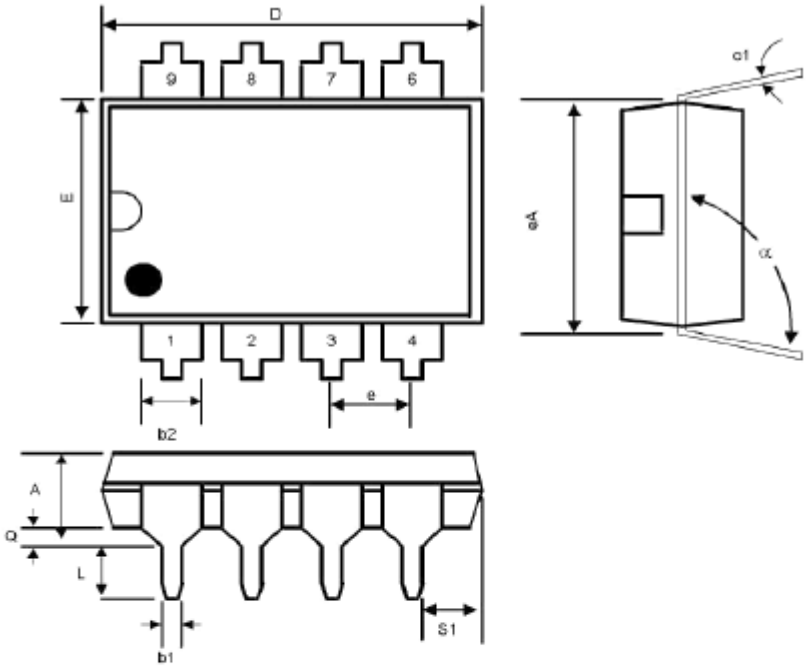
PACKAGE MECHANICAL DATA

SOP8 PACKAGE OUTLINE DIMENSIONS



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.188	0.197	4.80	5.00	-
B	0.149	0.158	3.80	4.00	-
C	0.228	0.244	5.80	6.20	-
D	0.050 BSC		1.27 BSC		-
E	0.013	0.020	0.33	0.51	-
F	0.004	0.010	0.10	0.25	-
H	0.053	0.069	1.35	1.75	-
J	0.011	0.019	0.28	0.48	
K	0.007	0.010	0.19	0.25	-
M	0.016	0.050	0.40	1.27	
L	0.150 REF		3.81 REF		-
e1	45^0		45^0		-
α	0^0	8^0	0^0	8^0	-

DIP8 PACKAGE OUTLINE DIMENSIONS



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b1	0.014	0.023	0.36	0.58	-
b2	0.045	0.065	1.14	1.65	-
c1	0.008	0.015	0.20	0.38	-
D	0.355	0.400	9.02	10.16	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	-
s1	0.005	-	0.13	-	-
α	90^0	105^0	90^0	105^0	-