

## TMOS V™ Power Field Effect Transistor N-Channel Enhancement-Mode Silicon Gate

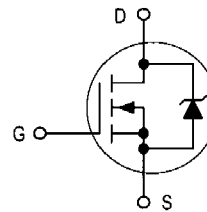
TMOS V is a new technology designed to achieve an on-resistance area product about one-half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E-FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

### New Features of TMOS V

- On-resistance Area Product about One-half that of Standard MOSFETs with New Low Voltage, Low  $R_{DS(on)}$  Technology
- Faster Switching than E-FET Predecessors

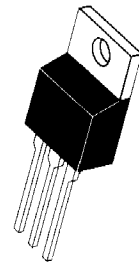
### Features Common to TMOS V and TMOS E-FETS

- Avalanche Energy Specified
- $I_{DSS}$  and  $V_{DS(on)}$  Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E-FET



**MTP50N06V**

TMOS POWER FET  
42 AMPERES  
60 VOLTS  
 $R_{DS(on)} = 0.028 \text{ OHM}$



TO-220AB

### MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	60	Vdc
Drain-Gate Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	60	Vdc
Gate-Source Voltage — Continuous	$V_{GS}$	$\pm 20$	Vdc
— Non-Repetitive ( $t_p \leq 10 \text{ ms}$ )	$V_{GSM}$	$\pm 25$	Vpk
Drain Current — Continuous @ $25^\circ\text{C}$	$I_D$	42	Adc
— Continuous @ $100^\circ\text{C}$	$I_D$	30	
— Single Pulse ( $t_p \leq 10 \mu\text{s}$ )	$I_{DM}$	147	Apk
Total Power Dissipation @ $25^\circ\text{C}$	$P_D$	125	Watts
Derate above $25^\circ\text{C}$		0.83	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy — Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 25 \text{ Vdc}$ , $V_{GS} = 10 \text{ Vdc}$ , $I_L = 42 \text{ Apk}$ , $L = 0.454 \mu\text{H}$ , $R_G = 25 \Omega$ )	$E_{AS}$	400	mJ
Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.2	$^\circ\text{C/W}$
— Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

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**MTP50N06V****ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Drain-Source Breakdown Voltage ( $V_{GS} = 0\text{ Vdc}$ , $I_D = 250\ \mu\text{Adc}$ ) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	60 —	— 69	— —	Vdc mV/°C
Zero Gate Voltage Drain Current ( $V_{DS} = 60\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ ) ( $V_{DS} = 60\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $T_J = 150^\circ\text{C}$ )	$I_{DSS}$	— —	— —	10 100	$\mu\text{Adc}$
Gate-Body Leakage Current ( $V_{GS} = \pm 20\text{ Vdc}$ , $V_{DS} = 0$ )	$I_{GSS}$	—	—	100	nAdc

**ON CHARACTERISTICS (1)**

Gate Threshold Voltage ( $V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{Adc}$ ) Temperature Coefficient (Negative)	$V_{GS(th)}$	2.0 —	2.7 3.0	4.0 —	Vdc mV/°C
Static Drain-Source On-Resistance ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 21\text{ Adc}$ )	$R_{DS(on)}$	—	0.025	0.028	Ohm
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ ) ( $I_D = 42\text{ Adc}$ ) ( $I_D = 21\text{ Adc}$ , $T_J = 150^\circ\text{C}$ )	$V_{DS(on)}$	— —	1.4 —	1.7 1.6	Vdc
Forward Transconductance ( $V_{DS} = 6.25\text{ Vdc}$ , $I_D = 20\text{ Adc}$ )	$g_{FS}$	16	23	—	mhos

**DYNAMIC CHARACTERISTICS**

Input Capacitance	$(V_{DS} = 25\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$C_{iss}$	—	1644	2320	pF
Output Capacitance		$C_{oss}$	—	465	660	
Reverse Transfer Capacitance		$C_{rss}$	—	112	230	

**SWITCHING CHARACTERISTICS (2)**

Turn-On Delay Time	$(V_{DD} = 25\text{ Vdc}$ , $I_D = 42\text{ Adc}$ , $V_{GS} = 10\text{ Vdc}$ , $R_G = 9.1\ \Omega$ )	$t_{d(on)}$	—	12	20	ns
Rise Time		$t_r$	—	122	250	
Turn-Off Delay Time		$t_{d(off)}$	—	64	110	
Fall Time		$t_f$	—	54	90	
Gate Charge (See Figure 8)	$(V_{DS} = 48\text{ Vdc}$ , $I_D = 42\text{ Adc}$ , $V_{GS} = 10\text{ Vdc}$ )	$Q_T$	—	47	70	nC
		$Q_1$	—	9	—	
		$Q_2$	—	21	—	
		$Q_3$	—	16	—	

**SOURCE-DRAIN DIODE CHARACTERISTICS**

Forward On-Voltage (1)	$(I_S = 42\text{ Adc}$ , $V_{GS} = 0\text{ Vdc}$ ) $(I_S = 42\text{ Adc}$ , $V_{GS} = 0\text{ Vdc}$ , $T_J = 150^\circ\text{C}$ )	$V_{SD}$	— —	1.06 0.99	2.5 —	Vdc
Reverse Recovery Time (See Figure 14)		$(I_S = 42\text{ Adc}$ , $V_{GS} = 0\text{ Vdc}$ , $di_S/dt = 100\text{ A}/\mu\text{s}$ )	$t_{rr}$	—	84	—
	$t_a$		—	73	—	
	$t_b$		—	11	—	
Reverse Recovery Stored Charge	$Q_{RR}$		—	0.28	—	$\mu\text{C}$

**INTERNAL PACKAGE INDUCTANCE**

Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	$L_D$	—	3.5 4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	$L_S$	—	7.5	—	nH