SI1902DL

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.385 at V_{GS} = 4.5 V	0.70
	0.630 at V_{GS} = 2.5 V	0.54

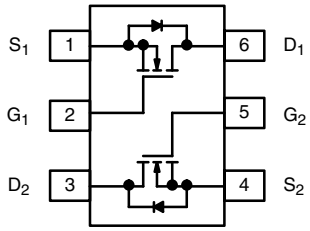
FEATURES

- TrenchFET® Power MOSFETS: 2.5 V Rated

Pb-free Available

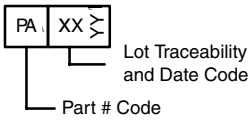
RoHS* COMPLIANT

SOT-363
SC-70 (6-LEADS)



Top View

Marking Code



Ordering Information: Si1902DL-T1 (with Tape and Reel)
Si1902DL-T1-E3 (Lead (Pb)-free with Tape and Reel)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		**Symbol**	**5 secs**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	20		V
Gate-Source Voltage		V_{GS}	±12		
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	0.70	0.66	A
	T_A = 85 °C		0.50	0.48	
Pulsed Drain Current		I_{DM}	1.0		
Continuous Source Current (Diode Conduction)[a]		I_S	0.25	0.23	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	0.30	0.27	W
	T_A = 85 °C		0.16	0.14	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 5 sec	R_{thJA}	360	415	°C/W
	Steady State		400	460	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	300	350	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

* Pb containing terminations are not RoHS compliant, exemptions may apply

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SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	0.6		1.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V			1	µA
		V_{DS} = 16 V_{GS} = 0 V, T_J = 85°C			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 4.5 V	1.0			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 0.66 A		0.320	0.385	Ω
		V_{GS} = 2.5 V, I_D = 0.40 A		0.560	0.630	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 0.66 A		1.5		S
Diode Forward Voltage[a]	V_{SD}	I_S = 0.23 A, V_{GS} = 0 V		0.8	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 0.66 A		0.8	1.2	nC
Gate-Source Charge	Q_{gs}			0.06		
Gate-Drain Charge	Q_{gd}			0.30		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 20 Ω I_D ≅ 0.5 A, V_{GEN} = 4.5 V, R_G = 6 Ω		10	20	ns
Rise Time	t_r			16	30	
Turn-Off DelayTime	$t_{d(off)}$			10	20	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 0.23 A, di/dt = 100 A/µs		20	40	

Notes:

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

b. Guaranteed by design, not subject to production testing.