

T-45-23-17



**MC14520B**  
See Page 6-288

**MC14521B**

**CMOS MSI**  
(LOW-POWER COMPLEMENTARY MOS)  
**24-STAGE FREQUENCY DIVIDER**

**24-STAGE FREQUENCY DIVIDER**

The MC14521B consists of a chain of 24 flip-flops with an input circuit that allows three modes of operation. The input will function as a crystal oscillator, an RC oscillator, or as an input buffer for an external oscillator. Each flip-flop divides the frequency of the previous flip-flop by two, consequently this part will count up to  $2^{24} = 16,777,216$ . The count advances on the negative going edge of the clock. The outputs of the last seven-stages are available for added flexibility.

- All Stages are Resettable
- Reset Disables the RC Oscillator for Low Standby Power Drain
- RC and Crystal Oscillator Outputs Are Capable of Driving External Loads
- Test Mode to Reduce Test Time
- $V_{DD}$  and  $V_{SS}$  Pins Brought Out on Crystal Oscillator Inverter to Allow the Connection of External Resistors for Low-Power Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range.

**L SUFFIX CERAMIC PACKAGE CASE 620**      **P SUFFIX PLASTIC PACKAGE CASE 648**

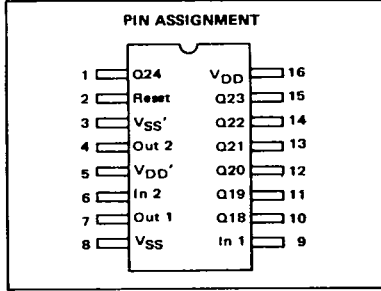
**ORDERING INFORMATION**

A Series: -55°C to +125°C  
MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to +85°C  
MC14XXXBCP (Plastic Package)  
MC14XXXBCL (Ceramic Package)

**MAXIMUM RATINGS\*** (Voltages Referenced to  $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} - 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient), per Pin	± 10	mA
$P_D$	Power Dissipation, per Package†	500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C



\*Maximum Ratings are those values beyond which damage to the device may occur.  
†Temperature Derating: Plastic "P" Package: -12mW/°C from 65°C to 85°C  
Ceramic "L" Package: -12mW/°C from 100°C to 125°C

**BLOCK DIAGRAM**

OUTPUT	COUNT CAPACITY
Q18	$2^{18} = 262,144$
Q19	$2^{19} = 524,288$
Q20	$2^{20} = 1,048,576$
Q21	$2^{21} = 2,097,152$
Q22	$2^{22} = 4,194,304$
Q23	$2^{23} = 8,388,608$
Q24	$2^{24} = 16,777,216$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	T <sub>low</sub> *		25°C			T <sub>high</sub> *		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage "0" Level V <sub>in</sub> = V <sub>DD</sub> or 0	V <sub>OL</sub>	5.0	-	0.05	-	0	0.05	-	0.05	Vdc	
		10	-	0.05	-	0	0.05	-	0.05		
		15	-	0.5	-	0	0.05	-	0.05		
	"1" Level V <sub>in</sub> = 0 or V <sub>DD</sub>	V <sub>OH</sub>	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
			10	9.95	-	9.95	10	-	9.95	-	
			15	14.95	-	14.95	15	-	14.95	-	
Input Voltage "0" Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	V <sub>IL</sub>	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc	
		10	-	3.0	-	4.50	3.0	-	3.0		
		15	-	4.0	-	6.75	4.0	-	4.0		
	"1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IH</sub>	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
			10	7.0	-	7.0	5.50	-	7.0	-	
			15	11.0	-	11.0	8.25	-	11.0	-	
Output Drive Current (AL Device) (V <sub>OH</sub> = 2.5 Vdc) Source (V <sub>OH</sub> = 4.6 Vdc) Pins 4 & 7 (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OH</sub> = 2.5 Vdc) Source (V <sub>OH</sub> = 4.6 Vdc) Pins 1, 10, (V <sub>OH</sub> = 9.5 Vdc) 11, 12, 13, 14 (V <sub>OH</sub> = 13.5 Vdc) and 15  (V <sub>OL</sub> = 0.4 Vdc) Sink (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	I <sub>OH</sub>	5.0	-1.2	-	-1.0	-1.7	-	-0.7	-	mAdc	
		5.0	-0.25	-	-0.2	-0.36	-	-0.14	-		
		10	-0.62	-	-0.5	-0.9	-	-0.35	-		
		15	-1.8	-	-1.5	-3.5	-	-1.1	-		
		5.0	-3.0	-	-2.4	-4.2	-	-1.7	-		
		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-		
	I <sub>OL</sub>	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc	
		10	1.6	-	1.3	2.25	-	0.9	-		
		15	4.2	-	3.4	8.8	-	2.4	-		
		5.0	-2.5	-	-2.1	-4.2	-	-1.7	-		
		5.0	-0.52	-	-0.44	-0.88	-	-0.36	-		
		5.0	-1.3	-	-1.1	-2.25	-	-0.9	-		
Output Drive Current (CL/CP Device) (V <sub>OH</sub> = 2.5 Vdc) Source (V <sub>OH</sub> = 4.6 Vdc) Pins 4 & 7 (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OH</sub> = 2.5 Vdc) Source (V <sub>OH</sub> = 4.6 Vdc) Pins 1, 10, (V <sub>OH</sub> = 9.5 Vdc) 11, 12, 13, 14 (V <sub>OH</sub> = 13.5 Vdc) and 15  (V <sub>OL</sub> = 0.4 Vdc) Sink (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	I <sub>OH</sub>	5.0	-1.0	-	-0.8	-1.7	-	-0.6	-	mAdc	
		5.0	-0.2	-	-0.16	-0.36	-	-0.12	-		
		10	-0.5	-	-0.4	-0.9	-	-0.3	-		
		15	-1.4	-	-1.2	-3.5	-	-1.0	-		
		5.0	-2.5	-	-2.1	-4.2	-	-1.7	-		
		5.0	-0.52	-	-0.44	-0.88	-	-0.36	-		
I <sub>OL</sub>	5.0	0.52	-	0.44	0.88	-	0.36	-	mAdc		
	10	1.3	-	1.1	2.25	-	0.9	-			
	15	3.6	-	3.0	8.8	-	2.4	-			
Input Current (AL Device)	I <sub>in</sub>	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdc	
Input Current (CL/CP Device)	I <sub>in</sub>	15	-	±0.3	-	±0.00001	±0.3	-	±1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	-	-	-	-	5.0	7.5	-	-	pF	
Quiescent Current (AL Device) (Per Package)	I <sub>DD</sub>	5.0	-	5.0	-	0.005	5.0	-	150	μAdc	
		10	-	10	-	0.010	10	-	300		
		15	-	20	-	0.015	20	-	600		
Quiescent Current (CL/CP Device) (Per Package)	I <sub>DD</sub>	5.0	-	20	-	0.005	20	-	150	μAdc	
		10	-	40	-	0.010	40	-	300		
		15	-	80	-	0.015	80	-	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.42 μA/kHz) f + I <sub>DD</sub>							μAdc	
		10	I <sub>T</sub> = (0.85 μA/kHz) f + I <sub>DD</sub>								
		15	I <sub>T</sub> = (1.4 μA/kHz) f + I <sub>DD</sub>								

\*T<sub>low</sub> = -55°C for AL Device, -40°C for CL/CP Device.  
T<sub>high</sub> = +125°C for AL Device, +85°C for CL/CP Device.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V_{1k}$$

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.003.

\*\*The formulas given are for the typical characteristics only at 25°C.

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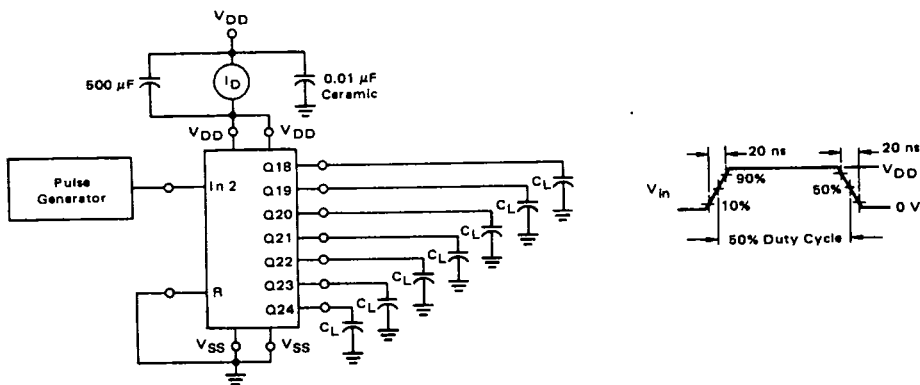
SWITCHING CHARACTERISTICS\* (CL = 50 pF, TA = 25°C)

Characteristic	Symbol	VDD Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time (Counter Outputs) tTLH, tTHL = (1.5 ns/pF) CL + 25 ns tTLH, tTHL = (0.75 ns/pF) CL + 12.5 ns tTLH, tTHL = (0.55 ns/pF) CL + 12.5 ns	tTLH, tTHL	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q18 tPHL, tPLH = (1.7 ns/pF) CL + 4415 ns tPHL, tPLH = (0.66 ns/pF) CL + 1667 ns tPHL, tPLH = (0.5 ns/pF) CL + 1275 ns Clock to Q24 tPHL, tPLH = (1.7 ns/pF) CL + 5915 ns tPHL, tPLH = (0.66 ns/pF) CL + 2167 ns tPHL, tPLH = (0.5 ns/pF) CL + 1675 ns	tPHL, tPLH	5.0 10 15  5.0 10 15	— — —  — — —	4.5 1.7 1.3  6.0 2.2 1.7	9.0 3.5 2.7  12 4.5 3.5	μs
Propagation Delay Time Reset to Qn tPHL = (1.7 ns/pF) CL + 1215 ns tPHL = (0.66 ns/pF) CL + 467 ns tPHL = (0.5 ns/pF) CL + 350 ns	tPHL	5.0 10 15	— — —	1300 500 375	2600 1000 750	ns
Clock Pulse Width	tWH(d)	5.0 10 15	385 150 120	140 55 40	— — —	ns
Clock Pulse Frequency	fcl	5.0 10 15	— — —	3.5 9.0 12	2.0 5.0 6.5	MHz
Clock Rise and Fall Time	tTLH, tTHL	5.0 10 15	— — —	— — —	15 5.0 4.0	μs
Reset Pulse Width	tWH(R)	5.0 10 15	1400 600 450	700 300 225	— — —	ns
Reset Removal Time	trem	5.0 10 15	30 0 -40	-200 -160 -110	— — —	ns

\*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 - POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



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FIGURE 2 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

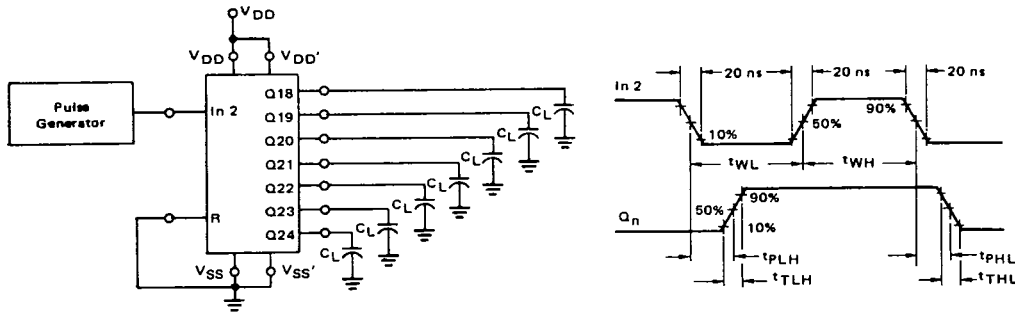
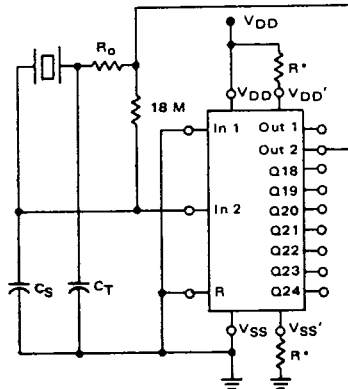


FIGURE 3 - CRYSTAL OSCILLATOR CIRCUIT



\* Optional for low power operation.  
10 kΩ < R < 70 kΩ

FIGURE 4 - TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

CHARACTERISTIC	500 kHz CIRCUIT	50 kHz CIRCUIT	UNIT
<b>Crystal Characteristics</b>			
Resonant Frequency	500	50	kHz
Equivalent Resistance, $R_S$	1.0	6.2	kΩ
<b>External Resistor/Capacitor Values</b>			
$R_0$	47	750	kΩ
$C_T$	82	82	pF
$C_S$	20	20	pF
<b>Frequency Stability</b>			
Frequency Change as a Function of $V_{DD}$ ( $T_A = 25^\circ C$ )			
$V_{DD}$ Change from 5.0 V to 10 V	+6.0	+2.0	ppm
$V_{DD}$ Change from 10 V to 15 V	+2.0	+2.0	ppm
Frequency Change as a Function of Temperature ( $V_{DD} = 10 V$ )			
$T_A$ Change from $-55^\circ C$ to $+25^\circ C$			
MC14521 only	-4.0	-2.0	ppm
Complete Oscillator*	+100	+120	ppm
$T_A$ Change from $+25^\circ C$ to $+125^\circ C$			
MC14521 only	-2.0	-2.0	ppm
Complete Oscillator*	-160	-560	ppm

\* Complete oscillator includes crystal, capacitors, and resistors.



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FIGURE 5 - RC OSCILLATOR STABILITY

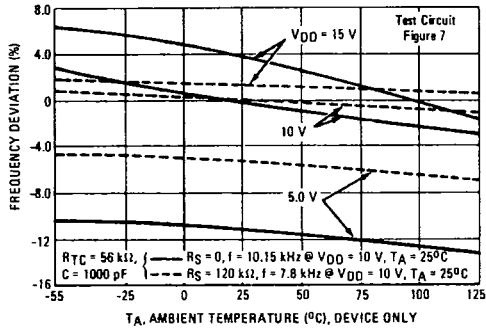


FIGURE 6 - RC OSCILLATOR FREQUENCY AS A FUNCTION OF R<sub>TC</sub> AND C

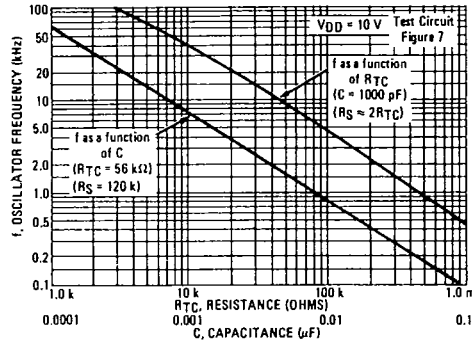


FIGURE 7 - RC OSCILLATOR CIRCUIT

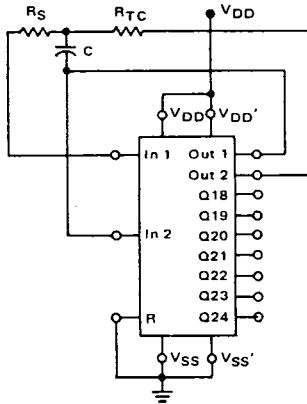
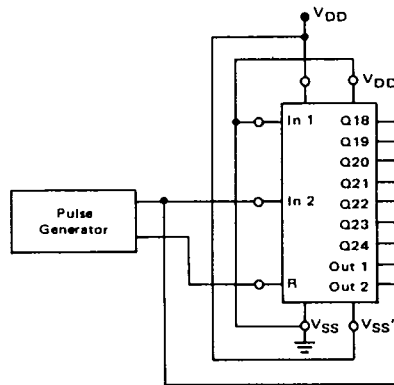


FIGURE 8 - FUNCTIONAL TEST CIRCUIT



FUNCTIONAL TEST SEQUENCE

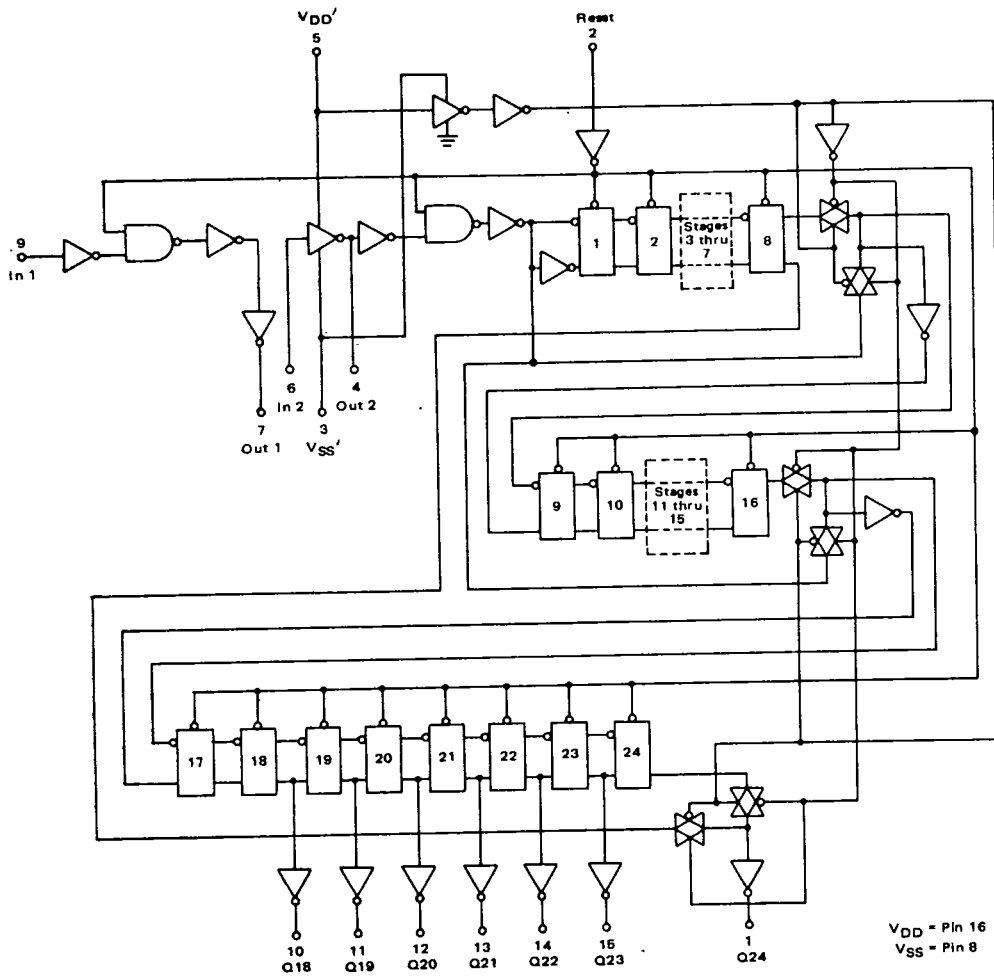
	INPUTS		OUTPUTS		COMMENTS			
	Reset	In 2	Out 2	Q18 thru Q24				
<p>A test function (see Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections, and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a logic "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into Input 2 (In 2) which will cause the counter to ripple from an all "1" state to an all "0" state.</p>	1	0	0	V <sub>DD</sub>	0	Counter is in three 8-stage sections in parallel mode. Counter is reset. In 2 and Out 2 are connected together.		
	0	1	1	↓	↓	↓	First "0" to "1" transition on In 2, Out 2 node.	
		0	0				255 "0" to "1" transitions are clocked into this In 2, Out 2 node.	
		1	1				1	The 255th "0" to "1" transition.
		0	0				1	1
		0	0				1	1
		1	0		1	Counter converted back to 24-stages in series mode.		
		1	0		1	Out 2 converts back to an output.		
		0	1		0	0	Counter ripples from an all "1" state to an all "0" stage.	



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LOGIC DIAGRAM



VDD = Pin 16  
VSS = Pin 8

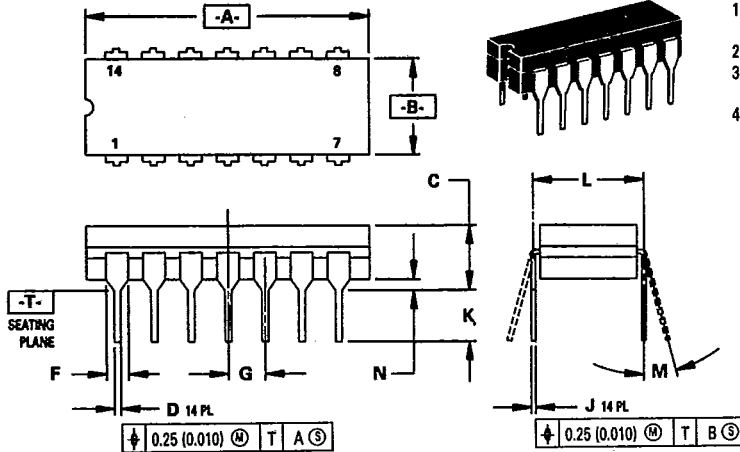
**PACKAGE DIMENSIONS**

T-90-20

The standard package availability for each device is indicated on the front page of the individual data sheets. Dimensions for the packages are given in this chapter. Surface mount packages may be special ordered by specifying the following suffixes: "D" (narrow SOIC), "DW" (wide SOIC), or "FN" (PLCC). For example, to order a quad NOR gate, use MC14001BD.

**14-PIN PACKAGE**

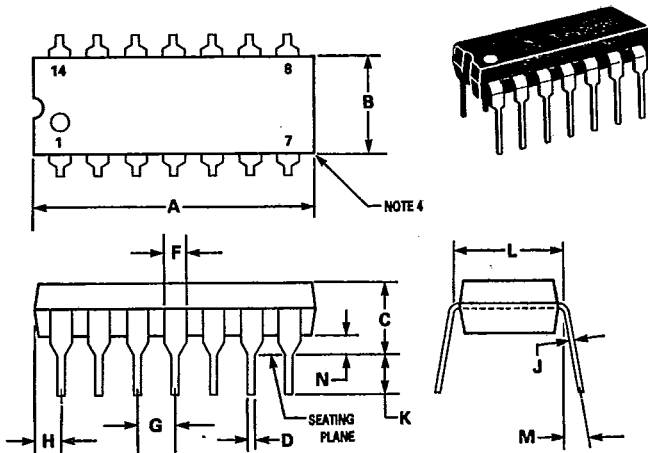
**CERAMIC PACKAGE  
CASE 632-08**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

**PLASTIC PACKAGE  
CASE 646-06**



- NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
  4. ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

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PACKAGE DIMENSIONS (Continued)

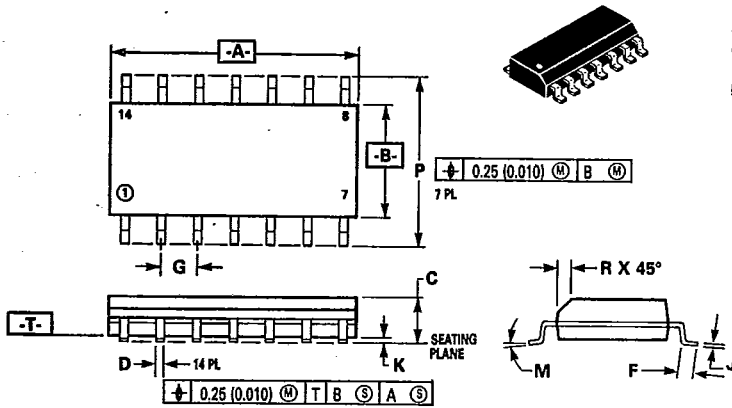
14-PIN PACKAGE

SOIC PACKAGE  
CASE 751A-02  
D SUFFIX

NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

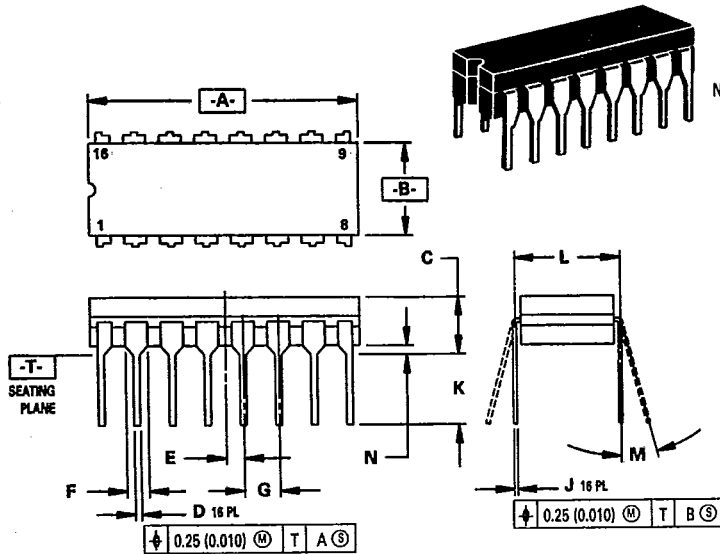




PACKAGE DIMENSIONS (Continued)

16-PIN PACKAGE

CERAMIC PACKAGE  
CASE 620-09

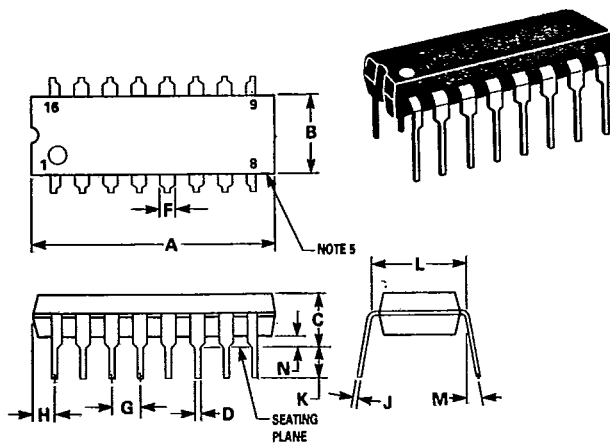


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

PLASTIC PACKAGE  
CASE 648-06



NOTES:

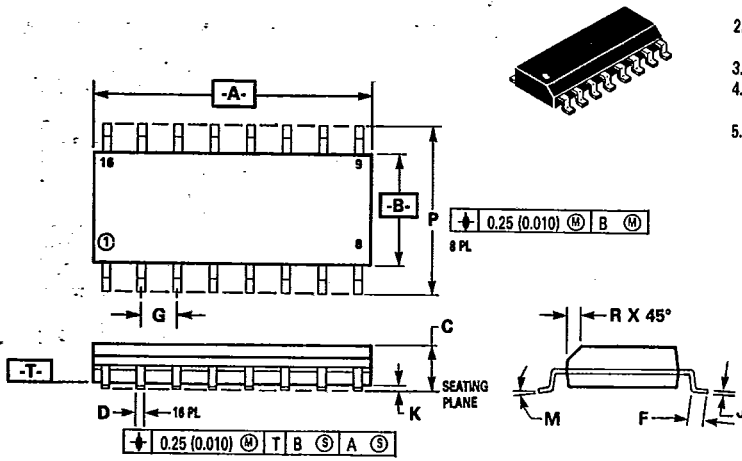
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS.
5. ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.040

PACKAGE DIMENSIONS (Continued)

16-PIN PACKAGE

SOIC PACKAGE  
CASE 751B-03  
D SUFFIX

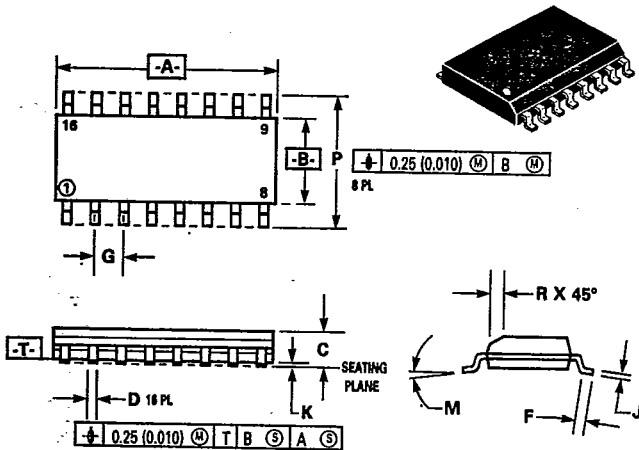


NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOIC PACKAGE  
CASE 751G-01  
DW SUFFIX



NOTES:

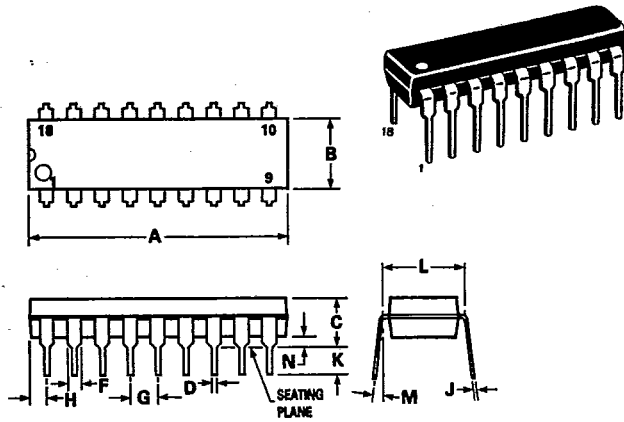
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
	0.25	0.75	0.010	0.029

PACKAGE DIMENSIONS (Continued)

18-PIN PACKAGE

PLASTIC PACKAGE  
CASE 707-02

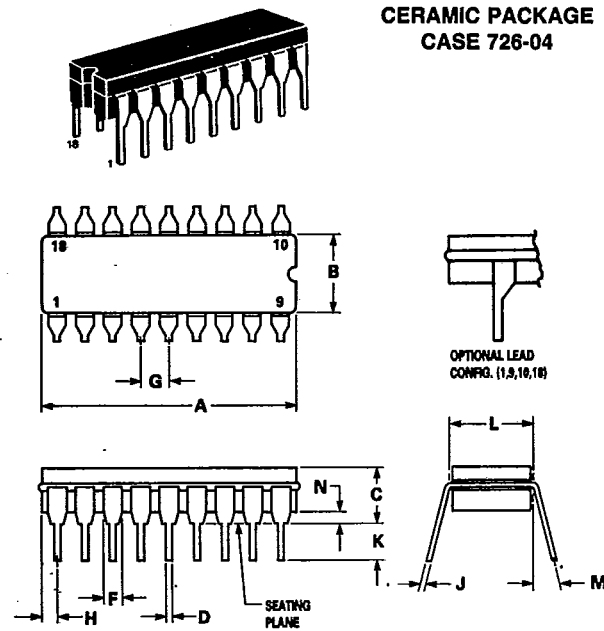


NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CERAMIC PACKAGE  
CASE 726-04



NOTES:

1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

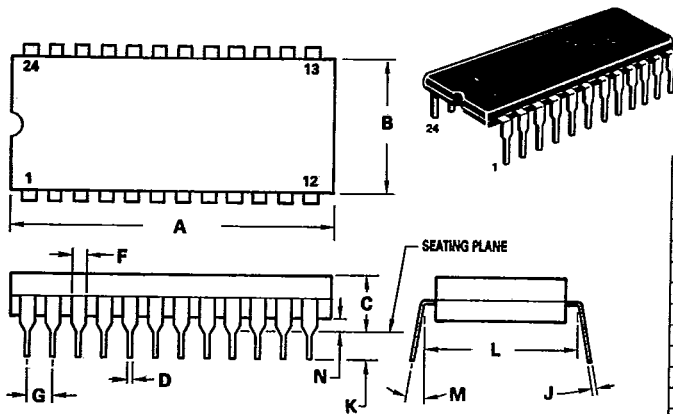
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

9

PACKAGE DIMENSIONS (Continued)

24-PIN PACKAGE

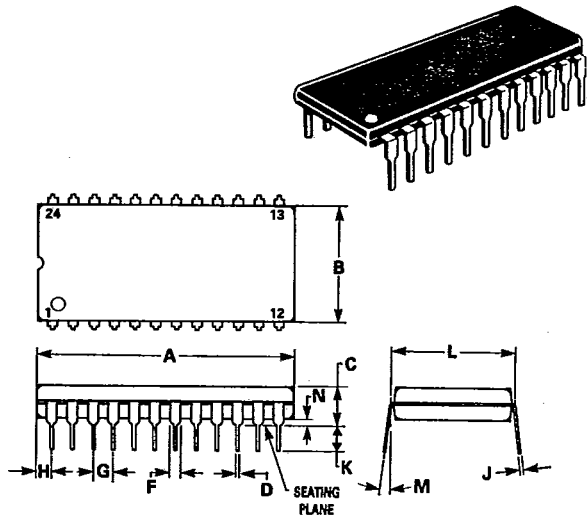
CERAMIC PACKAGE  
CASE 623-05



- NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

PLASTIC PACKAGE  
CASE 709-02



- NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
  2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040