ispLSI® 6192

High Density Programmable Logic with Dedicated Memory and Register/Counter Modules

Features

- **A FAMILY OF HIGHLY INTEGRATED, CELL-BASED, PROGRAMMABLE LOGIC DEVICES CONSISTING OF:**
  - **— Memory Module**
  - **— Register/Counter Module**
  - **— Programmable Logic Module**
  - **— 159 User Logic/Memory/Register/Counter Pins**
  - **— 25000-Gate Overall Density**
- **MEMORY MODULE OPTIONS**
  - **— FIFO (6192FF), Single-Port RAM (6192SM) or Dual-Port RAM (6192DM)**
  - **— Programmable Organizations:**
    - **Single 256 x 18 or 512 x 9**
    - **Dual 128 x 18 or 256 x 9 (6192SM)**
  - **— 31 Dedicated Data and Control Interface Pins**
  - **— Programmable Almost Empty and Almost Full Flags (FIFO)**
  - **— Dedicated Arbitration/Busy Logic (Dual-Port RAM)**
- **REGISTER/COUNTER MODULE**
  - **— 8 Cascadable 16-Bit Functions**
  - **— 9 Programmable Modes Including Counter, Timer, Shift Register and Register Options**
  - **— 24 Dedicated Module Data and Control Pins Including Terminal Count Flags**
  - **— Automatic Preload, Count Up/Down Options**
- **HIGH DENSITY PROGRAMMABLE LOGIC MODULE**
  - **— 8000-Gate General Purpose Programmable Logic Block**
  - **— 192 General Purpose Logic Registers**
  - **— 24-Input, Twin Generic Logic Blocks (GLBs) Implement Any Registered or Combinatorial Functions**
  - **— High-Speed Global Interconnects**
  - **— 96 I/O Pins with Input Registers**
  - **— Security Cell Prevents Unauthorized Design Copying**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 77 MHz Maximum Operating Frequency**
  - **— t_{pd} = 15 ns Propagation Delay**
  - **— f_{cnt} = 125 MHz Counter Frequency**
  - **— 50MHz FIFO Data Rate**
  - **— 20ns Memory Access Time**
  - **— Electrically Erasable and Reprogrammable**
  - **— Unused Product Term Shutdown Saves Power**
- **IN-SYSTEM PROGRAMMABLE**
  - **— Supports ISP™ or ispJTAG™ Programming**
  - **— Change Logic and Interconnects in Seconds**
  - **— Reprogram Soldered Devices for Debugging**
- **IEEE 1149.1 BOUNDARY SCAN COMPATIBLE**

Functional Block Diagram

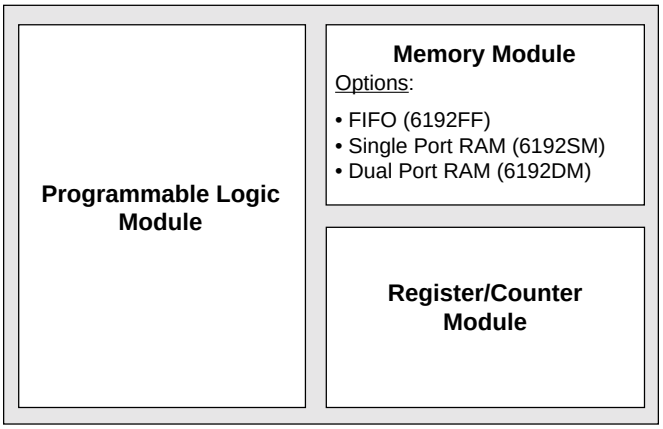

Table 1. ispLSI 6192 Device Features

	Memory Module Options			Register/Counter Module	General Programmable Logic Module
Functions	FIFO 6192FF	Single-Port SRAM 6192SM	Dual-Port SRAM 6192DM	Programmable Register / Counter / Timer / Shift Register	Universal: Registered or Combinatorial
Organization (Programmable)	Single: 512 x 9 or 256 x 18 Dual: 128 x 18 or 256 x 9 (6192SM Only)			Cascadeable 8 x 16 Bit Words	192 Macrocells
External Interface	18 I/O & 13 Control Pins			16 I/O & 8 Control Pins	96 I/O / 5 Clocks / 2 Global Output Enables
Performance	20ns Memory Access Time (Tacc)			125MHz Counter Frequency (Fcnt)	15ns Logic Delay (Tpd) 77MHz Frequency (Fmax)
Programmability	In-System Programmable				
Testability	IEEE 1149.1 Boundary Scan Test				
Package	208-Pin Metal Quad Flat Pack (MQFP)				

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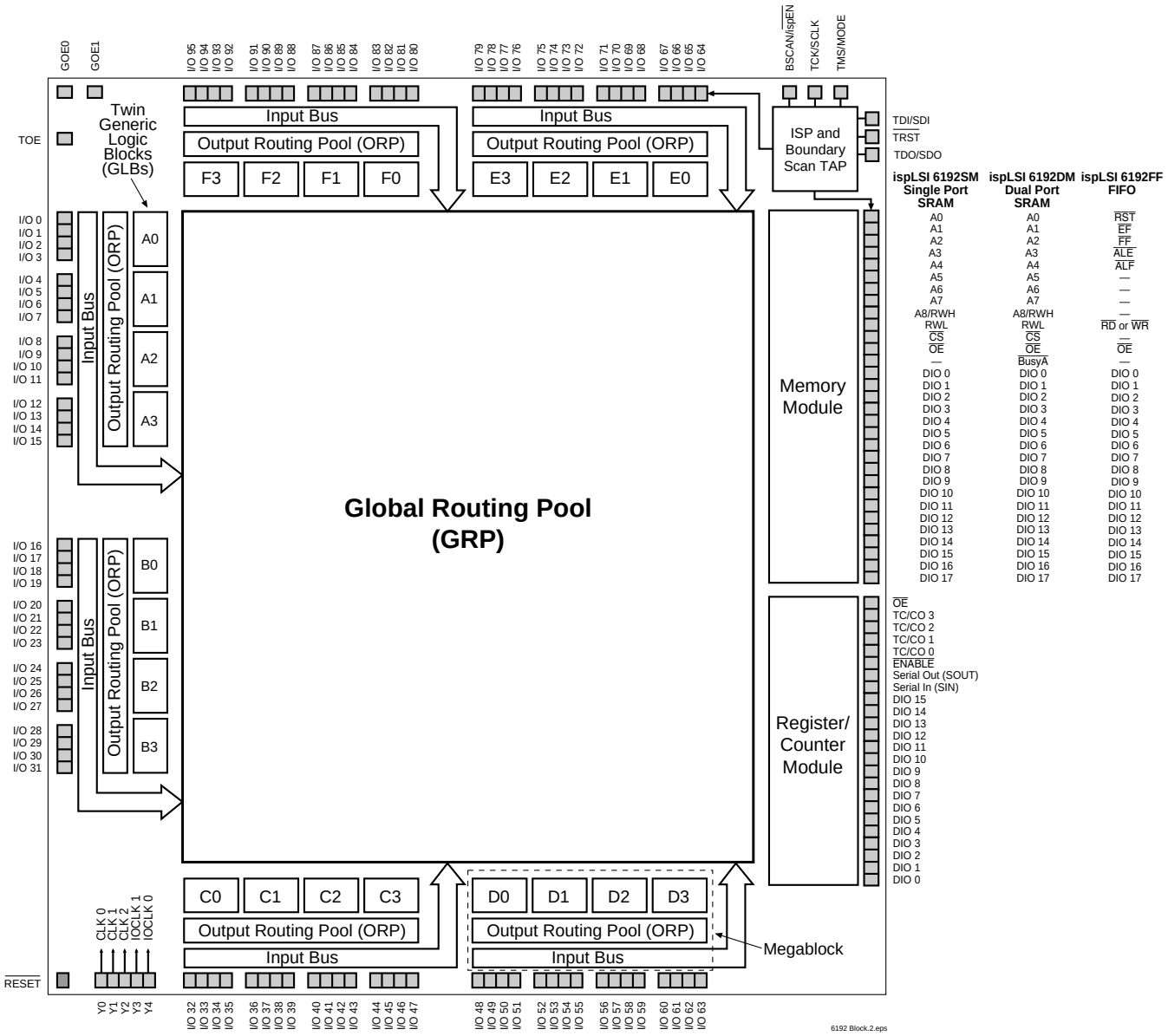
May 1999

Functional Block Diagram

Figure 1. ispLSI 6192 Functional Block Diagram



ispLSI 6192SM Single Port SRAM	ispLSI 6192DM Dual Port SRAM	ispLSI 6192FF FIFO
A0	A0	$\overline{RST}$
A1	A1	$\overline{EF}$
A2	A2	$\overline{FF}$
A3	A3	$\overline{ALE}$
A4	A4	$\overline{ALF}$
A5	A5	—
A6	A6	—
A7	A7	—
A8/RWH	A8/RWH	—
RWL	RWL	$\overline{RD}$ or $\overline{WR}$
$\overline{CS}$	$\overline{CS}$	—
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
—	BusyA	—
DIO 0	DIO 0	DIO 0
DIO 1	DIO 1	DIO 1
DIO 2	DIO 2	DIO 2
DIO 3	DIO 3	DIO 3
DIO 4	DIO 4	DIO 4
DIO 5	DIO 5	DIO 5
DIO 6	DIO 6	DIO 6
DIO 7	DIO 7	DIO 7
DIO 8	DIO 8	DIO 8
DIO 9	DIO 9	DIO 9
DIO 10	DIO 10	DIO 10
DIO 11	DIO 11	DIO 11
DIO 12	DIO 12	DIO 12
DIO 13	DIO 13	DIO 13
DIO 14	DIO 14	DIO 14
DIO 15	DIO 15	DIO 15
DIO 16	DIO 16	DIO 16
DIO 17	DIO 17	DIO 17

$\overline{OE}$
TC/CO 3
TC/CO 2
TC/CO 1
TC/CO 0
$\overline{ENABLE}$
Serial Out (SOUT)
Serial In (SIN)
DIO 15
DIO 14
DIO 13
DIO 12
DIO 11
DIO 10
DIO 9
DIO 8
DIO 7
DIO 6
DIO 5
DIO 4
DIO 3
DIO 2
DIO 1
DIO 0

Note:
Since certain signal names are duplicated on Memory Module and Register/Counter Module pins ($\overline{OE}$, DIO), the notation:
$\overline{OE}$ (RAM)
$\overline{OE}$ (RC)
DIO (RAM)
DIO (FIFO)
DIO (RC)
will be used periodically in this data sheet to differentiate signals.

Refer to table on Module I/O Cell Connectivity regarding the use of Module I/O Cells as inputs to the Global Routing Pool.

Description

The ispLSI 6192 device is a High Density, Cell-Based Programmable Logic Devices that contain a dedicated Memory Module, a dedicated Register/Counter Module and an 8000-gate general-purpose Programmable Logic block. Output Routing Pools (ORP) and a Global Routing Pool (GRP) give complete interconnectivity between these elements. The Cell-Based architecture with dedicated modules have been added to enhance the functionality, performance and utilization of the devices.

The ispLSI 6192 family is offered in three versions: the 6192FF (FIFO), 6192SM (Single Port RAM) and 6192DM (Dual Port RAM). All three devices employ the same general-purpose programmable logic module and register/counter module, with only the memory module functionality changing. The pinouts of the three devices are different only in the memory module control interface pins.

Memory Module

Lattice Semiconductor offers a dedicated dual-port FIFO module in the 6192FF device. The FIFO is user configurable as a 256 x 18 or 512 x 9 block and is connected to the external world through dedicated FIFO I/O pins. The other data port of the FIFO goes to the GRP. A variety of FIFO control flags such as Full ($\overline{FF}$), Almost Full ($\overline{ALF}$), Almost Empty ($\overline{ALE}$) and Empty ($\overline{EF}$) are available as dedicated device outputs. These signals are also available as inputs to the GRP to facilitate use by on-chip logic. The FIFO operation is discussed at length in the following sections.

The 6192SM features a single-port memory module. The module can be organized either as a single 256 x 18 or 512 x 9 single port memory or as two smaller 128 x 18 or 256 x 9 single port memories. The external interface features memory address input pins (A0-A8), Read/Write (RWL, RWH), Chip Select ($\overline{CS}$), Output Enable ($\overline{OE}$) control lines, and 18 bidirectional data lines. The memory can be accessed from this external interface or from the internal GRP based on the user's design.

The 6192DM has functionality similar to the 6192SM, but access from the GRP or external pins is supported concurrently. Dedicated arbitration logic and Busy flags help to resolve issues arising from simultaneous access from both ports of the same memory location. The Busy signal from the external port ($\overline{BusyA}$) is available at a dedicated device pin. The dual-port memory is configurable as a single 256 x 18 or 512 x 9 memory.

Register/Counter Module

An additional feature of the 6192 devices is a dedicated Register/Counter module. Eight 16-bit blocks are available to function as registers or shift registers. In addition, four of these blocks can be programmed to operate as loadable Up/Down counters. These four blocks include carry-in and carry-out connections to allow counter cascading up to 64 bits. The Register/Counter block also has a 16-bit data port connected to the GRP along with a variety of control inputs and status flag outputs.

Programmable Logic Module

The basic unit of general-purpose programmable logic on the 6192 devices is the Twin Generic Logic Block (Twin GLB). There are a total of 24 of these Twin GLBs in the 6192 devices. Each Twin GLB has 24 inputs, a programmable AND array and two OR/Exclusive-OR Arrays as well as eight outputs which can be configured independently to be combinatorial or registered. All Twin GLB logic inputs come from the GRP.

Four Twin GLBs, 16 I/O cells and one ORP form a logic Megablock. The 16 I/O cells within a Megablock share one Product Term Output Enable and two Global Output Enable signals. The outputs of four Twin GLBs are connected to a set of 16 I/O cells by the ORP. The ispLSI 6192 device contains six of these Megablocks.

The GRP has, as its inputs, the outputs from all of the Twin GLBs and all of the inputs from the bidirectional I/O cells as well as independent bidirectional data bus ports from the FIFO and Register/Counter blocks. Flag outputs from these modules as well as control inputs are also connected to the GRP. All these signals are made available to the inputs of the Twin GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

All GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other logic

block on the device. The device has 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, a latched input, an output or a bidirectional I/O pin with 3-state control. Output signal levels are TTL compatible and the output drivers can source 4mA and sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise. The devices are packaged in space saving 208-pin Metal Quad Flat Pack (MQFP) packages.

Clocks in the ispLSI 6192 device are provided through five dedicated clock pins. The five pins provide three clocks to the Twin GLBs and two clocks to the I/O cells.

In-System Programmability

The ispLSI 6192 devices features 5-Volt in-system programmability and in-system diagnostic capabilities. Through this capability, the devices offer non-volatile “on-the-fly” reprogrammability of logic and memory to support truly reconfigurable systems.

Boundary Scan

The 6192 families also have Boundary Scan capability, consisting of dedicated cells connected between the on-chip system logic and the device’s input and the output pins. All I/O pins have associated boundary scan registers, with 3-state I/O using three boundary scan registers and inputs using one. The device supports all IEEE 1149.1 mandatory instructions, which include BYPASS, EXTEST and SAMPLE.

General Purpose Programmable Logic Module

The following is a brief description of the general purpose programmable logic module. For additional information on this module see the 1000/E Family Architectural Description in the Lattice Semiconductor Data Book or CD-ROM.

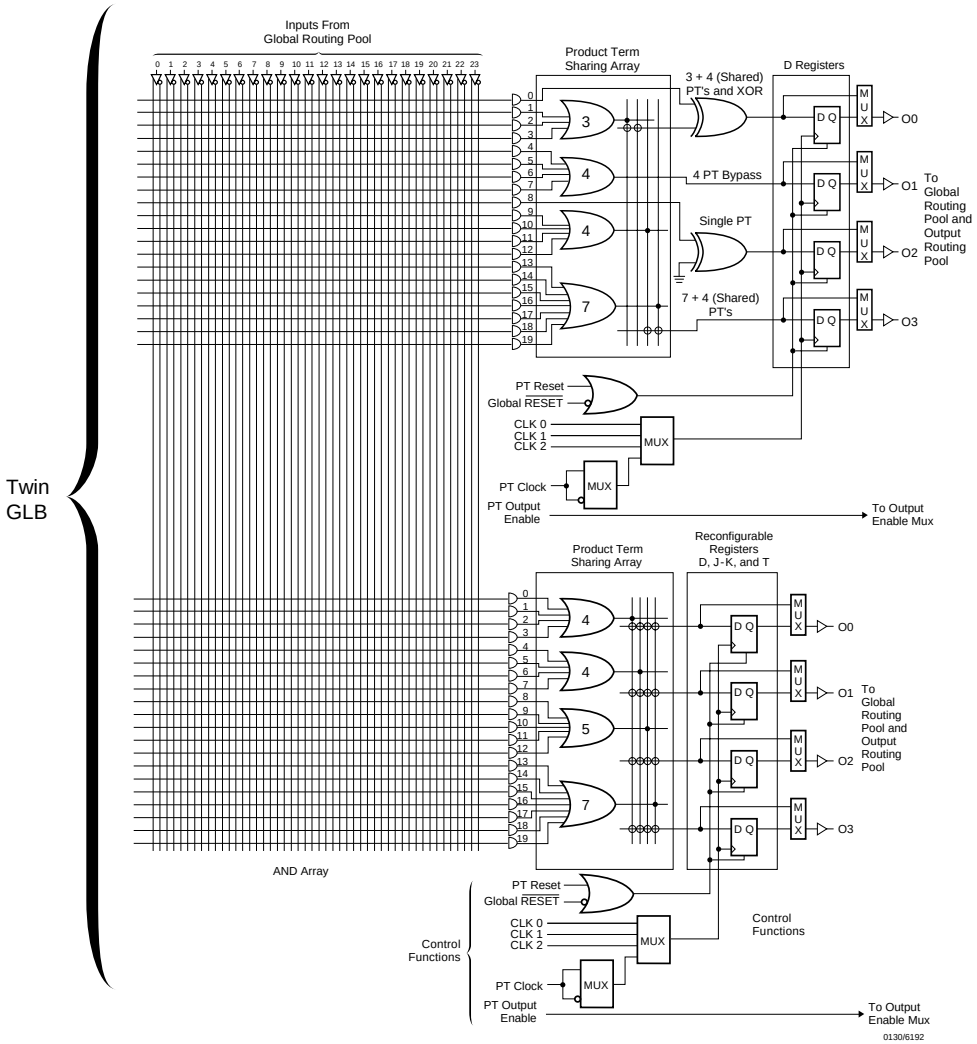
Generic Logic Block

The Twin GLB is the standard logic block of the Lattice Semiconductor ispLSI 6192 family. This Twin GLB has 24 inputs, eight outputs and the logic necessary to implement most standard logic functions. The internal logic of the Twin GLB is divided into four separate sections: the AND Array, Product Term Sharing Array, Reconfigurable Registers, and Control section.

The AND array consists of two sets of 20 product terms which are the logical product of any of the 24 Twin GLB inputs. These inputs all come from the GRP, and are either feedback signals from any of the 24 Twin GLBs, inputs from the external I/O Cells or outputs from the memory or Register/Counter Modules. All Twin GLB input signals are available to the product terms in both the logical true and complemented forms which makes Boolean logic reduction easier.

The two Product Term Sharing Arrays (PTSA) take the 20 product terms each and allocate them to two groups of four Twin GLB outputs. There are four OR gates, with four, four, five and seven product term inputs respectively. The output of any of these OR gates can be routed to any of the four Twin GLB outputs, and if more product

Figure 2. ispLSI 6192 Twin GLB



terms are needed, the PTSA can combine them as necessary. If the user's main concern is speed, the PTSA can use a bypass circuit with four Product Terms to increase the performance of the cell. This can be done to any or all of the eight outputs of the Twin GLB.

The Reconfigurable Registers consist of four D-type flip-flops with an XOR gate on the input. The XOR gate in the GLB can be used either as a logic element or to reconfigure the D-type flip-flop to emulate a J-K or T-type flip-flop. This greatly simplifies the design of counters, comparators and ALU type functions. The registers can be bypassed if the user needs a combinatorial output. Each register output is brought back into the Global Routing Pool and is also brought to the I/O cells via the Output Routing Pool. Reconfigurable registers are not available when the four product term bypass is used. Figure 2 illustrates the mixed mode configurations of the Twin GLB.

Various signals which control the operation of the GLB outputs are driven from the Control Functions. The clock for the registers can come from any of three CLK0-2 inputs or from a product term within the GLB. The Reset Signal for the GLB can come from the Global Reset pin ($\overline{\text{RESET}}$) or from a product term within the block. The Global Reset pin is always connected and is logically "ORed" with the PT reset (if used). An active reset signal always sets the Q of the registers to the logic 0 state. The Output Enable for the I/O cells associated with the GLB comes form a product term within the block. Use of a product term for output enable makes it unavailable for use as a general-purpose logic term.

Megablock Structure

Four Twin GLBs, 16 I/O cells and one ORP make up a Megablock. Each Twin GLB has a maximum fan-in of 24 inputs, and no dedicated inputs associated with any Megablock. Each Twin GLB has eight associated outputs. A total of 32 GLB outputs are fed to the ORP. However, only 16 out of the 32 outputs feed to 16 I/O cells. The Megablock structure is shown in figure 3.

Figure 3. ispLSI 6192 Family Megablock Block Diagram

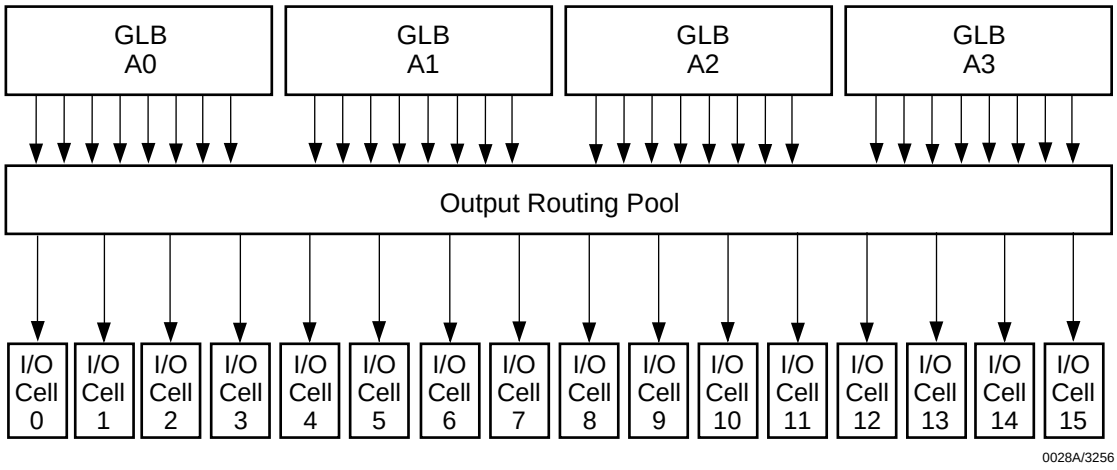


Figure 4. ispLSI 6192 Family Global Clock Structure

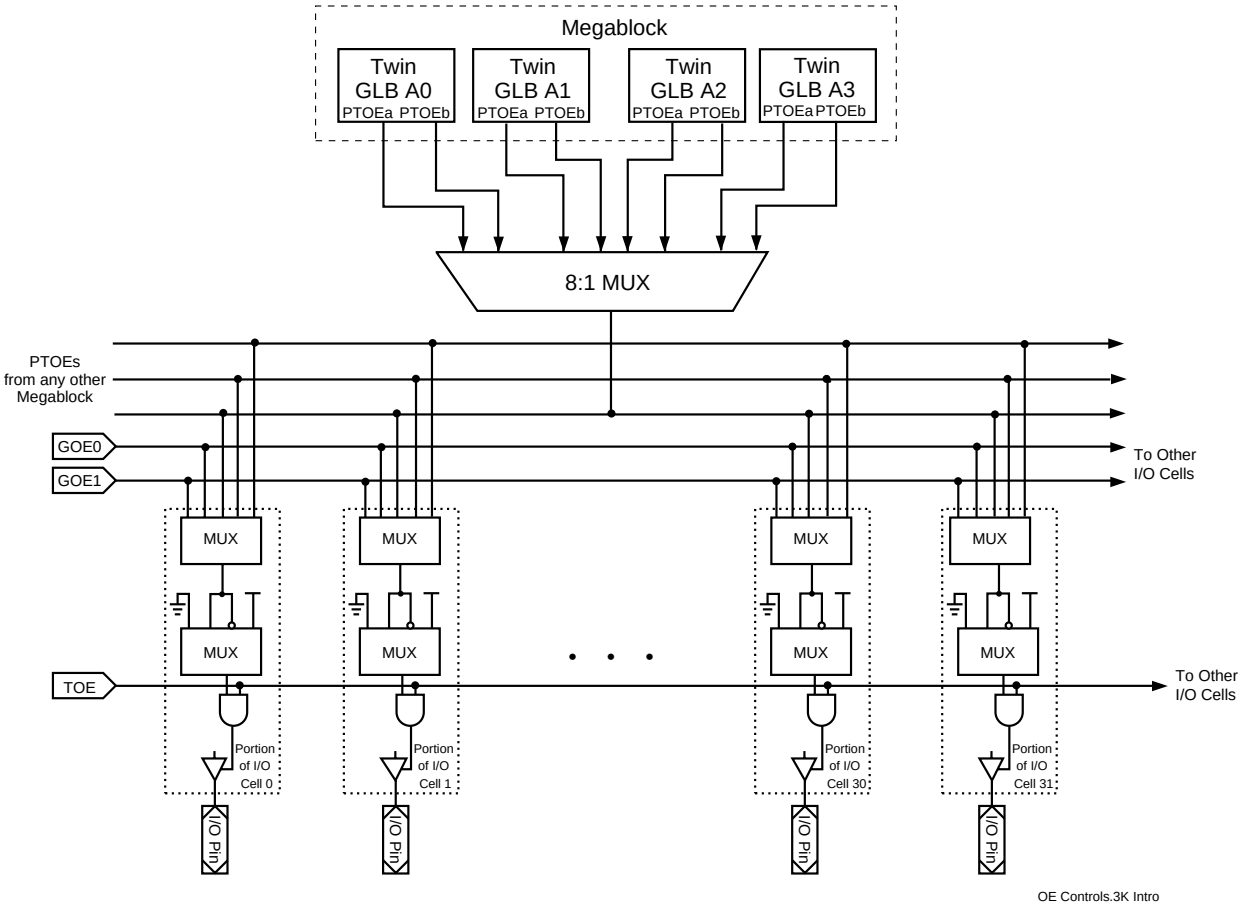
Global Clock Structure

The global clock structure is made up of five global clock input pins, Y0, Y1, Y2, Y3, and Y4. This is shown in figure 4. Three of the clock pins are dedicated for GLB clocks and the remaining two clock pins are dedicated for I/O register clocks. All input clock signals are fed directly to the GLB clock input via a clock multiplexer. The GLB global clocks do not have inversion capability, but the product term clock does have inversion capability before it reaches the clock multiplexer.

Output Enable Controls

A global test OE signal (TOE) is hardwired to all I/O cells and is useful to perform static testing of all the 3-state output buffers within the device. In addition to the test OE signal, two global OEs (GOE0 and GOE1) are connected to all I/O pins. The product term OE is shared between two Megablocks resulting in twice the GLBs being able to use a single OE signal. The Megablock OE signal and global OE signals are fed to an OE multiplexer. The OE signals, with the exception of the test OE, have inversion capability after going through the OE multiplexer as shown in figure 5.

Figure 5. ispLSI 6192 Family Output Enable Controls



Boundary Scan

Boundary Scan (IEEE 1149.1 compatible) is a test feature incorporated within the device to provide on-chip test capabilities during PCB testing. Five input signal pins, BSCAN, TDI, TCK, TMS, $\overline{\text{TRST}}$, and one output signal pin, TDO, are associated with the boundary scan logic cells. These signals share the same dedicated signal pins used for ISP programming. The signal BSCAN is associated with the $\overline{\text{ispEN}}$ pin, TDI corresponds to the SDI pin, TCK corresponds to the SCLK pin, TMS corresponds to the MODE pin, and TDO corresponds to the SDO pin. When $\overline{\text{ispEN}}$ is asserted low, the MODE, SDI, SDO, and SCLK options become active for ISP programming. Otherwise, BSCAN, TDI, TCK, TMS, TDO, and $\overline{\text{TRST}}$ options become active for boundary scan testing of the device. The boundary scan block diagram is shown in figure 6. TDI is the test data serial input, TCK is the boundary scan clock associated with the serial shift register, TMS is the test mode select input, TDO is the test data output, and finally $\overline{\text{TRST}}$ is the reset signal pin.

The user interfaces to the boundary scan circuitry through the Test Access Port (TAP). The TAP consists of a control state machine, instruction decoder and instruction register.

The TAP is controlled using the test control lines: Test Data IN (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Reset ($\overline{\text{TRST}}$) and Test Clock (TCK).

The TAP controls the operation of the Boundary Scan Registers after decoding the instruction code sent to the instruction register (see table 3).

The Boundary Scan Registers for the I/O cells are shown in figure 7. As illustrated in the figure, each General-Purpose I/O cell contains 3 registers, 2 latches and 5 multiplexers to implement the ability to capture the state of the I/O cell or set the state of the output path of the cell or function as a conventional I/O cell. Module I/O cells eliminate the output enable registers (OE control comes from OE pins).

The Boundary Scan Registers required for an input only cell are shown in figure 8. An input only cell can only have its state captured, which only requires one MUX and one register. Output-only cells are shown in figure 9. Here, two registers control the output and output enable.

All of the input, output and I/O cells are serially connected together in a long chain. The SCAN OUT of one cell is connected to the SCAN IN of the next cell. The cells are connected in the following order: TDI to I/O47 through I/O32, Y4, Y3, Y2, Y1, $\overline{\text{RESET}}$, TOE, GOE1, GOE0, Y0, I/O31 through I/O0, $\overline{\text{BusyA}}$, A0/$\overline{\text{RST}}$(FIFO), A1/$\overline{\text{EF}}$, A2/$\overline{\text{FF}}$, A3/$\overline{\text{ALE}}$, A4/$\overline{\text{ALF}}$, A6, A7, A8/RWH, RWL/$\overline{\text{RD}}$ or $\overline{\text{WR}}$, $\overline{\text{CS}}$, $\overline{\text{OE}}$(RAM), DI/O0 through DI/O17(RAM or FIFO), DI/O0 through DI/O15(RC), $\overline{\text{OE}}$(RC), SIN, SOUT, ENABLE, TC/CO0 through TC/CO3, I/O48 through I/O95, to TDO.

Note that input-only pins add only one register to control the inputs to the Boundary Scan chain (A0, A5, A6, A7, A8, RWL, $\overline{\text{CS}}$, SIN, ENABLE, Y0-Y4, $\overline{\text{RESET}}$, TOE, GOE0, GOE1). Output-only pins add two registers to the chain ($\overline{\text{BusyA}}$, SOUT, TC/C0-3) to control the output and output enable. Pins that function as input or output add three registers to the chain (I/O0-95, A1/$\overline{\text{EF}}$, A2/$\overline{\text{FF}}$, A3/$\overline{\text{ALE}}$, A4/$\overline{\text{ALF}}$) to control inputs, outputs and enables. DI/O0-17(RAM or FIFO) and DI/O0-15(RC) add two registers to the chain per pin for input/output control (output enable for these pins is generated from the respective $\overline{\text{OE}}$ pin register. $\overline{\text{OE}}$(RC) adds two registers to control its input and the output enable for DI/O0-15(RC). $\overline{\text{OE}}$(RAM) adds three registers: one to control its input and two to control the output enables for the high and low bytes of the DI/O(RAM) pins.

Figure 6. Boundary Scan Block Diagram

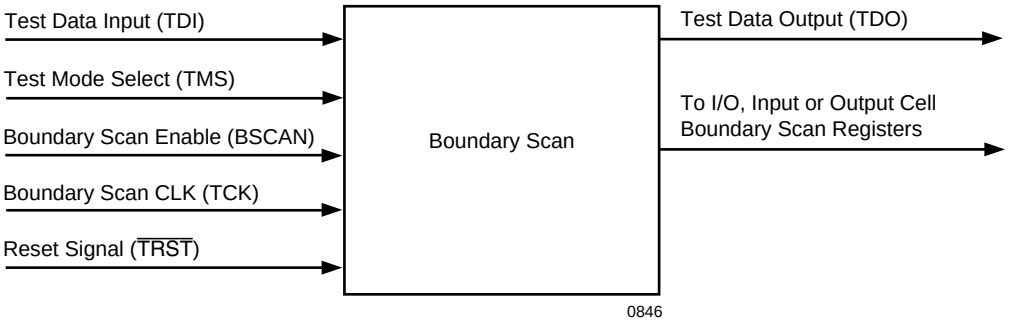


Figure 7. Boundary Scan Registers for I/O Cells

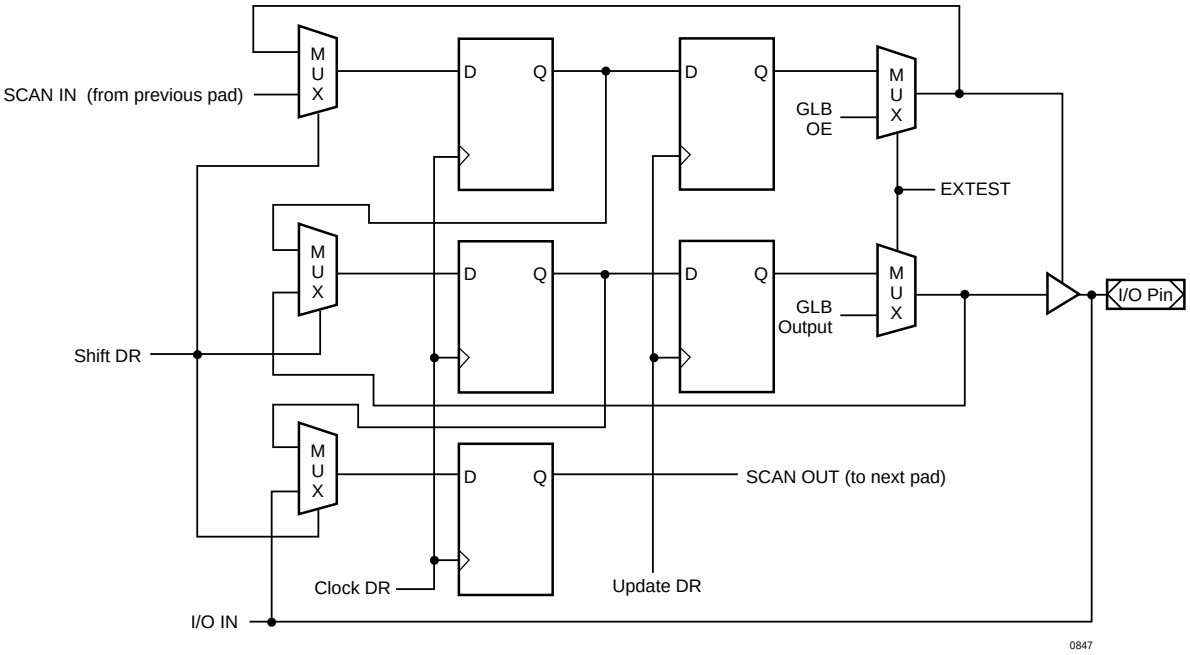


Figure 8. Boundary Scan Registers for an Input Only Cell

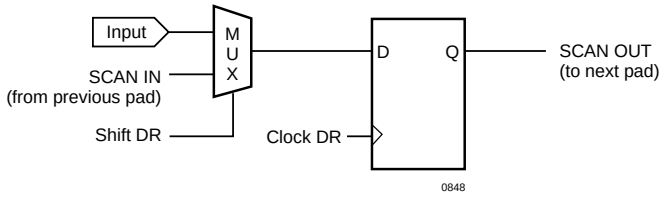


Figure 9. Boundary Scan Registers for Output-Only Cell

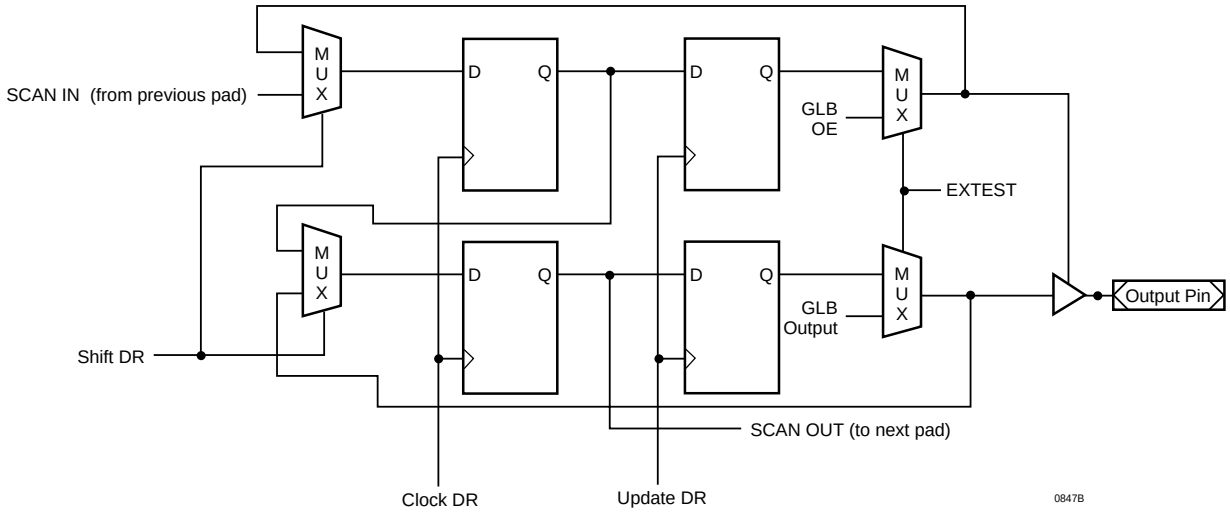


Table 2. Boundary Scan Timing Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
t_{rst}	Reset Time from Valid V_{CC}		100	–	–	µs
t_{su}	Setup Time		60	–	–	ns
t_h	Hold Time		10	–	–	ns
t_{co}	Clock to Output		–	–	60	ns
t_{clkh}	Clock Pulse Duration, High		60	–	–	ns
t_{clkl}	Clock Pulse Duration, Low		60	–	–	ns
t_{ispE}	$\overline{ispEN}$ / BSCAN to TDO		–	–	1	µs

Table 2 - 0028Aisp-3K/6K

Figure 10. Boundary Scan Waveforms

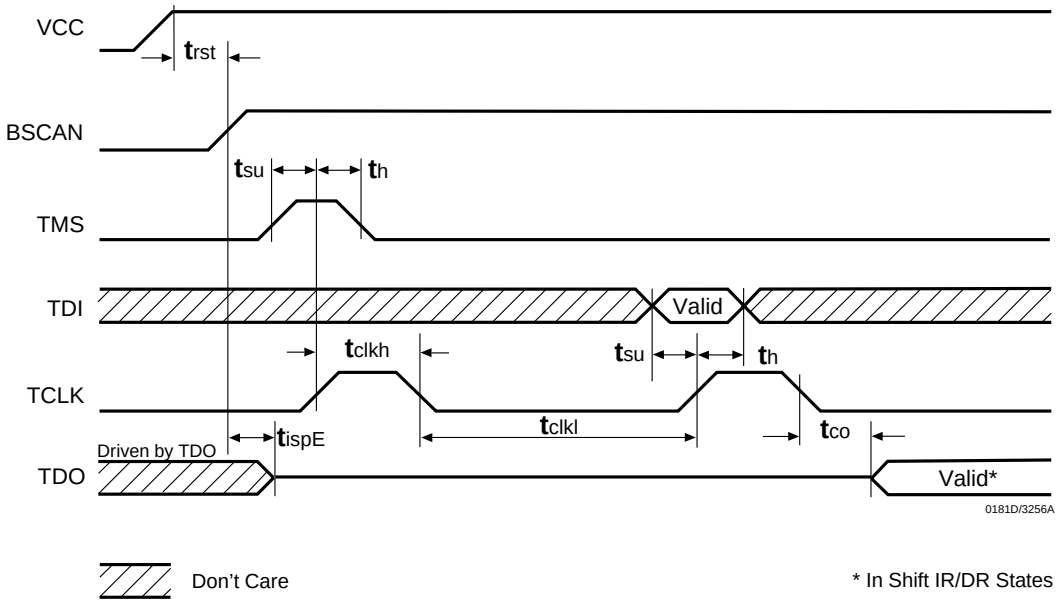


Table 3. Boundary Scan Instruction Codes

Instruction Name	Code	Description
SAMPLE/ PRELOAD	11100	Loads and shifts data into BScan registers
EXTEST	00000	Drives external I/O with BScan registers
BYPASS	11111	Bypasses registers of selected device(s)

Note: LSB shifts in first.

Table 10- 0007

FIFO Description (6192FF)

Integration of high-speed static RAM technology with dedicated internal support logic yields a high-performance, high-density FIFO memory module on the ispLSI 6192FF. A FIFO is a First-In/First-Out buffer that acts as an elastic buffer between two synchronous or asynchronous systems with simultaneous read/write accesses. The data rate between the two systems can be regulated by monitoring the status flags and throttling the read and write accesses.

Because data is produced and accepted at different rates, it is important to monitor the boundary conditions (Full or Empty) of the data buffer. Failure to act on the boundary conditions will result in data overflow or underflow. The Empty and Full flags can also be fed back internally to inhibit further Read and Write operations until the FIFO is no longer empty or full.

While offering the basic features of a FIFO, the dedicated FIFO module in the 6192FF device also provides two new user-programmable flags: Almost-Empty and Almost-Full. These flags can be used as early warning flags in critical real-time applications such as data acquisition, high-speed data link and pipeline Digital Signal Processing applications. In a multi-tasking environment, the Almost-Empty and Almost-Full Flags can also be used to set the interrupt request in advance, so that the CPU has sufficient time to perform the switching task.

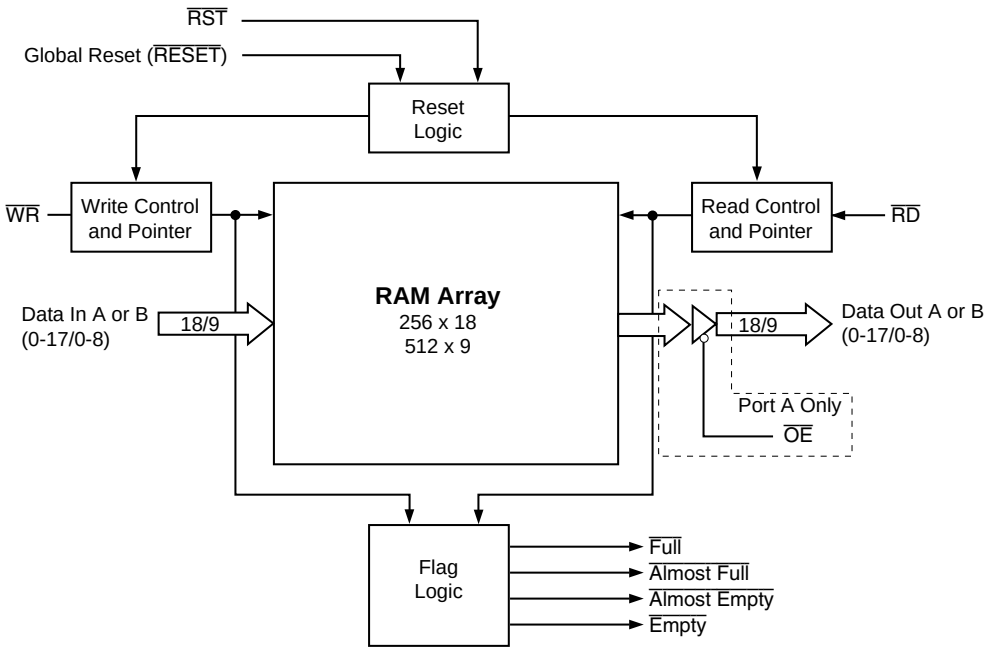
Figure 11 illustrates the functionality of the FIFO. Data In, Write ($\overline{WR}$), Read ($\overline{RD}$) and Reset ($\overline{RST}$) form the inputs and Data Out, Full ($\overline{FF}$), Almost Full ($\overline{ALF}$), Almost Empty ($\overline{ALE}$) and Empty ($\overline{EF}$) constitute the Outputs of the FIFO module. When $\overline{WR}$ is active, data can be written into the RAM array sequentially, independent of Read. When $\overline{RD}$ is active, data can be read from the RAM array sequentially, again, independent of Write. The dedicated module reset or global reset pin of the device can be used to reset the internal address pointers to the first location of RAM array, and all the flags to an empty state. The FIFO signals the empty and full condition by asserting the Empty and Full flags, respectively. The Almost Empty and Almost Full flags can be used to set the interrupt request in advance.

Read, Write and Reset inputs into the FIFO also have user-programmable polarity control so these normally active low signals can be individually defined as active high or active low.

The FIFO is user configurable and can be configured as:

Description	Ports Used
256 x 18 FIFO	A to B
256 x 18 FIFO	B to A
512 x 9 FIFO	A to B
512 x 9 FIFO	B to A

Figure 11. FIFO Module Functional Block Diagram



FIFO Operation

The FIFO can be configured in two directions: Port A to B, where data flows from the dedicated FIFO I/O pins to the GRP, and Port B to A, where data flows from GRP to I/O pins. Accesses between ports can be asynchronous. The module utilizes an 18- or 9-bit wide data bus to make it user configurable as a 256 x 18 or 512 x 9 block.

A write cycle is initiated on the falling edge of the Write ($\overline{WR}$) provided the Full Flag ($\overline{FF}$) is not set. Data is stored in the RAM array sequentially and independently of any ongoing read operation. When the FIFO is full, the Full Flag goes low (becomes active), and further write operations are inhibited to prevent data overflow, i.e., the external Write ($\overline{WR}$) is blocked internally from going low. Upon the completion of a valid read operation, the Full Flag will go high allowing a valid write to begin. If the FIFO is not read after a Reset, the Full Flag will go low after 256 (256 x 18) or 512 (512 x 9) writes. The Almost Full Flag ($\overline{ALF}$) is programmable via E^2CMOS cells on the device. It can be programmed to go low at any given location. It does not, however, inhibit further write operations. The Almost Full location must be above the Almost Empty Flag location.

A read cycle is initiated on the falling edge of Read ($\overline{RD}$) if the Empty Flag ($\overline{EF}$) is not set. The data is accessed from the RAM array sequentially, independent of any ongoing write operations. After Read goes high, the Data Outputs (Data Out 0-17) will return to a high impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting the further read operations. The data outputs will remain in a high impedance state while the FIFO is empty. When the FIFO is empty, the internal read pointer is blocked from going low. Once a valid write operation has been accomplished, the Empty Flag will go high and a valid read can then begin. The Almost Empty Flag can be programmed to go low at any given point but does not inhibit further read operations. This location has to be below the Almost Full Flag location.

Figure 12. Full Flag from Last Write Timing Waveform

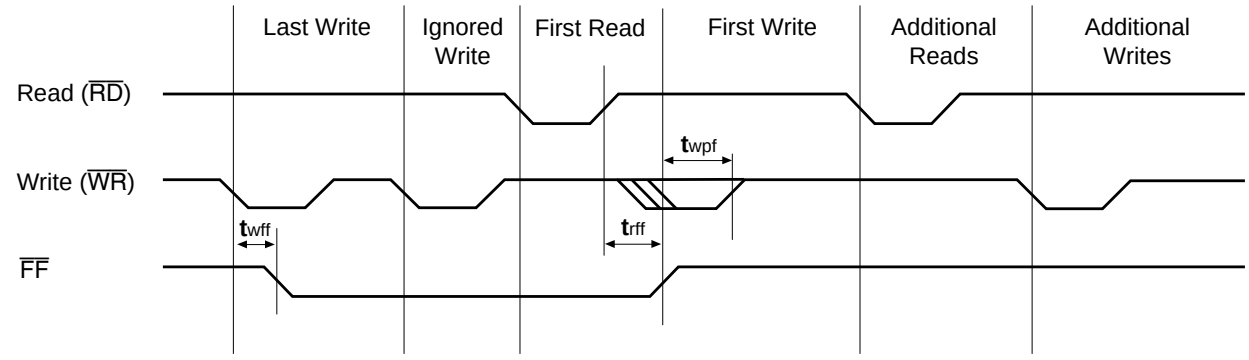
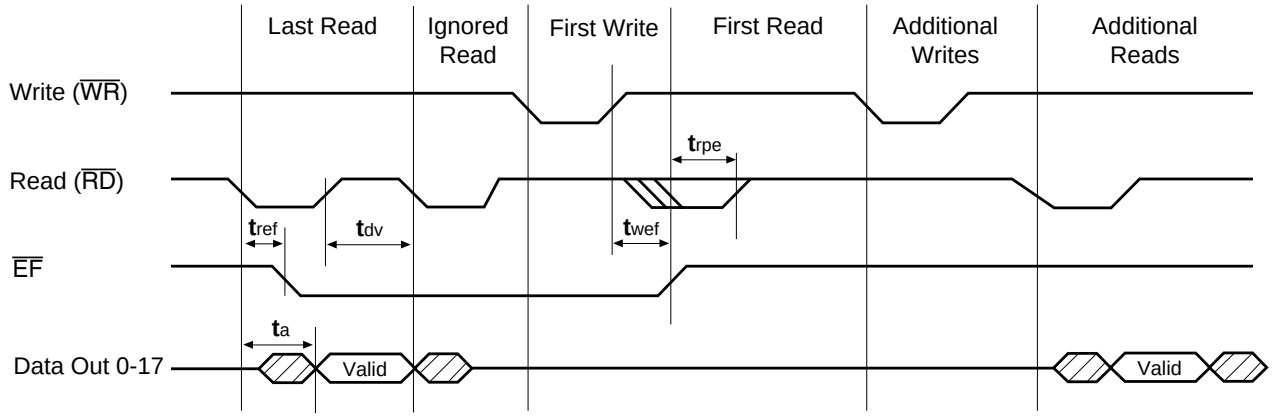


Figure 13. Empty Flag from Last Read Timing Waveform



Reset is accomplished whenever the FIFO Reset ($\overline{RST}$) input is taken to a low state. During reset, internal read and write pointers are set to the first location of the FIFO memory array. Almost Full and Full Flags are cleared (high), and Almost Empty and Empty Flags are set (low). A reset is required after power up before a write operation can take place.

Figure 14. Almost-Empty/Almost-Full Flag Timing Waveform

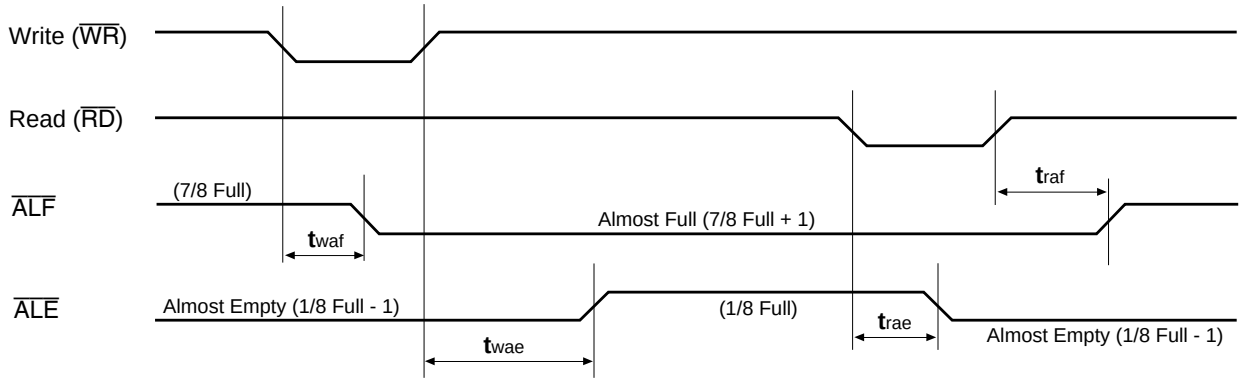


Figure 15. Asynchronous Write and Read Operation Timing Waveform

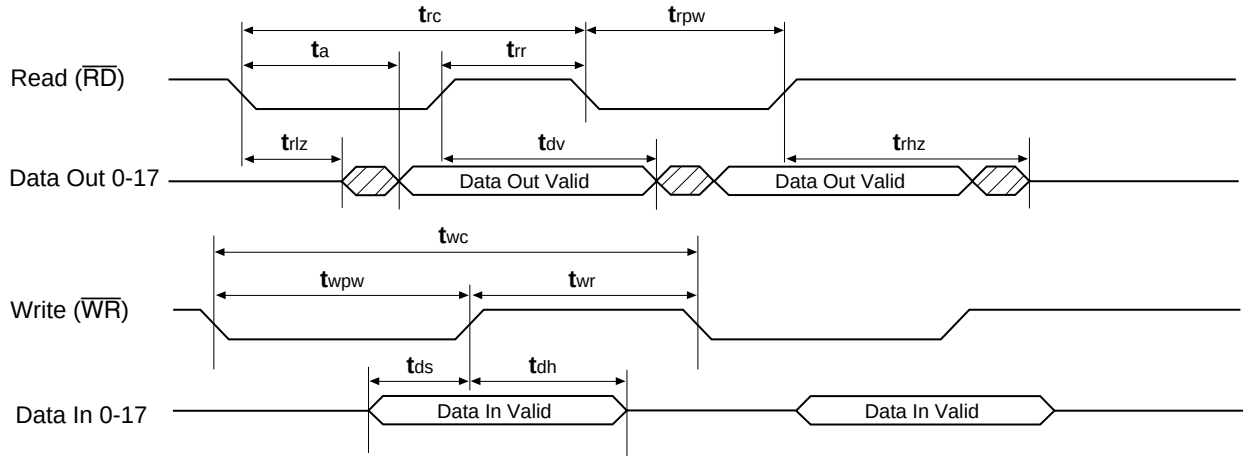
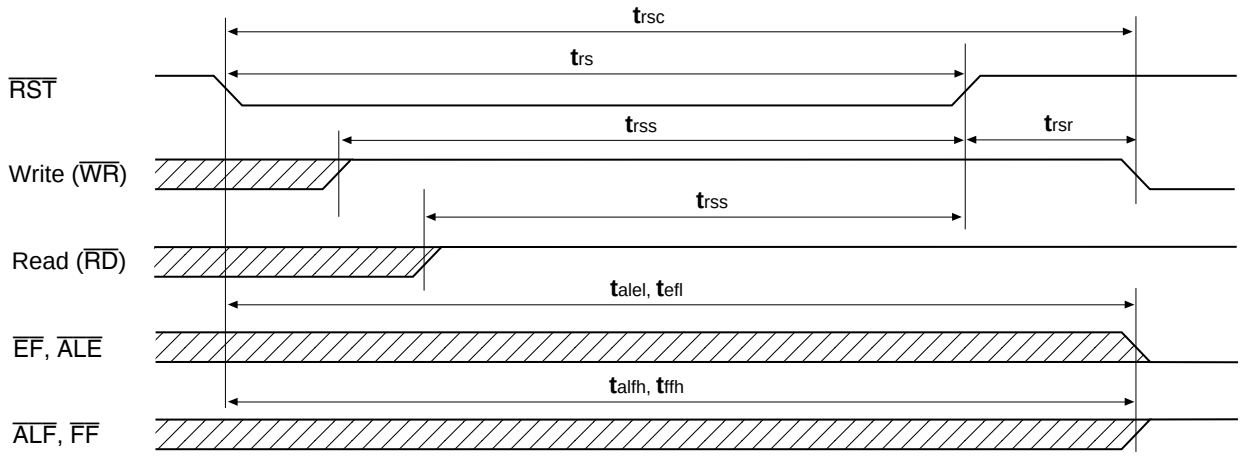


Figure 16. FIFO Reset Timing Waveform



FIFO Interfaces

Port A to B Configuration

Figure 17 below shows the port A to B configuration of the FIFO. Port A is connected to the I/O cells and port B to the GRP of the device. I/O cells (Port A) are used to write data into the FIFO when the Write signal goes low. The GRP (Port B) is driven with the data from the FIFO when the Read signal goes low. The status of the various control flags is passed to the I/O cells and GRP.

In the 512 x 9 FIFO configuration, the high-order 9 bits (Data In A9-17) are used for writing in data. The remaining data I/O pins are pulled high.

Figure 18 below shows the port B to A configuration of the FIFO. The GRP inputs (Port B) provide data to the FIFO when the Write signal goes low. I/O cells read data from the FIFO when the Read signal goes low. The I/O cells are in the high impedance state when the Read signal is high. The status of various control flags is passed to the I/O cells and GRP.

When not used for memory interfacing, the DIO 0-17 (FIFO) and $\overline{ALE}$ and $\overline{ALF}$ pins may be used for general-pupose logic inputs into the GRP.

Port B to A Configuration

Figure 17. Port A to B Configuration

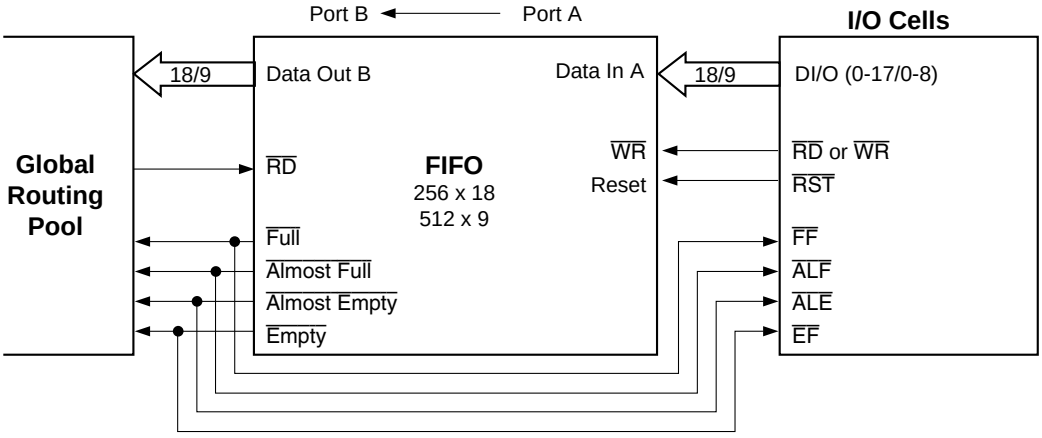
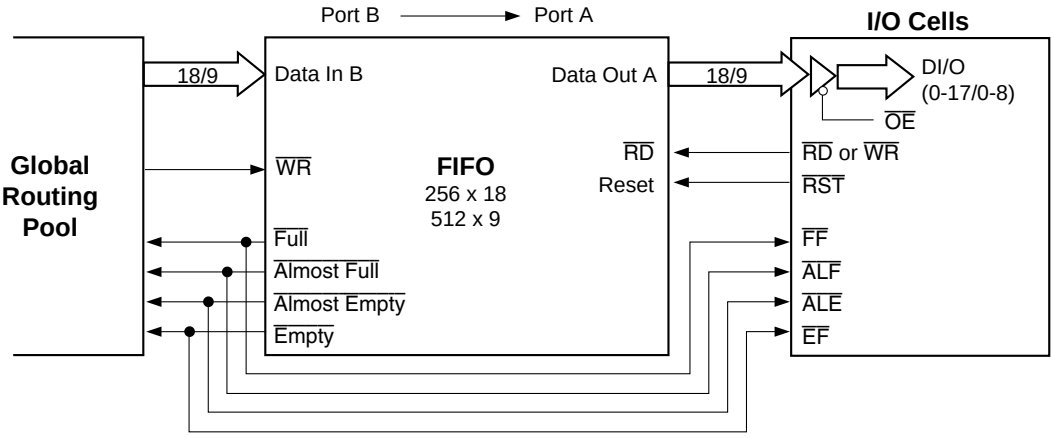


Figure 18. Port B to A Configuration



Dual Port RAM Module Description (6192DM)

A dual port static RAM constitutes the memory module in the ispLSI 6192DM device. The dual port RAM is organized as a 512 x 9 memory module with a parity bit added to each byte of data. The memory module can be accessed for read or write concurrently via two separate ports as long as both ports do not access the same memory location at the same time.

Figure 19 illustrates the functionality of the Dual Port RAM. It can be sub-divided into 3 parts: Memory Array, Address Decoders and the Control and Arbitration Logic.

The 18-bit data bus is bidirectional and can be used to read data from the memory array or write data to the memory array. A byte read/write operation involves 8-bits of data and a parity bit. 8 address bits (ADDR 0-7) are used to access a particular word location in memory array. RWH is associated with the higher 9 data bits and RWL is used for lower 9 data bits. There are 2 RWH and 2 RWL lines, one pair for each port. These are inputs to the Control logic to select the type of operation to be performed. Depending on the configuration. It can be a word read/write operation, or byte read and/or write operation. $\overline{CS}$ is the Chip Select line. There is a separate $\overline{CS}$ for each port. The $\overline{CS}$ line has to be active in order to perform a read/write operation on the memory module.

All the input signals, control as well as the data lines, are user selectable to be active high or low. The Dual Port RAM has a default configuration of active low for the $\overline{CS}$.

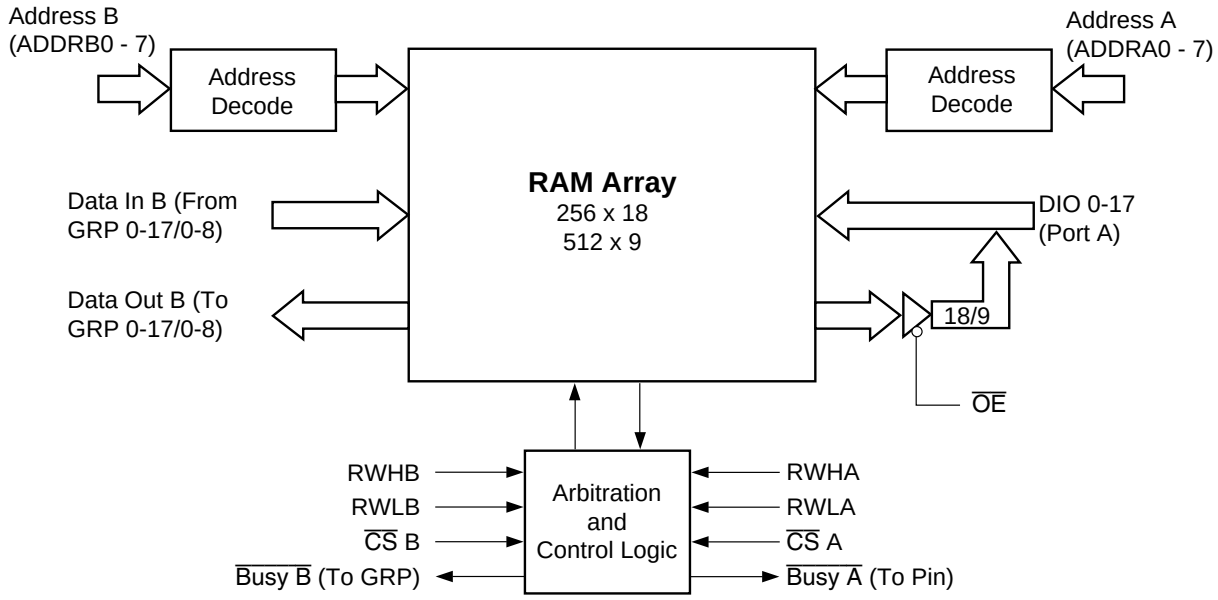
When not used for memory interfacing, the DIO 0-8 (RAM) and A3-A7 pins may be used for general-purpose logic inputs into the GRP.

The Dual Port RAM is user configurable and can be configured as any of the following:

Description	Ports Used
256 x 18 Dual Port RAM	A & B
256 x 18 Dual Port RAM w/Byte Write (9 Bit Write)	A & B
512 x 9 Dual Port RAM	A & B

Port A interfaces with the external world through DIO pins and Port B is internal to the device via the GRP.

Figure 19. Dual Port RAM Functional Block Diagram



Dual Port RAM Configurations

256 x 18 Dual Port RAM

Figure 20 below shows the 256 x 18 and 512 x 9 configurations of the Dual Port RAM. ADDRA 0-7 form the 8-bit address bus used to access one of the 256 locations from Port A which is connected to the external pins. ADDRB 0-7 form the 8-bit address bus used to access one of the 256 locations from Port B which is connected to the GRP. RWLA is the control line which determines the type of operation to be performed with the 18-bit data bus from the DIO pins. A high RWLA signal reads 18-bits of data from the memory location pointed to by the address bus. A low RWLA signal writes 18-bits of data to the location pointed by the address bus. The $\overline{CSA}$ line has to be low to have port A respond to a read/write operation. In this configuration, RWHA and RWHB are not used.

The same operations on the B Port are controlled by RWLB and $\overline{CSB}$. For this port, control signals and data interface with the GRP.

256 x 18 Dual Port RAM w/Byte (9-bit) Write

In this mode, RWL is the control line which determines the type of operation to be performed on the lower 9 bits of the memory location. RWH is the control line used to select the type of operation to be performed on the higher 9 bits of the memory location. All other operating characteristics are similar to the previous mode.

This mode is an ideal way to pack 9-bit data into 18-bit memory by simply alternating the RWL and RWH states. This mode can also be used to perform bus width conversion whereby one port operates at 9-bits and the second port operates at 18-bits

512 x 9 Dual Port RAM

This mode uses 9 address bits to select one of 512 locations. ADDRA 0-7 form the 8 address bits and RWH is used as the 9th address bit (MSB). In this configuration, the high order bits (bits 9-17) of the 18-bit data bus are used to transfer data to the RAM. RWL is the control line used to select the type of operation to be performed on the specified memory location.

Arbitration

The two ports may act like independent RAMs, however the arbitration and control logic as well as the Memory core are shared by both ports as shown previously. When the $\overline{CS}$ is inactive the RAM will ignore any operation, read or write on that port.

The dual port RAM can be written to or read from asynchronously and simultaneously by each port at the same time (except for the same address). If the same address location is accessed by both ports, the arbitration logic evaluates which port will win out. The port that wins will have a logic 1 or a busy inactive on its Busy Flag. Busy will go low for the port that loses. If the address is the same for both ports and there is >5ns between the port accesses, the Busy signal is activated and which port has to wait is determined on a first-come, first-served basis.

When the addresses on Port A and B are the same and the $\overline{CSA}$ and $\overline{CSB}$ both go low within 5ns of each other or if $\overline{CSA}$ and $\overline{CSB}$ are both low and the address for both ports change to the same location within 5ns, the arbitration is unpredictable: either port may win.

Figure 20. Dual Port RAM Configurations

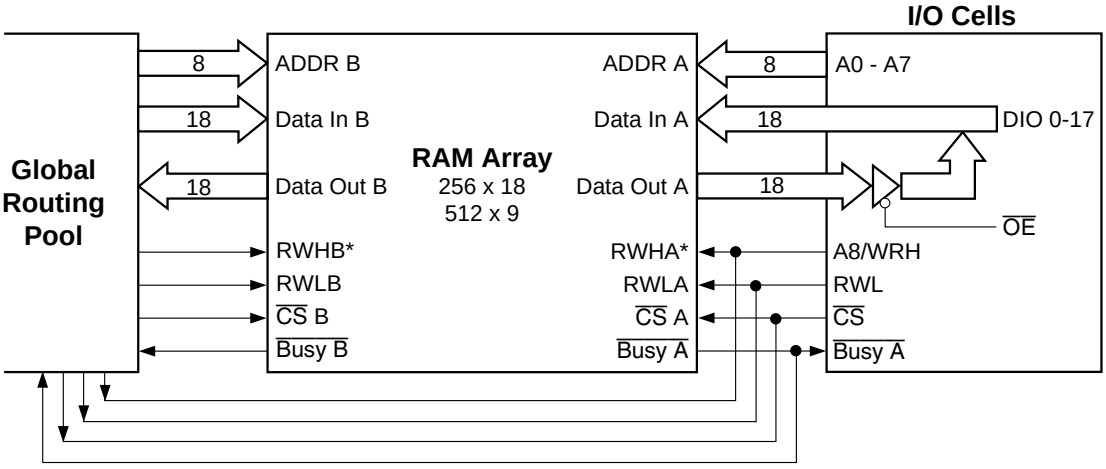


Figure 21. Dual Port RAM with $\overline{\text{Busy}}$ Timing Diagram

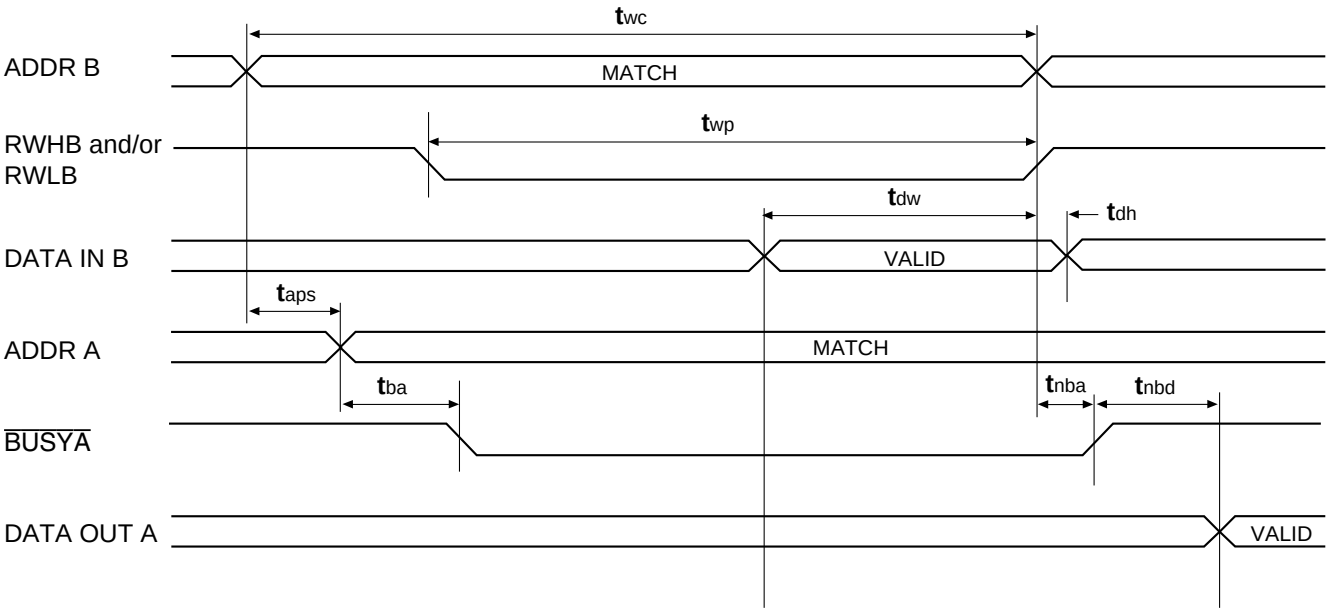


Figure 22. Dual Port RAM Contention Cycle ($\overline{\text{CS}}$ Arbitration) Timing Diagram

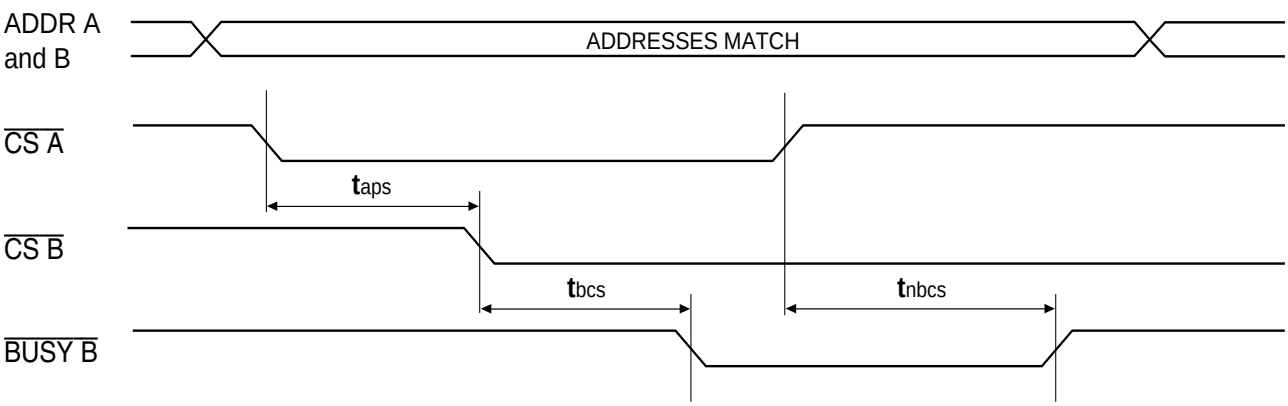


Figure 23. Dual Port RAM Contention Cycle (Address Valid Arbitration) Timing Diagram

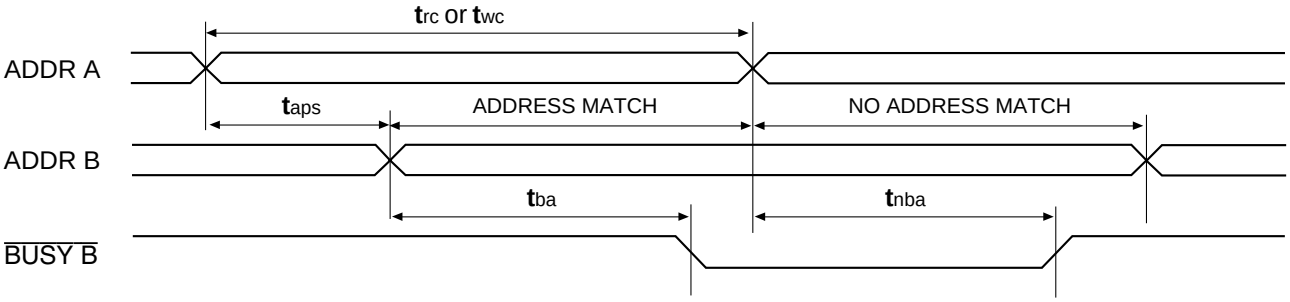


Figure 24. Dual Port RAM Write Cycle (RW Controlled) Timing Diagram

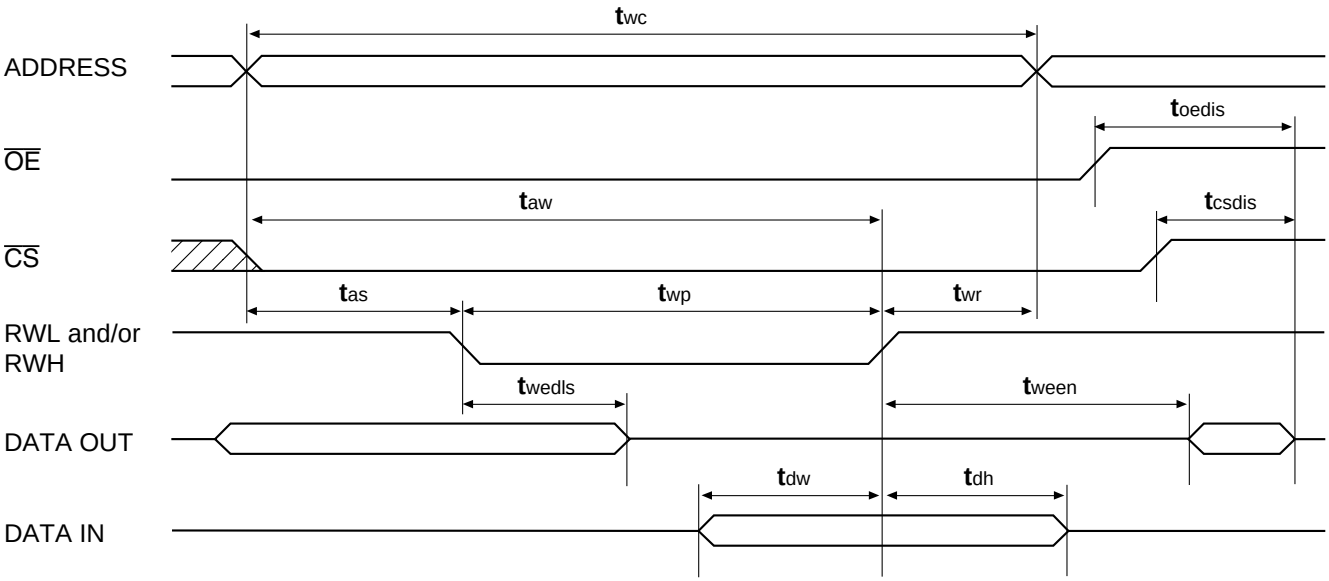
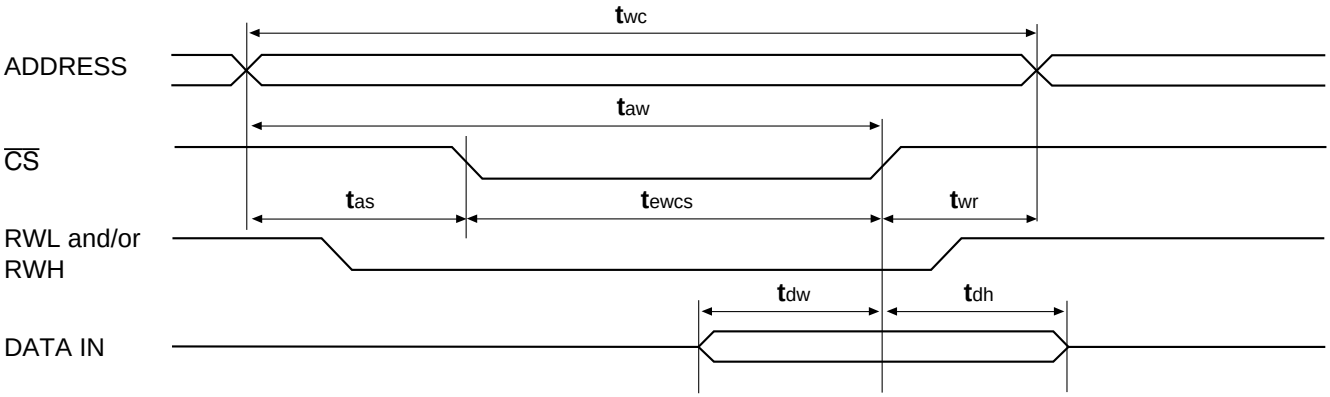


Figure 25. Dual Port RAM Write Cycle ($\overline{CS}$ Controlled) Timing Diagram



Single Port RAM Description (6192SM)

Single port Static RAM constitutes the memory module in the 6192SM device. As a single-port memory, only one port is used to access the memory for data reads and writes. The 6192SM can be configured to operate either as one large single-port memory or as two smaller single-port memories.

When used as a large single-port RAM, the memory can be organized as 256 x 18 or 512 x 9. Either Port A or Port B can be used to control the single-port RAM as shown in Figure 26. A byte read/write mode similar to that of the dual-port RAM is also provided to allow independent control of the upper and lower 9-bit banks of the memory.

When used as two independent smaller single-port memories, each memory can be organized as 128 x 18 or 256 x 9. The two memories, however, must have identical configurations. Port A, therefore controls one single-port memory and Port B controls the other single-port memory as shown in Figure 27. Both memories can operate simultaneously and independently. Byte read/write mode also applies to the dual single-port RAM configuration.

When not used for memory interfacing, the DIO0-8 (RAM) and A3-A7 pins may be used for general purpose inputs into the GRP.

The RAM is user configurable and can be configured as:

Description	Single Memory Port Used	Dual Memory Ports Used
128 x 18 Single Port RAM	—	A and B
128 x 18 Single Port RAM w/Byte Write (9 Bit Write)	—	A and B
256 x 9 Single Port RAM	—	A and B
256 x 18 Single Port RAM	A or B	—
256 x 18 Single Port RAM w/Byte Write (9 Bit Write)	A or B	—
512 x 9 Single Port RAM	A or B	—

Figure 26. Single Port RAM Functional Block Diagram (Single RAM Block)

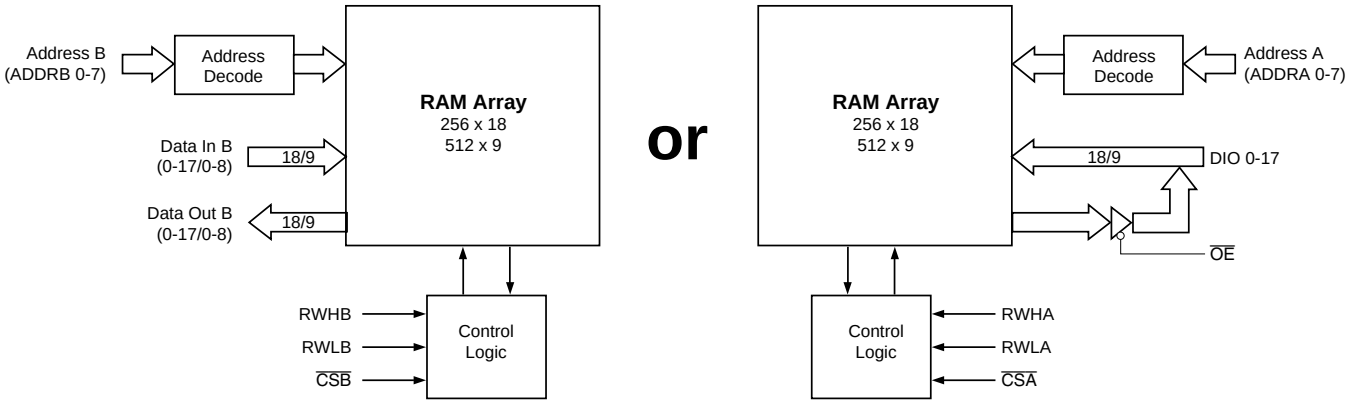
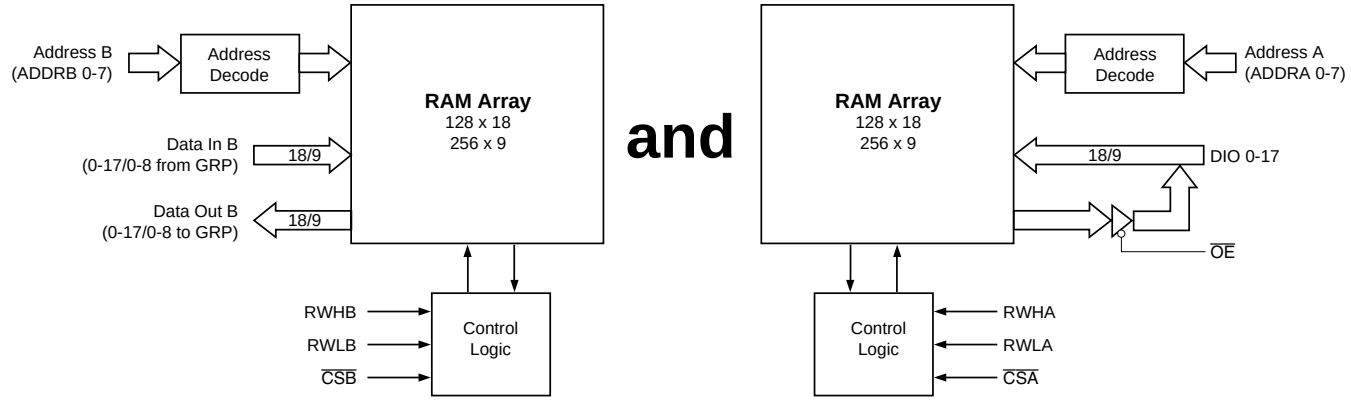


Figure 27. Single Port RAM Functional Block Diagram (Dual RAM Blocks)



Port A interfaces with the external world through the dedicated I/O pins and Port B is internal to the device, through the GRP.

Single Port RAM Configurations

256 x 18 Single Port RAM (Port A or B)
Figure 28 shows the port A configuration of the Single Port RAM. A0-7 form the 8-bit address bus used to select one of the 256 locations. RWLA is the control line which determines the type of operation to be performed with the 18-bit data bus. A high RWLA signal reads out 18-bits of data from the location pointed to by the address bus. A low RWLA signal writes in 18-bits of data to the location pointed to by the address bus. The $\overline{CS}$ line has to be low (active-low) to have the RAM respond to a read/write operation. As shown below, the control lines can come from the I/O cells and/or from the GRP, as defined by the software.

When in port B configuration (figure 29), the GRP drives the address bus, data bus and the various control lines.

256 x 18 Single Port RAM w/Byte (9-bit) Write (Port A or B)
In this mode, RWL is the control line which determines the type of operation to be performed on the lower 9 bits of the memory location using the lower 9-bits of the 18-bit data bus. Similarly, RWH is the control line to select the type of operation to be performed using the higher 9 bits of the memory location with the higher 9 bits of the 18-bit data bus. All other operating characteristics are similar to the previous mode.

512 x 9 Single Port RAM (Port A or B)
This mode uses 9 address bits to select one of the 512 locations. A0-A7 form the 8 address bits and RWH is used as the 9th address bit (MSB). In this configuration, the higher 9 bits of the 18-bit data bus are used to transfer data. RWL is the control line used to select the type of operation to be performed on the specified memory location.

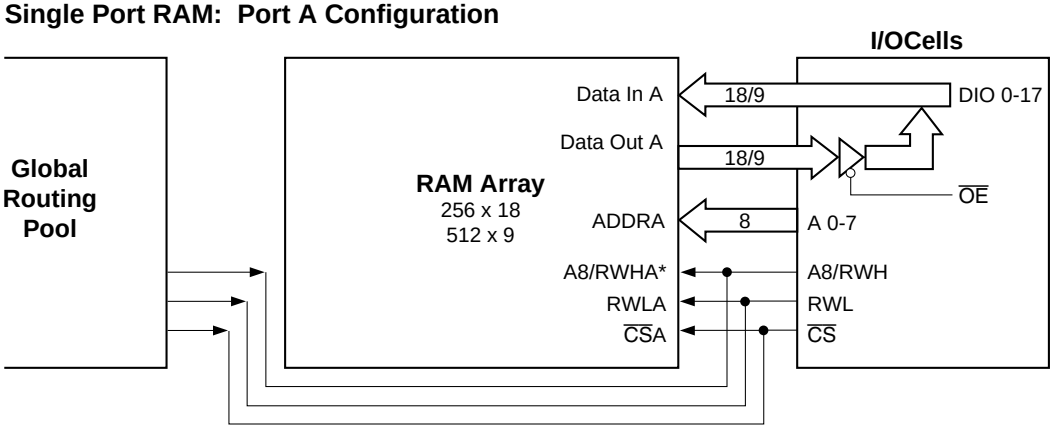
The 6192SM can also be configured as two separate smaller single port RAMs with Port A controlling one and Port B controlling the other. Both RAMs can operate simultaneously. Each smaller memory operates exactly the same way as the larger memory except for the address bit A7.

Dual 128 x 18 Single Port RAM (Port A and B)
This mode uses A0-A6 address bits to select one of the 128 locations. A7 is not used in this mode. RWLA and $\overline{CSA}$ control the operations for Port A. RWLB and $\overline{CSB}$ determine the operations for Port B.

Dual 128 x 18 Single Port RAM with Byte Write (Port A and B)
RWLA and RWLB control the read/write operations for the lower order 9 bits of their respective memories. RWHA and RWHB control the operation for the higher order 9 bits.

Dual 256 x 9 Single Port RAM (Port A and B)
A7 is used as the most significant address bit required to access the 256 locations in the memory. The higher order 9 bits of the 18-bit bus are used to transfer data. RWL is the control line used to select the type of operation to be performed.

Figure 28. Single Port RAM: Port A Configuration



Note (*)
1. In 256 x 18 Single Port RAM configuration, A8/RWH is left unconnected.
2. In 256 x 18 Single Port RAM configuration with Byte Write configuration, A8/RWH acts as a control line to select the type of operation to be performed with the high 9 bits of the 18 bit data bus.
3. In 512 x 9 Single Port RAM configuration, A8/RWH is used as the most significant Address bit

Figure 29. Single Port RAM: Port B Configuration

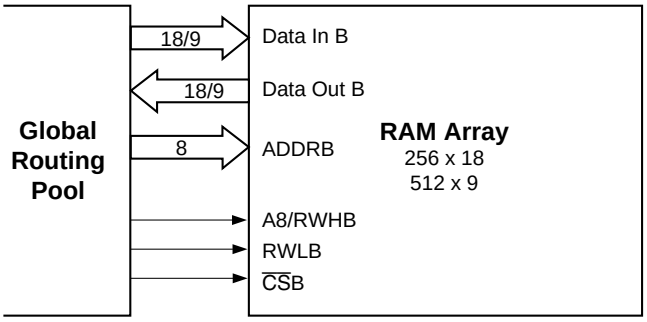


Figure 30. Single Port RAM Read Cycle Timing Diagram

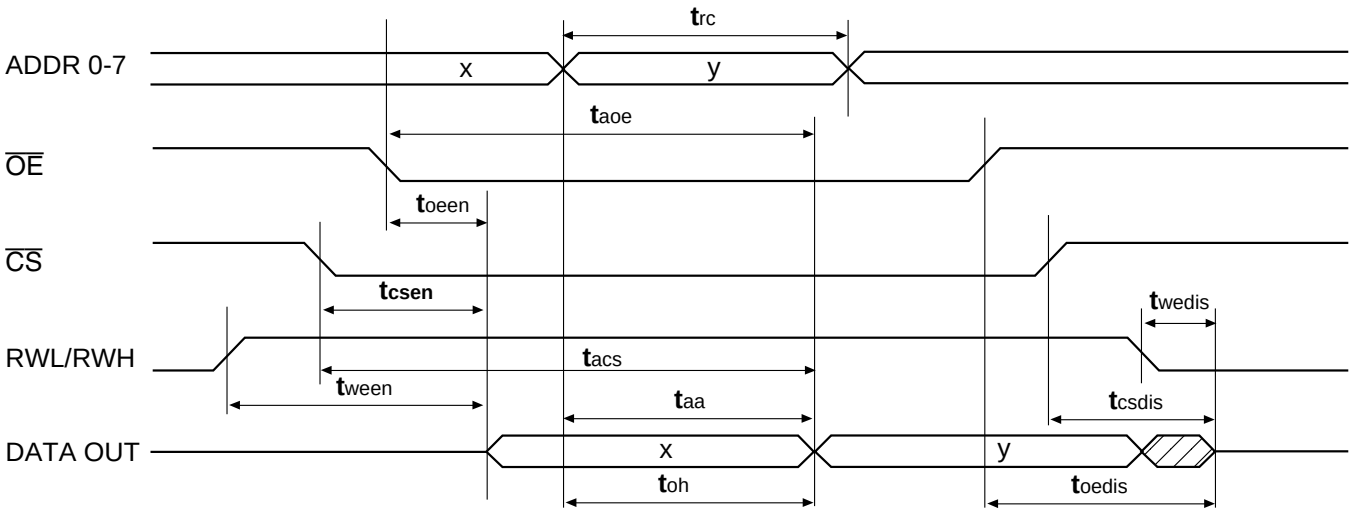
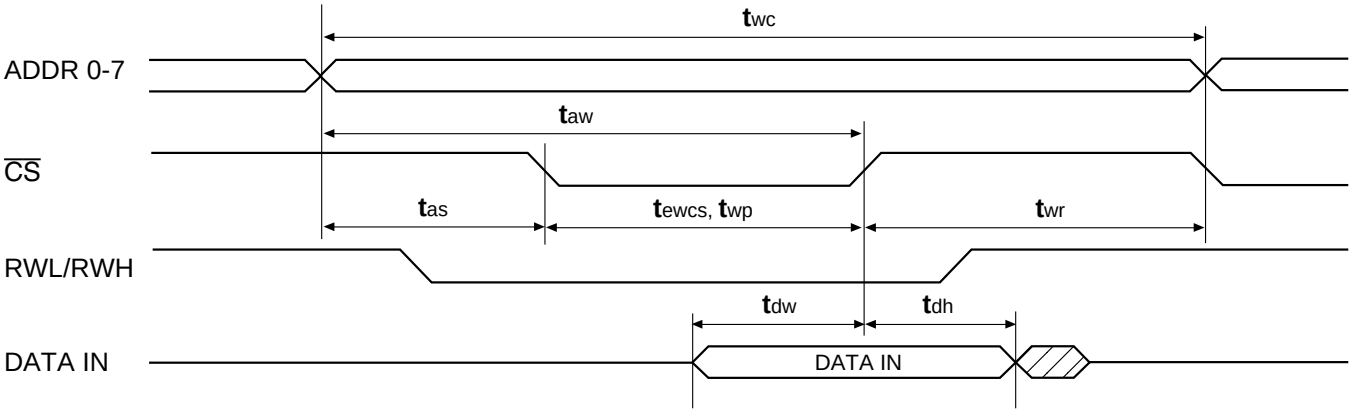


Figure 31. Single Port RAM Write Cycle (CS Controlled) Timing Diagram



Register/Counter Module Description

The Register/Counter module consists of a group of eight 16-bit Banks with control and data interfaces to both the GRP and a dedicated group of device pins. The Register File/Counter has a 16-bit bidirectional parallel data interface, Serial Data In (SIN), Serial Data Out (SOUT), and Output Enable ($\overline{OE}$) pins along with four Carry Out (COUT) pins that correspond to the counter/timer functions described below. The Banks in the Register/Counter Module can be configured by the user to implement:

- •Registers
- •Counters
- •Timers (Modulo Counter)
- •Shift Registers

In addition, Banks can be cascaded to form larger functions; for example, eight Banks can be cascaded in the Parallel-to-Serial mode to form a 128-bit parallel-to-serial shift register.

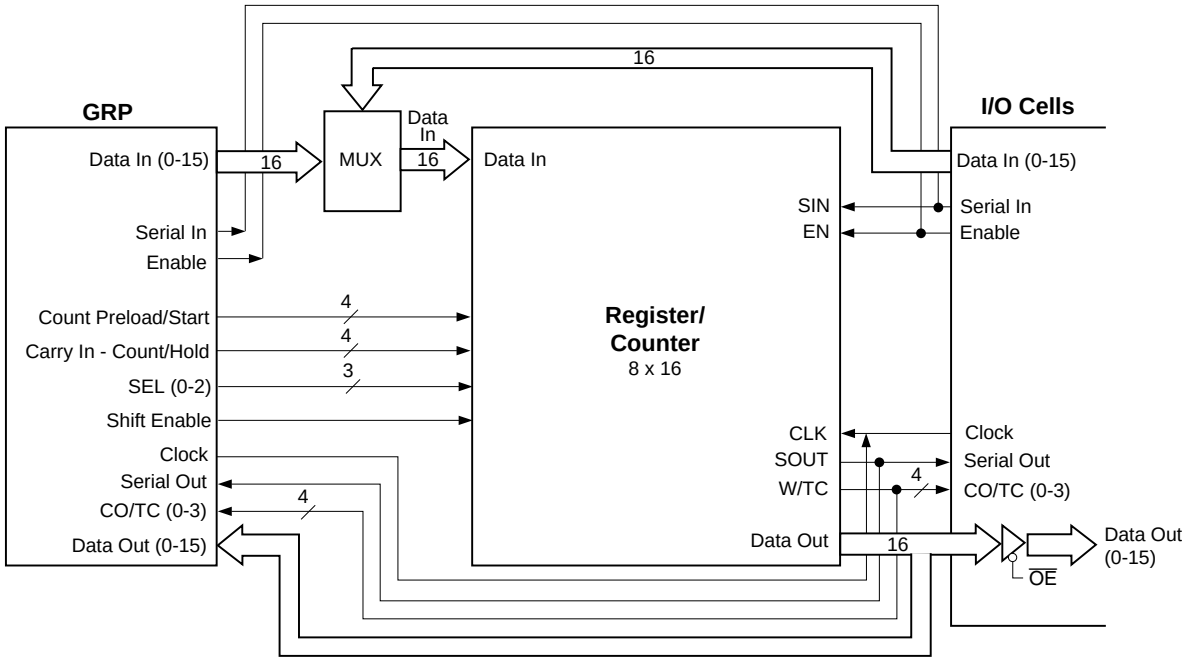
The ispDS design software allows the designer to choose one of nine predefined configurations or Modes for the Register/Counter module. Depending on the Mode chosen (discussed later), the Data Interfaces to the module can be configured as:

- •Parallel to Parallel
- •Serial to Parallel
- •Parallel to Serial
- •Serial to Serial

The Banks are addressed independently for read and write operations by using the three Select (SEL0-2) lines. These signals are driven from the 6192 GRP. All eight banks can be configured as register files, but only four of them (Banks 1,3,5,7) can be configured as 16 bit loadable up/down counters or as 16 bit loadable up/down Modulo counters. Each counter/timer Bank can be individually configured by the user. The up/down mode and 8 or 16 bit operation of the counter/timer are configured when the device is programmed based upon the user's design

Select Inputs			Bank Selected
SEL 2	**SEL 1**	**SEL 0**	**Bank #**
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Figure 32. Register/Counter Module Connectivity



inputs. All the eight word banks can be configured as shift registers.

When the dedicated Register/Counter I/O pins (DIO 0-15) are not used for the Register/Counter module, they can be used as input-only pins for the general-purpose programmable logic block. In this mode, the data pins of the unused module feed directly into the device's Global Routing Pool (GRP).

The data inputs, data outputs and the control signals for the Register/Counter Module can be either active high or active low. Other control signals (SEN, SEL0-2, etc.) come only from the GRP. Data inputs and SIN and Enable control signals can come from I/O cells or the GRP. Data output signals can go to I/O and the GRP to be used in other logic.

Each Bank can use a unique Clock configuration. The Clock is selectable from either one of the three GLB clocks, the I/O clock 0 (Y4) or a product term clock (PTCK). The user has the ability to select the true or complement of the selected clock.

There are two Reset functions within the Register/Counter Module, the Global Reset and PT Bank Reset. The Global Reset resets all the registers in programmable logic module and register/counter module. The Global Reset is active low. The Product Term (PT) Bank Reset, in conjunction with the Select lines, is used to individually reset the banks. The PT Bank Reset is active high.

The Register/Counter Module I/O pins (DIO 0-15 (RC))can be controlled by either the Global Output Enable (GOE) or the Module Output Enable ($\overline{OE}$) through a user-programmable option. The user has the choice of selecting either of these signals on an I/O by I/O basis. The OE can also be selected to be active high or low on an I/O by I/O basis.

Register/Counter Module Configuration Options

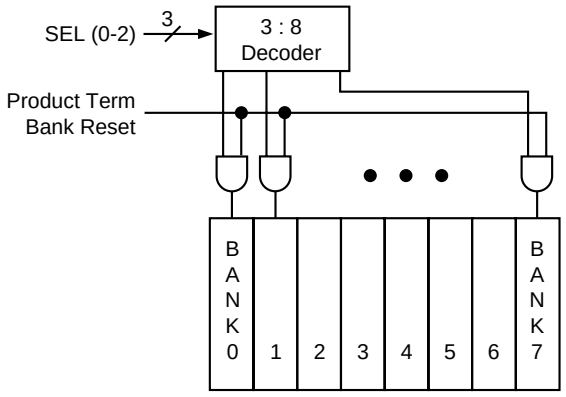
There are nine pre-defined Register/Counter configurations or modes which are supported by Lattice Semiconductor's ispDS software. These are:

1. 8-Bank Register File
2. 8-Bank Parallel to Serial Shift Register
3. 8-Bank Serial to Parallel Shift Register
4. 8-Bank Serial to Serial Shift Register
5. 4-Bank Parallel Load Up/Down Counter with 4-Bank Register File
6. 4-Bank Adjacent Load Up/Down Counter with 4-Bank Adjacent Register File
7. 4-Bank Parallel Load Up/Down Timer with 4-Bank Register File
8. 4-Bank Adjacent Load Up/Down Timer with 4-Bank Adjacent Register File
9. 4-Bank Custom Preset Load Up/Down Timer with 4-Bank Register File

In the above modes, counters and timers can be loaded either 8 or 16 bits at a time.

The following sections will discuss each of these operating modes in detail.

Figure 33. Product Term Bank Reset



Configuration #1: 8-Bank Register File

The register file is organized as eight words of 16 bits each. Sixteen data inputs are available to supply the data to be stored. The Select lines permit direct access to read or write the data to any of these words. In order to write data to a location in the file, the SEL0-2 lines must point to the correct location and the Enable input must go active. The write operation is synchronous to the clock. Data must be stable at the Register/Counter module inputs a minimum set-up time (tregsu) prior to low-to-high transition on the Clock for it to be correctly written into the file. Similarly, Enable signal must be stable a minimum set-up time (tensu) prior to the low-to-high transition of the clock. Data from the location pointed to by SEL0-2 is always presented at the multiplexer outputs (Data Out 0-15). However, to insure the data is valid, the read operation should be done when the Enable is inactive or after the falling edge of the clock.

For example, if the Select line Address is 011(binary) and the Enable signal is low, the data is clocked into the Bank 3.

Figure 34. Register/Counter Option #1: 8-Bank Register File

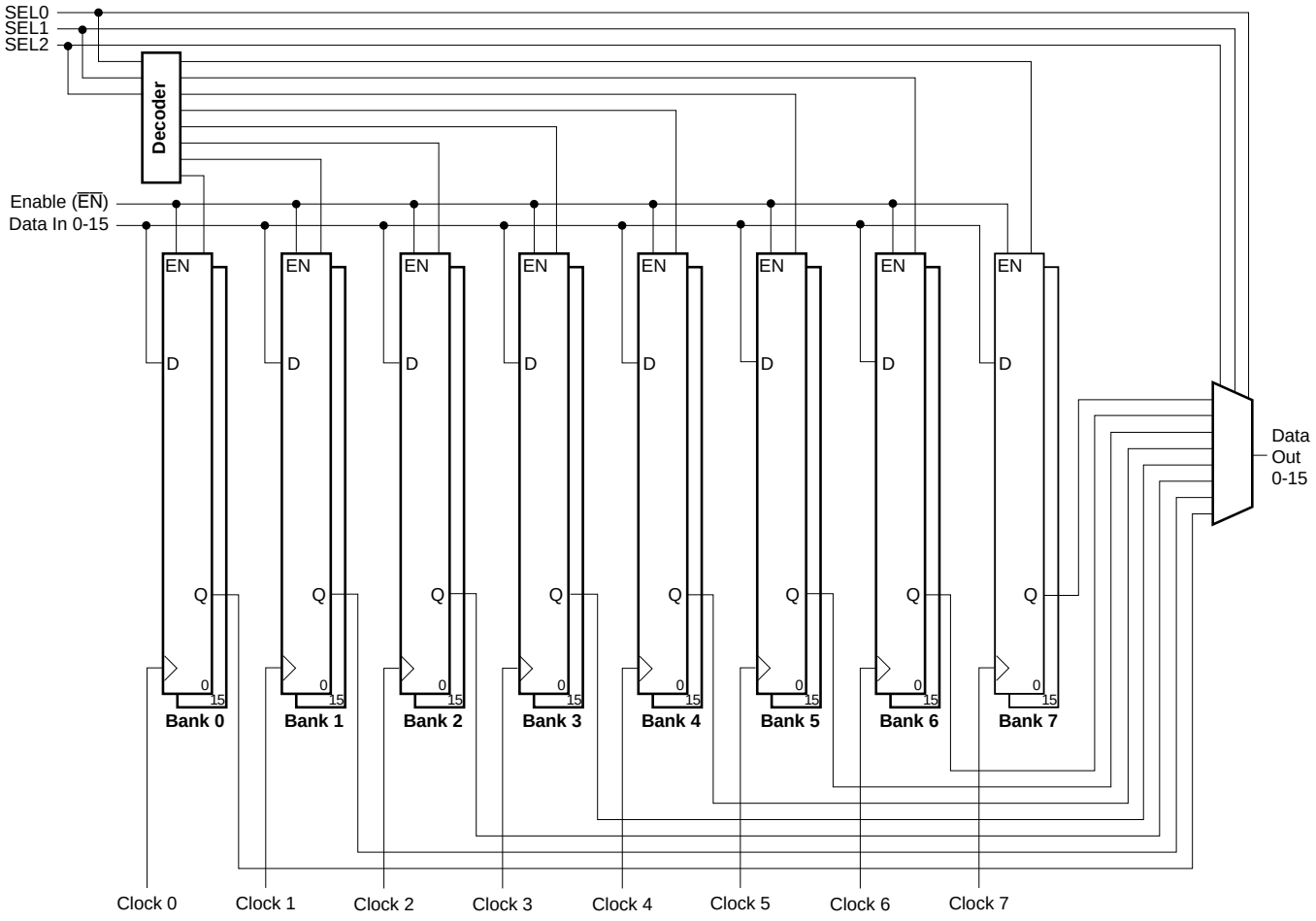
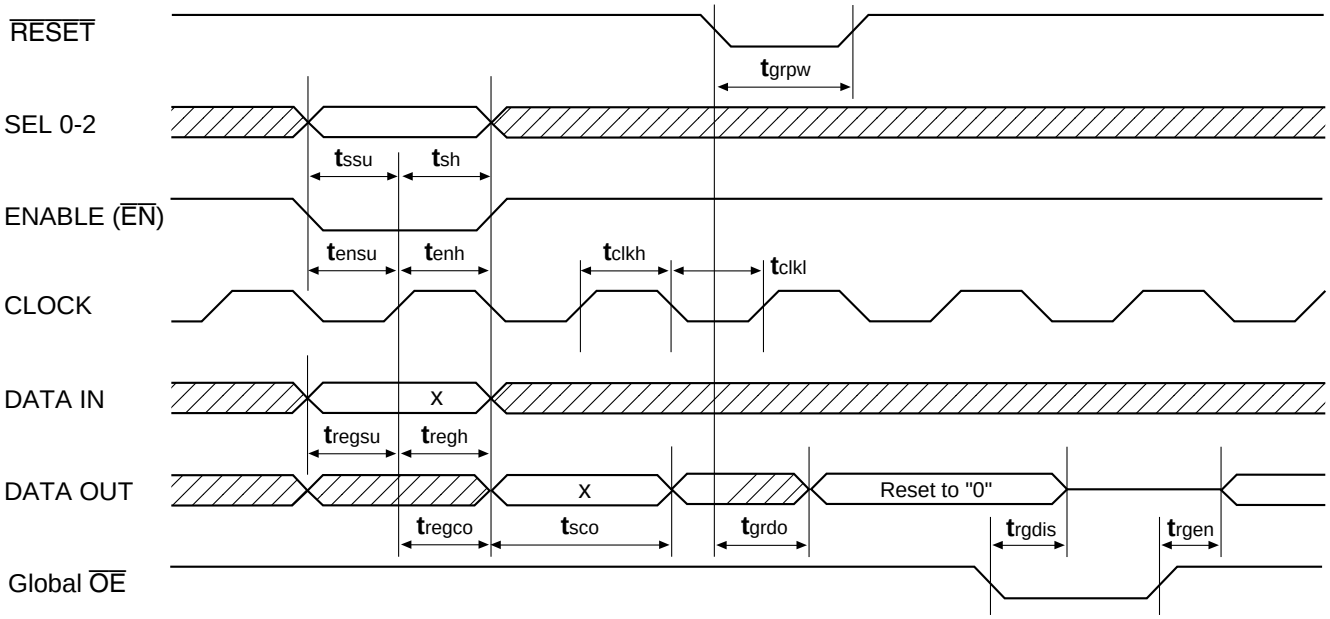


Figure 35. Register Parallel Read/Write Timing Diagram



Configuration #2: 8-Bank Parallel to Serial Shift Register

This configuration is used to convert data from a parallel to serial format. In this mode, each bank functions as a 16-bit shift register with all 8 Bank s serially cascaded from Bank 0 to Bank 7 to form a 128-bit shift register chain. Here, the parallel data write operation is the same as with the Register File configuration. As previously discussed, the Enable line must be low for the Write operation to be performed. Depending on the parallel load operation, the chain can be used as a 1-bit to 128-bit shift register. Data is read out of the Serial Out (SOUT) pin (connected to the LSB of Bank 7) serially on each Clock transition when the Shift Enable ($\overline{SEN}$) is Low.

Figure 36. Register/Counter Option #2: 8-Bank Parallel to Serial Shift Register

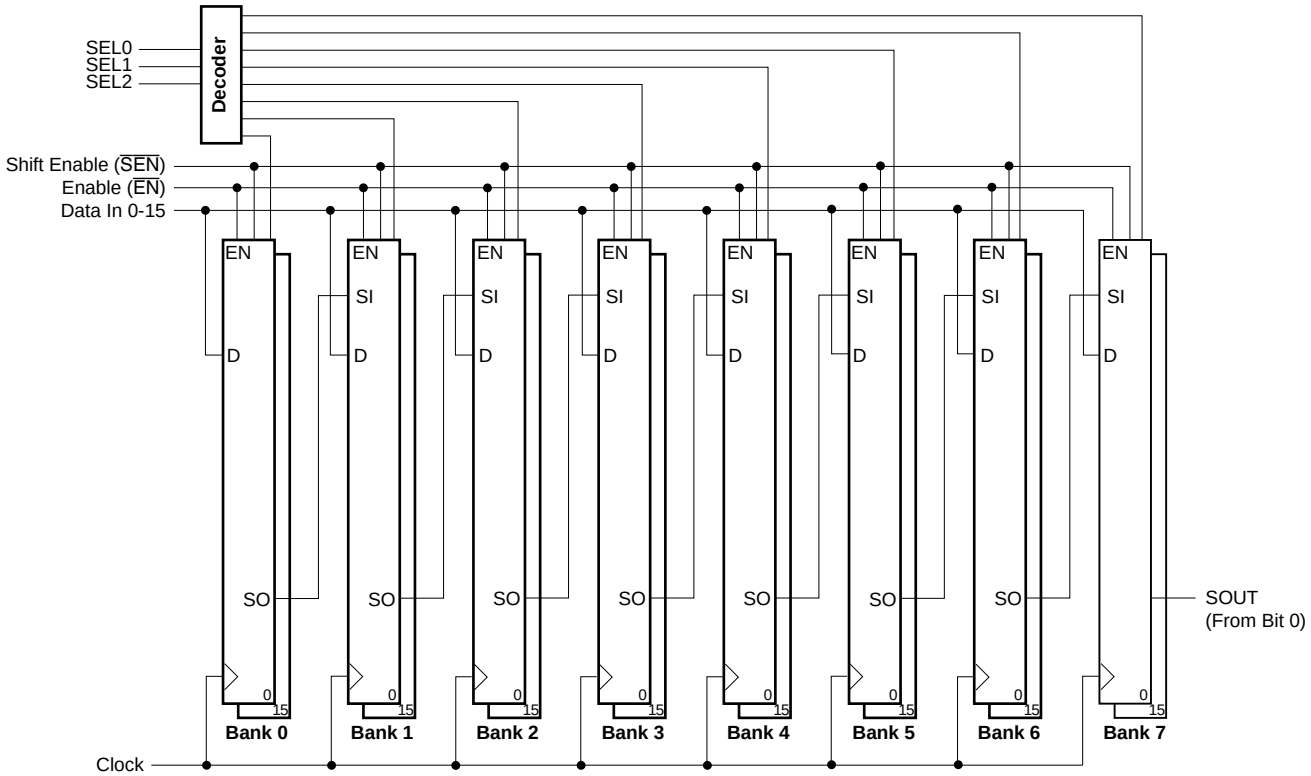


Figure 37. Shift Register Parallel Load/Shift Timing Diagram

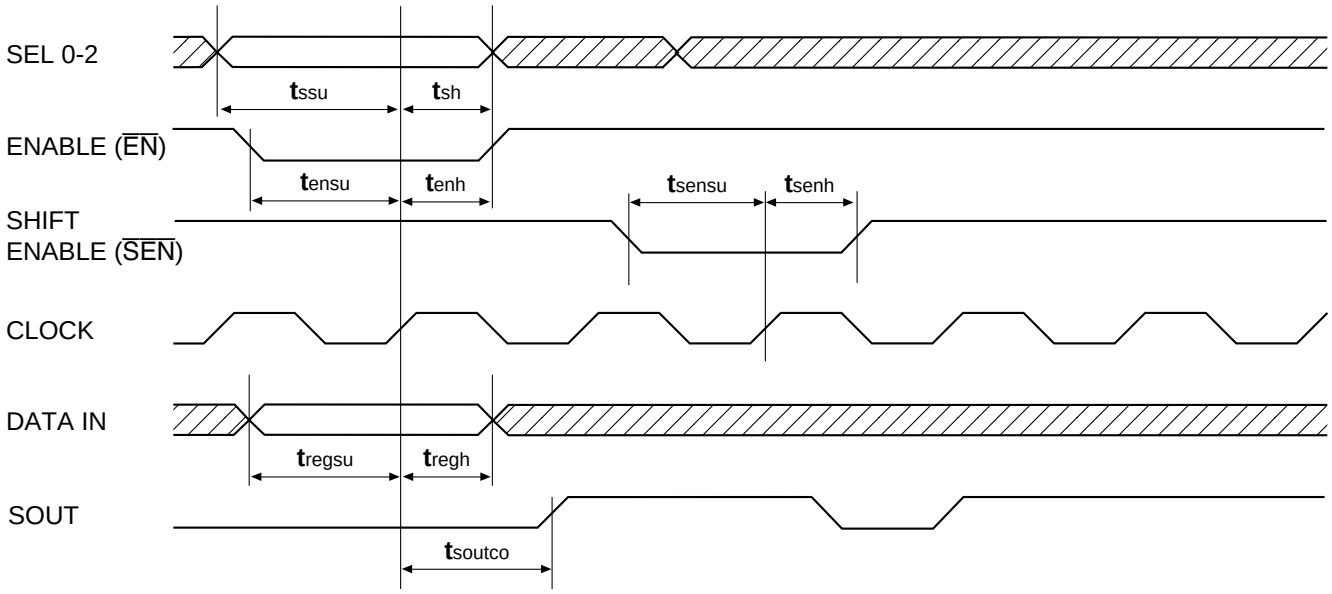
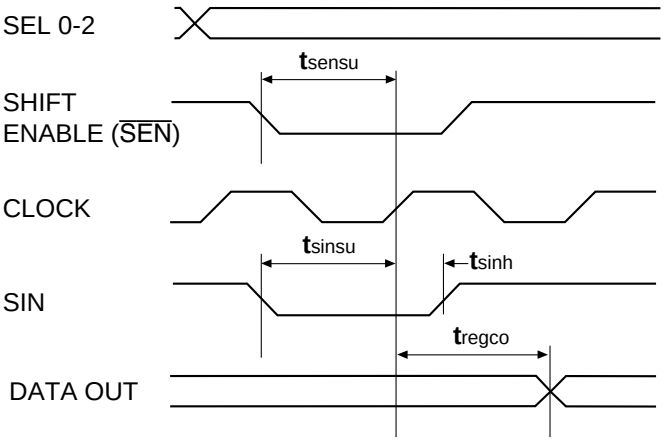


Figure 38. Shift Register Serial Load/Shift Timing Diagram



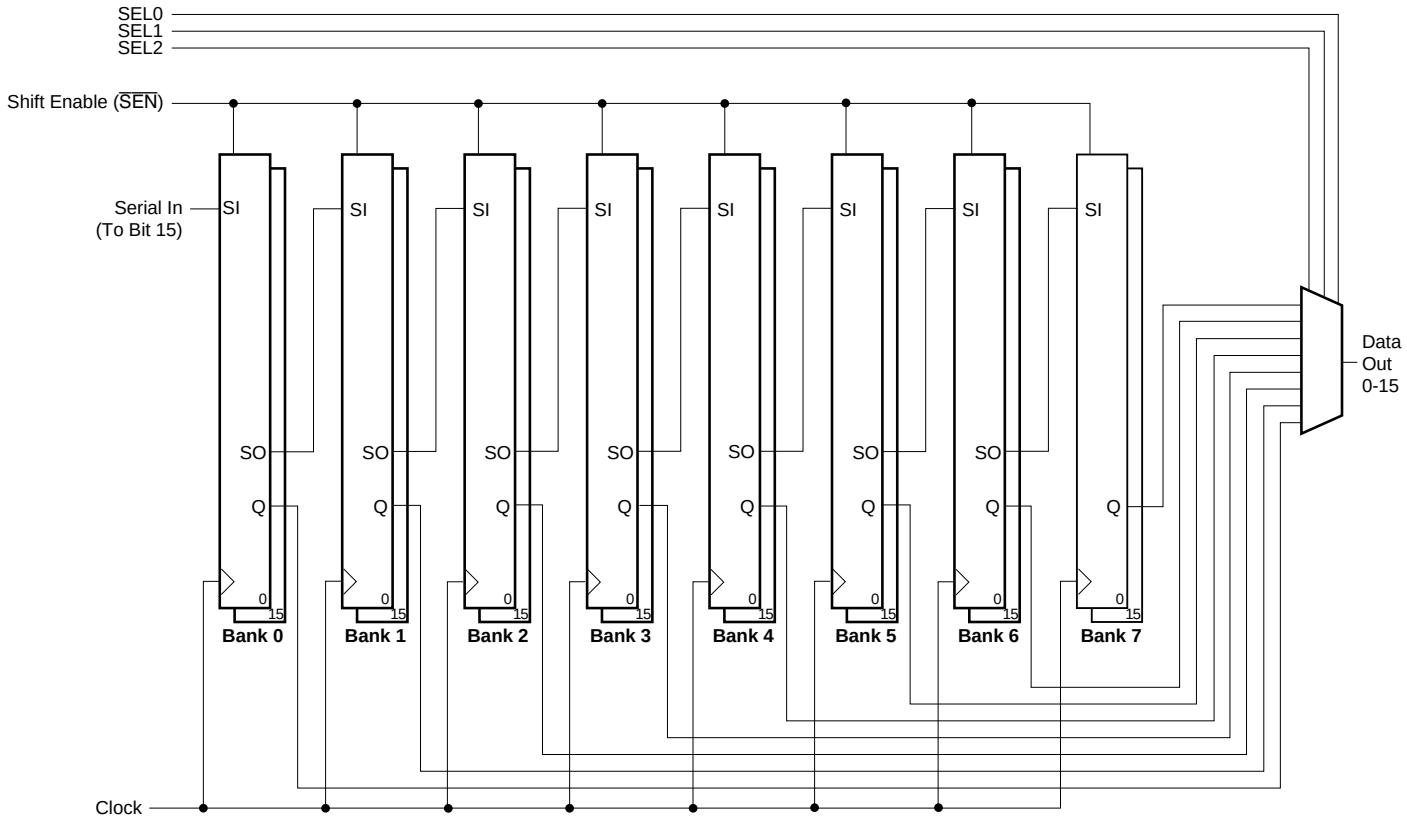
Configuration #3: 8-Bank Serial to Parallel Shift Register

This configuration is used to convert the data presented on the SIN input from serial to parallel format. All 8 banks are cascaded together. The serial out line(LSB) of one bank is automatically connected to the next bank's serial in line (MSB) and so on to form a 128-bit shift register. Depending on the use of SEL0-2, the shift register chain can be used as a 1-bit to 128-bit shift register.

The serial write operation takes place when Shift Enable ($\overline{SEN}$) is Low. The serial data is clocked into Bank 0 (see figure 38).

The Read operation is same as Parallel-to-Parallel configuration. Here also, the read operation should be performed when the Enable is inactive or after the falling edge of the clock.

Figure 39. Register/Counter Option #3: 8-Bank Serial to Parallel Shift Register

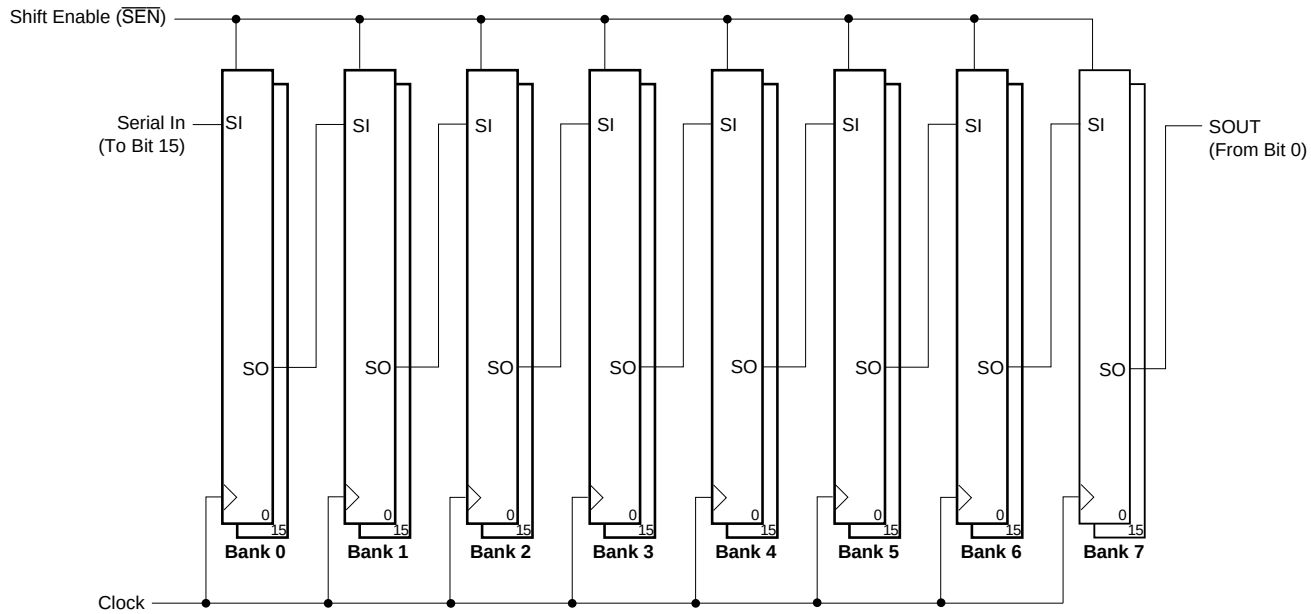


Configuration #4: 8-Bank Serial to Serial Shift Register

This configuration is used to shift data in and serially shift data out. The bank are cascaded together to form a 128 bit shift register. The data flow is from the Most Significant Bit (MSB) to the Least Significant Bit of each bank. The LSB of Bank 0 is connected to the (MSB) of Bank 1 and so on. The Serial Data In (SIN) is on Bank 0 and the Serial data out (SOUT) is on Bank 7.

Both the read and write operations are serial in this mode of operation in this configuration. The Shift Enable signal controls the Shift or Hold activity of the data. When the Shift Enable is low, the banks will begin shifting data (MSB to LSB) synchronously. When the signal is High, the banks retain the last data without shifting.

Figure 40. Register/Counter Option #4: 8-Bank Serial to Serial Shift Register



Configuration #5: 4 Bank Parallel Load Up/Down Counter with 4-Bank Register File

Four of the eight banks can be configured as 8- or 16-bit loadable, up or down counters. These word banks are Bank 1, Bank 3, Bank 5 and Bank 7. The counters are addressed for read and write operations in the same manner as the Register File by using SEL (0-2) and Enable. The counters are parallel loaded from the Data In (DIN) lines and are read out to the Data Out (DOUT) lines. The 8 or 16 bit data is loaded into the counter bank selected by the select lines. Whether 8 or 16 bit data is transferred is determined by the operating mode defined for the specific counter when the device is programmed. Load (Write) occurs when Enable (EN) signal is low and a there is a low-to-high clock edge.

Each counter has independent Carry In-Count/Hold (CICH) and Carry Out (COUT) lines, which allow the designer to have independent control of each counter, thus giving more flexibility in his design. These lines can have several alternative uses. The Carry In and Carry Out lines can be used to cascade counters to form very large counters, up to 64 bits. The Carry In can also be used as a Count/Hold control: when the signal is High, the counter will count. When low, it will hold the counter at the present count. The Carry Out line can also be used to tell when the counter has reached its maximum or terminal count (TC).

The count operation will only take place when the Carry In-Count/hold is high and there is a low-to-high clock edge. When the counters reach FFFFH during counting up or 0000H when counting down, their contents "roll-over" on the next clock pulse to 0000H and FFFFH respectively, and counting continues, assuming Carry-In is active (see figure 42).

In Mode #5, 4 Banks (1,3,5,7) are configured as counters which operate as described immediately above, and 4 Banks (0,2,4,6) operate as Register files as described in Mode #1 above.

Figure 41. Register/Counter Option #5: 4 Bank Parallel Load Up/Down Counter with 4 Bank Register File

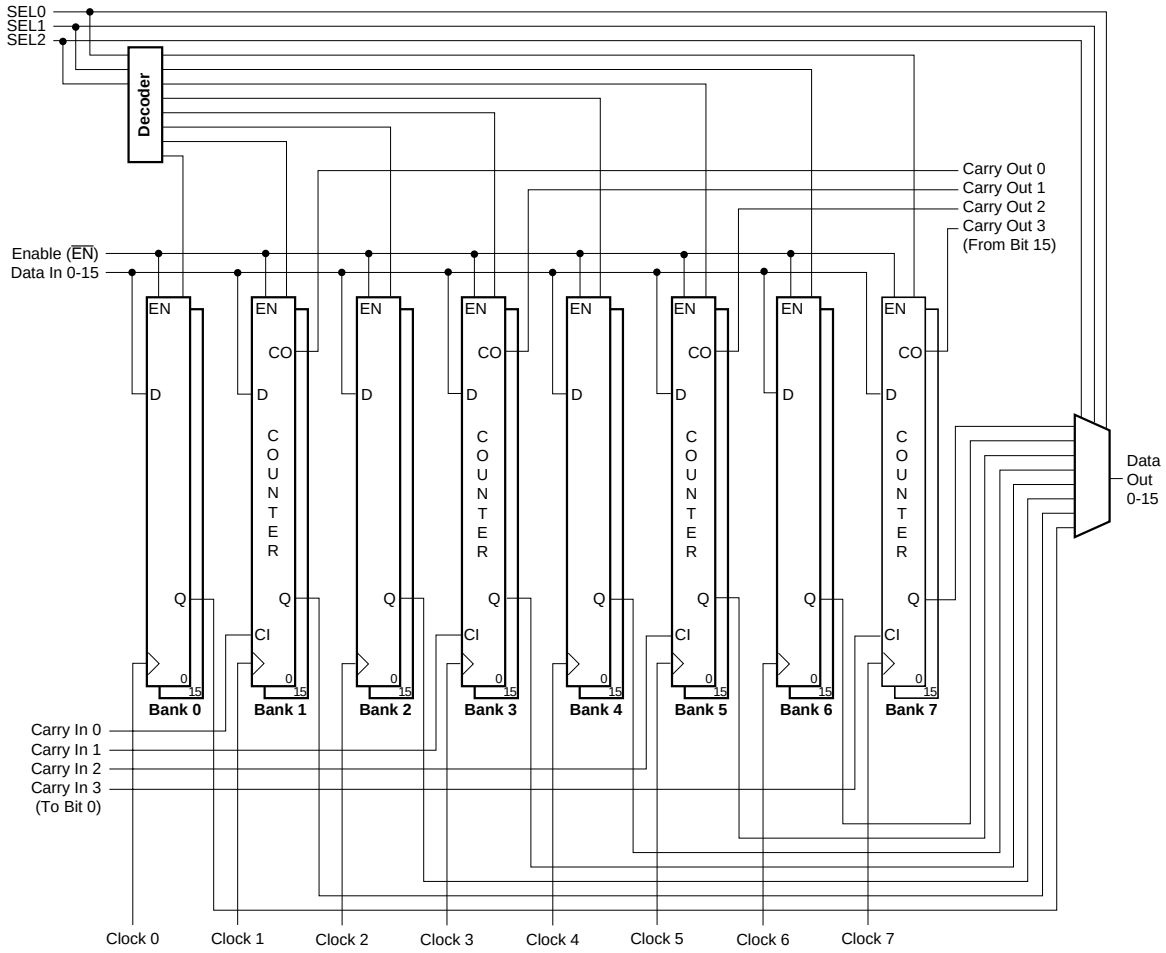
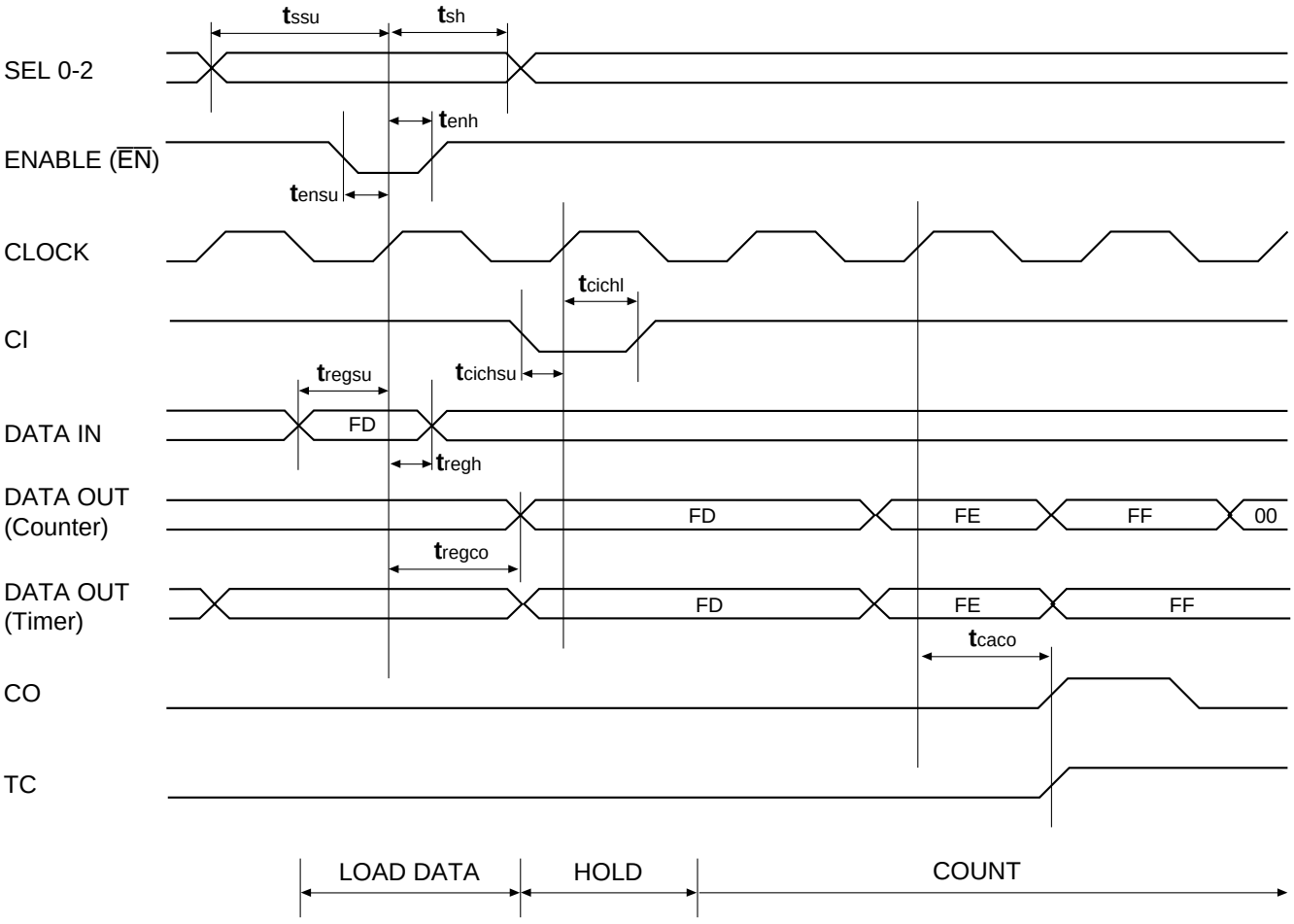


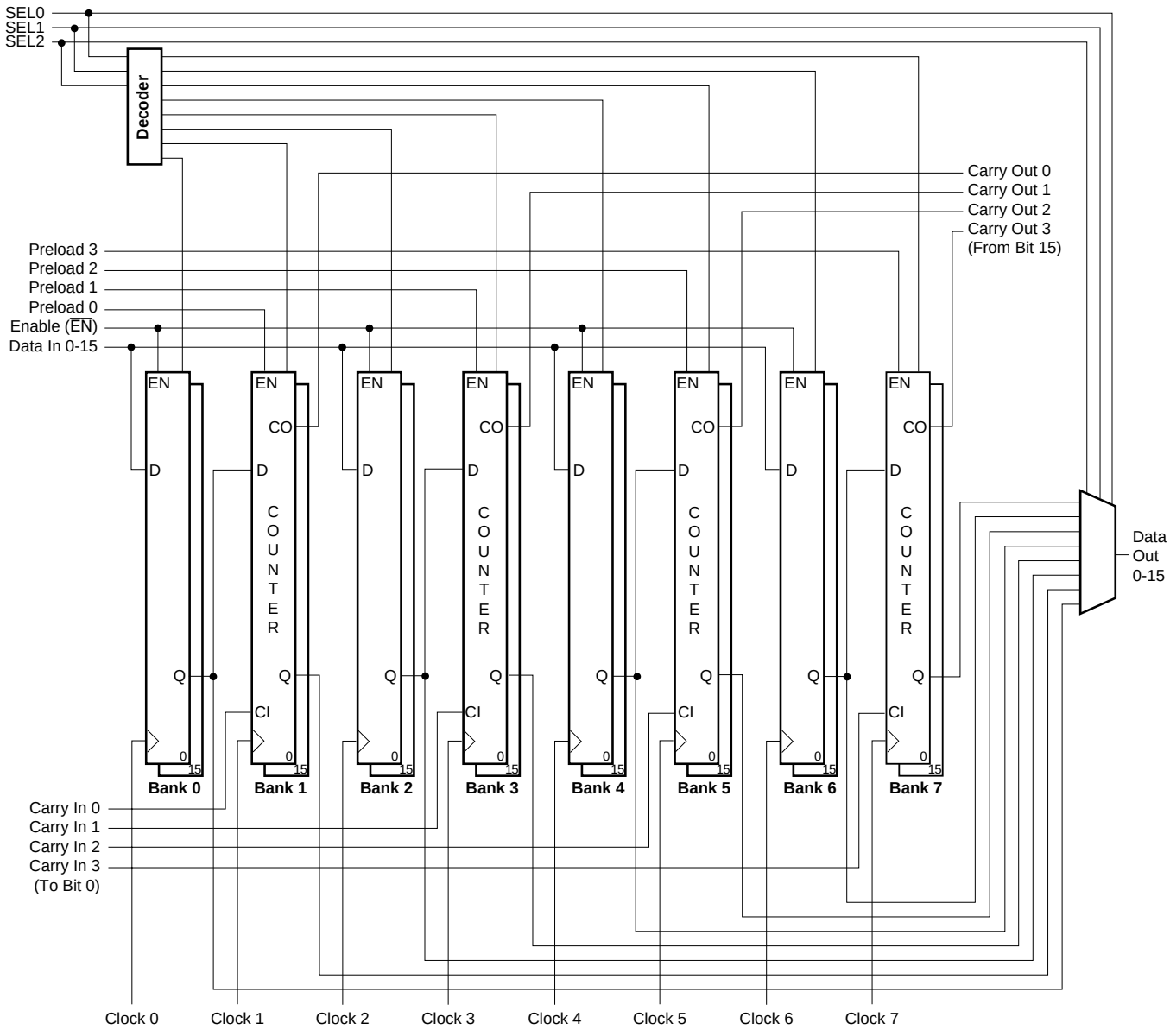
Figure 42. Counter/Timer Timing Diagram



Configuration #6: 4 Bank Adjacent Load Up/Down Counter with 4 Bank Adjacent Register File

In this mode, the counters function as described in Mode #5 above. However, rather than being parallel loaded from the Data In lines when Enable is low, the counters are loaded from the adjacent registers during a load. Banks 0, 2, 4, 6 are used to hold the preload data for counter Banks 1, 3, 5, and 7, respectively. The preload data is loaded into the selected register file bank in the usual manner when a clock occurs and the Enable is low. Data is loaded into the adjacent counter when th corresponding Preload is low and there is a rising clock edge.

Figure 43. Register/Counter Option #6: 4 Bank Adjacent Load Up/Down Counter with 4 Bank Adjacent Register File



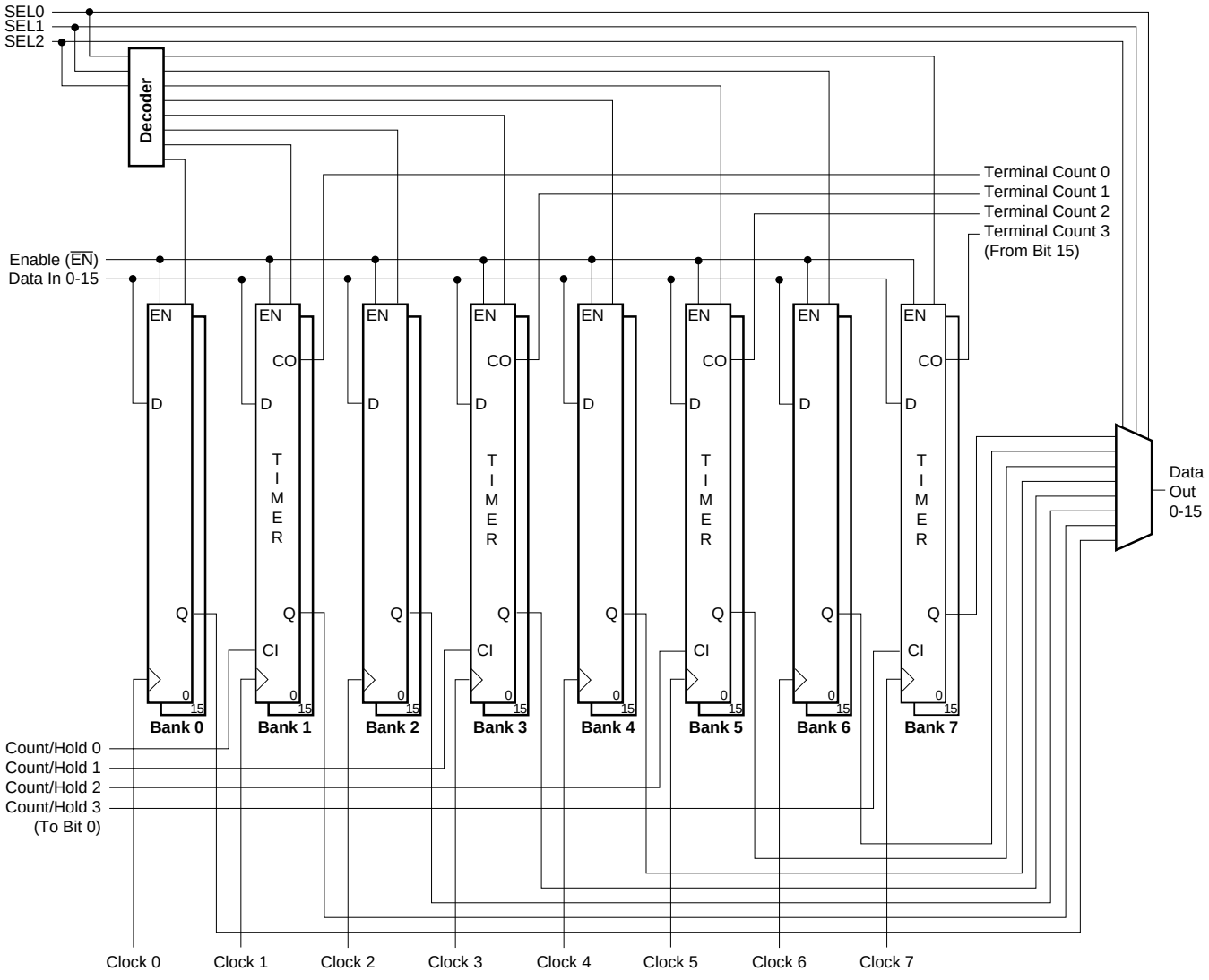
Configuration #7: 4 Bank Parallel Load Up/Down Timer with 4 Bank Register File

Four of the eight banks in the Register/Counter module can be configured as 8- or 16-bit loadable, up or down timers. These word banks are Bank 1, Bank 3, Bank 5 and Bank 7. The timers are addressed for loading and reading in the same manner as the Register File (Mode #1). The counters are parallel loaded from the Data In (DIN) lines and are read out to the Data Out (DOUT) lines. The 8 or 16 bit data is loaded into the timer bank selected based on the operating mode specified for the timer and programmed into the device. The load occurs when the Enable signal is low and there is a rising clock edge.

Each timer has an independent Carry In-Count/Hold line which allows the designer to have independent control of each timer, thus giving more flexibility. Timer operation is different from counter operation in that a timer will stop counting once the terminal count (FFFFH for an Up Timer and 0000H for a Down Timer) is reached. The Timer will begin counting again only after the timer is reloaded using the Enable and SEL0-2 lines. Also, each timer has a independent Carry Out/Terminal Count output. The carryin-count/hold and the count preload/start signals must be high for the timer to operate.

In Mode #7, 4 Banks (1,3,5,7) are configured as timers which operate as described immediately above, and 4 Banks (0,2,4,6) operate as Registers as described in Mode #1 above.

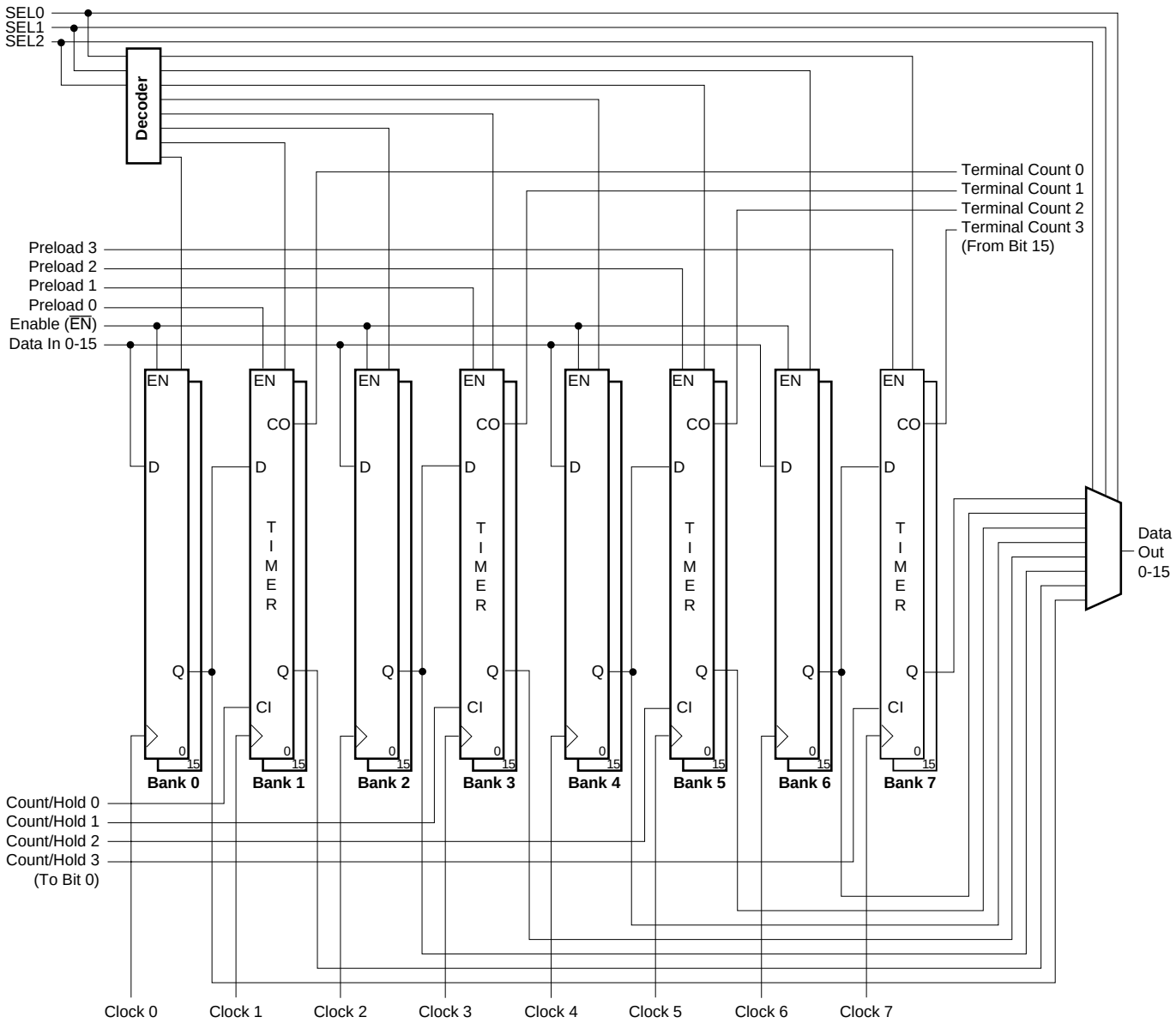
Figure 44. Register/Counter Option #7: 4 Bank Parallel Load Up/Down Timer with 4 Bank Register File



Configuration #8: 4 Bank Adjacent Load Up/Down Timer with 4 Bank Adjacent Register File

In this mode, the timers function as described in Mode #7 above. However, rather than being parallel loaded from the DIN lines when Enable is low, the counters are loaded from the adjacent registers during a load. Banks 0, 2, 4, 6 are used to hold the preload data for counter Banks 1, 3, 5, and 7, respectively. The preload data is loaded into the selected register file bank in the usual manner when a clock occurs and the Enable is low. Data is loaded into the adjacent counter when Preload is low and there is a rising clock edge.

Figure 45. Register/Counter Option #8: 4 Bank Adjacent Load Up/Down Timer with 4 Bank Adjacent Register File

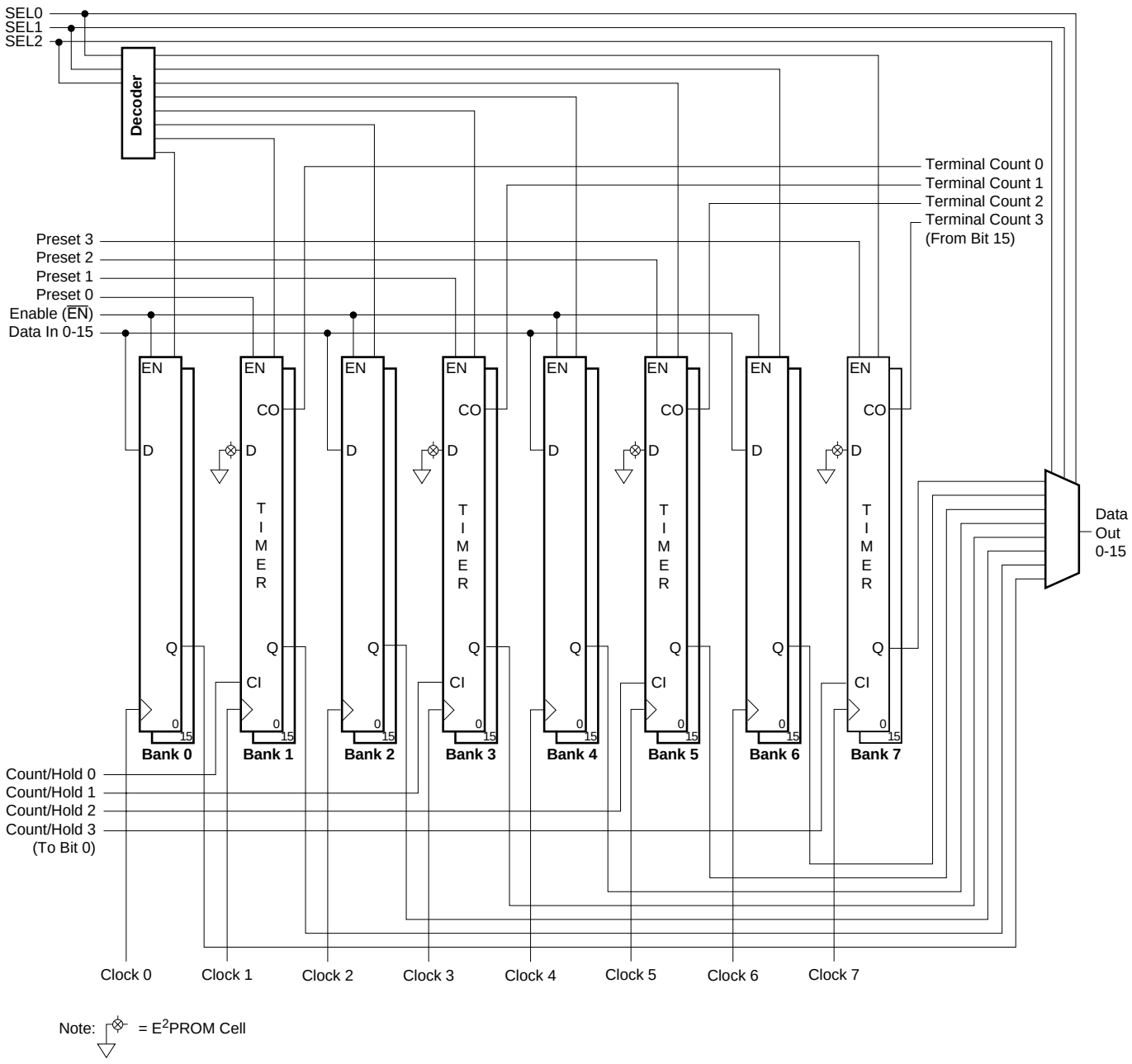


Configuration #9: 4 Bank Custom Preset Load Up/Down Timer with 4 Bank Register File

In this mode, the timers function as described in Mode #7 above. However, rather than being parallel loaded from the DIN lines, or from the adjacent registers, in Mode #9 the Timers are loaded from dedicated E^2PROM (Read-Only Memory) locations. The preset data in these locations is determined by the user when the logic is designed using the ispDS software and is programmed into the device using non-volatile technology. The data from these locations is loaded into the counter whenever Preset is low and there is a clock edge.

In Mode #9, 4 Banks (1,3,5,7) are configured as timers which operate as described immediately above, and 4 Banks (0,2,4,6) operate as Registers as described in Mode #1 above.

Figure 46. Register/Counter Option #9: 4 Bank Custom Preset Load Up/Down Timer with 4 Bank Register File



I/O Cells

The 6192 family of devices has 3 types of programmable I/O cells. They can be classified as:

- General Bidirectional I/O Cell
- Module Bidirectional I/O Cell
- Module I/O Cell

General Bidirectional I/O Cell

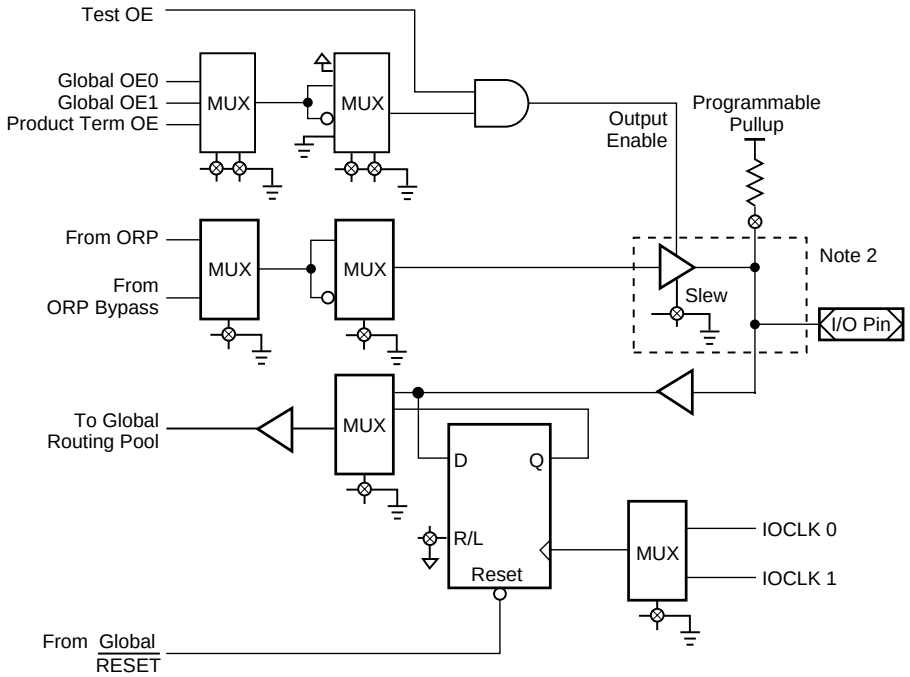
The general bidirectional I/O cell structure, associated with Megablocks A, B, C, D, E and F is similar to Lattice Semiconductor's 3000 family I/O cells (see figure 47). They are used to route input, output or bi-directional signals connected to the I/O pin. Each I/O cell contains Boundary Scan Registers (see Boundary Scan section). A global Test OE signal is hardwired to all I/O cells and is used to 3-state all output buffers within the device. In addition to the test OE signal, two software selectable global OEs are connected to each of these I/O cells. A Product Term OE and global OE signals are fed to an OE multiplexer to allow one of the three signals to control the output. This OE signal can also be inverted.

The output signal can come from one of two sources, the ORP or the faster ORP bypass. A pair of multiplexers selects which signal will be used, and its polarity. There is also a software programmable slew rate control. Slew rate control allows non-timing-critical signals to run at a slower rate which improves system noise immunity. The software has the capability to enable and disable the slew rate control bit on an individual I/O basis.

When the I/O cell is used as an input, the data goes to the input register and a selection multiplexer which selects either the direct data input or the input register output. The output of the multiplexer then goes to the GRP. The input register can be configured as a level sensitive transparent latch or an edge triggered D-type flip-flop to store the incoming data. Each I/O cell can individually select one of the two clock signals (IOCLK 0 or IOCLK 1). The input register reset signal is hard wired to the global reset ($\overline{\text{RESET}}$) signal which is driven by the active low chip reset pin.

There is an active pull-up resistor on the I/O pins which is automatically used when the pin is not used in the design. This improves the noise immunity and reduces I_{cc} for the device. An option exists to have active pull-up resistors connected to all pins.

Figure 47. General-Purpose Bidirectional I/O Cell



Note:

1. Represents an E^2CMOS Cell.
2. See Boundary Scan section for details.

Module Bidirectional I/O Cell

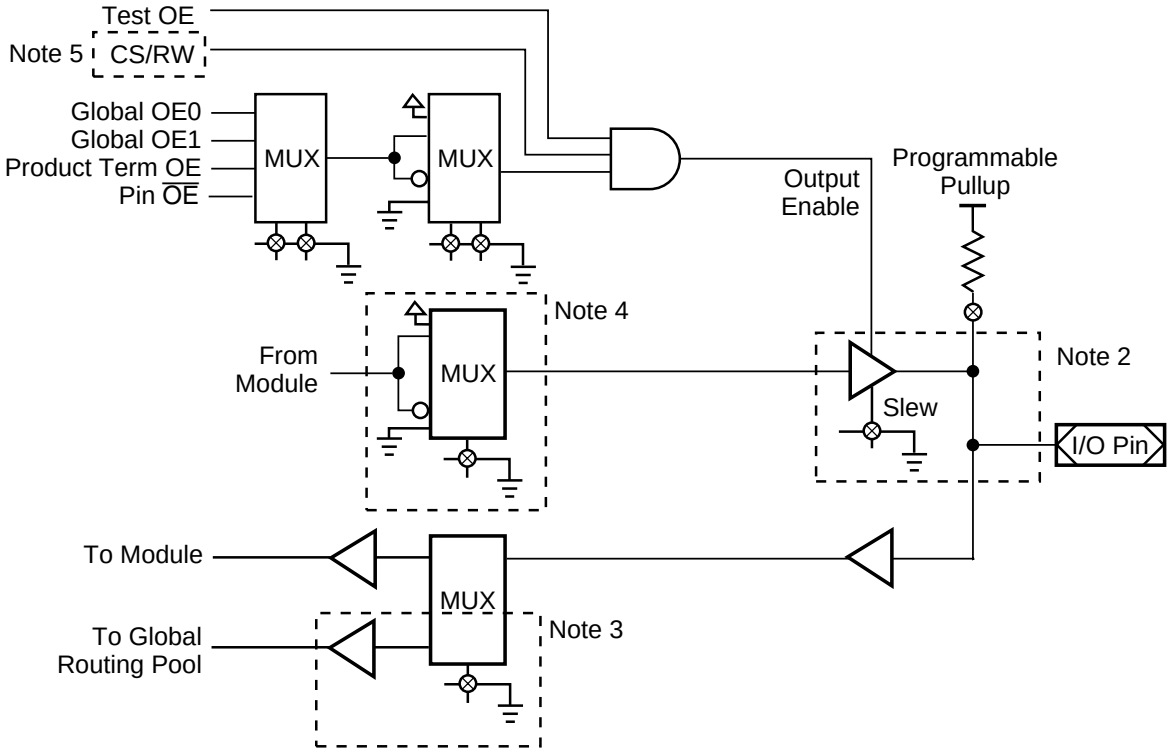
Module bidirectional I/O cells are associated with the bidirectional data bus in the memory module and the register/counter module. The structure of these cells is similar to that of the general bi-directional I/O cells, with some differences. Figure 48 illustrates two signals that are hard-wired to module data I/O cells: Test OE and CS/RW. Test OE is driven by the TOE pin and is wired to all the module data I/O cells. CS/RW is generated by logic internal to the memory module and is only wired to the data I/O cells associated with this module. CS/RW is high only when the chip is selected and the memory is to be read. Thus, an inactive Chip Select forces the pin driver in each of these I/O cells to the high impedance state.

Figure 48 shows Pin $\overline{OE}$, Product Term OE, and two Global OE signals. These are fed to an OE multiplexer to allow one of these four signals or its inversion to control the output driver. The logic output from the Register/Counter module has an inversion capability in the I/O cell while the memory module does not (see figure 48, note 4).

Selected data I/O cells (0-8) in the memory module have an alternative use: these pins can be used as general-purpose inputs to the GRP when the memory module is used in 512 x 9 configuration or left unused in the design. The data I/O cells (0-15) in the register/counter module can also be used as general-purpose inputs to the GRP provided the register/counter module is left unused in the design (see figure 48, note 3).

In the module bidirectional I/O cell, unlike in the general bidirectional I/O cell where the slew rate is individually controllable for each outputs, either all or none of the output data bits can be programmed to have slew rate control.

Figure 48. Module Bidirectional I/O cell



Note:

1. Represents an E^{2}CMOS Cell.
2. See Boundary Scan section for details.
3. Selected Module I/O pins only (DIO0-8(MEM) and DIO0-15(RC))
4. Register/Counter Module data I/O cell only.
5. Memory Module data I/O cell only.

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Module I/O Cell

Module I/O cells are associated with the logic control signals of the memory module and register/counter module. They are controlled by the software and can be programmed as simple inputs or outputs. A multiplexer is used to select the polarity of the output signal coming from the module.

The control signals (TC/CO(0-3), SOUT) of the register/counter module use output pins. The slew rate is individually controllable for each output. SIN and ENABLE are input pins.

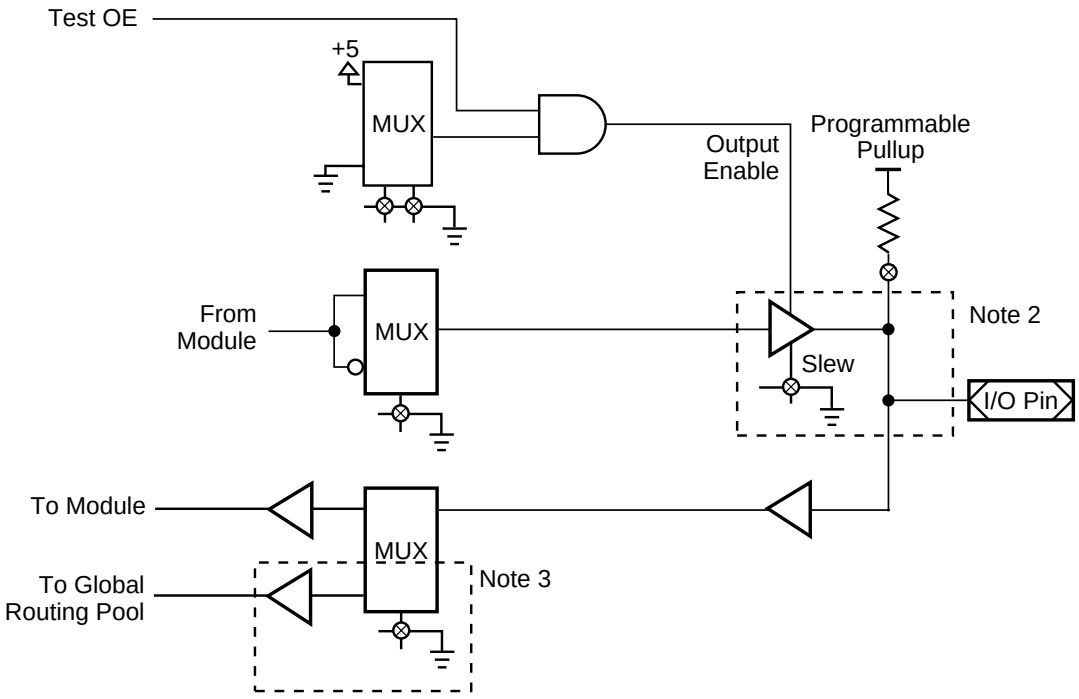
Selected I/O cells in the memory module can be used as general-purpose logic inputs if the memory module is left unused (see figure 49, note 3).

The table below summarizes various types of I/O cells used by the module. They are classified as Module Bidirectional I/O cells and Module Unidirectional I/O cells.

The output signals come from the module. Some of them can be configured with the help of a polarity selection multiplexer. When the I/O cell is used as an input, the data goes to the module. Some of the I/O cells have an additional capability of being used as inputs to the GRP when the module is left unused in the design.

Module Unidirectional I/O cells can be used either as an input or an output. When used as an output cell, TOE will always 3-state the output buffer. It also has a programmable slew rate control. When used as an input cell as shown in the table there are two versions: one that drives the module only, and a second version which can drive the GRP if the module is not used.

Figure 49. Module I/O Cell



Note:

1. Represents an E^{2}CMOS Cell.
2. See Boundary Scan section for details.
3. Only in Memory Module ($\overline{ALE}$ & $\overline{ALF}$ in FIFO and A3 - A7 in RAM).

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Module I/O Cell Connectivity

	Signal Name	Module Bidirectional I/O Cell				Module Unidirectional I/O Cell			
		Basic	Input to		Output From Module	Basic	Input to		Output From Module
			Module	GRP			Module	GRP	
Register/ Counter Interface	DIO 0-15	√[2]	√	√	√[3]				
	TC/CO 0-3, SOUT					√[1]			√[3]
	$\overline{OE}$, SIN, $\overline{ENABLE}$						√		
FIFO Interface	DIO 0-8	√[2]	√	√	√				
	DIO 9-17	√[2]	√		√				
	$\overline{EF}$, $\overline{FF}$					√[1]	√		√[3]
	$\overline{ALE}$, $\overline{ALF}$					√[1]	√	√	√[3]
	$\overline{RST}$, $\overline{OE}$, $\overline{RD}$ or $\overline{WR}$						√		
RAM Interface	DIO 0-8	√[2]	√	√	√				
	DIO 9-17	√[2]	√		√				
	A0, $\overline{OE}$, RWL						√		
	A1, A2					√[1]	√		
	A3, A4					√[1]	√	√	
	A5, A6, A7						√	√	
	A8/RWH, $\overline{CS}$						√	√	

Note:
1. TOE and programmable slew rate controls.
2. GOE, PTOE, TOE and programmable slew rate controls.
3. Output polarity selection multiplexer.

Absolute Maximum Ratings [1]

Supply Voltage V_{cc} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} +1	V

Table 2 - 0005/3256

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	Typical	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	10	pf	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V
C_2	Clock Capacitance	15	pf	V_{CC} = 5.0V, V_Y = 2.0V

Table 2 - 0006/6192

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles

Table 2- 0008B

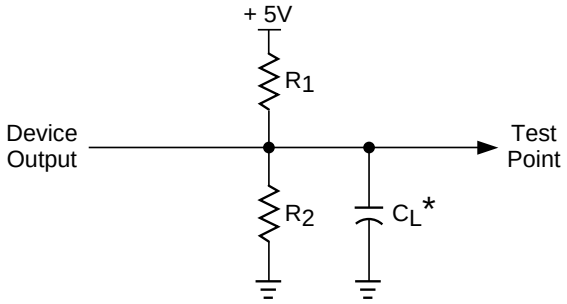
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

Table 2 - 0003

3-state levels are measured 0.5V from steady-state active level.

Figure 50. Test Load



*C_L includes Test Fixture and Probe Capacitance.

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Output Load conditions (See figure 50)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH}-0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL}+0.5V	470Ω	390Ω	5pF

Table 2 - 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	—	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{OL} \le V_{IL}$ (Max.)	—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
I_{IL-PU}	I/O Active Pull-Up Current	$0V \le V_{IN} \le V_{IL}$ (Max.)	—	—	-150	µA
I_{IL-isp}	BSCAN/$\overline{ispEN}$ Input Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (Max.)	—	—	-150	µA
I_{OS}	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V	—	—	-200	mA
I_{CC}[2,4]	Operating Power Supply Current	V_{IL} = 0V, V_{IH} = 3.0V, f_{TOGGLE} = 1MHz	—	150	—	mA

1. One output at a time for a maximum duration of one second. V_{OUT}= 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using sixteen 16-bit counters.
3. Typical values are at V_{CC}= 5V and T_A= 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this datasheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC}.

External Switching Characteristics: Programmable Logic Module[1, 2, 3]

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	
tpd1	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	—	15	—	20	ns
tpd2	A	2	Data Propagation Delay	—	18	—	24.5	ns
fmax (Int.)	A	3	Clock Frequency with Internal Feedback[3]	77	—	57	—	MHz
fmax (Ext.)	—	4	Clock Frequency with External Feedback	50	—	37	—	MHz
fmax (Tog.)	—	5	Clock Frequency, Max Toggle[4]	83	—	63	—	MHz
tsu1	—	6	GLB Reg. Setup Time before Clock, 4PT bypass	9.5	—	12.5	—	ns
tco1	A	7	GLB Reg. Clock to Output Delay, ORP bypass	—	9	—	12	ns
th1	—	8	GLB Reg. Hold Time after Clock, 4PT bypass	0	—	0	—	ns
tsu2	—	9	GLB Reg. Setup Time before Clock	11	—	15	—	ns
tco2	—	10	GLB Reg. Clock to Output Delay	—	10.5	—	14	ns
th2	—	11	GLB Reg. Hold Time after Clock	0	—	0	—	ns
tr1	A	12	Ext. Reset Pin to Output Delay	—	15	—	20	ns
trw1	—	13	Ext. Reset Pulse Duration	10	—	13.5	—	ns
tptoeen	B	14	Input to Output Enable	—	18	—	24.5	ns
tptoedis	C	15	Input to Output Disable	—	18	—	24.5	ns
tgoeen	B	16	Global OE Output Enable	—	11	—	13.5	ns
tgoedis	C	17	Global OE Output Disable	—	11	—	13.5	ns
ttoeen	B	18	Test OE Output Enable	—	17	—	23	ns
ttoedis	C	19	Test OE Output Disable	—	17	—	23	ns
twh	—	20	Ext. Sync. Clock Pulse Duration, High	4	—	5	—	ns
twl	—	21	Ext. Sync. Clock Pulse Duration, Low	4	—	5	—	ns
tsu3	—	22	I/O Reg. Setup Time before Ext. Sync. Clock (Y3, Y4)	6	—	8	—	ns
th3	—	23	I/O Reg. Hold Time after Ext. Sync. Clock (Y3, Y4)	0	—	0	—	ns

1. Unless noted otherwise, all parameters use 20 PTXOR path and ORP.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

Internal Timing Parameters: Programmable Logic Module[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{iobp}	24	I/O Register Bypass	–	2.4	–	3.3	ns
t_{iolat}	25	I/O Latch Delay	–	12.4	–	15.8	ns
t_{iosu}	26	I/O Register Setup Time before Clock	7.2	–	9.6	–	ns
t_{ioh}	27	I/O Register Hold Time after Clock	-5.2	–	-7.0	–	ns
t_{ioco}	28	I/O Register Clock to Out Delay	–	4.2	–	5.3	ns
t_{ior}	29	I/O Register Reset to Out Delay	–	3.6	–	4.9	ns
GRP							
t_{grp}	30	GRP Delay	–	3.0	–	4.1	ns
GLB							
t_{4ptbp}	31	4 Product Term Bypass Path Delay	–	5.9	–	7.6	ns
t_{1ptxor}	32	1 Product Term/XOR Path Delay	–	6.4	–	8.8	ns
$t_{20ptxor}$	33	20 Product Term/XOR Path Delay	–	7.4	–	10.1	ns
t_{xoradj}	34	XOR Adjacent Path Delay[3]	–	8.1	–	11.1	ns
t_{gbp}	35	GLB Register Bypass Delay	–	0.1	–	0.1	ns
t_{gsu}	36	GLB Register Setup Time before Clock	1.8	–	2.4	–	ns
t_{gh}	37	GLB Register Hold Time after Clock	6.0	–	8.2	–	ns
t_{gco}	38	GLB Register Clock to Output Delay	–	1.8	–	2.2	ns
t_{gro}	39	GLB Register Reset to Output Delay	–	2.8	–	3.8	ns
t_{ptre}	40	GLB Product Term Reset to Register Delay	–	10.5	–	14.2	ns
t_{ptoe}	41	GLB Product Term Output Enable to I/O Cell Delay	–	5.4	–	7.3	ns
t_{ptck}	42	GLB Product Term Clock Delay	3.2	6.3	4.3	8.5	ns
ORP							
t_{orp}	43	ORP Delay	–	2.7	–	3.6	ns
t_{orpbp}	44	ORP Bypass Delay	–	1.2	–	1.6	ns

Table 2 - 0036A/6192

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Internal Timing Parameters: Programmable Logic Module[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	45	Output Buffer Delay	–	2.4	–	3.3	ns
t_{obs}	46	Output Buffer Delay, Slow Slew	–	12.4	–	13.3	ns
t_{oen}	47	I/O Cell OE to Output Enabled	–	7.2	–	9.8	ns
t_{odis}	48	I/O Cell OE to Output Disabled	–	7.2	–	9.8	ns
Clocks							
$t_{gy0/1/2}$	49	Clock Delay, Y0 or Y1 or Y2 to Global GLB Clock Line	3.6	3.6	4.9	4.9	ns
$t_{ioy3/4}$	50	Clock Delay, Y3 or Y4 to I/O Cell Global Clock Line	1.2	5.2	1.6	7.0	ns
Global Reset							
t_{gr}	51	Global Reset to GLB and I/O Registers	–	7.1	–	9.6	ns

Table 2 - 0037A/3256

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

External Switching Characteristics: FIFO Module[1]

Over Recommended Operating Conditions

PARAMETER	TEST[2] COND.	#[1]	DESCRIPTION	-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	
ts	—	52	Shift Frequency	—	50	—	33.3	MHz
trc	A	53	Read Cycle Time	20	—	30	—	ns
ta	A	54	Read Pulse to Data Access Time	—	12	—	20	ns
trr	A	55	Read Recovery Time	5	—	10	—	ns
trpw	—	56	Read Pulse Width	15	—	20	—	ns
tdv	A	57	Data Held Valid from Read Pulse Inactive	3	—	3	—	ns
twc	—	58	Write Cycle Time	20	—	30	—	ns
twpw	—	59	Write Pulse Width	15	—	20	—	ns
twr	—	60	Write Recovery Time	5	—	10	—	ns
tds	—	61	Data Setup Time	13	—	18	—	ns
tdh	—	62	Data Hold Time	0	—	0	—	ns
trsc	—	63	Reset Cycle Time	20	—	30	—	ns
trs	—	64	Reset Pulse Width	15	—	20	—	ns
trsr	A	65	Reset Recovery Time	5	—	10	—	ns
tefl	A	66	Reset Active to Empty Flag Active	—	20	—	25	ns
tffh	A	67	Reset Active to Full Flag Inactive	—	20	—	25	ns
talel	A	68	Reset Active to Almost Empty Flag Active	—	25	—	30	ns
talfh	A	69	Reset Active to Almost Full Flag Inactive	—	25	—	30	ns
trff	A	70	Read Inactive to Full Flag Inactive	—	20	—	25	ns
traf	A	71	Read Inactive to Almost Full Flag Inactive	—	25	—	30	ns
trhz	A	72	Read Inactive to Data Out Disable	—	15	—	20	ns
trlz	A	73	Read Active to Data Out Enable	0	—	0	—	ns
trss	A	74	Read or Write Inactive to Reset Inactive	15	—	20	—	ns
trae	A	75	Read Active to Almost Empty Flag Active	—	25	—	30	ns
tref	A	76	Read Active to Empty Active	—	20	—	25	ns
trpe	A	77	Read Pulse Width after Empty Flag Inactive	15	—	20	—	ns
twff	—	78	Write Active to Full Flag Active	—	20	—	25	ns
twaf	—	79	Write Active to Almost Full Flag Active	—	25	—	30	ns
twae	—	80	Write Inactive to Almost Empty Flag Inactive	—	25	—	30	ns
twef	—	81	Write Inactive to Empty Flag Inactive	—	20	—	25	ns
twpf	—	82	Write Pulse Width after Full Flag Inactive	15	—	20	—	ns

1. Refer to Timing Model in this data sheet for further details.
2. Reference Switching Test Conditions section.

Internal TIming Parameters: FIFO Module[1]

Over Recommended Operating Conditions

PARAMETER	#	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
ts	83	Shift Frequency	—	50	—	28.5	MHz
trc	84	Read Cycle Time	25	—	35	—	ns
terdv	85	End Read Pulse to Next Data Valid	—	12	—	20	ns
trr	86	Read Recovery Time	10	—	15	—	ns
trpw	87	Read Pulse Width	15	—	20	—	ns
twc	88	Write Cycle Time	20	—	30	—	ns
twpw	89	Write Pulse Width	15	—	20	—	ns
twr	90	Write Recovery Time	5	—	10	—	ns
tds	91	Data Setup Time	18	—	23	—	ns
tdh	92	Data Hold Time	0	—	0	—	ns
trsc	93	Reset Cycle Time	25	—	30	—	ns
trs	94	Reset Pulse Width	15	—	20	—	ns
trsr	95	Reset Recovery Time	10	—	10	—	ns
tefl	96	Reset Active to Empty Flag Active	—	15	—	18	ns
tffh	97	Reset Active to Full Flag Inactive	—	15	—	18	ns
talel	98	Reset Active to Almost Empty Flag Active	—	20	—	23	ns
talfl	99	Reset Active to Almost Full Flag Inactive	—	20	—	23	ns
trff	100	Read Inactive to Full Flag Inactive	—	15	—	18	ns
traf	101	Read Inactive to Almost Full Flag Inactive	—	20	—	23	ns
trss	102	Read or Write Inactive to Reset Inactive	15	—	20	—	ns
trae	103	Read Active to Almost Empty Flag Active	—	20	—	23	ns
tref	104	Read Active to Empty Active	—	15	—	18	ns
trpe	105	Read Pulse Width after Empty Flag Inactive	15	—	20	—	ns
twff	106	Write Active to Full Flag Active	—	15	—	18	ns
twaf	107	Write Active to Almost Full Flag Active	—	20	—	23	ns
twae	108	Write Inactive to Almost Empty Flag Inactive	—	20	—	23	ns
twef	109	Write Inactive to Empty Flag Inactive	—	15	—	18	ns
twpf	110	Write Pulse Width after Full Flag Inactive	15	—	20	—	ns
Generic Path							
tmemmio	111	Delay Added for Memory Out to MIO	—	1	—	2	ns
fmemgrp	112	Delay Added for Memory Out to GRP	—	1	—	2	ns
tmiomem	113	Delay Added for MIO to Memory	—	4	—	5	ns
tgrpmem	114	Delay Added for GRP to Memory	—	4	—	5	ns

1. Internal Timing Parameters are not tested and are for reference only.

External Switching Characteristics: RAM Module (Port A Only)[1]

Over Recommended Operating Conditions

PARAMETER	TEST[2] COND.	#[1]	DESCRIPTION	-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	
Read Cycle								
trc	—	115	Read Cycle Time	20	—	25	—	ns
taa	A	116	Address Access Time	—	20	—	25	ns
tacs	A	117	Chip Select Access Time	—	15	—	20	ns
taoe	A	118	OE Pin Access Time	—	12	—	15	ns
toh	A	119	Output Hold from Address Change	2	—	2	—	ns
toeen	B	120	OE Pin to Data Output Enable	0	—	0	—	ns
toedis	C	121	OE Pin to Data Output Disable	—	12	—	15	ns
tcsen	B	122	Chip Select to Data Output Enable	0	—	0	—	ns
tcsdis	C	123	Chip Select to Data Output Disable	—	15	—	20	ns
Write Cycle								
twc	—	124	Write Cycle Time	20	—	25	—	ns
taw	—	125	Address Valid to Write End	15	—	20	—	ns
tas	—	126	Address Setup to Write Start	0	—	0	—	ns
tewcs (tcw)	—	127	Chip Select to End of Write	15	—	20	—	ns
twp	—	128	Write Pulse Width	15	—	20	—	ns
twr	—	129	Write Recovery Time	0	—	0	—	ns
tdw	—	130	Data Valid to Write End	15	—	20	—	ns
tdh	—	131	Data Hold from Write End	0	—	0	—	ns
tween	—	132	RW High to Data Output Enable	0	—	0	—	
twedis	—	133	RW Low to Data Output Disable	—	15	—	20	ns
Busy Timing								
tba	—	134	Busy from Address Match	—	15	—	20	ns
tnba	—	135	Not Busy from Address Mismatch	—	15	—	20	ns
tbcs	—	136	Busy from Chip Select Active	—	15	—	20	ns
tnbcs	—	137	Not Busy from Chip Select Inactive	—	15	—	20	ns
taps	—	138	Arbitration Priority Setup Time	5	—	8	—	ns
tnbd	—	139	Not Busy to Read Data Valid	—	20	—	30	ns

1. Refer to Timing Model in this data sheet for further details.
2. Reference Switching Test Conditions section.

Internal TIming Parameters: RAM Module (Port B Only)

Over Recommended Operating Conditions

PARAMETER	#	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Read Cycle							
trc	140	Read Cycle Time	25	—	30	—	ns
taa	141	Address Access Time	—	20	—	28	ns
toh	142	Output Hold from Address Change	0	—	0	—	ns
Write Cycle							
twc	143	Write Cycle Time	25	—	30	—	ns
taw	144	Address Valid to Write End	17	—	22	—	ns
tas	145	Address Setup to Write Start	0	—	0	—	ns
tewcs (tcw)	146	Chip Select to End of Write	17	—	22	—	ns
twp	147	Write Pulse Width	15	—	20	—	ns
twr	148	Write Recovery Time	0	—	0	—	ns
tdw	149	Data Valid to Write End	17	—	22	—	ns
tdh	150	Data Hold from Write End	0	—	0	—	ns
Busy Timing							
tba	151	Busy from Address Match	—	10	—	13	ns
tnba	152	Not Busy from Address Mismatch	—	10	—	13	ns
tbcs	153	Busy from Chip Select Active	—	10	—	13	ns
tnbcs	154	Not Busy from Chip Select Inactive	—	10	—	13	ns
taps	155	Arbitration Priority Setup Time	5	—	8	—	ns
tnbd	156	Not Busy to Read Data Valid	—	20	—	30	ns
Generic Path							
tmemmio	157	Delay Added for Memory Out to MIO	—	1	—	2	ns
fmemgrp	158	Delay Added for Memory Out to GRP	—	1	—	2	ns
tmiomem	159	Delay Added for MIO to Memory	—	4	—	5	ns
tgrpmem	160	Delay Added for GRP to Memory	—	4	—	5	ns

External Switching Characteristics: Register/Counter Module[1]

Over Recommended Operating Conditions

PARAMETER	TEST[2] COND.	#[1]	DESCRIPTION	-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	
tregco	A	161	Clock to Parallel Data Out	—	15	—	20	ns
tregsu	—	162	Parallel Data In Setup to Clock	8	—	12	—	ns
tregh	—	163	Parallel Data In Hold from Clock	0	—	0	—	ns
tgrdo	A	164	Global Reset to Data Out	—	20	—	25	ns
tgrpw	—	165	Global Reset Pulse Duration	12	—	15	—	ns
trgen	B	166	Global OE Output Enable	—	15	—	20	ns
trgdis	C	167	Global OE Output Disable	—	15	—	20	ns
tclkh	—	168	Clock High Period	4	—	5	—	ns
tclkl	—	169	Clock Low Period	4	—	5	—	ns
Shift Register								
tsft	—	170	Clock Frequency, Max. Shift Rate	125	—	100	—	MHz
tsoutco	—	171	Clock to SOUT	—	17	—	20	ns
tsinsu	—	172	SIN Setup to Clock	8	—	12	—	ns
tsinh	—	173	SIN Hold from Clock	0	—	0	—	ns
Counter/Timer								
fmax	—	174	16-bit Counter	125	—	100	—	MHz
fmax	—	175	16-bit Timer	125	—	100	—	MHz
tcaco	A	176	Clock to Carry Out/TC (16-bit)	—	18	—	22	ns

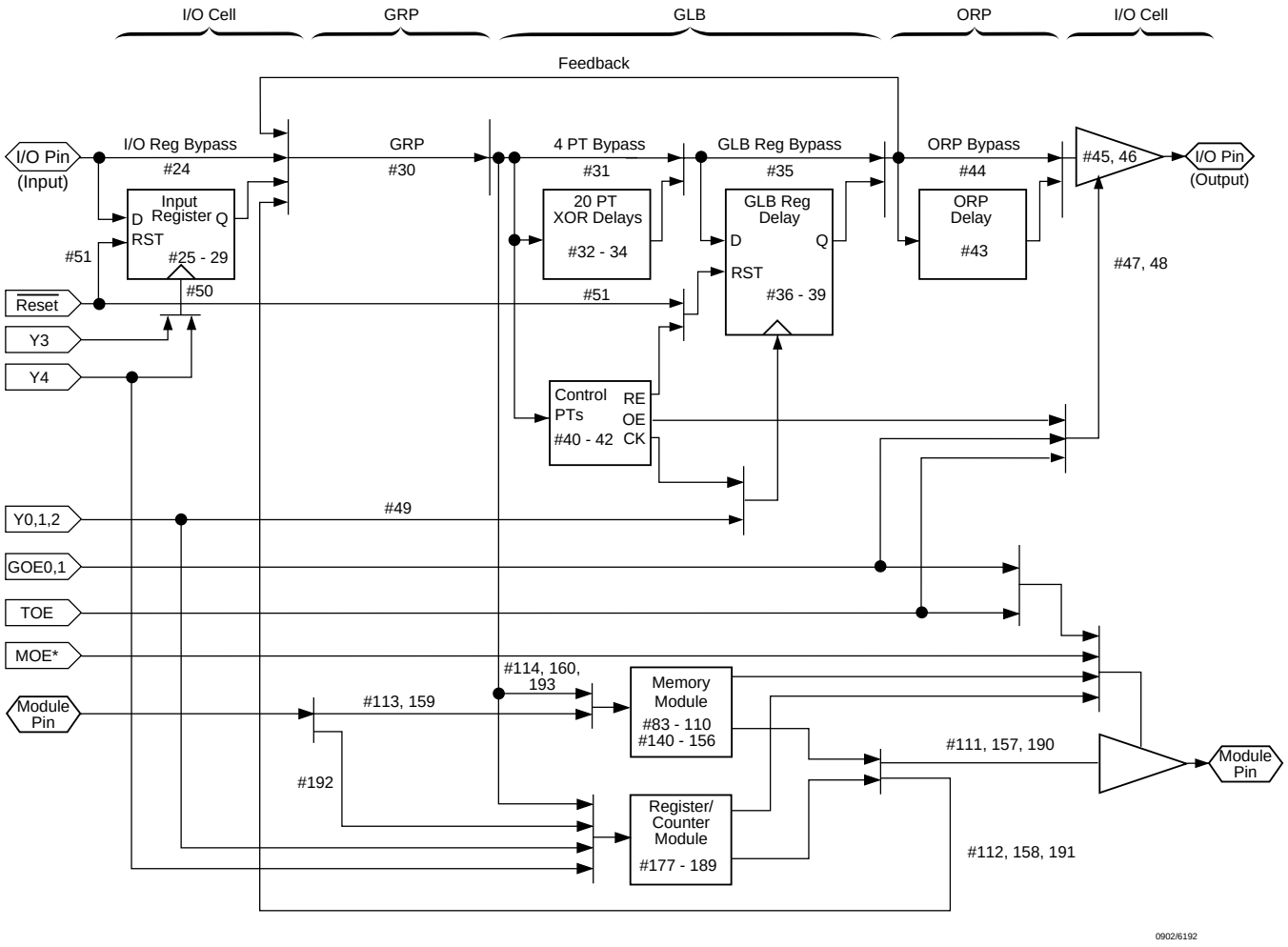
1. Refer to Timing Model in this data sheet for further details.
2. Reference Switching Test Conditions section.

Internal TIming Parameters: Register/Counter Module

Over Recommended Operating Conditions

PARAMETER	#	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Generic Timings							
tsco	177	Select to Parallel Data Out	—	14.6	—	17.6	ns
tssu	178	Select Setup to Clock	7.6	—	11.9	—	ns
tsh	179	Select Hold to Clock	0	—	0	—	ns
tensu	180	Enable/Preload/Preset Setup to Clock	7.6	—	11.9	—	ns
tenh	181	Enable/Preload/Preset Hold from Clock	0	—	0	—	ns
tptrdo	182	Product Term Reset to Data Out	—	11.9	—	13.4	ns
tptrpw	183	Product Term Reset Pulse Duration	12	—	15	—	ns
Shift Register							
tsensu	184	ShiftEn Setup to Clock	7.6	—	11.9	—	ns
tsenh	185	ShiftEn Hold to Clock	0	—	0	—	ns
Counter/Timer							
tcaco	186	Clock to Carry Out/TC (16-bit)	—	13.4	—	15.1	ns
tcichsu	187	Carry In/Count Hold Setup to Clock	7.6	—	11.9	—	ns
tcichh	188	Carry In/Count Hold Hold to Clock	0	—	0	—	ns
tcichco	189	Carry In/Count Hold to Carry Out/TC					ns
Generic Path							
trcmio	190	Delay Added for Reg./Counter Out to MIO	—	1	—	2	ns
frcgrp	191	Delay Added for Reg./Counter Out to GRP	—	1	—	2	ns
tmiorc	192	Delay Added for MIO to Reg./Counter	—	4	—	5	ns
tgrprc	193	Delay Added for GRP to Reg./Counter	—	4	—	5	ns

ispLSI 6192 Timing Model

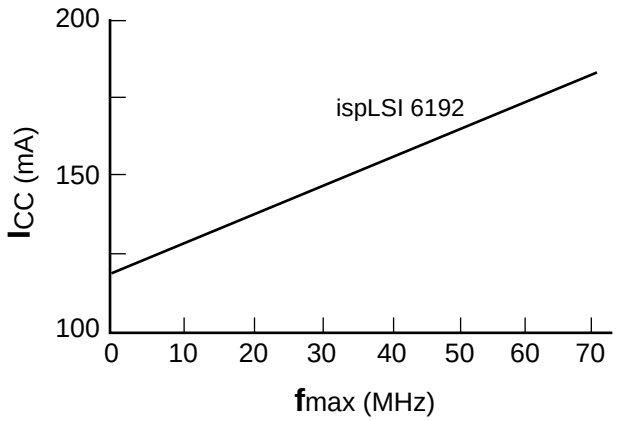


* = Dedicated Module Output Enable

Power Consumption

Power Consumption in the ispLSI 6192 device depends on two primary factors: the speed at which the device is operating and the number of product terms used. Figure 51 shows the relationship between power and operating speed.

Figure 51. Typical Device Power Consumption vs fmax



Notes: Typical Current at 5V, 25° C

0127A/6192

Pin Description: Programmable Logic Module

NAME	MQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 4 I/O 5 - I/O 9 I/O 10 - I/O 14 I/O 15 - I/O 19 I/O 20 - I/O 24 I/O 25 - I/O 29 I/O 30 - I/O 34 I/O 35 - I/O 39 I/O 40 - I/O 44 I/O 45 - I/O 49 I/O 50 - I/O 54 I/O 55 - I/O 59 I/O 60 - I/O 64 I/O 65 - I/O 69 I/O 70 - I/O 74 I/O 75 - I/O 79 I/O 80 - I/O 84 I/O 85 - I/O 89 I/O 90 - I/O 94 I/O 95	32, 33, 34, 36, 37, 38, 40, 41, 42, 43, 44, 45, 47, 48, 49, 51, 52, 53, 54, 55, 56, 58, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 79, 80, 82, 83, 84, 85, 86, 87, 88, 89, 90, 92, 94, 95, 96, 97, 169, 170, 171, 172, 173, 175, 176, 177, 179, 181, 182, 183, 184, 186, 187, 188, 189, 190, 192, 193, 194, 196, 198, 199, 200, 201, 203, 204, 205, 206, 207, 1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 15, 16, 17, 18, 19, 20	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0 and GOE1	75 and 73	Input - Global Output Enable input pins.
TOE	72	Input - Test Output Enable pin. TOE tristates all I/O pins when a logic low is driven
$\overline{\text{RESET}}$	25	Input - Active Low Global Reset pin which resets all of the GLB and I/O registers in the device.
Y0, Y1 and Y2	22, 24, 78	Input - Dedicated Clock pins - These clock inputs are connected to one of the clock inputs of all the GLBs on the device.
Y3 and Y4	77, 76	Input - Dedicated Clock pins - These clock inputs are connected to one of the clock inputs of all the I/O cells in the device.
$\overline{\text{ispEN}}$/BSCAN [2]	26	Input - Boundary Scan Enable. Dedicated in-system programming Enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI/TDI [2]	27	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is low, this is the Serial Data In pin to load programming data into the device. When $\overline{\text{ispEN}}$ is high, this pin is used as the Test Data In for the Boundary Scan operation
SCLK/TCLK [2]	28	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is low, this is the Serial Clock input pin for device programming. When $\overline{\text{ispEN}}$ is high, this is the Test Clock pin used for the Boundary Scan operation.
MODE/TMS [2]	29	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is low, this is the Mode pin to control the isp state machine operations. When $\overline{\text{ispEN}}$ is high, this is the Test Mode Select input for the Boundary Scan operation.
$\overline{\text{TRST}}$/NC [1, 2]	71	Input - Test Reset, active low to reset the Boundary Scan State Machine.
SDO/TDO [2]	136	Output - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it is the Serial Data Out pin used to read the isp data. When $\overline{\text{ispEN}}$ is high it functions as Test Data Out pin for the Boundary Scan operation.
GND	11, 23, 35, 46, 59, 70, 81, 93, 104, 116, 128, 141, 152, 158, 164, 174 180, 185, 191, 197, 202, 208	Ground (GND)
Vcc	13, 21, 31, 39, 57, 74, 91, 118 126, 137, 145, 162, 178, 195	Vcc

Table 2 - 0002/6192

1. NC pins are not to be connected to any active signal, Vcc or GND.
2. Pins have dual function capability.

Pin Description: Register/Counter Module

NAME	MQFP PIN NUMBERS	DESCRIPTION
DI/O 0 - DI/O 4 (RC) DI/O 5 - DI/O 9 (RC) DI/O 10 - DI/O 14 (RC) DI/O 15 (RC)	139, 140, 142, 143, 144, 146, 147, 148, 149, 150, 151, 153, 154, 156, 157, 159	Input/Output Pins - These are the external data pins used by the Register/Counter module. They are tristated when the $\overline{OE}$(RC) pin is inactive (high). They can be used as general-purpose logic inputs if the Register/Counter module does not use the external data interface.
TC/CO0 - TC/CO3	165, 166, 167, 168,	Output Pins - Terminal count (timers) or Carry Out (counters) outputs. Used only in timer or counter modes for Register/Counter module.
$\overline{ENABLE}$	163	Input Pin - Active low Enable pin used to write data from DI/O(RC) pins to selected bank of Register/Counter.
SIN	160	Input Pin - Serial data input to Bit 15 of Bank 0. Used only in shift register configuration.
SOUT	161	Output Pin - Serial data output from Bit 0 of Bank 7. Used only in shift register configurations.
$\overline{OE}$ (RC)	138	Input Pin - Register/Counter Output Enable pin. Enables the DI/O(RC) pins when active low.

Table 2 - 0002/6192 Reg/Ctr

Pin Description: FIFO Module

NAME	MQFP PIN NUMBERS	DESCRIPTION
DI/O 0 - DI/O 4 (FIFO) DI/O 5 - DI/O 9 (FIFO) DI/O 10 - DI/O 14 (FIFO) DI/O 15 - DI/O 17 (FIFO)	113, 114, 115, 117, 119, 120, 121, 122, 123, 124, 125, 127, 129, 130, 131, 132, 133, 134	Input/Output Pins - These are the external data I/O pins used by the FIFO. For the 512 x 9 FIFO configuration, the higher 9 bits are used. These pins tristate when $\overline{RD}$ goes inactive (high).
$\overline{RST}$	99	Input Pin - Active low $\overline{Reset}$ input used to reset the internal read and write pointers to the first location of the RAM array.
$\overline{RD}$ or $\overline{WR}$	110	Input Pin - Active Low. This is a dual function pin. When data is read from the FIFO to the external pins it acts as a read enable pin ($\overline{RD}$) for Port B to A configuration. When data is written to the FIFO from the external pins it acts as a write control pin ($\overline{WR}$) for Port A to B configuration. When $\overline{RD}$ is low, data is read from the RAM array sequentially. When $\overline{WR}$ is low, data is written to the RAM array
$\overline{FF}$	101	Output Pin - Active low Full Flag pin to indicate that the FIFO is full and further write operation is inhibited.
$\overline{EF}$	100	Output Pin - Active low Empty Flag pin to indicate the FIFO is empty and further read operation is inhibited.
$\overline{ALF}$	103	Output Pin - Active low Almost Full Flag. It can be programmed to activate at any location. Can be used as a general-purpose logic input if not used for external FIFO interfacing.
$\overline{ALE}$	102	Output Pin - Active low Almost Empty Flag. It can be programmed to activate at any location. It has to be below the Almost Full Flag. Can be used as a general-purpose logic input if not used for external FIFO interfacing.

Table 2 - 0002/6192FF

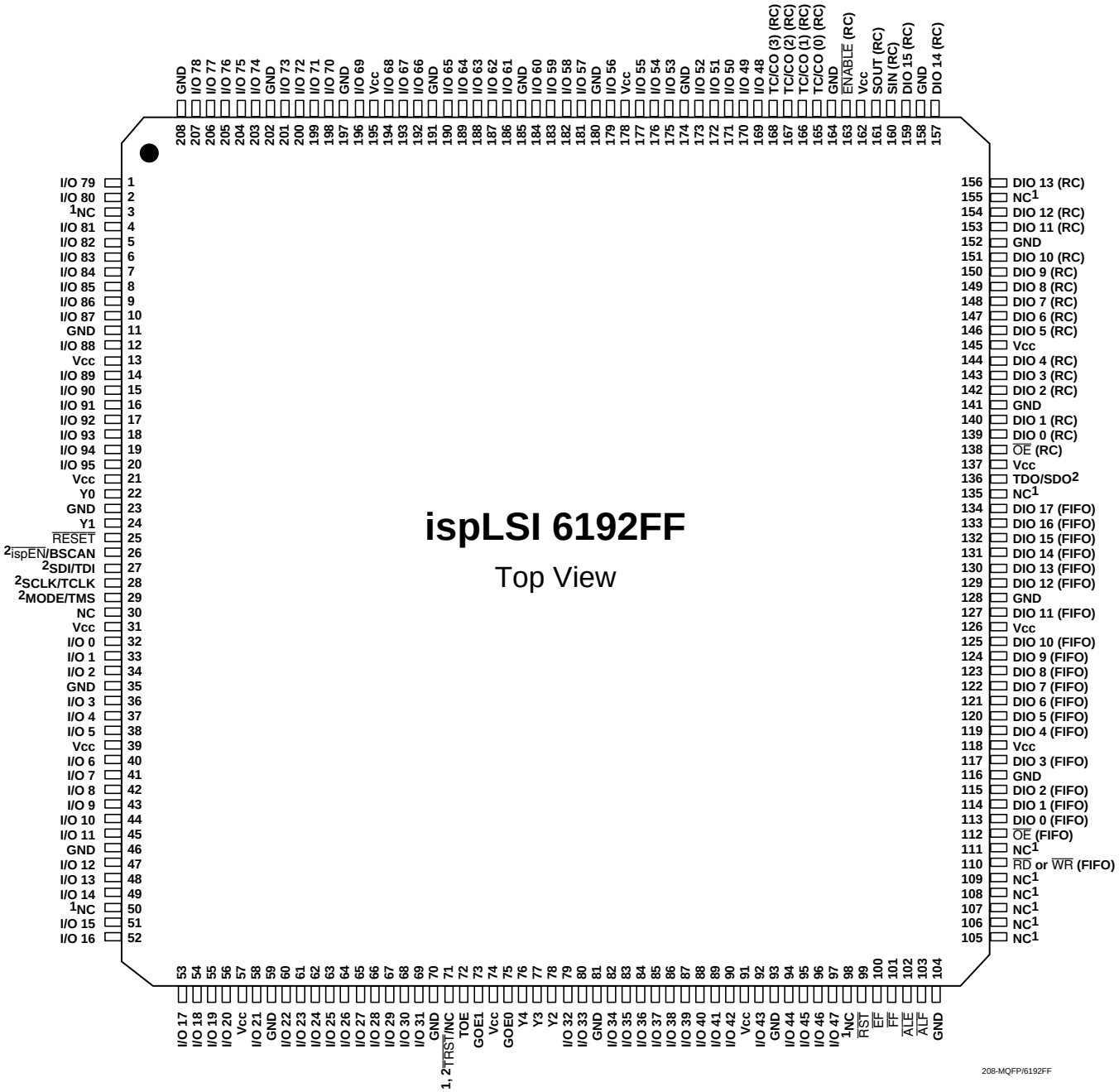
Pin Description: Dual Port and Single Port RAM Module

NAME	MQFP PIN NUMBERS	DESCRIPTION
DI/O 0 - DI/O 4 (RAM) DI/O 5 - DI/O 9 (RAM) DI/O 10 - DI/O 14 (RAM) DI/O 15 - DI/O 17 (RAM)	113, 114, 115, 117, 119, 120, 121, 122, 123, 124, 125, 127, 129, 130, 131, 132, 133, 134	Input/Output Pins - These are the data I/O pins used by the RAM. For the 512x9 RAM configuration, the high order 9 bits are used. These pins tristate when $\overline{OE}$(RAM) or $\overline{CS}$(RAM) goes inactive. In addition, if the RWH and/or RWL pin are in the write state (low), the appropriate byte(s) of DI/O will tristate. DI/O 0-8 can also be used for general-purpose logic inputs if not needed for RAM interfacing from the I/O cellls (Single Port RAM only).
A0 - A3 A4 - A7	99, 100, 101, 102, 103, 105, 106, 108	Input Pins - Address inputs to access locations in the RAM array. A3 - A7 can also be used as general-purpose logic inputs if not needed for RAM interfacing from the I/O cells.
A8/RWH	109	Input Pin - Used as read/write control line for upper byte RAM when in byte write mode. The RAM performs a read operation when RWH is high and write operation when RWH is low. Used as 9th address bit when RAM is configured as 512x9. Can be used as a general-pupose logic input if not needed for external RAM interfacing.
RWL	110	Input Pin - Controls the read/write operation of the memory module. When operating in the byte write mode, RWL controls the read/write of the lower order byte while RWH controls the read/write operation of the higher order byte.
$\overline{CS}$	111	Input Pin - Chip select. Must be active low to perform read or write from external RAM interface. Can be used as a general-pupose logic input if not needed for external RAM interfacing.
$\overline{OE}$	112	Input Pin - RAM output enable. Controls DI/O(RAM) pin tristating. Pins tristate when $\overline{OE}$ is inactive (high). Outputs enabled when $\overline{OE}$ active (low).
$\overline{BusyA}$ (Dual Port RAM Only)	98	Output Pin - Active low busy pin indicating that Port A has lost the arbitration when both Port A and Port B are attempting to access the same RAM location simultaneously.

Table 2 - 0002/6192DP/SP

Pin Configuration: ispLSI 6192FF

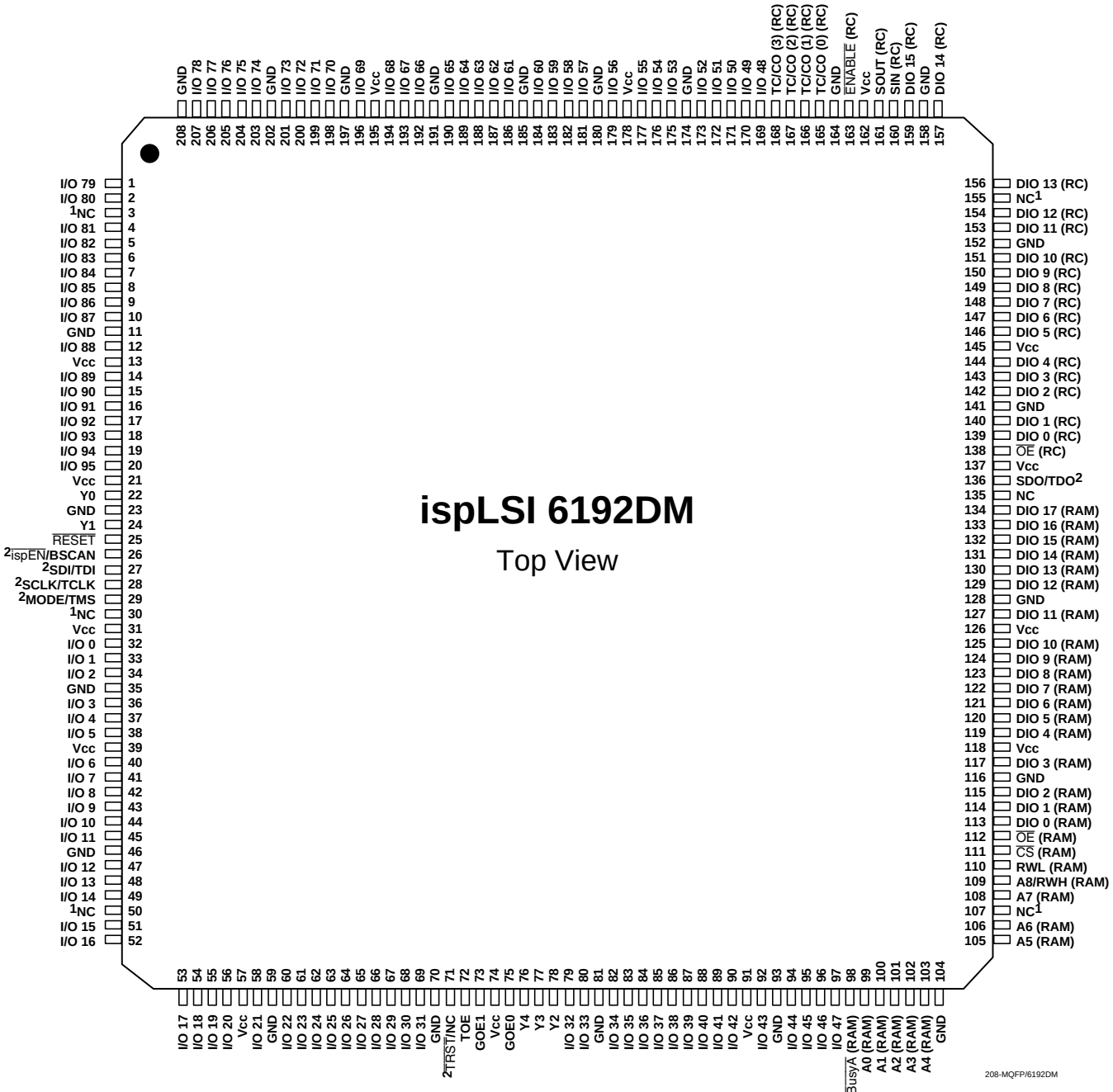
ispLSI 6192FF 208-Pin MQFP Pinout Diagram



1. NC pins are not to be connected to any active signal, Vcc or GND.
2. Pins have dual function capability.

Pin Configuration: ispLSI 6192DM

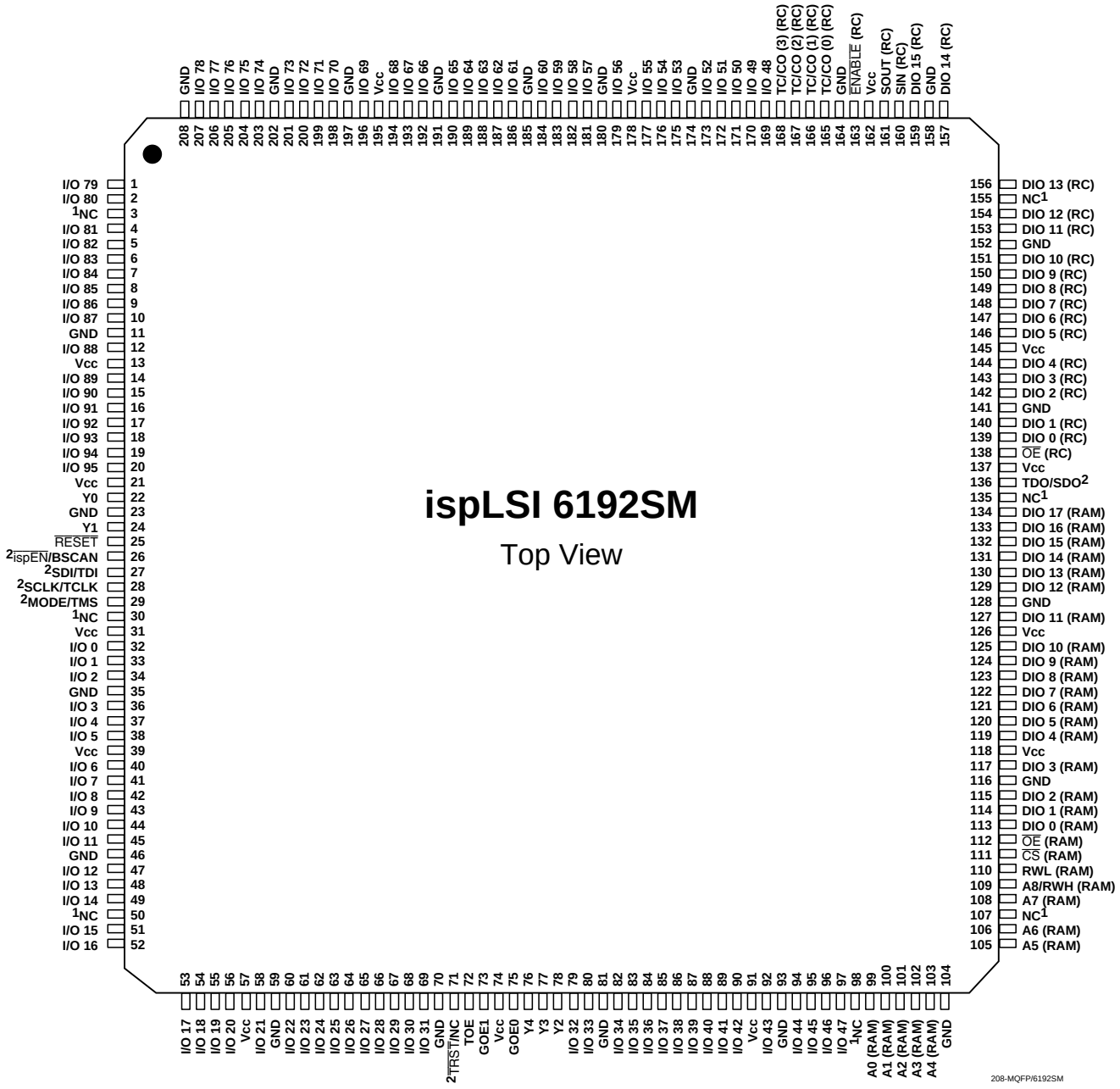
ispLSI 6192DM 208-Pin MQFP Pinout Diagram



1. NC pins are not to be connected to any active signal, Vcc or GND.
2. Pins have dual function capability.

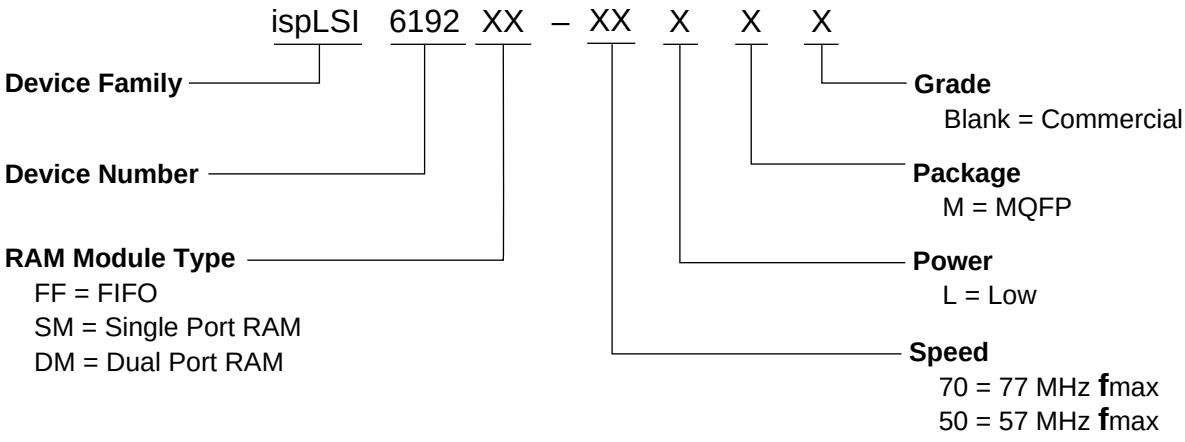
Pin Configuration: ispLSI 6192SM

ispLSI 6192SM 208-Pin MQFP Pinout Diagram



1. NC pins are not to be connected to any active signal, Vcc or GND.
2. Pins have dual function capability.

Part Number Description



0212/6192

Ordering Information

RAM Module	fmax	tpd	Ordering Number	Package
FIFO	77	15	ispLSI 6192FF-70LM	208-Pin MQFP
	57	20	ispLSI 6192FF-50LM	208-Pin MQFP
Single Port RAM	77	15	ispLSI 6192SM-70LM	208-Pin MQFP
	57	20	ispLSI 6192SM-50LM	208-Pin MQFP
Dual Port RAM	77	15	ispLSI 6192DM-70LM	208-Pin MQFP
	57	20	ispLSI 6192DM-50LM	208-Pin MQFP