

# MN3711CFP

## 4.5mm (1/4 inch) 510H CCD Area Image Sensor

### ■ Overview

The MN3711CFP is a 4.5mm (1/4 inch) Interline Transfer CCD (IT-CCD) solid state image sensor device.

This device uses photodiodes in the optoelectric conversion section and CCDs for signal read out. The electronic shutter function has made possible an exposure time of 1/10000 seconds. Further, this device has the features of high sensitivity, low noise, broad dynamic range, and low smear.

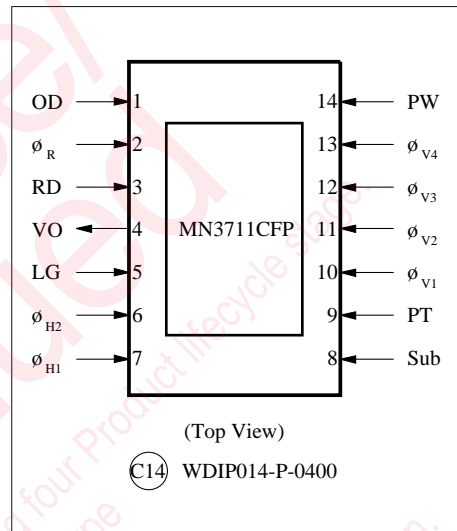
This device has a total of 270K pixels (542 horizontal × 494 vertical) and provides stable and clear images with a resolution of 330 horizontal TV-lines and 350 vertical TV-lines.

Type No.	Size	System	Color or B/W
MN3711CFP	4.5mm (1/4 inch)	NTSC	Color

### ■ Features

- Total number of pixels: 542 (horizontal) × 494 (vertical)
- High sensitivity
- Low noise
- Broad dynamic range
- Low smear
- Low image lag
- Electronic shutter function present
- No image distortion
- Small size enables design of compact equipment
- High reliability
- 14 Pin DIL ceramic package

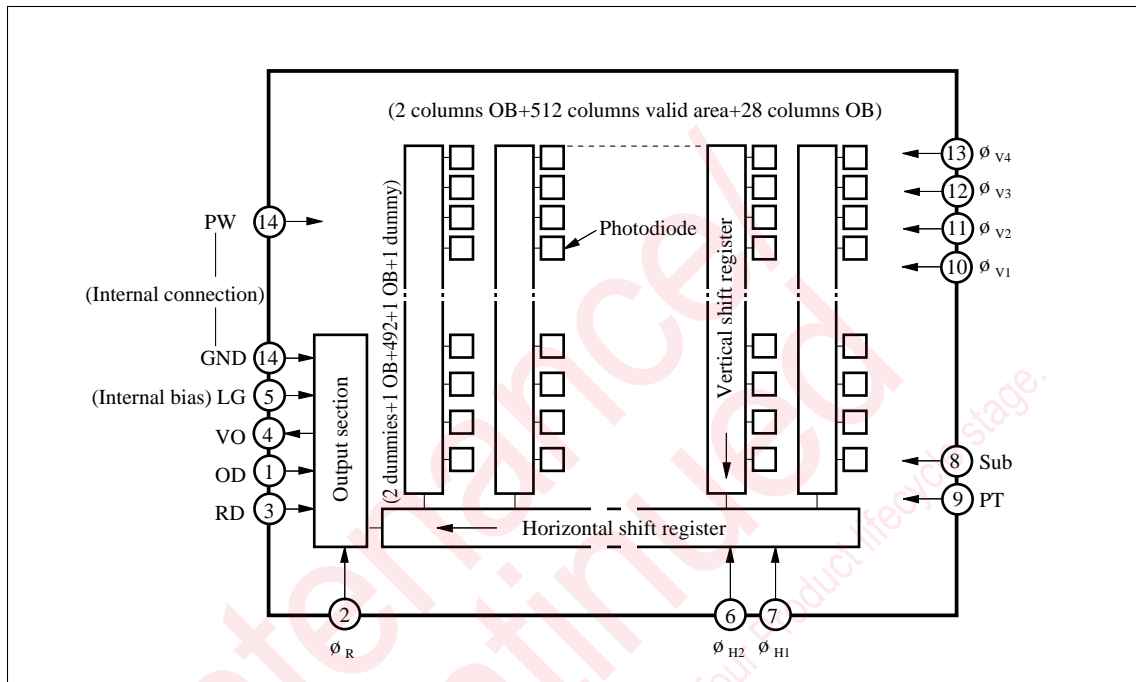
### ■ Pin Assignments



### ■ Applications

- Compact lightweight camcoders
- Cameras for surveillance, measurement, and medical use

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Descriptions	Pin No.	Symbol	Descriptions
1	OD	Output drain	8	Sub	Substrate
2	$\phi_R$	Reset pulse	9	PT	P-well for protection circuit
3	RD	Reset drain	10	$\phi_{V1}$	Vertical shift register clock pulse (1)
4	VO	Video output	11	$\phi_{V2}$	Vertical shift register clock pulse (2)
5	LG	Output load transistor gate	12	$\phi_{V3}$	Vertical shift register clock pulse (3)
6	$\phi_{H2}$	Horizontal register clock pulse (2)	13	$\phi_{V4}$	Vertical shift register clock pulse (4)
7	$\phi_{H1}$	Horizontal register clock pulse (1)	14	PW	P-well

■ Absolute Maximum Ratings and Operating Conditions

Parameter	Symbol	Rating <sup>Note 2)</sup>		Operating condition <sup>Note 1)</sup>			Unit	
		min	max	min	typ	max		
Reset drain voltage	V <sub>RD</sub>	-0.2	18	14.5	15.0	15.5	V	
Output drain voltage	V <sub>OD</sub>	-0.2	18	14.5	15.0	15.5	V	
Output load transistor gate voltage <sup>Note 3)</sup>	V <sub>LG</sub>	(Supplied internally)					V	
Protection P well voltage	V <sub>PT</sub>	-10.0	0.2	ϕ <sub>V(L)</sub> -1.2	ϕ <sub>V(L)</sub> -1.0	ϕ <sub>V(L)</sub> -0.7	V	
P well voltage	V <sub>PW</sub>	Reference voltage		—	0	—	V	
Reset pulse voltage	H-L	V <sub>ϕR(H-L)</sub> <sup>*1</sup>	—	18	4.7	5.0	5.3	V
	Bias	V <sub>ϕR(Bias)</sub> <sup>*1</sup>	-0.2	—	0	Adjust	5.0	V
Horizontal register clock pulse voltage 1		V <sub>ϕH1(H)</sub>	—	18	4.7	5.0	5.3	V
		V <sub>ϕH1(L)</sub>	-0.2	—	0	0	0	V
Horizontal register clock pulse voltage 2		V <sub>ϕH2(H)</sub>	—	18	4.7	5.0	5.3	V
		V <sub>ϕH2(L)</sub>	-0.2	—	0	0	0	V
Vertical shift register clock pulse voltage 1		V <sub>ϕV1(H)</sub>	—	18	14.5	15.0	15.5	V
		V <sub>ϕV1(M)</sub>	—	—	-0.2	0	0.2	V
		V <sub>ϕV1(L)</sub>	-9	—	-7.3	-7.0	-6.7	V
Vertical shift register clock pulse voltage 2		V <sub>ϕV2(M)</sub>	—	15	0.8	1.0	1.2	V
		V <sub>ϕV2(L)</sub>	-9	—	-7.3	-7.0	-6.7	V
Vertical shift register clock pulse voltage 3		V <sub>ϕV3(H)</sub>	—	18	14.5	15.0	15.5	V
		V <sub>ϕV3(M)</sub>	—	—	-0.2	0	0.2	V
		V <sub>ϕV3(L)</sub>	-9	—	-7.3	-7.0	-6.7	V
Vertical shift register clock pulse voltage 4		V <sub>ϕV4(M)</sub>	—	15	0.8	1.0	1.2	V
		V <sub>ϕV4(L)</sub>	-9	—	-7.3	-7.0	-6.7	V
Substrate voltage		V <sub>Sub</sub> <sup>*2</sup>	-0.2	45	3.0	Adjust	14.5	V
		ϕ V <sub>Sub</sub> <sup>*2</sup>	—	—	24.5	25.0	25.5	V
Operating temperature	T <sub>opr</sub>	-10	70	—	25.0	—	°C	
Storage temperature	T <sub>stg</sub>	-30	80	—	—	—	°C	

Note 1) The initial setting of V<sub>Sub</sub> shall be 8.0V and shall be adjusted to the minimum voltage at which no blooming is caused at a light input of 100 times the standard value. The standard light input is the one when the exposure is done at an aperture of F/8 using a light source of 2856K and 1050nt, and placing a color temperature conversion filter LB-40 (Hoya) and an IR cutting filter CAW-500 (t=2.5mm) in the light path. (F/1.4 20.5nt)

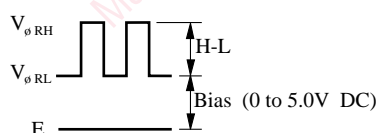
If any FPN picture is present at the minimum operating condition of V<sub>Sub</sub>, it should be adjusted to the minimum voltage at which there is no FPN picture.

When any overflow charge is present, it should be adjusted to the minimum voltage at which the overflow charge is eliminated in the range under 13.5V.

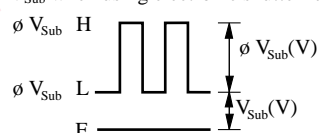
Note 2) Absolute maximum ratings:  
 $-0.2 < V_{Sub} - V_{PT} < +55$  (V)  
 $-0.2 < V_{ϕV} - V_{PT} < +24.5$  (V)

Note 3) The LG pins should each be grounded via a capacitor of 0.047μF or more.

\*1



\*2 V<sub>Sub</sub> when using electronic shutter function

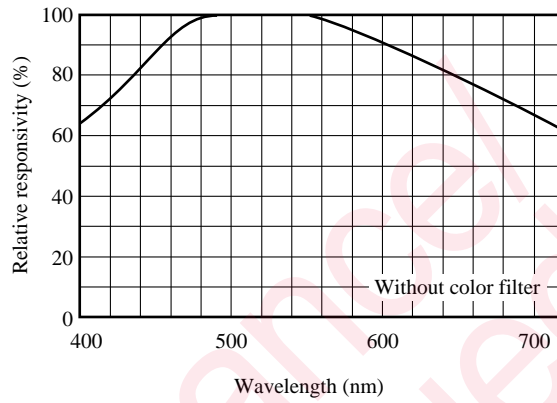


■ Optical Characteristics

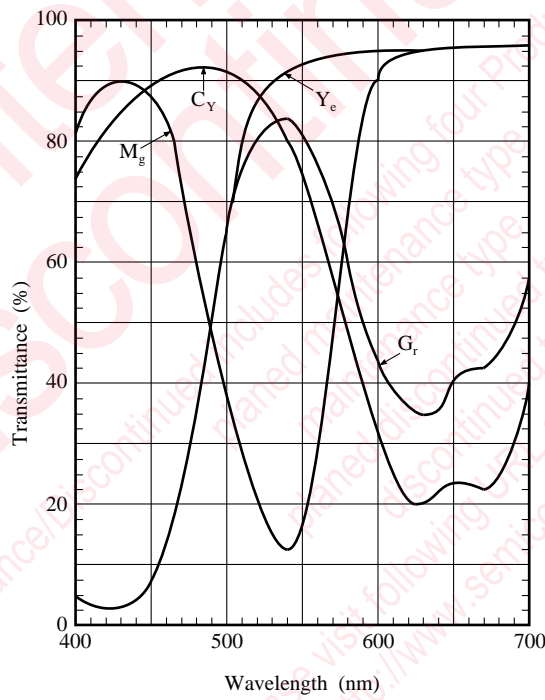
Type No.	Color or B/W	Valid pixels		S/N typ. (dB)	Saturation output typ. (mV)	Sensitivity F8 typ. (mV)	Vertical smear Sm typ. (%)	Image lag typ. (%)	Horizontal resolution typ. (TV-lines)	Vertical resolution typ. (TV-lines)
		H	V							
MN3711CFP	Color	512	492	58	650	200	0.01	0	330	350

■ Graphs of Characteristics

CCD Spectral Characteristics



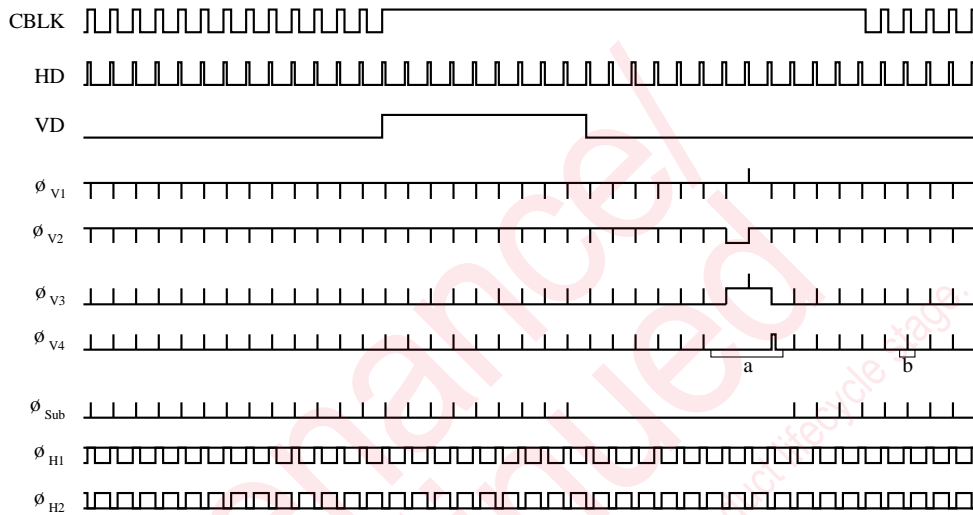
Color Filter Spectral Characteristics



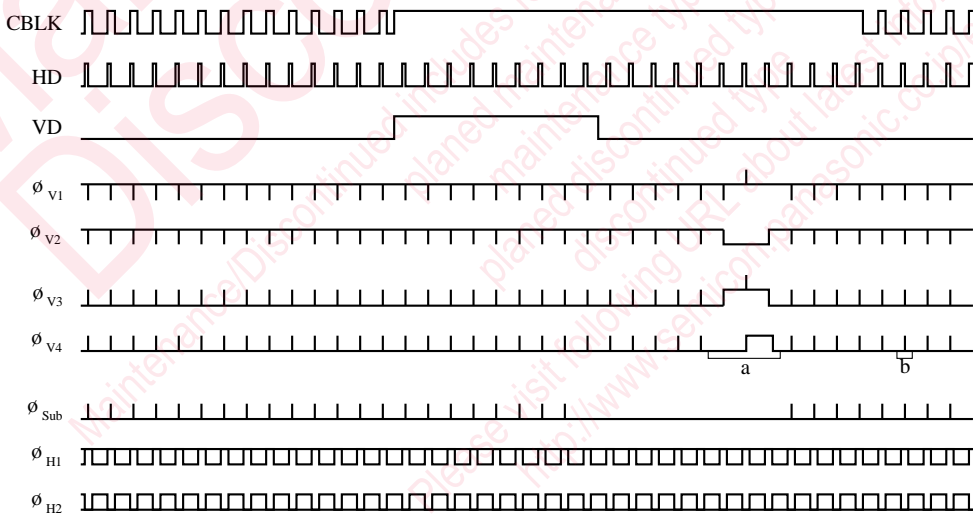
■ Example of Recommended Driving Pulses

• V Rate timing

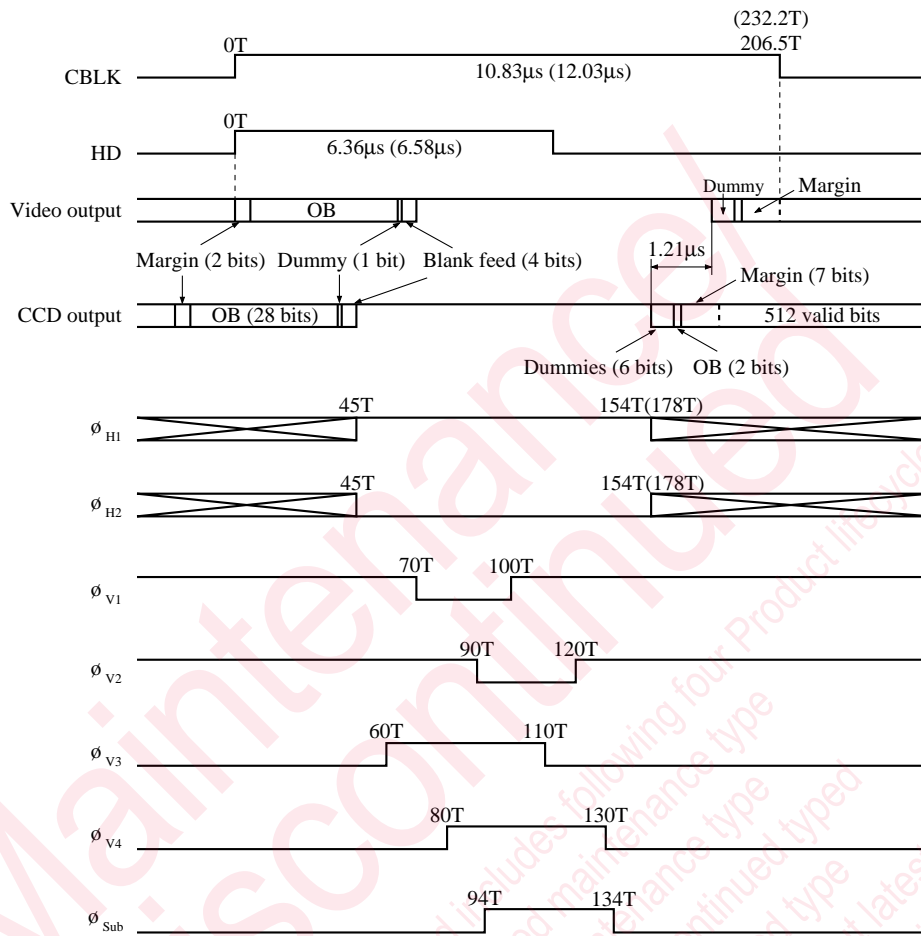
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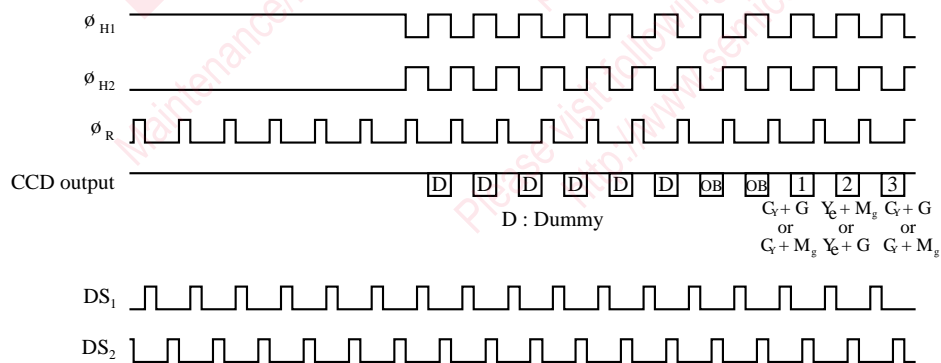
< Field B >



• H Rate timing



• High speed pulse timing



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