256Kx1 High Speed Monolithic SRAM CMOS

FEATURES

- 128Kx8 bit CMOS Static
- Random Access Memory
  - Fast Access Times of 35, 45, 55ns
  - Data Retention Function (LP)
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- JEDEC Approved Pinouts
  - 24 pin Ceramic DIP (Package 3)
  - 28 pad Ceramic LCC (Package 14)
  - 28 lead Ceramic Flatpack (Package 79)
- Single +5V (±10%) Supply Operation

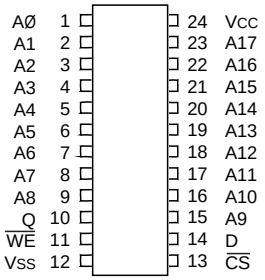
The EDI88128CS is a high speed, high performance, megabit density Monolithic CMOS Static RAM organized as 128Kx8.

The device has eight bi-directional input-output lines to provide simultaneous access to all bits in a word. An automatic power down feature permits the on-chip circuitry to enter a very low standby mode and be brought back into operation at a speed equal to the address access time.

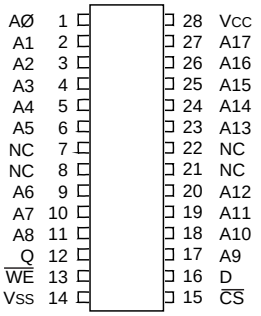
A Low Power version with 2V Data Retention (EDI88128LPS) is also available for battery back-up opperation. Military product is available compliant of MIL-PRF-38535.

FIG. 1 PIN CONFIGURATION

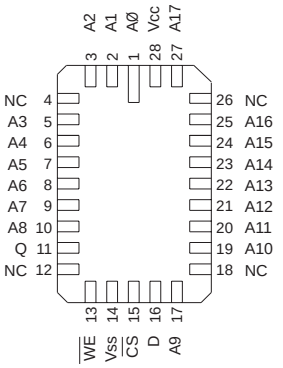
24 DIP
TOP VIEW



28 FLATPACK
TOP VIEW



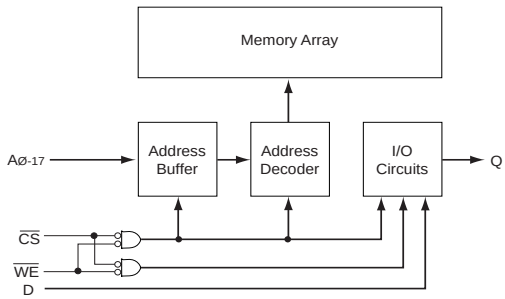
28 CLCC
TOP VIEW



PIN DESCRIPTION

D	Data Input
Q	Data Output
A0-17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
VCC	Power (+5V ±10%)
VSS	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on any pin relative to Vss	-0.5 to 7.0	V
Operating Temperature T_A (Ambient) Commercial	0 to +70	°C
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Plastic	-65 to +150	°C
Power Dissipation	1	W
Output Current	20	mA
Junction Temperature, T_J	175	°C

NOTE:
Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	Standby	High Z	I_{CC2}, I_{CC3}
L	H	Output Deselect	High Z	I_{CC1}
L	H	Read	Data Out	I_{CC1}
L	L	Write	Data In	I_{CC1}

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	-0.3	—	+0.8	V

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max LCC, DIP, Flatpack	Unit
Address Lines	C_I	V_{IN} = Vcc or Vss, f = 1.0MHz	10	pF
Data Lines	$C_{D/Q}$	V_{OUT} = Vcc or Vss, f = 1.0MHz	12	pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS

(V_{CC} = 5V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}		-5	—	+5	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = 0V to V_{CC}		-5	—	+5	µA
Operating Power Supply Current	I_{CC1}	$\overline{WE}$, $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA, Min Cycle		—	80	120	mA
Standby (TTL) Power Supply Current	I_{CC2}	$\overline{CS}$ ≥ V_{IH}, V_{IN} ≤ V_{IL}, V_{IN} ≥ V_{IH}		—	2	20	mA
Full Standby Power Supply Current	I_{CC3}	$\overline{CS}$ ≥ V_{CC} -0.2V V_{IN} ≥ Vcc -0.2V or V_{IN} ≤ 0.2V	C	—	1	3	mA
			LP	—	0.5	1.5	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	—	—	V

NOTE: DC test conditions: V_{IL} = 0.3V, V_{IH} = Vcc -0.3V

AC CHARACTERISTICS – READ CYCLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Symbol JEDEC	Symbol Alt.	35ns Min	35ns Max	45ns Min	45ns Max	55ns Min	55ns Max	Units
Read Cycle Time	t_{AVAV}	t_{RC}	35		45		55		ns
Address Access Time	t_{AVQV}	t_{AA}		35		45		55	ns
Chip Enable Access Time	t_{ELQV}	t_{ACS}		35		45		55	ns
Chip Enable to Output in Low Z (1)	t_{ELQX}	t_{CLZ}	5		5		5		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	t_{CHZ}	0	20	0	20	0	20	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	5		5		5		ns
Chip Enable to Power Up (1)	t_{ELICCH}	t_{PU}	0		0		0		ns
Chip Enable to Power Down (1)	t_{EHICCL}	t_{PD}		35		45		55	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – WRITE CYCLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Symbol JEDEC	Symbol Alt.	35ns Min	35ns Max	45ns Min	45ns Max	55ns Min	55ns Max	Units
Write Cycle Time	t_{AVAV}	t_{WC}	35		45		55		ns
Chip Enable to End of Write	t_{ELWH} t_{ELEH}	t_{CW} t_{CW}	30 30		35 35		45 45		ns ns
Address Setup Time	t_{AVWL} t_{AVEL}	t_{AS} t_{AS}	0 0		0 0		0 0		ns ns
Address Valid to End of Write	t_{AVWH} t_{AVEH}	t_{AW} t_{AW}	30 30		35 35		45 45		ns ns
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	25 25		25 25		30 30		ns ns
Write Recovery Time	t_{WHAX} t_{EHAX}	t_{WR} t_{WR}	5 5		5 5		5 5		ns ns
Data Hold Time	t_{WHDX} t_{EHDX}	t_{DH} t_{DH}	0 0		0 0		0 0		ns ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	15	0	15	0	20	ns
Data to Write Time	t_{DVWH} t_{DVEH}	t_{DW} t_{DW}	20 20		25 25		25 25		ns ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CONDITIONS

Figure 1

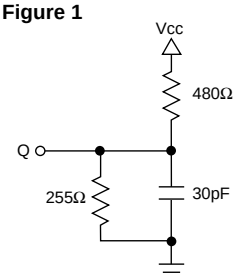
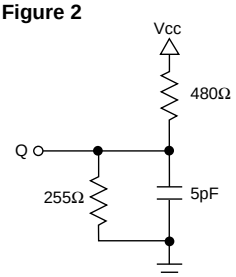


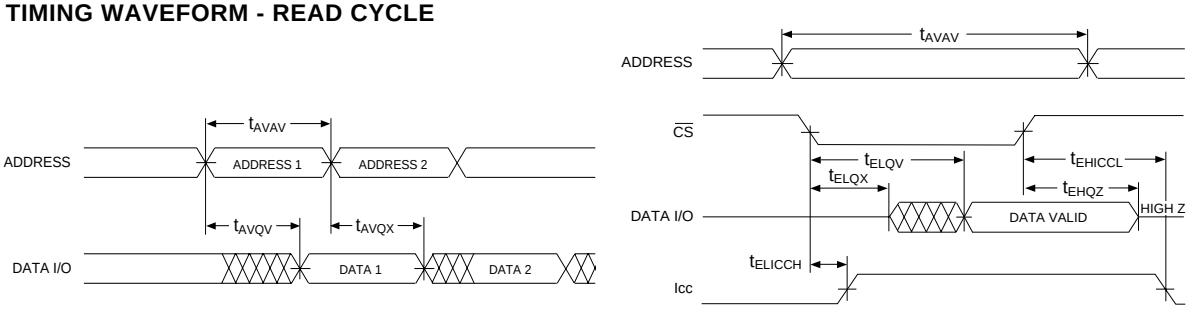
Figure 2



Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, CL = 5pF Figure 2)

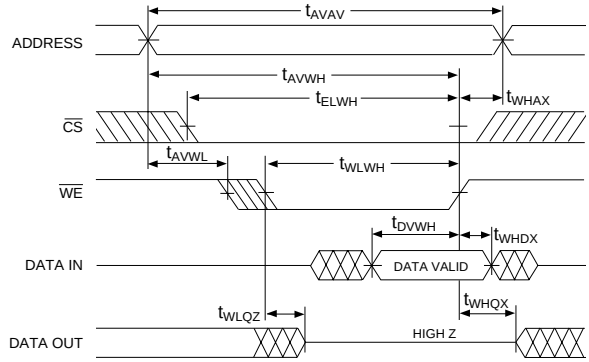
FIG. 2
TIMING WAVEFORM - READ CYCLE



READ CYCLE 1 ($\overline{WE}$ HIGH; $\overline{OE}$, $\overline{CS}$ LOW)

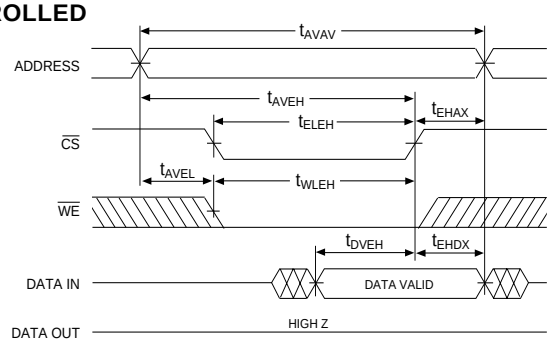
READ CYCLE 2 ($\overline{WE}$ HIGH)

FIG. 3
WRITE CYCLE - $\overline{WE}$ CONTROLLED



WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

FIG. 4
WRITE CYCLE - $\overline{CS}$ CONTROLLED



WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

DATA RETENTION CHARACTERISTICS (EDI81256LP ONLY)

(T_A = -55°C to +125°C)

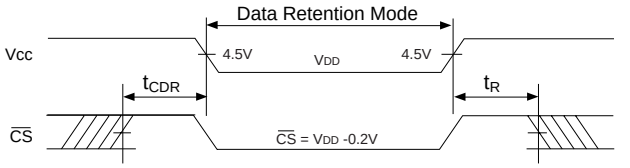
Characteristic Low Power Version only	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V_{DD}	V_{DD} = 2.0V	2	–	–	V
Data Retention Quiescent Current	I_{CCDR}	$\overline{CS} \geq V_{DD}$ -0.2V	–	50	500	µA
Chip Disable to Data Retention Time (1)	T_{CDR}	$V_{IN} \geq V_{DD}$ -0.2V	0	–	–	ns
Operation Recovery Time (1)	T_R	or $V_{IN} \leq$ 0.2V	T_{AVAV}*	–	–	ns

NOTE:

1. Parameter guaranteed by design, but not tested.

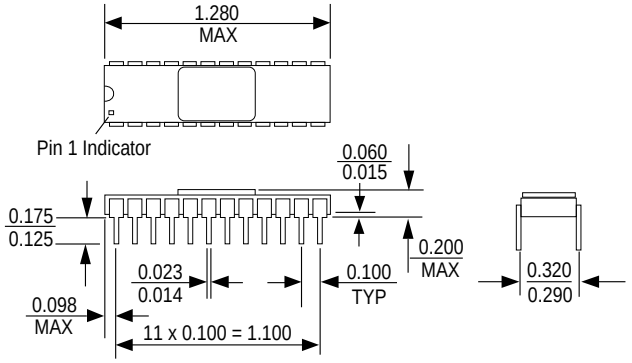
* Read Cycle Time

FIG. 5
DATA RETENTION - $\overline{CS}$ CONTROLLED



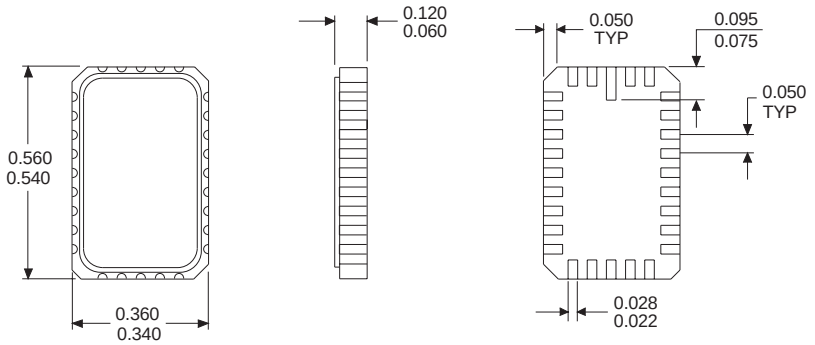
DATA RETENTION, $\overline{CS}$ CONTROLLED

PACKAGE 3: 24 PIN SIDEBRAZED CERAMIC DIP (300 mils wide)



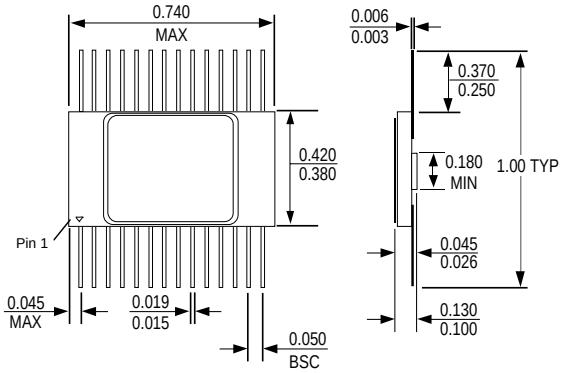
ALL DIMENSIONS ARE IN INCHES

PACKAGE 14: 28 PAD CERAMIC LCC



ALL DIMENSIONS ARE IN INCHES

PACKAGE 79: 28 PIN CERAMIC FLATPACK



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

EDI 8 8 128 CS X X X

WHITE ELECTRONIC DESIGNS

SRAM

ORGANIZATION, 128Kx8

TECHNOLOGY:
- C = CMOS Standard Power
- LP = Low Power

ACCESS TIME (ns)

PACKAGE TYPE:
- C = 32 lead Sidebrazed DIP, 300 mil (Package 3)
- F = 32 lead Ceramic Flatpack (Package 79)
- L = 32 pad Ceramic LCC (Package 14)

DEVICE GRADE:

B =	MIL-STD-883 Compliant	
M =	Military Screened	-55°C to +125°C
I =	Industrial	-40°C to +85°C
C =	Commercial	0°C to +70°C