μPC3250T7L

SiGe CMOS/BiCMOS Integrated Circuit
IF Down-converter MMIC for Ku-band LNB Converter

R09DS0052EJ0100
Rev.1.00
Oct 23, 2012

DESCRIPTION

The μPC3250T7L is a CMOS/BiCMOS MMIC for Ku-band LNB converter.

This device is housed in a 24-pin plastic QFN (Quad Flat Non-Leaded) (T7L) package.

FEATURES

- Low power consumption : 3.3 V/63 mA, 208 mW
- Switched LO frequency : 9.75 G Hz, 10.6 GHz, 10.75 GHz
- 2 step Gain selected function : 41 dB/36 dB
- Low noise figure : 7.5 dB
- Fully integrated Mixer/Oscillator/PLL synthesizer/IF Amplifier/4-channel FET bias supply circuit/ Polarity control voltage detector/Tone control signal detector
- Integrated power save detector
- 24-pin plastic QFN (T7L) package (4.0 × 4.0 × 0.6 mm)

APPLICATIONS

- Ku-band Low Noise Block (LNB) converters for satellite receiver (DVB-S, ABS-S application)

ORDERING INFORMATION

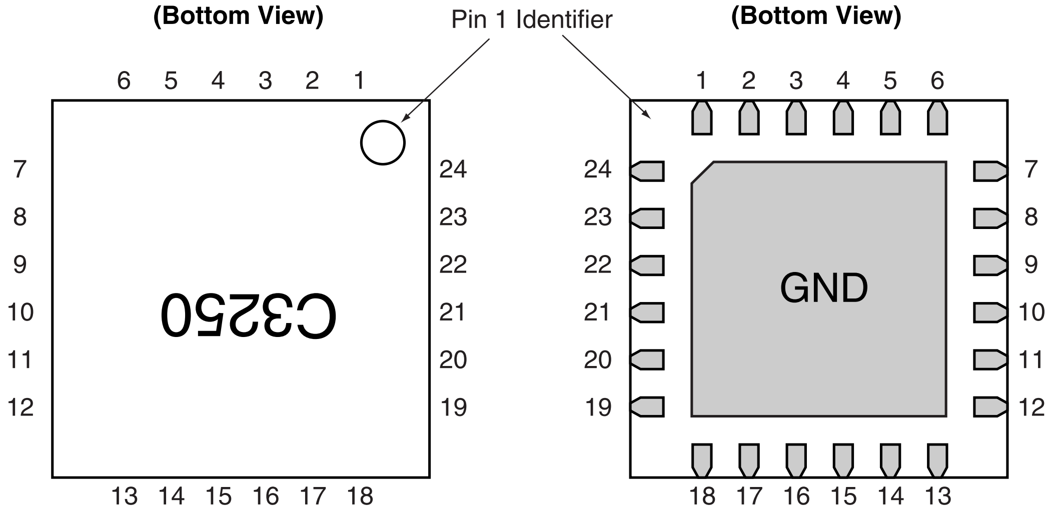
Part Number	Order Number	Package	Marking	Supplying Form
μPC3250T7L-E1	μPC3250T7L-E1-A	24-pin plastic QFN (0.5 mm pitch) (Pb-Free)	C3250	• Embossed tape 12 mm wide • Pin 7 to 12 face the perforation side of the tape • Qty 5 kpcs/reel • Dry packing specification (MSL 3 Equivalent)

Remark To order evaluation samples, please contact your nearby sales office.
Part number for sample order: μPC3250T7L

CAUTION

Observe precautions when handling because these devices are sensitive to electrostatic discharge.

PIN CONNECTIONS



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	NC	7	V_{DV}	13	G_{SW}	19	V_{DDPLL}
2	RF_{in}	8	V_{GV}	14	CVNeg	20	TonePol
3	NC	9	$V_{D}1$	15	XO2	21	IF_{out}
4	R_{cal}	10	$V_{G}1$	16	XO1	22	V_{CCIF}
5	V_{DH}	11	$V_{D}2$	17	V_{ref}	23	V_{CCRF}
6	V_{GH}	12	$V_{G}2$	18	CP_{out}	24	LO_{sel}

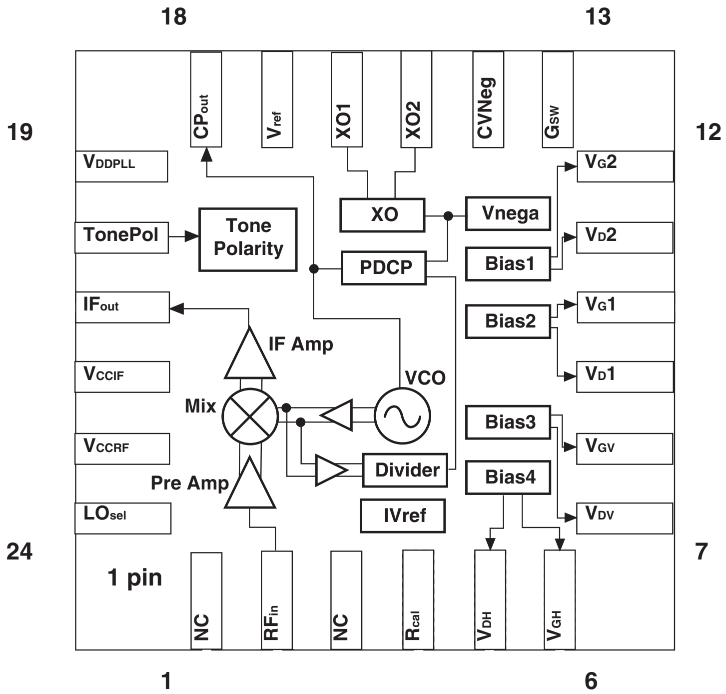
Remark NC means no connection pin.
Heat sink of bottom side of this device is connected to GND.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{CCRF}, V_{CCIF}, V_{DDPLL}	+4.0	V
Control Voltage (TonePol, LO_{sel}, G_{SW})	V_{POLA}, V_{LOsel}, G_{SW}	+4.0	V
Power dissipation[Note]	P_{tot}	1.53	mW
Storage Temperature	T_{stg}	–55 to +125	°C
Operating Ambient Temperature	T_A	–40 to +85	°C
Input Power	P_{in}	0	dBm

Note: Mounted on double-sided copper-clad 50 × 50 × 0.51 mm laminated PWB, T_A = +85°C

BLOCK DIAGRAM



Pin No.	Name	Description
1	NC	No Connection
2	RF_{in}	Ku band RF signal input, AC coupling required.
3	NC	No Connection
4	R_{cal}	LNFET drain current adjust by resister
5	V_{DH}	Horizontal LNFET drain voltage supply
6	V_{GH}	Horizontal LNFET gate bias voltage
7	V_{DV}	Vertical LNFET drain voltage supply
8	V_{GV}	Vertical LNFET gate bias voltage
9	V_D1	Common LNFET drain voltage supply 1
10	V_G1	Common LNFET gate bias voltage 1
11	V_D2	Common LNFET drain voltage supply 2
12	V_G2	Common LNFET gate bias voltage 2
13	G_{SW}	Gain control input terminal
14	CVNeg	Negative voltage line decoupling
15	XO2	Crystal oscillator connection terminal 2
16	XO1	Crystal oscillator connection terminal 1
17	V_{ref}	Reference voltage line decoupling
18	CP_{out}	Charge pump output, connect capacitor for loop filter
19	V_{DDPLL}	PLL Power supply terminal. Decoupling capacitor required
20	TonePol	Tone and Polarity control signal input terminal
21	IF_{out}	L band IF signal output, AC coupling required
22	V_{CCIF}	IF Power supply terminal. Decoupling capacitor required
23	V_{CCRF}	RF Power supply terminal. Decoupling capacitor required
24	LO_{sel}	Local Oscillator frequency control input terminal

Remark NC means no connection pin.
Heat sink of bottom side of this device is connected to GND.

RECOMMENDED OPERATING RANGE (T_A = +25°C, unless otherwise specified)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CCRF}, V_{CCIF}, V_{DDPLL}	+3.0	+3.3	+3.6	V
High level of Control Voltage (LO_{sel}, G_{SW})	$V_{\_High}$	V_{DD} – 0.5	–	V_{DD} Note 1	V
Low level of Control Voltage (LO_{sel}, G_{SW})	$V_{\_Low}$	0	–	0.5	V
Operating Ambient Temperature	T_A	–40	+25	+85	°C
RF Input frequency	f_{RF}	10.7	–	12.75	GHz
IF Output frequency	f_{IF}	950	–	2 150	GHz
LO frequency	f_{LO}	–	9.75	–	GHz
		–	10.6	–	
		–	10.75	–	
TONE control signal frequency	f_{TONE}	18	22	26	kHz
TONE control signal voltage	V_{TONE}	0.4	0.6	0.8	Vp-p
Polarity control voltage Note 2	V_{POLA}	13	–	18	V
Input Voltage of pin 20 (TonePol)	V_{TP}	0	–	V_{DD}	V
Adjustment supply current for each FET	I_D	5	10	18	mA

Notes: 1 V_{DD} : Supply Voltage = V_{CCRF} = V_{CCIF} = V_{DDPLL}

2 See the evaluation (application) circuit.
The detail connection of pin 20 (TonePol) is shown in the evaluation circuit.
This pin cannot be directly connected to 13 V/18 V polarity control voltage.
The polarity control voltage must be divided to a low voltage by the external resistors.

ELECTRICAL CHARACTERISTICS
(T_A = +25°C, V_{CCRF} = V_{CCIF} = V_{DDPLL} = +3.3 V, Z_S = Z_L = 50 Ω, f_{xtal} = 25 MHz, unless otherwise specified)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Total Supply Current 1 Note (V_{CCRF}, V_{CCIF}, V_{DDPLL}) Normal mode (High Gain selected)	$I_{CC}1$	V_{POLA} > 7.0 V , Non-RF input, G_{SW} = +3.3 V (without FETs bias supply current)	50	63	80	mA
Total Supply Current 2 Note (V_{CCRF}, V_{CCIF}, V_{DDPLL}) Normal mode (Low Gain selected)	$I_{CC}2$	V_{POLA} > 7.0 V , Non-RF input, G_{SW} = 0 V (without FETs bias supply current)	48.5	61.5	78.5	mA
Total Supply Current 3 Note (V_{CCRF}, V_{CCIF}, V_{DDPLL}) Power Save mode	$I_{CC}3$	V_{POLA} = 0 V (< 3.6V) Non-RF input (without FETs bias supply current)	–	5	10	mA

Note: See the evaluation (application) circuit.
The detail connection of pin 20 (TonePol) is shown in the evaluation circuit.
This pin cannot be directly connected to 13 V/18 V polarity control voltage.
The polarity control voltage must be divided to a low voltage by the external resistors.

ELECTRICAL CHARACTERISTICS
(T_A = +25°C, V_{CCRF} = V_{CCIF} = V_{DDPLL} = +3.3 V, G_{SW} = +3.3 V, Z_S = Z_L = 50 Ω, f_{xtal} = 25 MHz, unless otherwise specified)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Conversion Gain 1 Note 1	$G_{conv}1$	f_{LO} = 9.75 GHz, f_{IF} = 1.5 GHz, P_{in} = –50 dBm	37	41	45	dB
Conversion Gain 2 Note 1	$G_{conv}2$	f_{LO} = 10.6 GHz, f_{IF} = 1.5 GHz, P_{in} = –50 dBm	37	41	45	dB
Conversion Gain 3 Note 1	$G_{conv}3$	f_{LO} = 10.75 GHz, f_{IF} = 1.5 GHz, P_{in} = –50 dBm	37	41	45	dB
POLA control Threshold Voltage 1 Note 1	$V_{th\_POLA}1$	Power Save mode to Normal mode Dividing resistor : 8.2 kΩ/51 kΩ	3.6	–	7.0	V
POLA control Threshold Voltage 2 Note 1 (Channel selection)	$V_{th\_POLA}2$	Vertical mode to Horizontal mode Dividing resistor : 8.2 kΩ/51 kΩ	15.2	15.7	16.2	V
TONE control signal Threshold Voltage Note 1 (Channel selection)	V_{th_TONE}	Low band to High band f_{TONE} = 22 kHz, Duty Cycle = 50%, Pulse wave Divider capacitor : 0.1 μF/0.1 μF	0.1	0.15	0.35	V_{p-p}
Drain Voltage H Note 1, 2	V_{DH}	V_{POLA} = 18 V, I_D = 10 mA, R_{cal} = 22 kΩ	1.8	2.0	2.2	V
Drain Voltage V Note 1, 2	V_{DV}	V_{POLA} = 13 V, I_D = 10 mA, R_{cal} = 22 kΩ	1.8	2.0	2.2	V
Drain Voltage 1 Note 1, 2	V_D1	I_D = 10 mA, R_{cal} = 22 kΩ	1.8	2.0	2.2	V
Drain Voltage 2 Note 1, 2	V_D2	I_D = 10 mA, R_{cal} = 22 kΩ	1.8	2.0	2.2	V
Drain Current H Note 1, 2	I_{DH}	V_{POLA} = 18 V, R_{cal} = 22 kΩ	8.5	10	11.5	mA
Drain Current V Note 1, 2	I_{DV}	V_{POLA} = 13 V, R_{cal} = 22 kΩ	8.5	10	11.5	mA
Drain Current 1 Note 1, 2	I_D1	R_{cal} = 22 kΩ	8.5	10	11.5	mA
Drain Current 2 Note 1, 2	I_D2	R_{cal} = 22 kΩ	8.5	10	11.5	mA
Gate Voltage H Note 1, 2 of FET OFF mode	V_{GH}	V_{POLA} = 13 V	–2.0	–2.5	–3.0	V
Gate Voltage V Note 1, 2 of FET OFF mode	V_{GV}	V_{POLA} = 18 V	–2.0	–2.5	–3.0	V

Notes: 1 See the evaluation (application) circuit.
The detail connection of pin 20 (TonePol) is shown in the evaluation circuit.
This pin cannot be directly connected to 13 V/18 V polarity control voltage.
The polarity control voltage must be divided to a low voltage by the external resistors.

2 See the graph of "R_{cal} vs. I_{DFET}, V_{DFET}." FET's drain current can be adjusted by the external resisters (R_{cal}).

STANDARD CHARACTERISTICS FOR REFERENCE
(T_A = +25°C, V_{CCRF} = V_{CCIF} = V_{DDPLL} = +3.3 V, G_{SW} = +3.3V, Z_S = Z_L = 50 Ω, f_{xtal} = 25 MHz, unless otherwise specified)

Parameter	Symbol	Test Conditions	Reference Value	Unit
Conversion Gain Flatness 1	$\Delta G_{conv}1$	f_{LO} = 9.75 GHz, f_{IF} = 0.95 G to 1.95 GHz, P_{in} = –50 dBm	2.5	dB
Conversion Gain Flatness 2	$\Delta G_{conv}2$	f_{LO} = 10.6 GHz, f_{IF} = 1.1 G to 2.15 GHz, P_{in} = –50 dBm	2.0	dB
Conversion Gain Flatness 3	$\Delta G_{conv}3$	f_{LO} = 10.75 GHz, f_{IF} = 0.95 G to 2.0 GHz, P_{in} = –50 dBm	2.0	dB
Noise Figure 1	NF1	f_{LO} = 9.75 GHz, f_{IF} = 1.5 GHz	7.5	dB
Noise Figure 2	NF2	f_{LO} = 10.6 GHz, f_{IF} = 1.5 GHz	7.5	dB
Noise Figure 3	NF3	f_{LO} = 10.75 GHz, f_{IF} = 1.5 GHz	7.5	dB
Gain 1 dB Compression Output Power 1	$P_{O(1\ dB)}1$	f_{LO} = 9.75 GHz, f_{IF} = 1.5 GHz	5	dBm
Gain 1 dB Compression Output Power 2	$P_{O\ (1\ dB)}2$	f_{LO} = 10.6 GHz, f_{IF} = 1.5 GHz	5	dBm
Gain 1 dB Compression Output Power 3	$P_{O(1\ dB)}3$	f_{LO} = 10.75 GHz, f_{IF} = 1.5 GHz	5	dBm
Output 3rd Order Intercept Point 1	OIP_31	f_{LO} = 9.75 GHz, $f_{IF}1$ = 1 500 MHz, $f_{IF}2$ = 1 501 MHz	16	dBm
Output 3rd Order Intercept Point 2	OIP_32	f_{LO} = 10.6 GHz, $f_{IF}1$ = 1 500 MHz, $f_{IF}2$ = 1 501 MHz	16	dBm
Output 3rd Order Intercept Point 3	OIP_33	f_{LO} = 10.75 GHz, $f_{IF}1$ = 1 500 MHz, $f_{IF}2$ = 1 501 MHz	16	dBm
RF Input Return Loss	RL_{RF}	f_{RF} = 10.7 G to 12.75 GHz	10	dB
IF Output Return Loss	RL_{IF}	f_{RF} = 950 M to 2 150 MHz	10	dB
Phase Noise 1	PN1	1 kHz offset	–78	dBc/Hz
Phase Noise 2	PN2	10 kHz offset	–80	dBc/Hz
Phase Noise 3	PN3	100 kHz offset	–88	dBc/Hz
Phase Noise 4	PN4	1 MHz offset	–108	dBc/Hz
Integrated phase noise density	$\Phi n\lambda$ (itg)	Integrated offset frequency 10 k to 15 MHz	1.7	°RMS
Local signal Leakage 1	$L_{o\_Leakage}1$	f_{LO} = 9.75 GHz, Local to RF_{in}	–58	dBm
Local signal Leakage 2	$L_{o\_Leakage}2$	f_{LO} = 10.6 GHz, Local to RF_{in}	–58	dBm
Local signal Leakage 3	$L_{o\_Leakage}3$	f_{LO} = 10.75GHz, Local to RF_{in}	–57	dBm
Total Circuit current 1 (Reference status 1)	$I_{CC}1$	2ch FET bias supplied V_{POLA} > 7.0 V, Non-RF	83	mA
Total Circuit current 2 (Reference status 2)	$I_{CC}2$	3ch FET bias supplied V_{POLA} > 7.0 V, Non-RF	93	mA

Note: See the evaluation (application) circuit.

STANDARD CHARACTERISTICS FOR REFERENCE
(T_A = +25°C, V_{CCRF} = V_{CCIF} = V_{DDPL}L = +3.3 V, G_{SW} = 0 V, Z_S = Z_L = 50 Ω, f_{xtal} = 25 MHz, unless otherwise specified)

Parameter	Symbol	Test Conditions	Reference Value	Unit
Conversion Gain 1	$G_{conv}1$	f_{LO} = 9.75 GHz, f_{IF} = 1.5 GHz, P_{in} = –50 dBm	36	dB
Conversion Gain 2	$G_{conv}2$	f_{LO} = 10.6 GHz, f_{IF} = 1.5 GHz, P_{in} = –50 dBm	36	dB
Conversion Gain 3	$G_{conv}3$	f_{LO} = 10.75GHz, f_{IF} = 1.5 GHz, P_{in} = –50 dBm	36	dB
Conversion Gain Flatness 1	$\Delta G_{conv}1$	f_{LO} = 9.75 GHz, f_{IF} = 0.95 G to 1.95 GHz, P_{in} = –50 dBm	2.5	dB
Conversion Gain Flatness 2	$\Delta G_{conv}2$	f_{LO} = 10.6 GHz, f_{IF} = 1.1 G to 2.15 GHz, P_{in} = –50 dBm	2.0	dB
Conversion Gain Flatness 3	$\Delta G_{conv}3$	f_{LO} = 10.75 GHz, f_{IF} = 0.95 G to 2.0 GHz, P_{in} = –50 dBm	2.0	dB
Noise Figure 1	NF1	f_{LO} = 9.75 GHz, f_{IF} = 1.5 GHz	7.5	dB
Noise Figure 2	NF2	f_{LO} = 10.6 GHz, f_{IF} = 1.5 GHz	7.5	dB
Noise Figure 3	NF3	f_{LO} = 10.75 GHz, f_{IF} = 1.5 GHz	7.5	dB
Gain 1 dB Compression Output Power 1	$P_{O(1\,dB)}1$	f_{LO} = 9.75 GHz, f_{IF} = 1.5 GHz	2	dBm
Gain 1 dB Compression Output Power 2	$P_{O(1\,dB)}2$	f_{LO} = 10.6 GHz, f_{IF} = 1.5 GHz	2	dBm
Gain 1 dB Compression Output Power 3	$P_{O(1\,dB)}3$	f_{LO} = 10.75 GHz, f_{IF} = 1.5 GHz	2	dBm
Output 3rd Order Intercept Point 1	$OIP_3 1$	f_{LO} = 9.75 GHz, $f_{IF}1$ = 1 500 MHz, $f_{IF}2$ = 1 501 MHz	12	dBm
Output 3rd Order Intercept Point 2	$OIP_3 2$	f_{LO} = 10.6 GHz, $f_{IF}1$ = 1 500 MHz, $f_{IF}2$ = 1 501 MHz	12	dBm
Output 3rd Order Intercept Point 3	$OIP_3 3$	f_{LO} = 10.75 GHz, $f_{IF}1$ = 1 500 MHz, $f_{IF}2$ = 1 501 MHz	12	dBm
RF Input Return Loss	RL_{RF}	f_{RF} = 10.7 G to 12.75 GHz	10	dB
IF Output Return Loss	RL_{IF}	f_{RF} = 950 M to 2 150 MHz	10	dB

Note: See the evaluation (application) circuit.

TRUTH TABLE

Local Oscillator frequency select pin function description (pin 24 (LO_{sel}))

LO_{sel}	LO_{sel} = Low (DVB-S mode)		LO_{sel} = High (ABS-S mode)
	Tone signal = 0 kHz	Tone signal = 22 kHz	–
Local Oscillator frequency	9.75 GHz	10.6 GHz	10.75 GHz

Note: The relationships between the LO_{sel} state and the pin connection are as follows.

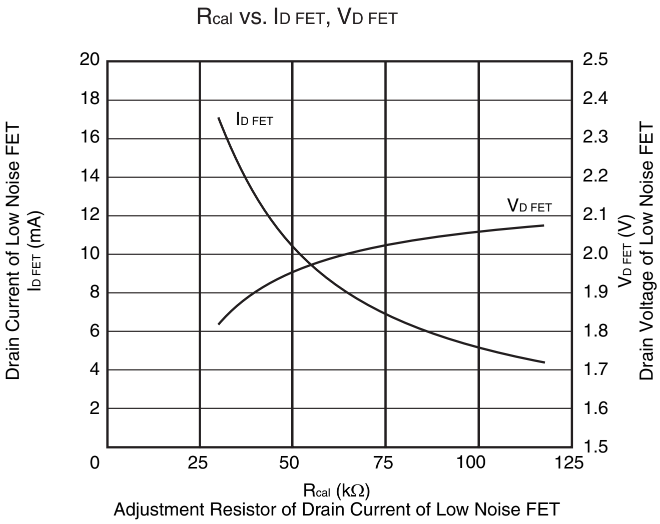
By connecting this pin to GND line (0 V DC), LO_{sel} becomes “Low” state.
By connecting this pin to V_{DD} line (V_{DD} DC), LO_{sel} becomes “High” state.
The V_{DD} described above means the power supply voltage. Its value is 3.3 V the same as V_{CCRF}, V_{CCIF}, and V_{DDPLL}.

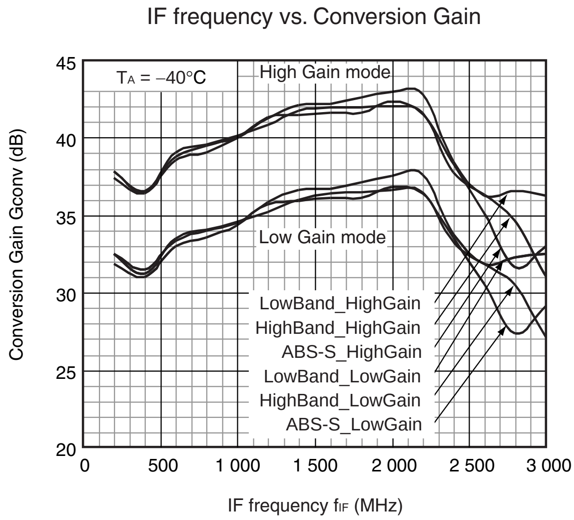
FET’s DC bias control pin function description (pin 20 (TonePol), polarity control voltage)

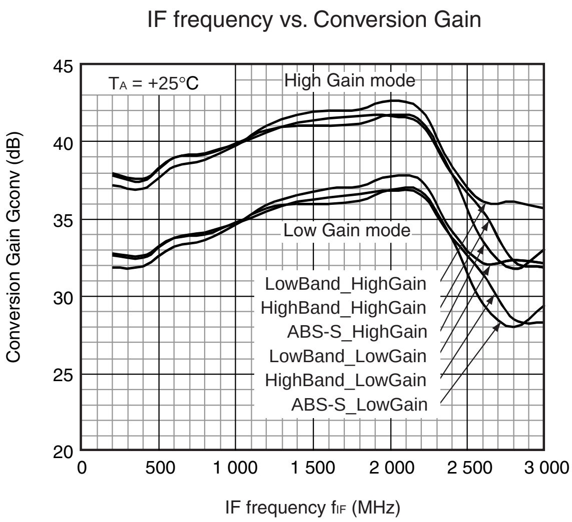
V_{POLA} \ FETs		Horizontal FET		Vertical FET		Common FET 1		Common FET 2	
		V_{GH}	V_{DH}	V_{GV}	V_{DV}	V_G1	V_D1	V_G2	V_D2
Normal mode	V_{POLA} > 16.2 V **Note**	Controlled (–2.5 V to +1 V)	Controlled (≈ 2 V)	Disable (–2.5V)	Disable (0 V)	Controlled (–2.5 V to +1 V)	Controlled (≈ 2 V)	Controlled (–2.5 V to +1 V)	Controlled (≈ 2 V)
	V_{POLA} < 15.2 V **Note**	Disable (–2.5 V)	Disable (0 V)	Controlled (–2.5 V to +1 V)	Controlled (≈ 2 V)	Controlled (–2.5 V to +1 V)	Controlled (≈ 2 V)	Controlled (–2.5 V to +1 V)	Controlled (≈ 2 V)
Power Save mode	V_{POLA} < 3.6 V **Note**	Disable (–2.5 V)	Disable (0 V)	Controlled (–2.5 V to +1 V)	Controlled (≈ 2 V)	Controlled (–2.5 V to +1 V)	Controlled (≈ 2 V)	Controlled (–2.5 V to +1 V)	Controlled (≈ 2 V)

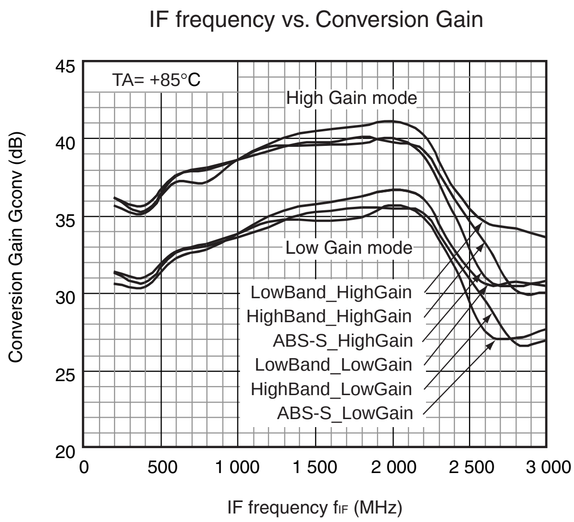
Note: Dividing Resistor: 8.2 kΩ/51 kΩ
See the evaluation (application) circuit.
The detail connection of pin 20 (TonePol) is shown in the evaluation circuit.
This pin cannot be directly connected to 13 V/18 V polarity control voltage.
The polarity control voltage must be divided to a low voltage.

TYPICAL CHARACTERISTICS
(T_A = +25°C, unless otherwise specified)



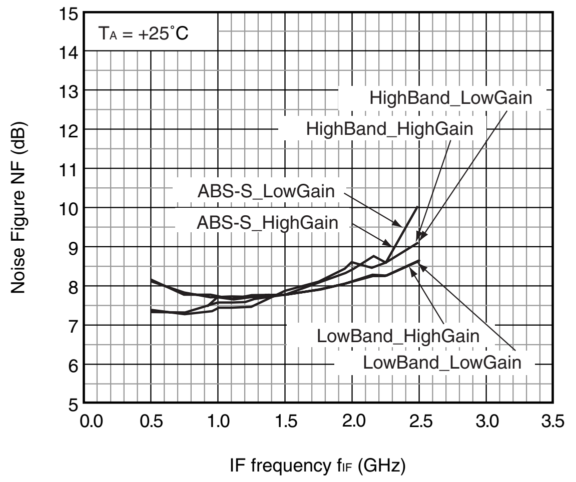




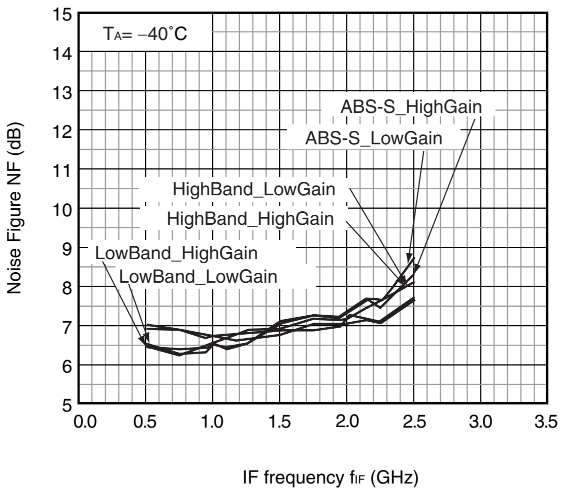


Remark The graphs indicate nominal characteristics.

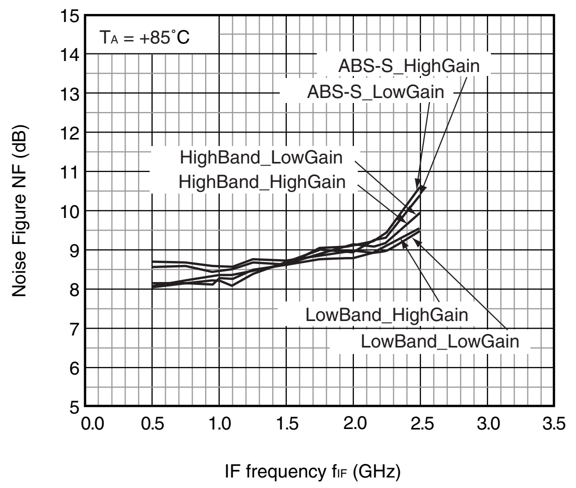
FREQUENCY VS. NOISE FIGURE



FREQUENCY VS. NOISE FIGURE

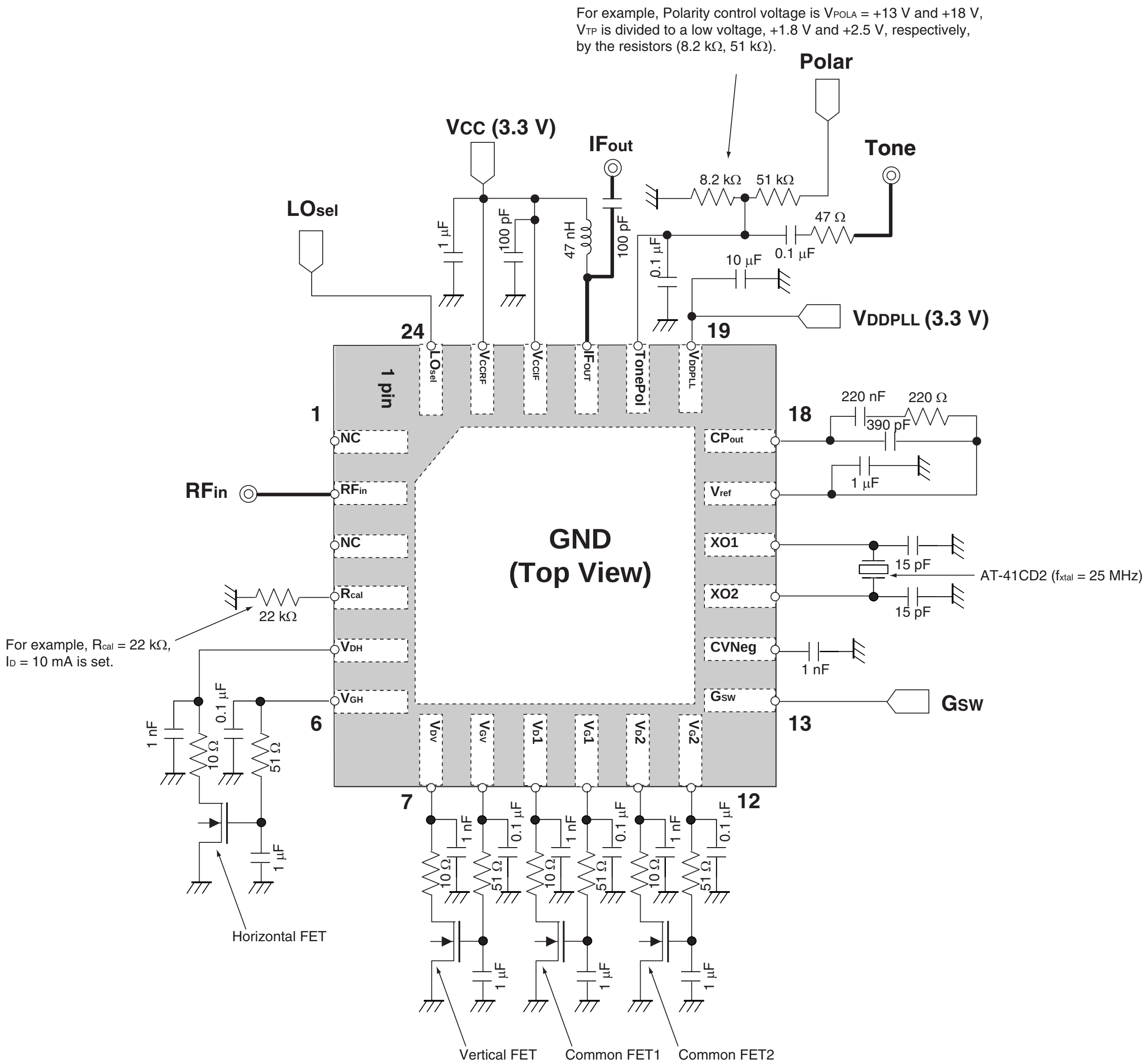


FREQUENCY VS. NOISE FIGURE



Remark The graphs indicate nominal characteristics.

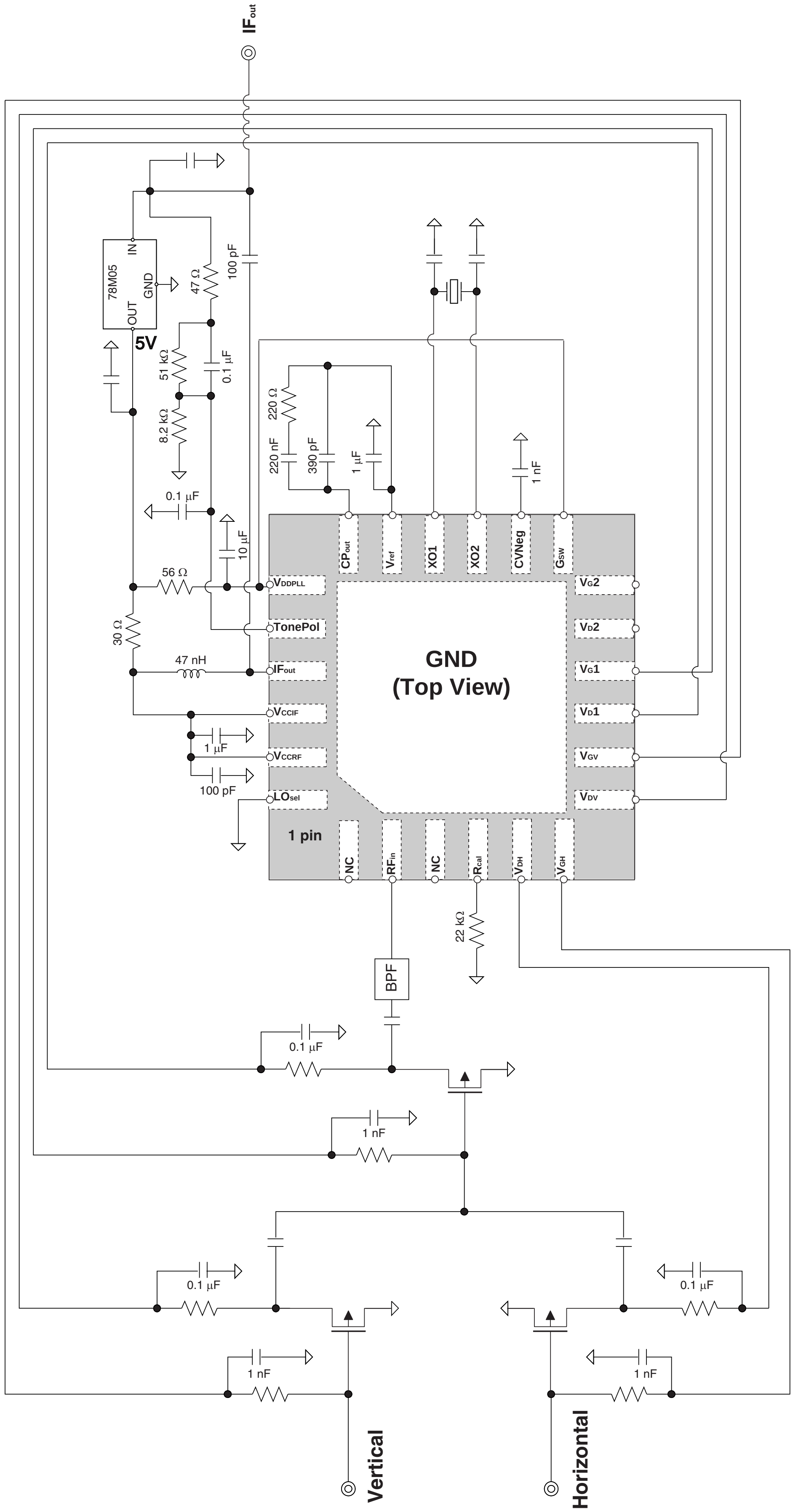
EVALUATION CIRCUIT



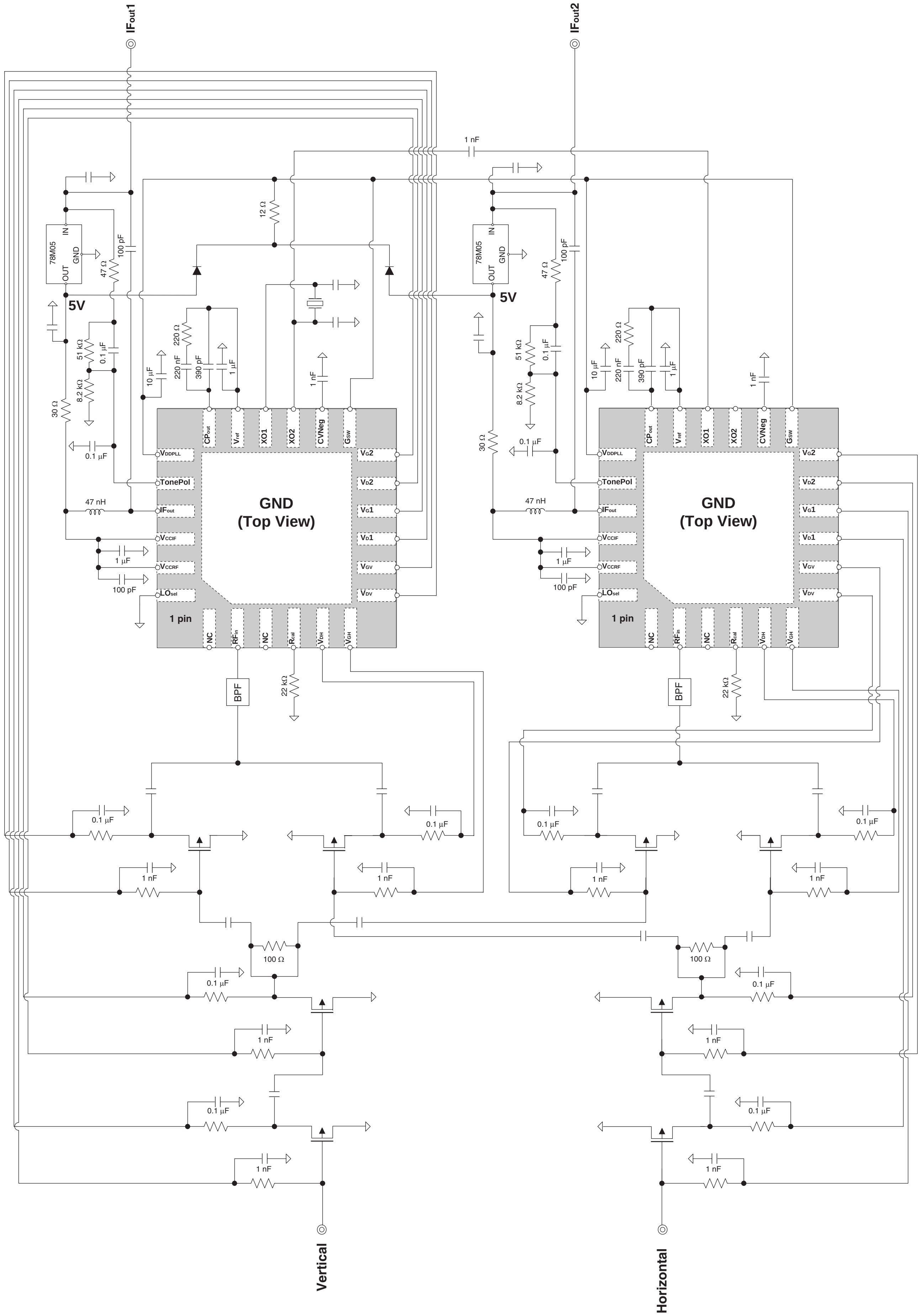
Remark NC means Non-Connection.
Heat sink (bottom side of the device) is connected to GND.
Board material is RO4003C (Rogers, t = 0.508 mm).

APPLICATION CIRCUIT

FOR SINGLE LNB (REFERENCE ONLY)

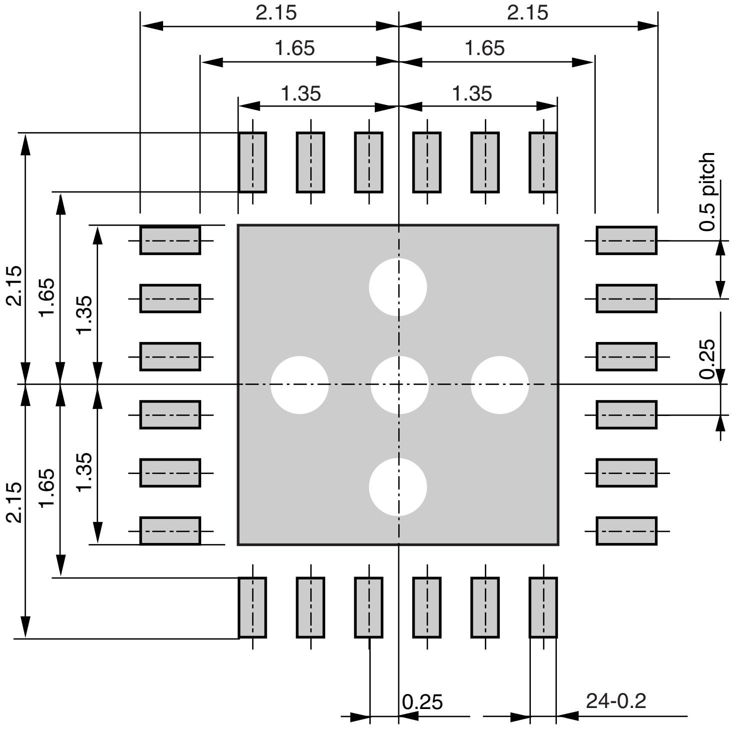


FOR TWIN LNB (DOUBLE SINGLE LNB) (REFERENCE ONLY)



MOUNTING PAD LAYOUT DIMENSIONS

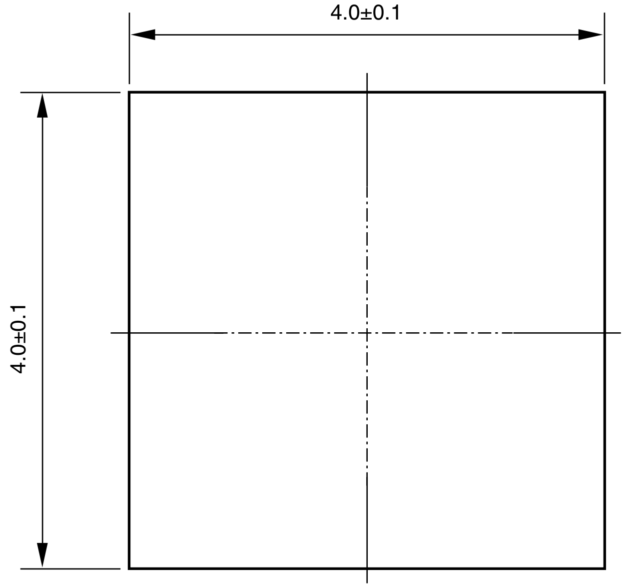
24-PIN PLASTIC QFN (T7L) PACKAGE (4.0 × 4.0 × 0.6 mm) (UNIT : mm)



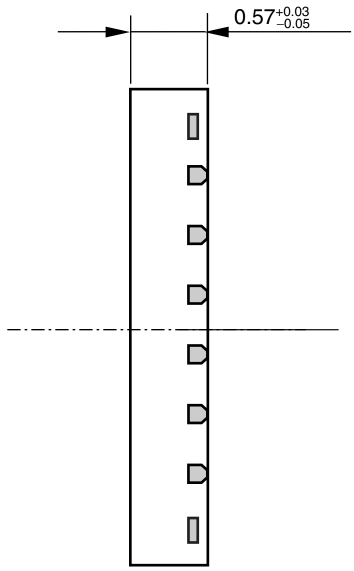
PACKAGE DIMENSIONS

24-PIN PLASTIC QFN (T7L) PACKAGE (4.0 × 4.0 × 0.6 mm) (UNIT : mm)

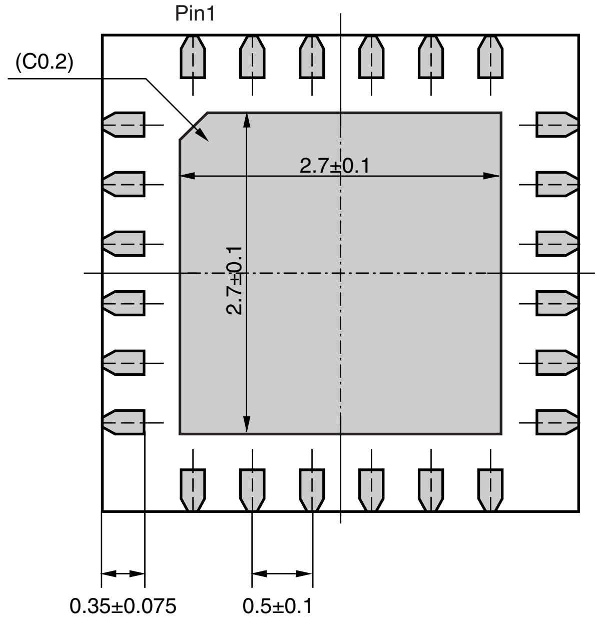
(Top View)



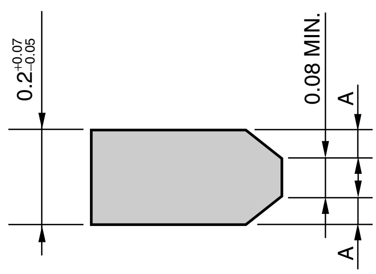
(Side View)



(Bottom View)



(Dimensions of Each Pin Part)



Remark A > 0

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions		Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature) Time at peak temperature Time at temperature of 220°C or higher Preheating time at 120 to 180°C Maximum number of reflow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 60 seconds or less : 120±30 seconds : 3 times : 0.2% (Wt.) or below	IR260
Partial Heating	Peak temperature (package surface temperature) Soldering time (per side of device) Maximum chlorine content of rosin flux (% mass)	: 350°C or below : 3 seconds or less : 0.2% (Wt.) or below	HS350

CAUTION

Do not use different soldering methods together (except for partial heating).

Revision History	μPC3250T7L Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Oct 23, 2012	–	First edition issued

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