CM6565

Noise Free 16 pin Self-Start Interleaved PFC with 180 Degree Phase Shift CRM PFC Controller for 90+/85+

GENERAL DESCRIPTION

The CM6565 is the industry first 16 pin self-start interleaved PFC with 180 degree phase shift CRM PFC controller for total power supply system efficiency greater 90% or 85%. The CM6565 is like a combination of two 180 degree phase shift CM6561s plus a lot of light load efficiency boost functions. CM6565 gives the best noise free performance of the offline power supply. The desired frequency range for each PFC controller should be above 35KHz.

Mismatches between two boost converters for the interleaved PFC can be less than +/-5%.

Basically, it is like two 6561s work together with 180 degree phase shift plus light load improvements.

1. IAC (pin 1), Multiplier input pin: Current input instead of Voltage input; it will enhance input current THD and the system will be less sensitive to the noise. The system can reduce one resistor between ground and IAC, multiplier input pin.

2. IAC (pin 1), Multiplier input pin: During the start up condition (the VCC is less than UVLO, 13V), IAC is connected to VCC, and the RAC resistor (between VIN pin and IAC pin) serves as a bleed resistor. Once the VCC is greater than UVLO, then, RAC resistor provides the sine wave current from VIN pin to IAC pin. After VCC is greater than UVLO, the voltage of the IAC pin is around 1.4V.

Therefore, the RAC resistor can be served as a bleed resistor. Usually, the value of the RAC is from 4Mega to 10Meg ohm.

3. IAC (pin 1), Multiplier input pin: During the start up, if the system turn-on time needs to be fast, an external high voltage bipolar and a diode can be added for VCC during the start-up, once VCC is greater than UVLO, 15V, IAC pin will go low and turn off the high voltage bipolar.

4. For the fast load transient and line transient, a transconductance error amplifier has been implemented between the output pin VEAO and the input pin VFB to replace the conventional OP. Since transconductance amplifier does not need the local feed back (OP needs the local feedback); therefore, its VFB can fast and accurately sense OVP condition not like traditional OP, operational amplifier can not sense VFB for OVP.

FEATURES

◆ Patent Filed #5,565,761, #5,747,977, #5,742,151, #5,804,950, #5,798,635, #6,091,233
◆ Industry first interleaved PFC with 180 phase shift
◆ CCM for EMI filter but CRM for PFC boost diodes
◆ Due to ZCS and about ZVS, it is about noise free
◆ Design for LCD TV or 90+ power supply
◆ Critical Conduction Mode (CRM) = ZCS with about ZVS
◆ Current input multiplier, IAC (Patented)
◆ For 90+ system, an LLC or SRC should be the PWM
◆ For 85+ system, an Dual Forward or a half bridge should be the PWM
◆ At light load, PFC bulk will drop ~ 40V at low line and Slave PFC will be disabled (Patented)
◆ PGB pin also can be used to turn on the CM6900/CM6901 which is LLC/SRC controller for 90+ applications
◆ VRMS does not need high voltage resistor; IAC determines VRMS1 and VRMS2
◆ AC Brown out by comparing VRMS2 with 1.25V on and 1.0V off
◆ No bleed resistor during the start up (Patented)
◆ Can ON-OFF high voltage bipolar during the system start up (Patented)
◆ 500mV Current Limit and about 130uS Current Loop Open time out protection
◆ Precision output over voltage protection comparator with 2.75V threshold which is 10% increased from 2.5V.
◆ GM for Fast line and load transient response (Patented)
◆ Soft Start pin at pin 6
◆ Open control loop protection/Tri-Fault Detect Comparator for UL1950 (Patented)
◆ 16.5V 50mA Shunt Regulator at VCC
◆ Micro power start-up current (60uA Typ.)
◆ Very low operating supply current (1.5mA Typ.)
◆ Internal start up timer
◆ 1% precision 3mA Buffered 7.5V reference
◆ Totem pole driver output current: 30ohm (VCC=15V) sourcing current and 15 ohm (VCC=15V) sink current
◆ 16-Pin DIP/SOIC packages

5. Open Control Loop protection/Tri-Fault Detect Comparator on VFB pin for easy passing the single fault protection test of the UL1950 regulation.

The CM6565's interleaved PFC has two PFC controllers, Master PFC and Slave PFC. The Slave PFC is lagged ~ 180 degree phase shift from the Master PFC. Both PFC controllers consisted of ZCS plus about ZVS functions. It provides the high efficient of power supply at both full load and at light load. To input EMI filter, the currents are overlapping and it looks like a CCM boost system with double frequency. The ZCS plus about ZVS on feature reduce the EMI noise further.

It has a superior performance multiplier making the device capable of working in universal input voltage range applications with an excellent THD.
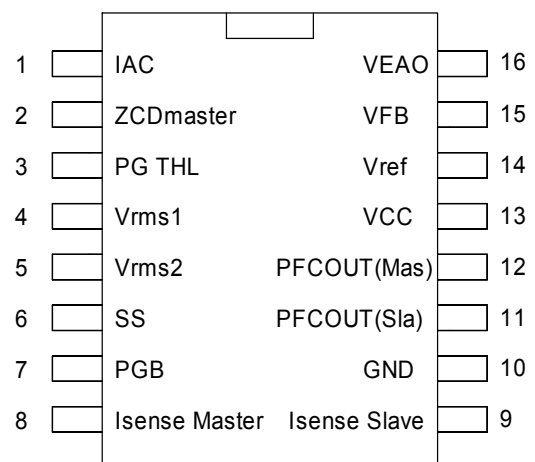
The totem pole output stage is capable of driving a power MOS or IGBT with +500mA source and -1A sink currents. The device is operating in transition mode and it is optimized for Electronic Lamp Ballast application, AC-DC adaptors and SMPS.

APPLICATIONS

- ◆ LCD TV
- ◆ Desktop PC Power Supply
- ◆ AC Adaptor
- ◆ Internet Server Power Supply
- ◆ IPC Power Supply
- ◆ UPS
- ◆ Battery Charger
- ◆ DC Motor Power Supply
- ◆ Monitor Power Supply
- ◆ Telecom System Power Supply
- ◆ Distributed Power

PIN CONFIGURATION

DIP-016 (P016)/SOP-016 (S08)
Top View

1	IAC	VEAO	16
2	ZCDmaster	VFB	15
3	PG THL	Vref	14
4	Vrms1	VCC	13
5	Vrms2	PFCOUT(Mas)	12
6	SS	PFCOUT(Sla)	11
7	PGB	GND	10
8	Isense Master	Isense Slave	9

PIN DESCRIPTION

Pin No.	Symbol	Description	Operating Voltage			Unit
			Min.	Typ.	Max.	
1	IAC	During Normal Operation: Multiplier input, it provides the information of line input voltage. It only needs one resistor (RAC) connected between line input and IAC pin. The value of RAC typically is between 4 Mega ohm to 10 Mega ohm		1.4		V
1	IAC	During the System Start up: RAC serves as a bleed resistor for VCC pin	0		VCC+1V	V
2	ZCDmaster	Master PFC Zero current detection input. The threshold of the pin is 80mV. When ZCDmaster is greater than ~ 80mV, PFCOUT (master) may go high. When ZCDmaster is less than ~ 80mV, PFCOUT (master) is low.	-0.3		0.7	V
3	PG THL	PG THL is an input I/O. The user can program the Low Threshold of the Power Good which can determine the comparator output of PGB (open drain) to be pulled high.	0.75		2.3	V
4	Vrms1	AC Brown out input. It mirrors the IAC (pin1) current to Vrm1 and Vrms1 uses it with Rrms1 and Crms1 to generate the first pole; then it uses the second RC pole to interface with Vrms2 (pin5). AC brown out uses the Vrms1 to determine brown out point. Its threshold is 3V with 1V hysteresis.	0		5	V
5	Vrms2	Gain Modulator/Multiplier Vrms input. The value of Vrms2 should be 50% of Vrms1 average value.	0		5	V
6	SS	PFC Soft Start pin: It supplies ~ 8uA to SS pin. It provides a close-loop soft start function during power supply start up. PFC Soft Start function can just need a simple capacitor to ground and it can be around 1uF.	0		VCC	V
7	PGB	PGB is the PG comparator output. The input of PGB comparator is using Vfb (pin 15) to compare with the high threshold, 2.365V (preset internally) and the low threshold, PGTHL (pin 3, Set by user). When 380V is ready, pin 7 is open-drain and it will be pulled low.	0		VCC	V

Pin No.	Symbol	Description	Operating Voltage			
			Min.	Typ.	Max.	Unit
8	Isense Master	The Input pin of the Master PFCCMP which is current sense comparator of the Master PFC control loop. The Power MOSFET current is sensed by a resistor and the resulting voltage needs to be filtered and it can be applied to this pin. Its maximum threshold is about 500mV. Its threshold is determined by the PFC multiplier output current and it is a sine wave current. Isense Master designed for cycle by cycle current shaping and cycle by cycle current limit. It also determines when the Isense Slave to turn off.	0		2	V
9	Isense Slave	The Input pin of the Slave PFCCMP which is current sense comparator of the Slave PFC control loop. The Power MOSFET current is sensed by a resistor and the resulting voltage needs to be filtered and it can be applied to this pin. Its maximum threshold is about 500mV. Its threshold is determined by the PFC multiplier output current and it is a sine wave current.	0		2	V
10	GND	Ground				
11	PFCOUT (Slave)	Slave PFC driver output; It can drive Power MOSFET and IGBT with 30 ohm pulled up and 15 ohm pulled down.	0		VCC	V
12	PFCOUT (Master)	Master PFC driver output; It can drive Power MOSFET and IGBT with 30 ohm pulled up and 15 ohm pulled down.	0		VCC	V
13	VCC	Supply voltage: It has a 50mA 16.5V shunt regulator.	10	15	18	V
14	Vref	1% Precision 7.5V Reference Pin and it sources maximum 3 mA		7.5		V
15	V_{FB}	PFC transconductance voltage error amplifier input; it also senses PFCOVP when VFB is greater than 2.75V and it also turns off PFC when VFB is less than 0.5V. It is also the Tri-Fault Protection input.	0	2.5	3	V
16	VEAO	PFC transconductance voltage error amplifier output; Low Power Detect Comparator input	0		6	V

BLOCK DIAGRAM
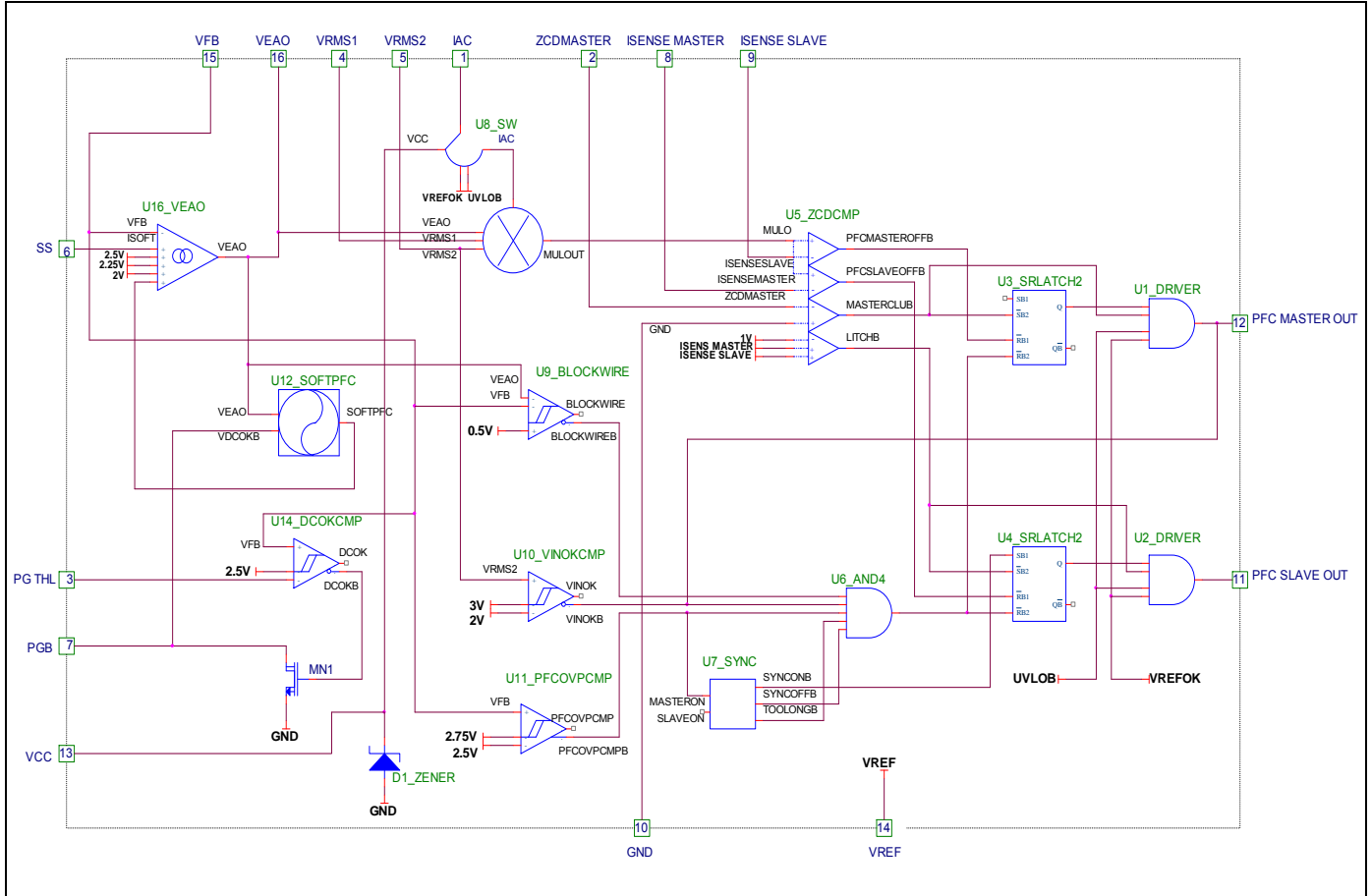
ORDERING INFORMATION

Part Number	Temperature Range	Package
CM6565GIP	-40℃ to 125℃	16-Pin PDIP (P016)
CM6565GIS	-40℃ to 125℃	16-Pin SOP (S016)

Note:
1.G : Suffix for Pb Free Product
2.Initial Accuracy : T_A=25℃

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are those values beyond which the device could be permanently damaged.

Parameter	Min.	Max.	Units
V_{CC} MAX		20	V
IAC (after start up)	GND-0.3	VCC	V
PFC OUT(Master) and PFC OUT (Slave)	GND – 0.3	VCC + 0.3	V
VEAO	GND-0.3	6.3	V
Voltage on Any Other Pin	GND – 0.3	8	V
I_{CC} Current (Average)		100	mA
Iac Input Current		200	uA
Iref		5	mA
Current Sense Input (ISENSEmaster and ISENSEslave)	-0.3	6	V
Zero Current Detector (ZCDmaster and PGTHL) (Source)		0.1	mA
Zero Current Detector (ZCDmaster and PGTHL) (Sink)		-0.1	mA
Junction Temperature	-40	150	℃
Storage Temperature Range	-65	150	℃
Operating Temperature Range	-40	125	℃
Lead Temperature (Soldering, 10 sec)		260	℃
Thermal Resistance (θ_{JA}) PDIP-016 SOP-016		 80 150	℃/W

ELECTRICAL CHARACTERISTICS unless otherwise stated, these specifications apply Vcc=+14V, T_A=Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6565			Unit
			Min.	Typ.	Max.	
	Supply Voltage Section (VCC)					
	Operating Range	After turn on	10		16.5	V
	Turn-on Threshold		12.74	13	13.26	V
	Hysteresis		2.85	3	3.15	V
	Supply Current Section (VCC)					
	Start-up Current	Before turn-on (V_{CC}=12V)		60		µA
	Operating Supply Current	C_L=1nF @ 70KHz		1.5	2	mA
	Shunt Regulator (VCC)					
	Zener Threshold Voltage	Apply VCC with Iop=20mA	16.2	16.75	17.4	V
	Voltage Error Amplifier (g_{mv})					
	Input Voltage Range		0		5.7	V
	Transconductance	$V_{NONINV} = V_{INV}$, VEAO = 3.75V	TBD	48	TBD	µmho
	Voltage Feedback Input Threshold	T_A=25℃	TBD	2.38	TBD	V
		11V<V_{CC}<18V	2.32		2.44	V
	Input Bias Current	Note 2	-1.0	-0.5		µA
	Output High Voltage		5.8	6.0		V
	Output Low Voltage			0.1	0.4	V
	AC Brown Out					
Vrms1	AC Brown Out Off Threshold	2.9	3	3.1		V
Vrms1	Brown Out Hysteresis		1			V
	Vrms1					
	Mismatched Current Mirror Ratio between IAC to Vrms	IAC = 25.28uA	-2	0	2	%

ELECTRICAL CHARACTERISTICS (Conti.) Unless otherwise stated, these specifications apply

Vcc=+15V, T_A=Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6565 Min.	CM6565 Typ.	CM6565 Max.	Unit
	Gain Modulator Section/ISENSEPFCmaster and ISENSEPFCslave (PFCCMP)					
	Gain1 (for wafer sort only)	Iac = 25.28uA, Vrms2 = 1.125V, Vfb=2.25V	TBD	5.33	TBD	
	Gain2 (for wafer sort only)	Iac = 32.8uA, Vrms2 = 1.45588V, Vfb=2.25V	TBD	4.08	TBD	
	Gain3 (for wafer sort only)	Iac = 65.9uA, Vrms2 = 2.91 V, Vfb=2.25V	TBD	1.89	TBD	
	Gain4	Iac = 79.44uA, Vrms2 = 3.51V, Vfb=2.25V	TBD	1.52	TBD	
	Output Max. Slope; dVmul/dIAC1	Iac = 25.28uA, Vrms2 = 1.125V, Vfb=2.25V	TBD	19.6	TBD	K ohm
	Output Max. Slope; dVmul/dIAC2	Iac = 32.8uA, Vrms2 = 1.45588V, Vfb=2.25V	TBD	15.1	TBD	K ohm
	Output Max. Slope; dVmul/dIAC3	Iac = 65.9uA, Vrms2 = 2.91 V, Vfb=2.25V	TBD	7.29	TBD	K ohm
	Output Max. Slope; dVmul/dIAC4	Iac = 79.44uA, Vrms2 = 3.51V, Vfb=2.25V	TBD	6.15	TBD	K ohm
	Maximum Multiplier output, Vmul	VEAO=6V, Vrms2=1.25V, IAC=30uA, Imul x 4.24Kohm	0.475	0.5	0.525	V
	PFCCMPmaster and PFCCMPslave					
	Miss-Matched Offset between master and slave		-20	0	20	mV
	Zero Current Detector (for ZCDmaster)					
	Input Threshold Voltage Rising Edge	Note 3		80		mV
	Upper Clamp Voltage	I_{ZCD}=20µA		0.6		V
	Lower Clamp Voltage	I_{ZCD}=-20uA		-0.6		V
	Output Section PFCout (master) and PFCout (slave)					
	Output Low Rdson	Iout=-20mA at room temp		15	30	ohm
		Iout=-100mA at room temp		15	30	ohm
		Iout=10mA, Vcc=9V at room temp		0.4	0.8	V
	Output High Rdson	Iout=20mA at room temp		30	45	ohm
		Iout=100mA at room temp		30	45	ohm
	Output Voltage Rise Time	C_L=1nF; Note 3		50		ns
	Output Voltage Fall Time	C_L=1nF; Note 3		40		ns

ELECTRICAL CHARACTERISTICS (Conti.) Unless otherwise stated, these specifications apply

Vcc=+14.5V, T$_A$=Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6565			Unit
			Min.	Typ.	Max.	
Light Load Threshold (Veao)						
	Light Load Threshold	Measure pin 7; an open drain	1.66	1.75	1.83	V
	Hysteresis		715	750	795	mV
Tri-Fault Detect Comparator						
	Fault Detect High	Sweep Vfb	2.70	2.75	2.85	V
	Time to Fault Detect High	0.1nF is connected Vfb pin VFB=Vfault detect low to VFB=OPEN		6	10	mS
	Fault Detect Low	Sweep Vfb	0.4	0.5	0.6	**V**
Restart Timer						
	Start Timer	Note 3		100		µs

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Includes all bias currents to other circuits connected to the V$_{FB}$ pin.

Note 3: Guaranteed by design, not 100% production test.

Interleaved PFC:

CM6565 is the industry first interleaved PFC. The patented interleaved PFC idea was starting around mid 90. The idea was to solve Qrr of 600V Boost diode at CCM. DCM boost does not have the Qrr issues, but DCM boost has much higher ripple current and it increases switching loss and it causes the troubles of EMI circuits. The interleaved PFC, it solves both ends. In the front end, two DCM boost converter currents combine together and it behaves like a CCM with two times the frequency. From the lab data, its efficiency can be above 95% at full load without ultra fast diodes.

CRM interleaved PFC can improve the efficiency of PFC further. CRM is ZCS at on time. By delaying the ZCD pin, it can get about ZVS switching.

The 180 degree phase shift is done by the internal timer. The PFCOUT (master) is the clock of the timer. The slave PFC does not have to sense any signal if the external boost inductor is matched well. Usually, the PFC sensing resistor value at Isense Slave (pin 9) can use less than the resistor value of the Isense Master (pin 8) PFC sensing resistor. It improves a bit of the efficiency.

To make PFC master and PFC slave components matched is important because it can reduce the power device cost. Also, the matched components can be ensured both master and slave PFCs work at CRM mode. Without the good matches, both PFC power device margin needs to over design to cover the worst mismatched condition.

Basically, it is like two 6561s work together with 180 degree phase shift + light load improvements.

Constant Power and Constant Bandwidth PFC:

The Gain Modulator with Vrms2, it keeps the power constant over universal line input. The Vrms1 and Vrms2 are derived from IAC current. By deriving Vrms1 from IAC, it improves the light load efficiency and it reduces the circuit and part counts. The product of Gain Modulator output current and Rmul determines the sine wave current and the maximum value is about 500mV.

Boost Light Load Efficiency:

CM6565 is designed for both 90+ systems or 85+ systems.
For 90+ systems, CM6565 interleaved CRM PFC is ready to interface with CM6900 which is a secondary SRC+SR controller or it can be interfaced with CM6901 which is a secondary LLC+SR controller. At light load, CM6565 will drop the PFC bulk voltage from 380V to 342V and the slave PFC will be disabled. Only the master PFC is on during the light load condition.

Boost Light Load Functions can be disabled by clamping pin 6 (SS) below 5V.

IAC (PIN 1):

IAC serves several functions:

During the system Start-Up, IAC pin is connected to VCC; therefore, the external RAC which is between IAC and line input voltage can be served as a Start-Up resistor (bleed resistor). Once VCC is greater than UVLO, 13V, IAC pin will be connected to the multiplier input which is a current mirror and IAC voltage is about 1.4V.
Usually, the value of the RAC is between 4 Mohm to 10 Mohm.
Green Mode with Fast Start Up with high voltage bipolar and low voltage diode.

The following circuit can be used for the Fast Start Up, if the on time needs to be less than 100mS and Green Mode Performance is needed.
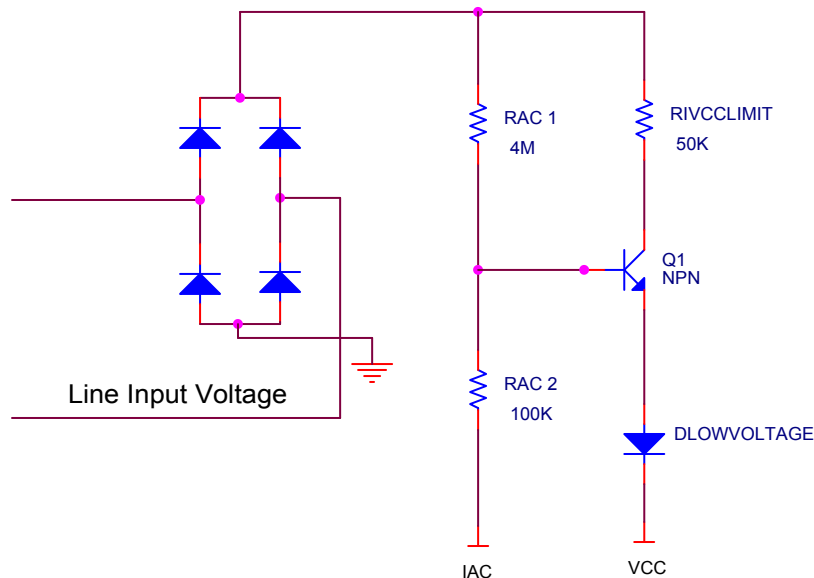
After VCC is greater than UVLO, IAC is connected to the input of the current mirror which is also the input of the multiplier. This current input multiplier is less sensitive to the noise since it is sensing current instead of the voltage, not like the conventional voltage input multiplier which senses the voltage and requires a two resistor network to sense the line input voltage information.

Vrms1 (PIN 4) and Vrms2 (PIN 5)

Vrms1 and Vrms2: These two pins will represent the rms value of the line input voltage information without using additional high voltage resistors. Vrms1 will take the IAC current + RC filters to obtain the voltage level with the first pole and the first pole frequency is about 12Hz. The second RC pole level at about 5 Hz is the Vrms2 level. Vrms1 takes this voltage information to determine the AC Brown Out Level. When Vrms1 is above 3V, both PFCout(master) and PFCout(slave) start with Veao Soft Start. When Vrms1 is below 2V, both Veao and SS are pulled down.

Vrms2 also is the input of Gain Modulator which provides the about constant power limit. The average value of 2 x Vrms2 needs to equal to the average value of the Vrms1.

VFB (PIN 15)

VFB also serves several functions:

1. Transconductance Amplifier speed up the load transient and the line transient.
2. VFB PIN is the inverting input of Transconductance Amp, GM.
3. Fast and Precision PFC Over Voltage Protection
4. CM6565 is implemented with GM; therefore, it does not require a local feedback (Which is a must item for the Conventional Operational Amplifier.) Its compensation network is connected between VEAO and GROUND and there is not feedback compensation network between VEAO and VFB.
5. Since there is no local feedback between VEAO and VFB, the VFB node can sense the PFC output voltage without any delay; not like the conventional operational amplifier (It has 100mS time constant. This may stress the 380V PFC output capacitor.) CM6565's PFCOVP use the VFB pin to sense the PFC over voltage condition without any delay.
6. Comply with UL1950, single fault protection without any additional external circuit. At VFB pin, CM6565 has been implemented with the tri-fault protection circuit to ensure the system power supply can comply with the UL1950.

VEAO (PIN 16)

VEAO is the output pin of GM. It can be used as the conventional OP but we not suggest because it will dramatically slow down the system speed. For the proper usage of the VEAO, the compensation network should be connected between VEAO and GROUND.

VEAO pin also is the input pin of the low-power-detect comparator. When VEAO potential goes low, it means the power supply system needs less power. When VEAO potential goes high, it means the power supply system needs more power. VEAO potential represents the power status of the power supply. CM6565 uses the VEAO potential to determine if the power supply is at either the light load or the heavy load.

ZCDmaster (PIN 2)

The master PFC will determine when the slave PFC to turn on. The ZCDmaster sense the demagnetized winding signal from the master PFC boost inductor and its threshold is 80mV. It does not require a diode to rectify the signal. ZCDmaster is clamped between -0.7V to +0.7V by two back-to-back diodes to ground. Do not sink or source more than 100uA. An RC filter may be needed to obtain the best ZVS performance while ZCS is sure thing.

Layout notice : the resister of connect the inductor and IC must be close to IC (pin2).

ISENSE master (PIN 8) and ISENSE slave (PIN 9)

Usually, ISENSE slave sensing function is reduced by reducing the PFC slave sensing resistor value to be less than 50% value of PFC master sensing resistor. Adding a much smaller value of PFC slave sensing resistor is to protect against any catastrophic fault conditions.

The ISENSE master is comparing the product of Gain Modulator Output current and Rmul and it provides the sine wave envelope to obtain the sine wave input current. The maximum threshold voltage, which is the product of Gain Modulator output current and Rmul, is about 500mV. A RC filter which has a 500Khz pole needs to be applied to avoid false triggered by the switching noise.

VCC (PIN 13)

CM6565's turn on and turn off VCC is like the other PFC product family; on at 13V and off at 10V. It has 50mA zener/shunt regulator threshold at ~ 16.75V at VCC. The minimum bypass capacitor should be greater than 1uF.

Vref (PIN 14)

Vref is 1% 3mA buffered 7.5V reference. It requires a 0.1uF to 0.01uF bypass capacitor to filter out the switching the noise.

SS (PIN 6)

SS pin 6 is the Soft Start Capacitor pin. CM6565 SS pin provides a close loop soft start for the interleaved CRM PFC.

The Charging Current is about 8uA. By clamping SS below 5V, it disables the 380V to 340V function at light load and both Master and Slave are on at light load. When SS is above 5V, both light load functions are enabled.

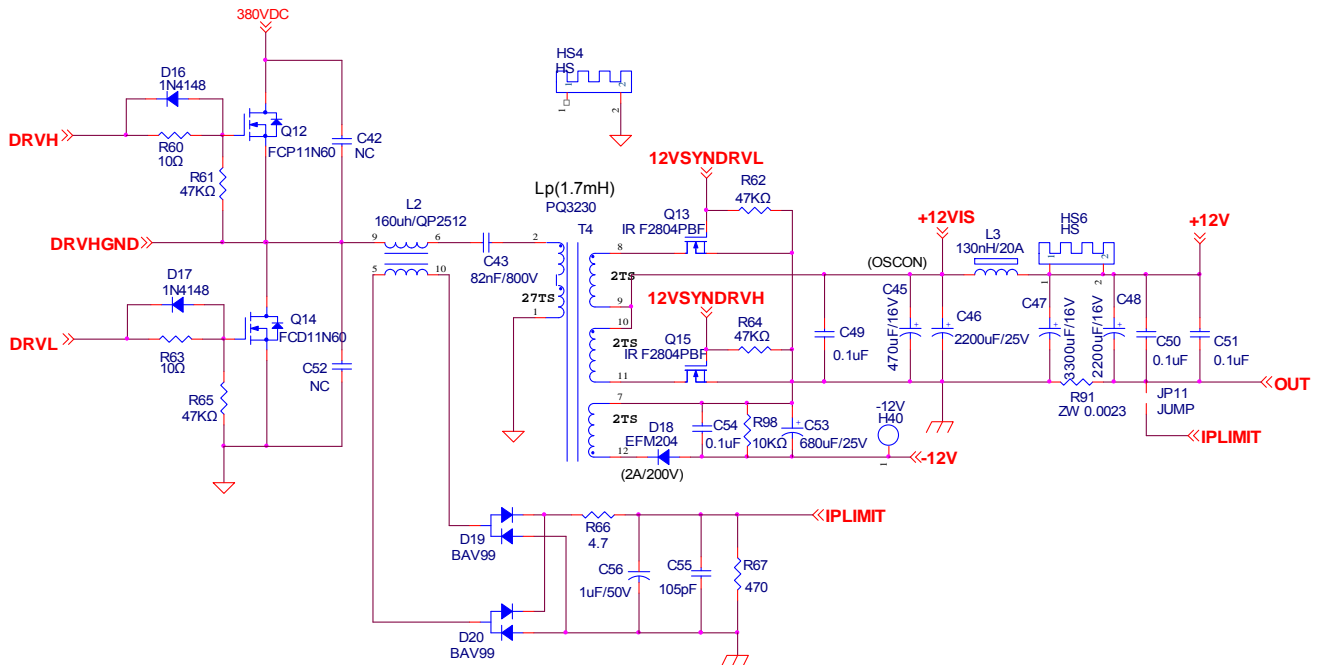# Interleaved CRM PFC (CM6565) Application Circuit
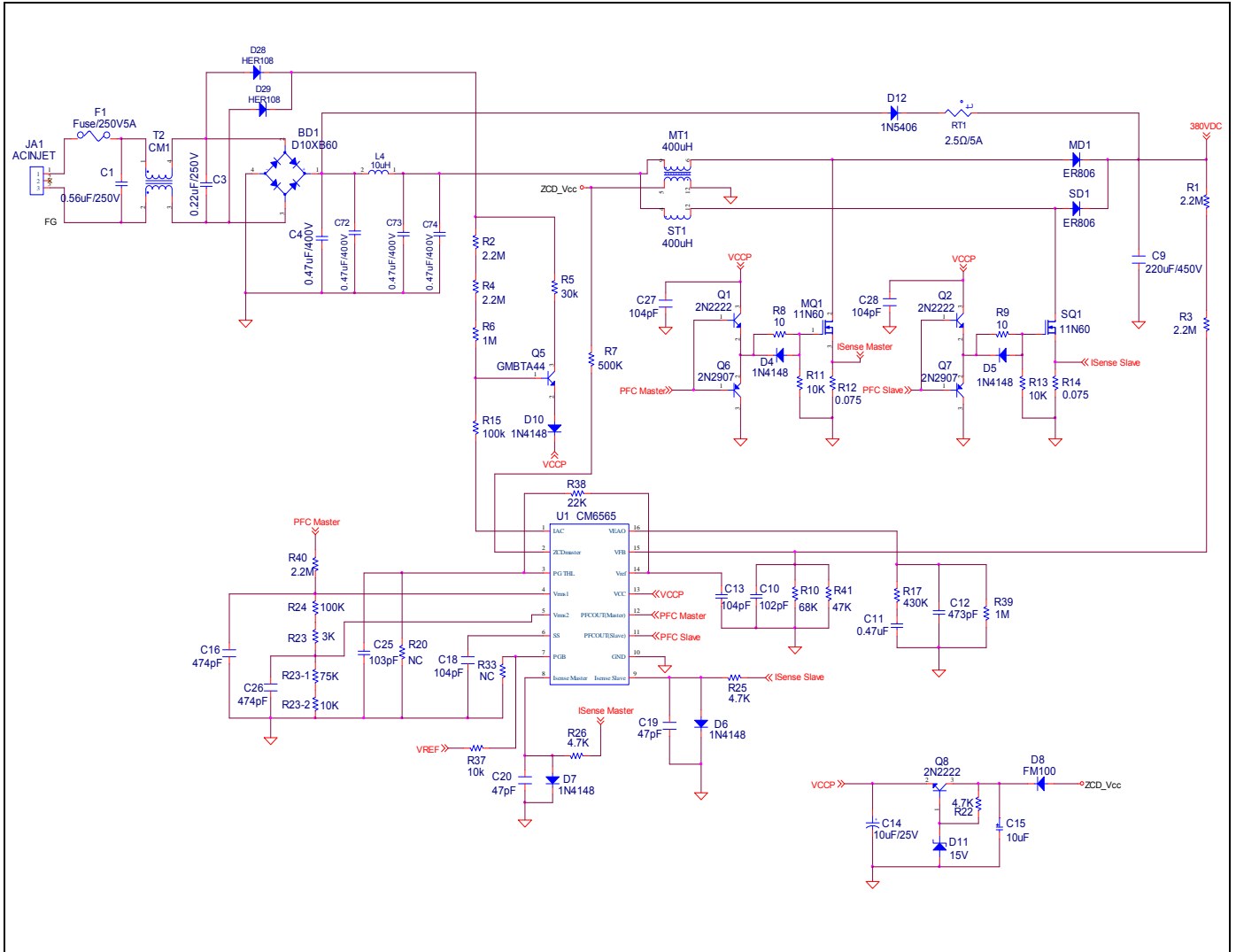
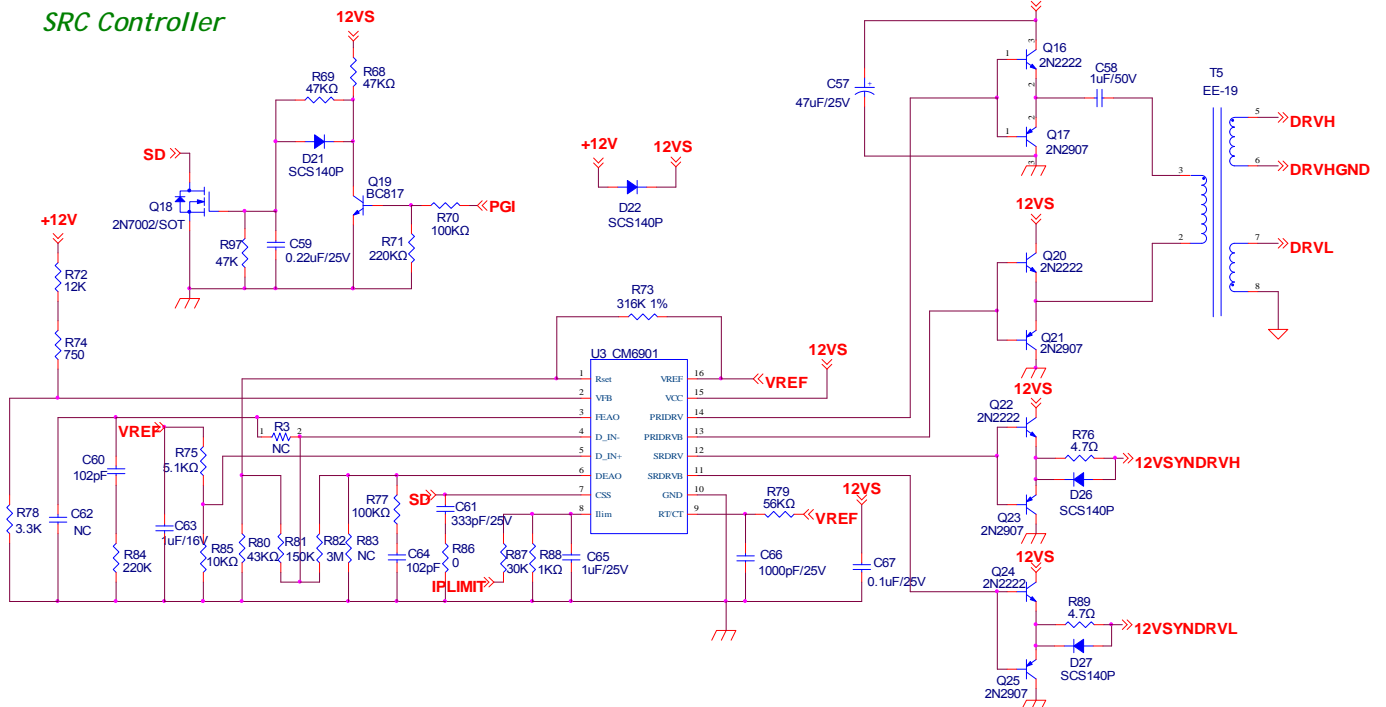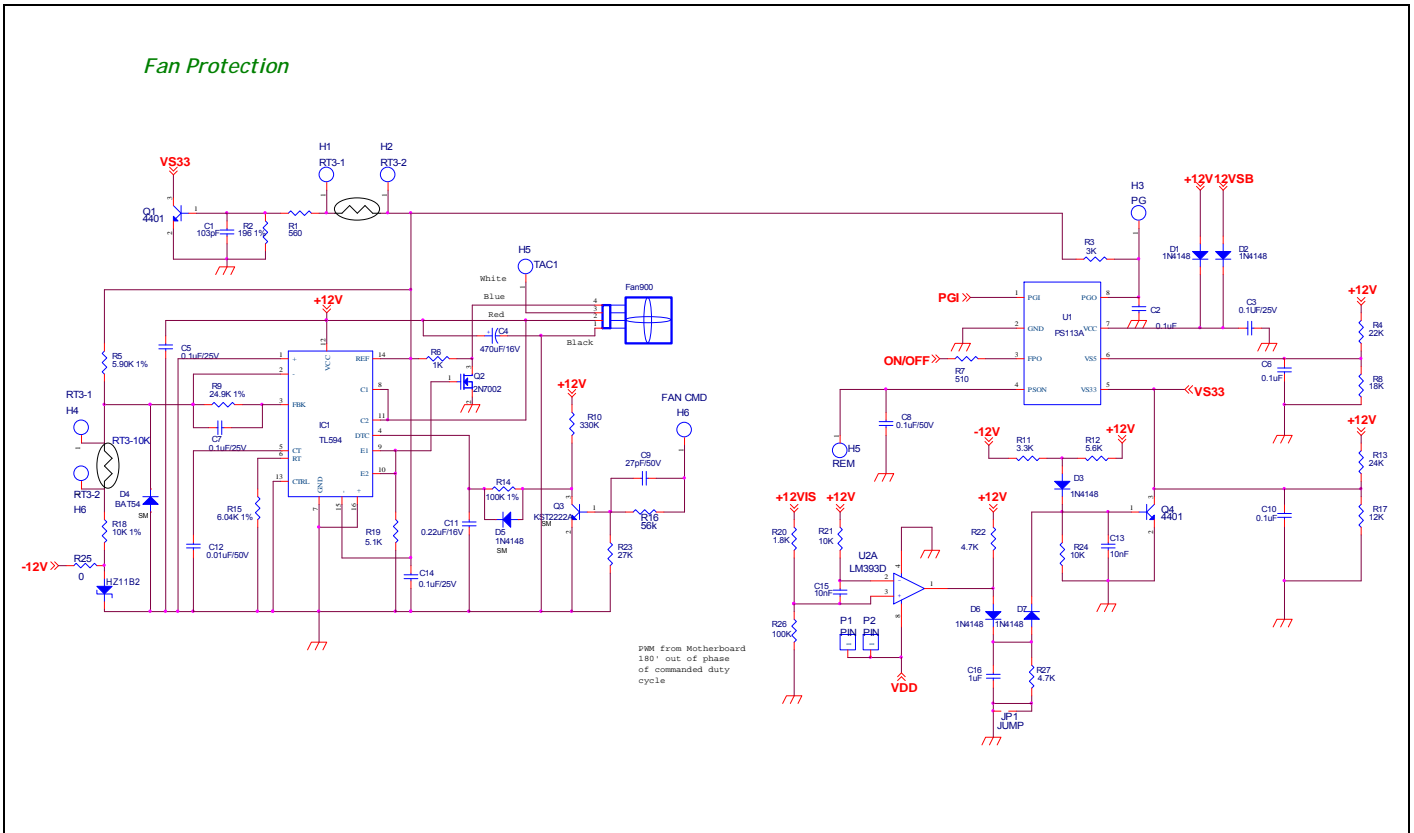## CM6565 + CM6901 Ninety-three Plus Desk Top Application Circuit
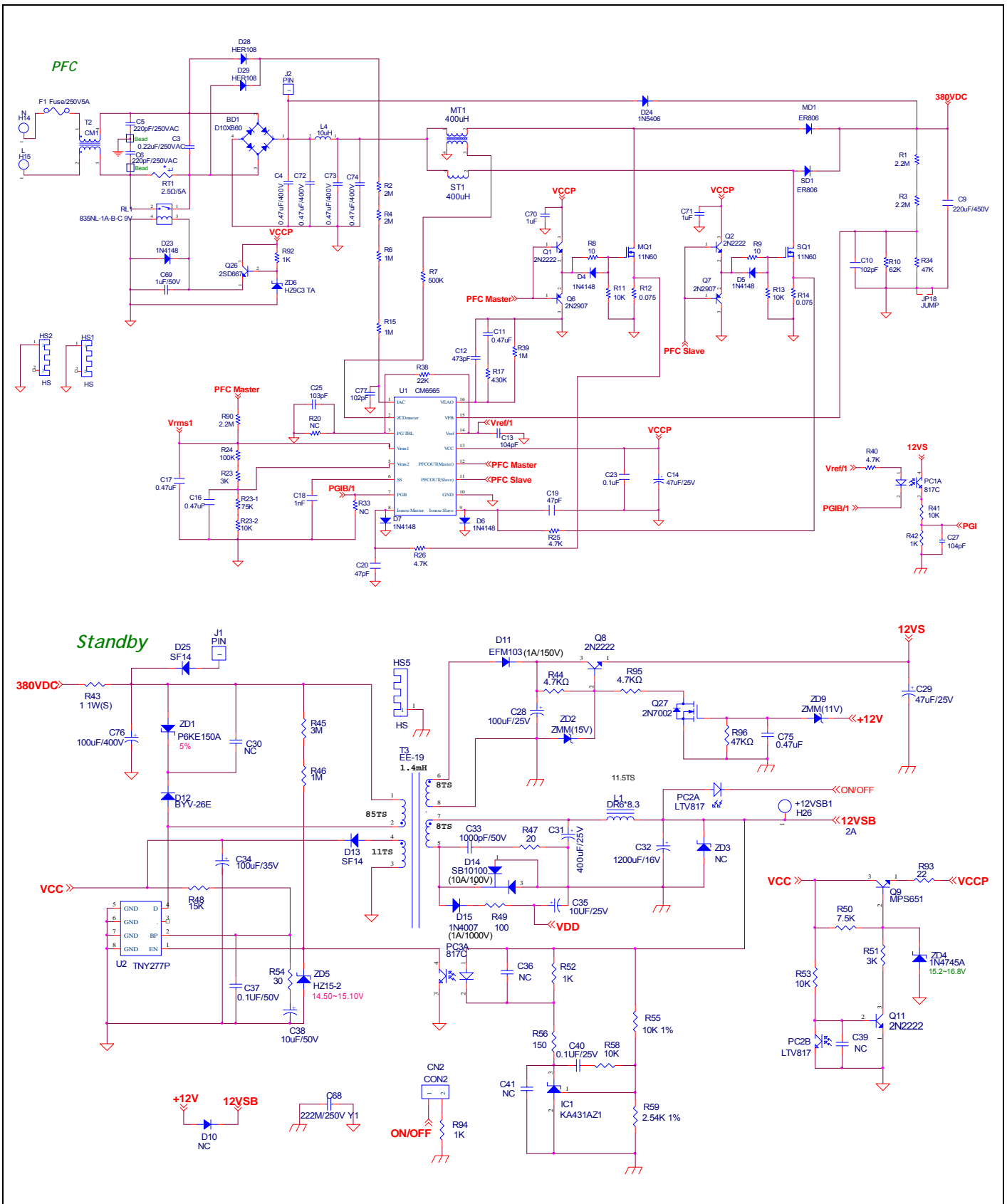
CHAMPION

DC-DC

SRC Controller

CHAMPION

Fan Protection

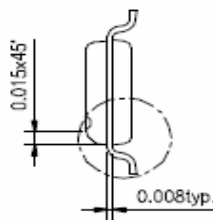## PACKAGE DIMENSION

16-PIN PDIP (P016)
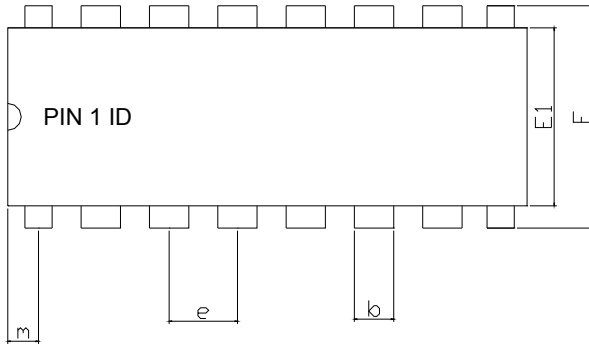
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	4.32	---	---	0.170
A1	0.38	---	---	0.015	---	---
b	1.40	---	1.65	0.055	---	0.065
b1	0.40	---	0.56	0.016	---	0.022
C	0.20	---	0.31	0.008	---	0.012
D	18.79	---	19.31	0.740	---	0.760
E	7.49	---	8.26	0.295	---	0.325
E1	6.09	---	6.61	0.240	---	0.260
e	---	2.54	---	---	0.100	---
L	3.18	---	---	0.125	---	---
m	0.50	---	---	0.02	---	---
θ	0°	---	15°	0°	---	15°
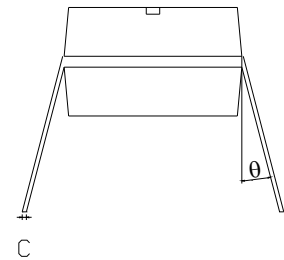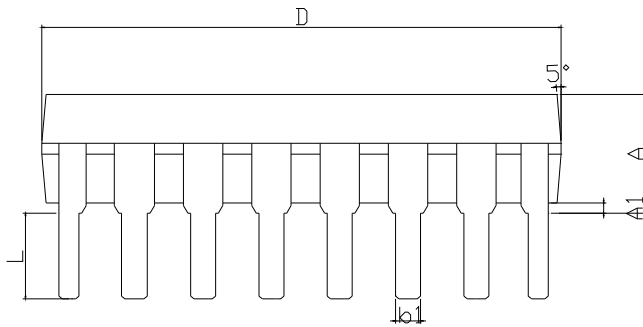
16-Pin SOP (S016)
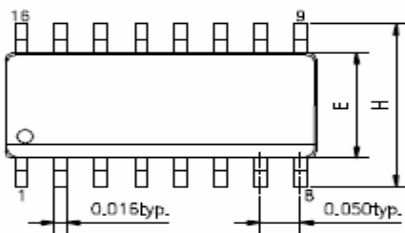
SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
A2	0.049	0.065
D	0.386	0.394
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ	0	8

UNIT : INCH
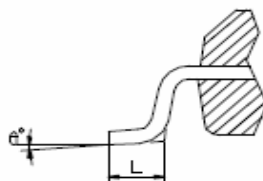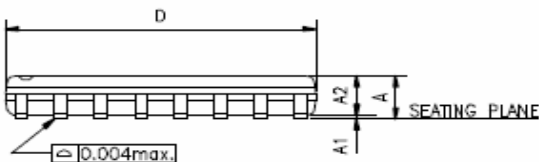
NOTES:
1. JEDEC OUTLINE : MS-012 AC.
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

IMPORTANT NOTICE

Champion Microelectronic Corporation (CMC) reserves the right to make changes to its products or to discontinue any integrated circuit product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

A few applications using integrated circuit products may involve potential risks of death, personal injury, or severe property or environmental damage.   CMC integrated circuit products are not designed, intended, authorized, or warranted to be suitable for use in life-support applications, devices or systems or other critical applications.   Use of CMC products in such applications is understood to be fully at the risk of the customer.   In order to minimize risks associated with the customer's applications, the customer should provide adequate design and operating safeguards.

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